

NCV7356

Advance Information Single Wire CAN Transceiver

The NCV7356 is a physical layer device for a single wire data link capable of operating with various Carrier Sense Multiple Access with Collision Resolution (CSMA/CR) protocols such as the Bosch Controller Area Network (CAN) version 2.0. This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor and/or dedicated logic devices which use the network.

The network shall be able to operate in either the normal data rate mode or a high-speed data download mode for assembly line and service data transfer operations. The high-speed mode is only intended to be operational when the bus is attached to an off-board service node. This node shall provide temporary bus electrical loads which facilitate higher speed operation. Such temporary loads should be removed when not performing download operations.

The bit rate for normal communications is typically 33 kbit/s, for high-speed transmissions like described above a typical bit rate of 83 kbit/s is recommended. The NCV7356 is designed in accordance to the Single Wire CAN Physical Layer Specification GMW3089 V2.3 and supports many additional features like undervoltage lockout, timeout for faulty blocked input signals, output blanking time in case of bus ringing and a very low sleep mode current.

Features

- Fully Compatible with J2411 Single Wire CAN Specification
- 60 μ A (max) Sleep Mode Current
- Operating Voltage Range 5.0 to 27 V
- Up to 100 kbps High-Speed Transmission Mode
- Up to 40 kbps Bus Speed
- Selective BUS Wake-Up
- Logic Inputs Compatible with 3.3 V and 5 V Supply Systems
- Control Pin for External Voltage Regulators
- Standby to Sleep Mode Timeout
- Low RFI Due to Output Wave Shaping
- Fully Integrated Receiver Filter
- Bus Terminals Proof Against Short-Circuits and Transients
- Loss of Ground Protection
- Protection Against Load Dump, Jump Start
- Thermal Overload and Short Circuit Protection
- ESD Protection of 4.0 kV on CAN Pin (2.0 kV on Any Other Pin)
- Undervoltage Lock Out
- Bus Dominant Timeout Feature
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

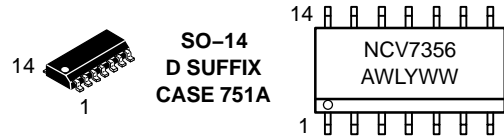
This document contains information on a new product. Specifications and information herein are subject to change without notice.



ON Semiconductor®

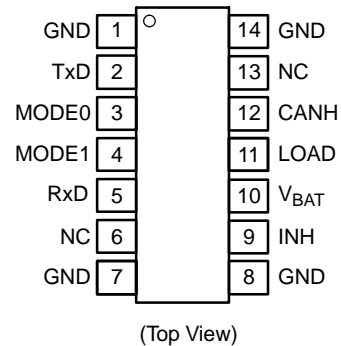
<http://onsemi.com>

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV7356D	SOIC-14	55 Units / Rail
NCV7356DR2	SOIC-14	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV7356

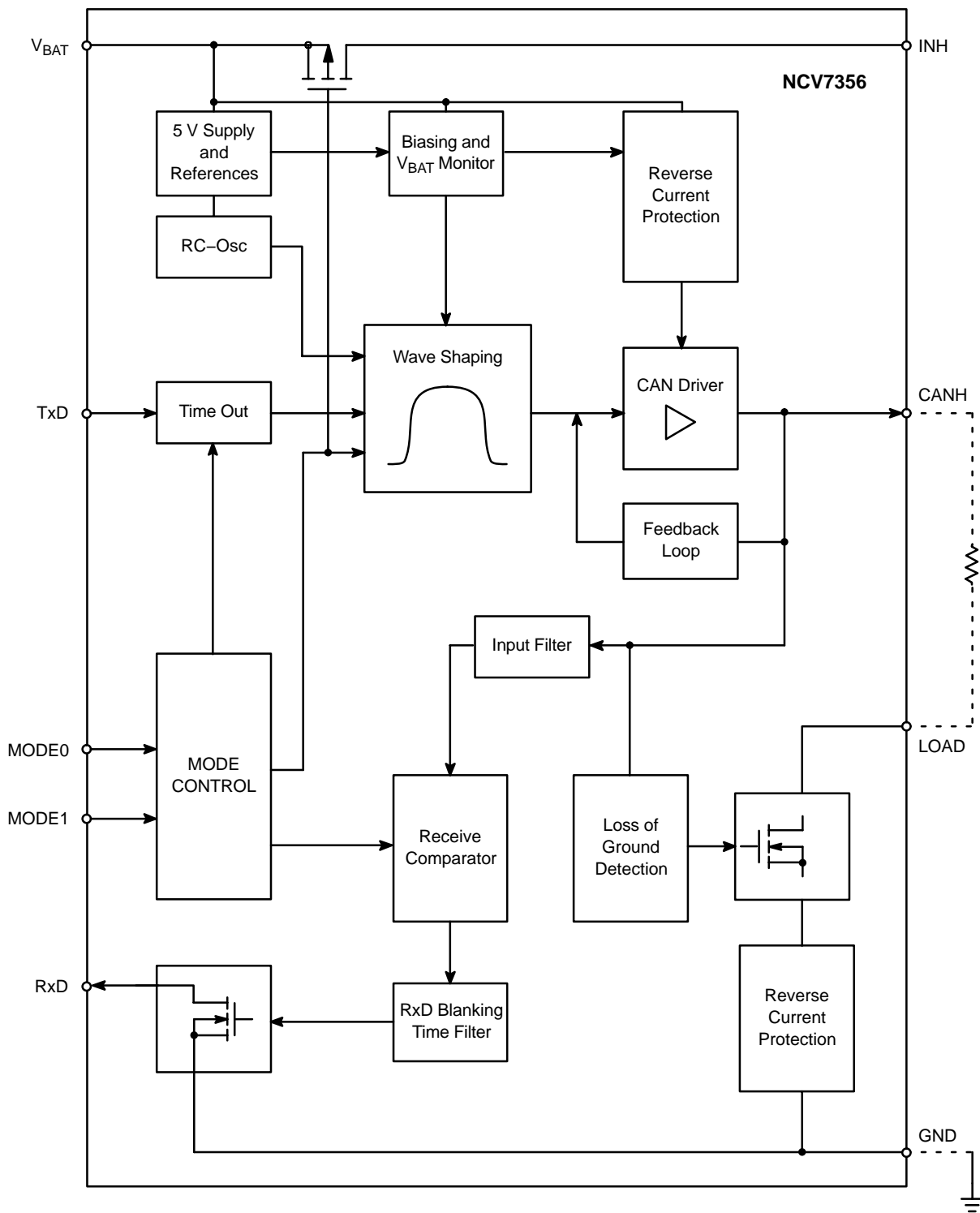


Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

Pin	Symbol	Description
1, 7, 8, 14	GND	Ground
2	TXD	Transmit data from microprocessor to CAN.
3	MODE0	Operating mode select input 0.
4	MODE1	Operating mode select input 1.
5	RXD	Receive data from CAN to microprocessor.
6, 13	NC	No Connection
9	INH	Control pin for external voltage regulator (high voltage high side switch)
10	V _{BAT}	Battery input voltage.
11	LOAD	Resistor load (loss of ground detection low side switch).
12	CANH	Single wire CAN bus pin.

Functional Description

TxD Input Pin

TxD Polarity

- TxD = logic 1 (or floating) on this pin produces an undriven or recessive bus state (low bus voltage)
- TxD = logic 0 on this pin produces either a bus normal or a bus high voltage dominant state depending on the transceiver mode state (high bus voltage)

If the TxD pin is driven to a logic low state while the sleep mode (Mode 0 = 0 and Mode 1 = 0) is activated, the transceiver can not drive the CANH pin to the dominant state.

The transceiver provides an internal pull up current on the TxD pin which will cause the transmitter to default to the bus recessive state when TxD is not driven.

TxD input signals are standard CMOS logic levels.

Timeout Feature

In case of a faulty blocked dominant TxD input signal, the CANH output is switched off automatically after the specified TxD timeout reaction time to prevent a dominant bus.

The transmission is continued by next TxD L to H transition without delay.

MODE0 and MODE1 Pins

The transceiver provides a weak internal pull down current on each of these pins which causes the transceiver to default to sleep mode when they are not driven. The mode input signals are standard CMOS logic level for 3.3V and 5V supply voltages.

MODE0	MODE1	Mode
L	L	Sleep Mode
H	L	High-Speed Mode
L	H	High Voltage Wake-Up
H	H	Normal Mode

Sleep Mode

Transceiver is in low power state, waiting for wake-up via high voltage signal or by mode pins change to any state other than 0,0. In this state, the CANH pin is not in the dominant state regardless of the state of the TxD pin.

High-Speed Mode

This mode allows high-speed download with bitrates up to 100 Kbit/s. The output waveshaping circuit is disabled in this mode. Bus transmitter drive circuits for those nodes which are required to communicate in high-speed mode are able to drive reduced bus resistance in this mode.

High Voltage Wake-Up Mode

This bus includes a selective node awake capability, which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake-up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non communicating low power “sleep” state. Communication at the lower, normal voltage levels shall not disturb the sleeping nodes.

Normal Mode

Transmission bit rate in normal communication is 33 Kbits/s. In normal transmission mode the NCV7356 supports controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the RC time constant of the total bus load.

RxD Output Pin

Logic data as sensed on the single wire CAN bus.

RxD Polarity

- RxD = logic 1 on this pin indicates a bus recessive state (low bus voltage)
- RxD = logic 0 on this pin indicates a bus normal or high voltage bus dominant state

RxD in Sleep Mode

RxD does not pass signals to the microprocessor while in sleep mode until a valid wake-up bus voltage level is received or the MODE0 and MODE 1 pins are not 0, 0 respectively. When the valid wake-up bus voltage signal awakens the transceiver, the RxD pin signals an interrupt (logic 0). If there is no mode change within 250 ms (typ), the transceiver re-enters the sleep mode.

When not in sleep mode all valid bus signals will be sent out on the RxD pin.

RxD will be placed in the undriven or off state when in sleep mode.

RxD Typical Load

Resistance: 2.7 kΩ

Capacitance: < 25 pF

Bus LOAD Pin

Resistor ground connection with internal open-on-loss-of-ground protection

When the ECU experiences a loss of ground condition, this pin is switched to a high impedance state.

The ground connection through this pin is not interrupted in any transceiver operating mode including the sleep mode. The ground connection only is interrupted when there is a valid loss of ground condition.

This pin provides the bus load resistor with a path to ground which contributes less than 0.1 V to the bus offset voltage when sinking the maximum current through one load resistor.

The transceiver's maximum bus leakage current contribution to V_{OL} from the LOAD pin when in a loss of ground state is 50 μA over all operating temperatures and $3.5 < V_{BAT} < 27$ V.

V_{BAT} Input Pin (Vehicle Battery Voltage)

The transceiver is fully operational as described in the Electrical Characteristics Table over the range 6.0 V < V_{BAT} < 18 V as measured between the GND pin and the V_{BAT} pin.

For 5.0 V < V_{Bat} < 6.0 V the bus operates in normal mode with reduced dominant output voltage and reduced receiver input voltage. High voltage wakeup is not possible (dominant output voltage is the same as in normal or high-speed mode).

The transceiver operates in normal mode when 18 V > V_{Bat} > 27 V at 85°C for one minute.

For $0 < V_{BAT} < 4.0$ V, the bus is passive (not driven dominant) and RxD is undriven (high), regardless of the state of the TxD pin (undervoltage lockout).

CAN BUS Input/Output Pin

Wave Shaping in Normal and High Voltage Wake-Up Mode

Wave shaping is incorporated into the transmitter to minimize EMI radiated emissions. An important contributor to emissions is the rise and fall times during output transitions at the “corners” of the voltage waveform. The resultant waveform is one half of a sin wave of frequency 50–65 kHz at the rising waveform edge and one quarter of this sin wave at falling or trailing edge.

Wave Shaping in High-Speed Mode

Wave shaping control of the rising and falling waveform edges are disabled during high-speed mode. EMI emissions requirements are waived during this mode. The waveform rise time in this mode is less than 1.0 μs.

Short Circuits

If the CAN BUS pin is shorted to ground for any duration of time, the current is limited as specified in the Electrical Characteristics Table until an overtemperature shutdown circuit disables the output high side drive source transistor preventing damage to the IC.

Loss of Ground

In case of a valid loss of ground condition, the LOAD pin is switched into high impedance state. The CANH transmission is continued until the undervoltage lock out voltage threshold is detected.

Loss of Battery

In case of loss of battery ($V_{BAT} = 0$ or open) the transceiver does not disturb bus communication. The maximum reverse current into the power supply system (V_{BAT}) doesn't exceed 500 μA.

INH Pin

The INH pin is a high-voltage highside switch used to control the ECU's regulated microcontroller power supply. After power-on, the transceiver automatically enters an intermediate standby mode, the INH output will go high (up to V_{BAT}) turning on the external voltage regulator. The external regulator provides power to the ECU. If there is no mode change within 250 ms (typ), the transceiver re-enters the sleep mode and the INH output goes to logic 0 (floating).

When the transceiver has detected a valid wake-up condition (bus HVWU traffic which exceeds the wake-up filter time delay) the INH output will become high (up to V_{BAT}) again and the same procedure starts as described after power-on. In case of a mode change into any active mode, the sleep timer is stopped and INH stays high (up to V_{BAT}). If the transceiver enters the sleep mode, INH goes to logic 0 (floating) after 250 ms (typ) when no wake-up signal is present

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The maximum ratings given in the table below are limiting values that do not lead to a

permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
Supply Voltage, Normal Operation	V _{BAT}	–	–0.3	18	V
Short-Term Supply Voltage, Transient	V _{BAT.LD}	Load Dump; t < 500 ms	–	40	V (peak)
		Jump Start; t < 1.0 min	–	27	V
Transient Supply Voltage	V _{BAT.TR1}	ISO 7637/1 Pulse 1 (Note 1)	–50	–	V
Transient Supply Voltage	V _{BAT.TR2}	ISO 7637/1 Pulses 2 (Note 1)	–	100	V
Transient Supply Voltage	V _{BAT.TR3}	ISO 7637/1 Pulses 3A, 3B	–200	200	V
CANH Voltage	V _{CANH}	V _{BAT} < 27 V	–20	40	V
		V _{BAT} = 0 V	–40		
Transient Bus Voltage	V _{CANHTR1}	ISO 7637/1 Pulse 1 (Note 2)	–50	–	V
Transient Bus Voltage	V _{CANHTR2}	ISO 7637/1 Pulses 2 (Note 2)	–	100	V
Transient Bus Voltage	V _{CANHTR3}	ISO 7637/1 Pulses 3A, 3B (Note 2)	–200	200	V
DC Voltage on Pin LOAD	V _{LOAD}	Via RT > 2.0 kΩ	–40	40	V
DC Voltage on Pins TxD, MODE1, MODE0, RxD	V _{DC}	–	–0.3	7.0	V
ESD Capability of CANH	V _{ESDBUS}	Human Body Model Eq. to Discharge 100 pF with 1.5 kΩ	–4000	4000	V
ESD Capability of Any Other Pins	V _{ESD}	Human Body Model Eq. to Discharge 100 pF with 1.5 kΩ	–2000	2000	V
Maximum Latch-Up Free Current at Any Pin	I _{LATCH}	–	–500	500	mA
Maximum Power Dissipation	P _{tot}	At T _A = 125°C	–	>400 (Note 3)	mW
Thermal Impedance	θ _{JA}	In Free Air	–	<70	°C/W
Storage Temperature	T _{STG}	–	–55	150	°C
Junction Temperature	T _J	–	–40	150	°C
Lead Temperature Soldering Reflow: (SMD styles only)	T _{slid}	60 second maximum above 183°C –5°C/+0°C allowable conditions	–	240 peak	°C

1. ISO 7637 test pulses are applied to V_{BAT} via a reverse polarity diode and >1.0 μF blocking capacitor.
2. ISO 7637 test pulses are applied to CANH via a coupling capacitance of 1.0 nF.
3. The application board shall be realized with a ground copper foil area > 150 mm².

NCV7356

ELECTRICAL CHARACTERISTICS ($V_{BAT} = 5.0$ to 27 V, $T_A = -40$ to $+125^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
GENERAL						
Undervoltage Lock Out	V_{BATUV}	–	4.0	–	4.8	V
Supply Current, Recessive, All Active Modes	I_{BATN}	$V_{BAT} = 18$ V, TxD Open	–	5.0	6.0	mA
Normal Mode Supply Current, Dominant	I_{BATN} (Note 4)	$V_{BAT} = 27$ V, MODE0 = MODE1 = H, TxD = L, $R_{load} = 200 \Omega$	–	30	35	mA
High-Speed Mode Supply Current, Dominant	I_{BATN} (Note 4)	$V_{BAT} = 16$ V, MODE0 = H, MODE1 = L, TxD = L, $R_{load} = 75 \Omega$	–	70	75	mA
Wake-Up Mode Supply Current, Dominant	I_{BATW} (Note 4)	$V_{BAT} = 27$ V, MODE0 = L, MODE1 = H, TxD = L, $R_{load} = 200 \Omega$	–	60	75	mA
Sleep Mode Supply Current	I_{BATS}	$V_{BAT} = 18$ V, TxD, RxD, MODE0, MODE1 Open	–	30	60	μA
Thermal Shutdown (Note 4)	T_{SD}	–	155	–	180	$^\circ\text{C}$
Thermal Recovery (Note 4)	T_{REC}	–	126	–	150	$^\circ\text{C}$

CANH

Bus Output Voltage	V_{oh}	$R_L > 200 \Omega$, Normal, $6.0 \text{ V} < V_{BAT} < 27 \text{ V}$	4.4	–	5.1	V
Bus Output Voltage Low Battery	V_{oh}	$R_L > 200 \Omega$, Normal, High-Speed $5.0 \text{ V} < V_{BAT} < 6.0 \text{ V}$	3.4	–	5.1	V
Bus Output Voltage High Battery	V_{oh}	$R_L > 75 \Omega$, High-Speed $8.0 \text{ V} < V_{BAT} < 16 \text{ V}$	4.2	–	5.1	V
Fixed Wake-Up Output High Voltage	$V_{ohWuFix}$	Wake-Up Mode, $R_L > 200 \Omega$, $11.2 \text{ V} < V_{BAT} < 27 \text{ V}$	9.9	–	12.5	V
Offset Wake-Up Output High Voltage	$V_{ohWuOffset}$	Wake-Up Mode, $R_L > 200 \Omega$, $5.5 \text{ V} < V_{BAT} < 11.2 \text{ V}$	$V_{BAT} - 1.5$	–	V_{BAT}	V
Recessive State Output Voltage	V_{ol}	Recessive State or Sleep Mode, $R_{load} = 6.5 \text{ k}\Omega$	-0.20	–	0.20	V
Bus Short Circuit Current	$-I_{CAN_SHORT}$	$V_{CANH} = 0$ V, $V_{BAT} = 27$ V, TxD = 0 V	50	–	350	mA
Bus Leakage Current During Loss of Ground	I_{LKN_CAN} (Note 5)	Loss of Ground, $V_{CANH} = 0$ V	-50	–	10	μA
Bus Leakage Current, Bus Positive	I_{LKP_CAN}	TxD High	-10	–	10	μA
Bus Input Threshold	V_{ih}	Normal, High-Speed Mode, $6.0 \leq V_{BAT} \leq 27 \text{ V}$	2.0	2.1	2.2	V
Bus Input Threshold Low Battery	V_{ihlb}	Normal, $5.0 \text{ V} < V_{BAT} < 6.0 \text{ V}$	1.6	1.7	2.2	V
Fixed Wake-Up Input High Voltage Threshold	$V_{ihWuFix}$ (Note 4)	Sleep Mode, $V_{BAT} > 11.2 \text{ V}$	6.6	–	7.9	V
Offset Wake-Up Input High Voltage Threshold	$V_{ihWuOffset}$ (Note 4)	Sleep Mode	$V_{BAT} - 4.3$	–	$V_{BAT} - 3.25$	V

LOAD

Voltage on Switched Ground Pin	V_{LOAD}	$I_{LOAD} = 5.0 \text{ mA}$	–	–	0.5	V
Voltage on Switched Ground Pin	V_{LOAD_LOB}	$I_{LOAD} = 7.0 \text{ mA}$, $V_{BAT} = 0 \text{ V}$	–	–	1.0	V
Load Resistance During Loss of Battery	R_{LOAD_LOB}	$V_{BAT} = 0$	$R_{LOAD} - 10\%$	–	$R_{LOAD} + 35\%$	Ω

4. Thresholds not tested in production, guaranteed by design.

5. Leakage current in case of loss of ground is the summary of both currents I_{LKN_CAN} and I_{LKN_LOAD} .

NCV7356

ELECTRICAL CHARACTERISTICS (continued) ($V_{BAT} = 5.0$ to 27 V, $T_A = -40$ to $+125^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
----------------	--------	-----------	-----	-----	-----	------

TXD, MODE0, MODE1

High Level Input Voltage	V_{ih}	$5.0 < V_{BAT} < 27$ V	2.0	–	–	V
Low Level Input Voltage	V_{il}	$5.0 < V_{BAT} < 27$ V	–	–	0.8	V
TxD Pull Up Current	$-I_{L_TXD}$	TxD = L, MODE0 and 1 = H $5.0 < V_{BAT} < 27$ V	20	–	50	μA
MODE0 and 1 Pull Down Resistor	R_{MODE_pd}		20	–	40	$\text{k}\Omega$

RxD

Low Level Output Voltage	V_{ol_rxd}	$I_{RxD} = 2.0$ mA	–	–	0.4	V
High Level Output Leakage	I_{ih_rxd}	$V_{RxD} = 5.0$ V	–10	–	10	μA
RxD Output Current	I_{rxd}	$V_{RxD} = 5.0$ V	–	–	70	mA

INH

High Level Output Voltage	V_{oh_INH}	$I_{INH} = -180$ μA	$V_{BAT} - 0.8$	$V_{BAT} - 0.5$	–	V
Leakage Current	I_{INH_lk}	MODE0 = MODE1 = L, INH = 0 V	–5.0	–	5.0	μA

TIMING MEASUREMENT LOAD CONDITIONS

Normal and High Voltage Wake-Up Mode		High-Speed Mode
min load / min tau	3.3 kohm / 540 pF	Additional 140 ohm tool resistance to ground in parallel
min load / max tau	3.3 kohm / 1.2 nF	
max load / min tau	200 ohm / 5.0 nF	Additional 120 ohm tool resistance to ground in parallel
max load / max tau	200 ohm / 20 nF	

ELECTRICAL CHARACTERISTICS (5.0 V ≤ V_{BAT} ≤ 27 V, -40°C ≤ T_A ≤ 125°C, unless otherwise specified.)

AC CHARACTERISTICS (See Figures 2, 3, and 4)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Transmit Delay in Normal and Wake-Up Mode, Bus Rising Edge (Note 6)	t _{Tr}	min and max loads per Page 9	2.0	–	6.3	μs
Transmit Delay in Wake-Up Mode to V _{ihWU} , Bus Rising Edge (Note 7)	t _{TWUr}	min and max loads per Page 9	2.0	–	18	μs
Transmit Delay in Normal Mode, Bus Falling Edge (Note 8)	t _{Tf}	min and max loads per Page 9	1.8	–	10	μs
Transmit Delay in Wake-Up Mode, Bus Falling Edge (Note 8)	t _{TWU1f}	min and max loads per Page 9	3.0	–	13.7	μs
Transmit Delay in High-Speed Mode, Bus Rising Edge (Note 9)	t _{THSr}	min and max loads per Page 9	0.1	–	1.5	μs
Transmit Delay in High-Speed Mode, Bus Falling Edge (Note 10)	t _{THSf}	min and max loads per Page 9	0.1	–	3.0	μs
Receive Delay, All Active Modes (Note 11)	t _{DR}	CANH High to Low Transition	0.3	–	1.0	μs
Receive Delay, All Active Modes (Note 11)	t _{RD}	CANH Low to High Transition	0.3	–	1.0	μs
Input Minimum Pulse Length, All Active Modes (Note 11)	t _{mpDR} t _{mpRD}	CANH High to Low Transition CANH Low to High Transition	0.15 0.15	– –	1.0 1.0	μs
Wake-Up Filter Time Delay	t _{WUF}	See Figure 3	10	–	70	μs
Receive Blanking Time After TxD L–H Transition	t _{rb}	See Figure 4	0.5	–	6.0	μs
TxD Timeout Reaction Time	t _{tout}	Normal and High-Speed Mode	–	20	–	ms
TxD Timeout Reaction Time	t _{toutwu}	Wake-Up Mode	–	30	–	ms
Delay from Normal to High-Speed and High Voltage Wake-Up Mode	t _{dnhs}	–	–	–	30	μs
Delay from High-Speed and High Voltage Wake-Up to Normal Mode	t _{dhsn}	–	–	–	30	μs
Delay from Normal to Standby Mode	t _{dsby}	V _{BAT} = 6.0 V to 27 V	–	–	500	μs
Delay from Sleep to Normal Mode	t _{dsnwu}	V _{BAT} = 6.0 V to 27 V	–	–	50	μs
Delay from Standby to Sleep Mode	t _{dsleep}	V _{BAT} = 6.0 V to 27 V	100	250	1000	ms

6. The maximum signal delay time for a bus rising edge is measured from V_{cmos_il} on the TxD input pin to the V_{ihMax} + V_{goff} max level on CANH at maximum network time constant, minimum signal delay time for a bus rising edge is measured from V_{cmos_ih} on the TxD input pin to 1 V on CANH at minimum network time constant. These definitions are valid in both normal and High Voltage Wake-Up (HVWU) mode.
7. The maximum signal delay time for a bus rising edge in HVWU mode is measured from V_{cmos_il} on the TxD input pin to the V_{ihWuMax} + V_{goff} max level on CANH at maximum network time constant, minimum signal delay time for a bus rising edge is measured from V_{cmos_ih} on the TxD input pin to 1 V on CANH at minimum network time constant.
8. Maximum signal delay time for a bus falling edge is measured from V_{cmos_ih} on the TxD input pin to 1 V on CANH at maximum network time constant, minimum signal delay time for a bus falling edge is measured from V_{cmos_il} on the TxD input pin to the V_{ihMax} + V_{goff} max level on CANH. These definitions are valid in both normal and HVWU mode.
9. The signal delay time in high-speed mode for a bus rising edge is measured from V_{cmos_il} on the TxD input pin to the V_{ihMax} + V_{goff} max level on CANH at maximum high-speed network time constant.
10. The signal delay time in high-speed mode for a bus falling edge is measured from V_{cmos_ih} on the TxD input pin to 1 V on CANH at maximum high-speed network time constant.
11. Receive delay time is measured from the rising / falling edge crossing of the nominal V_{ih} value on CANH to the falling (V_{cmos_il_max}) / rising (V_{cmos_ih_min}) edge of RxD. This parameter is tested by applying a square wave signal to CANH. The minimum slew rate for the bus rising and falling edges is 50 V/μs. The low level on bus is always 0V. For normal mode and high-speed mode testing the high level on bus is 4 V. For HVWU mode testing the high level on bus is V_{BAT} – 2 V.

BUS LOADING REQUIREMENTS

Characteristic	Symbol	Min	Typ	Max	Unit
Number of System Nodes	–	2	–	32	–
Network Distance Between Any Two ECU Nodes	Bus Length	–	–	60	m
Node Series Inductor Resistance (If required)	R_{ind}	–	–	6.0	Ω
Ground Offset Voltage	V_{goff}	–	$0.1 \times V_{BAT}$	1.5	V
Ground Offset Voltage	$V_{gofflowbat}$	–	–	0.7	V
Device Capacitance (Unit Load)	C_{ul}	135	150	300	pF
Network Total Capacitance	C_{tl}	396	–	19000	pF
Device Resistance (Unit Load)	R_{ul}	6435	6490	6565	Ω
Device Resistance (Min Load)	R_{min}	2000	–	–	Ω
Network Total Resistance	R_{tl}	200	–	3332	Ω
Network Time Constant (Note 12)	τ	1.0	–	4.0	μs
Network Time Constant in High-Speed Mode	τ	–	–	1.5	μs
High-Speed Mode Network Resistance to GND	R_{load}	75	–	135	Ω

12. The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emission. The maximum value is selected to ensure proper communication modes. Not all combinations of R and C are possible.

TIMING DIAGRAMS

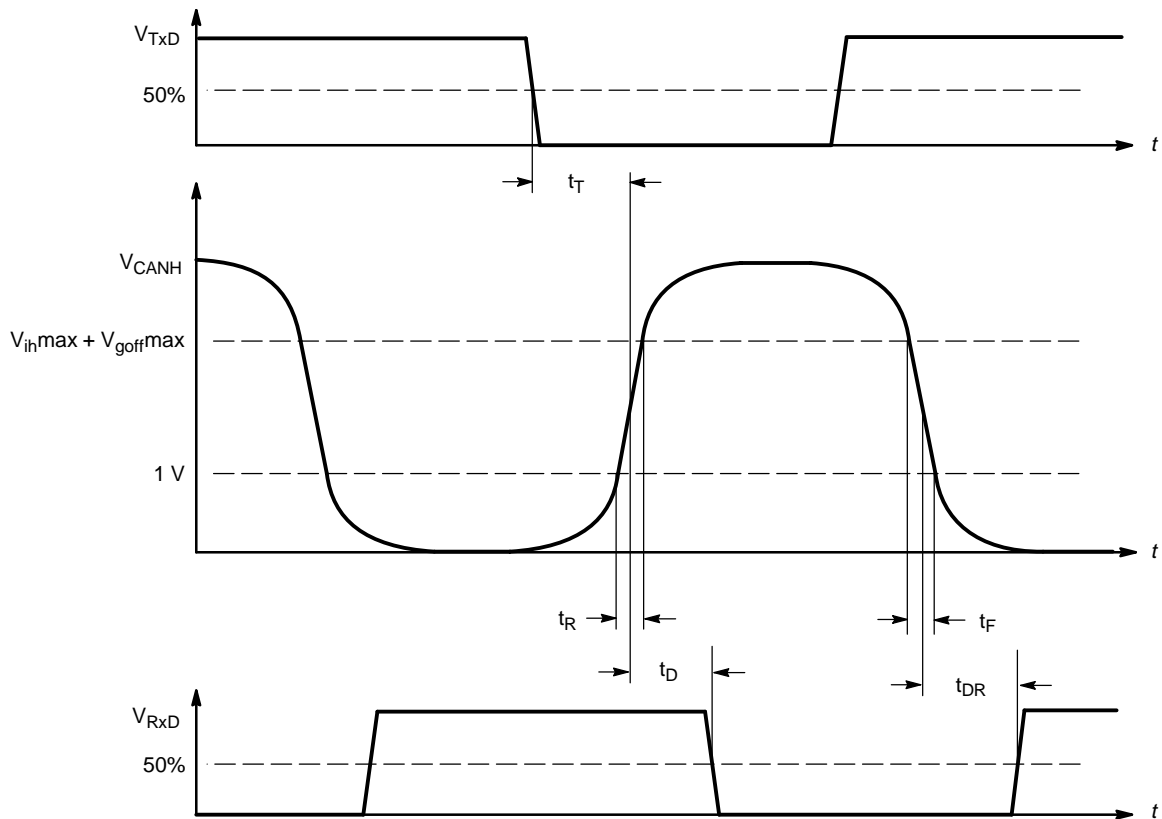


Figure 2. Input/Output Timing

TIMING DIAGRAMS

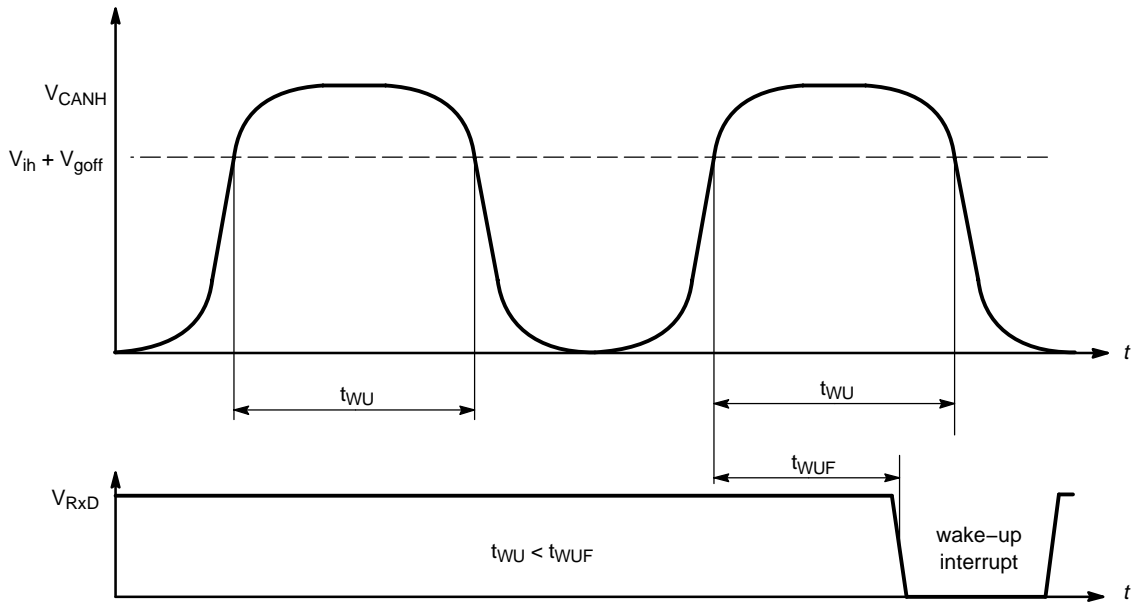


Figure 3. Wake-Up Filter Time Delay

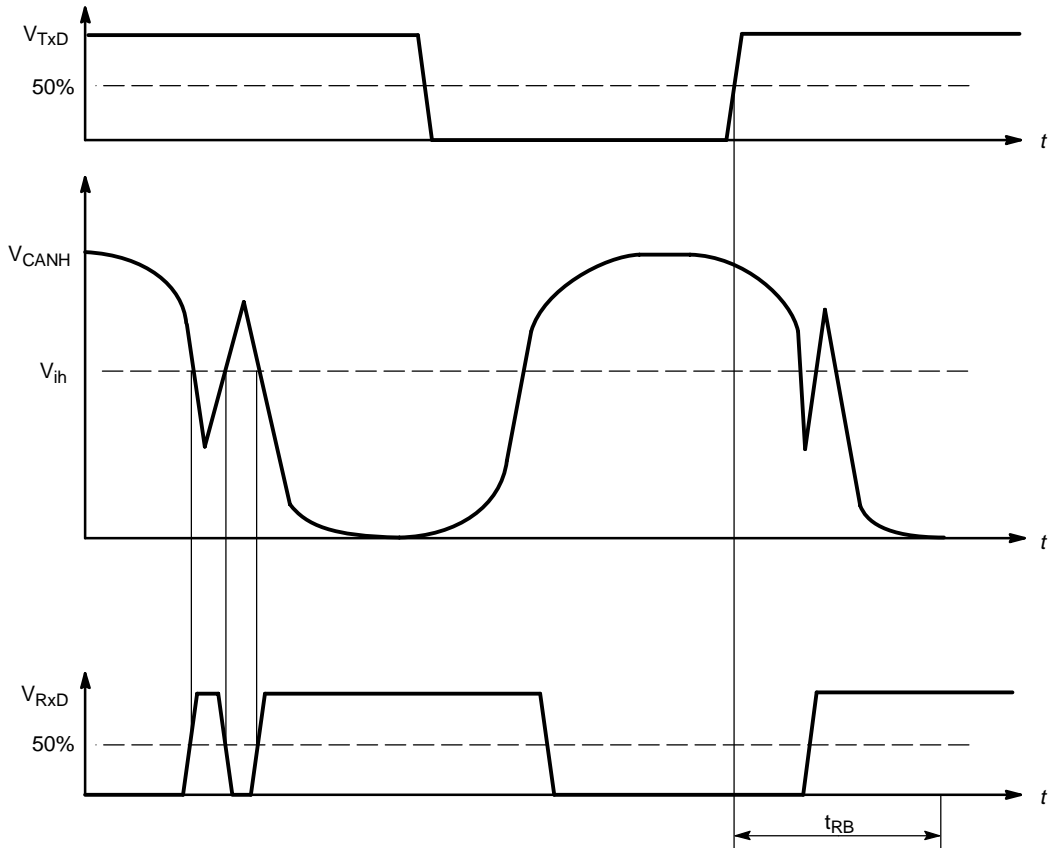


Figure 4. Receive Blanking Time

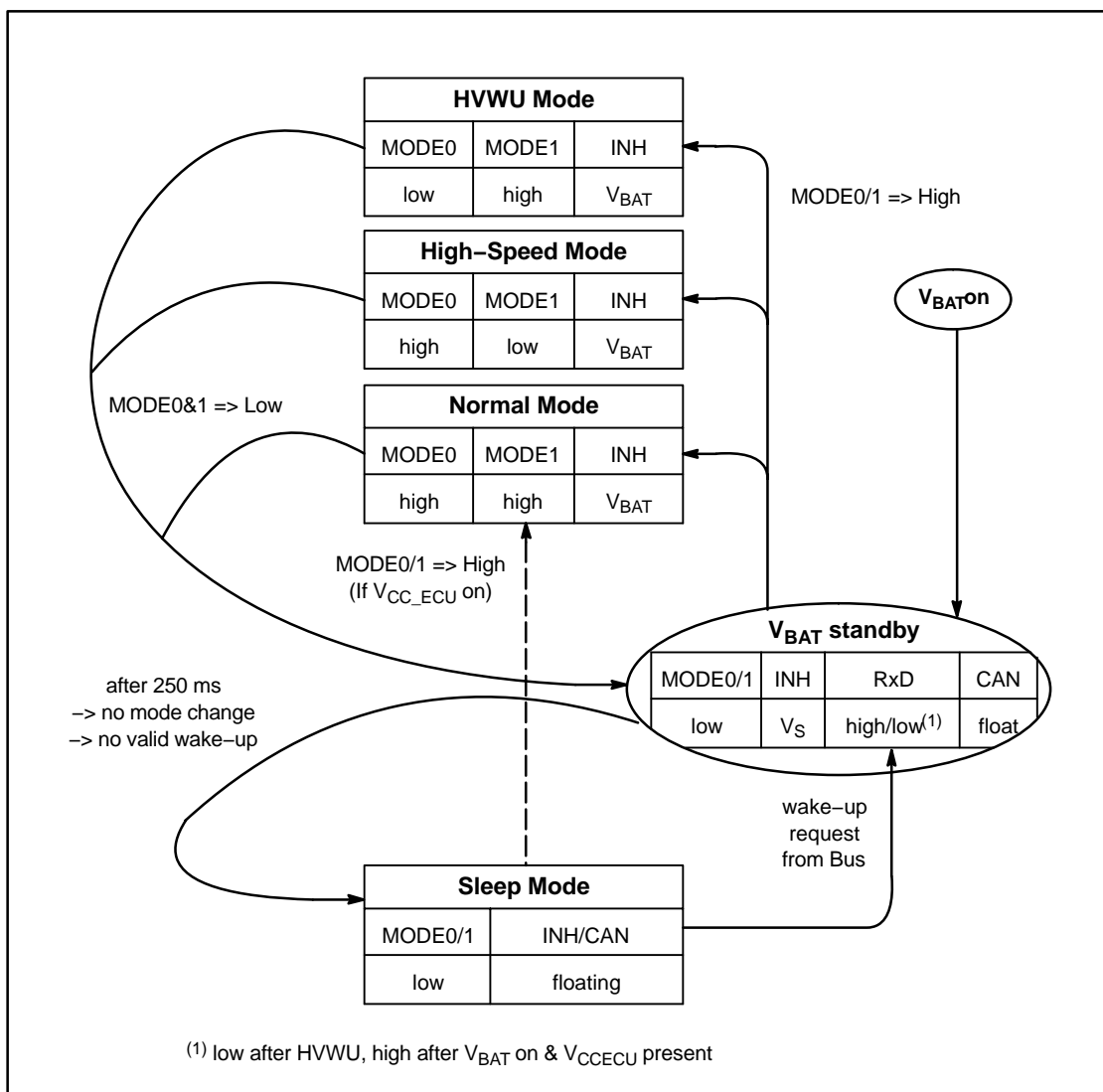
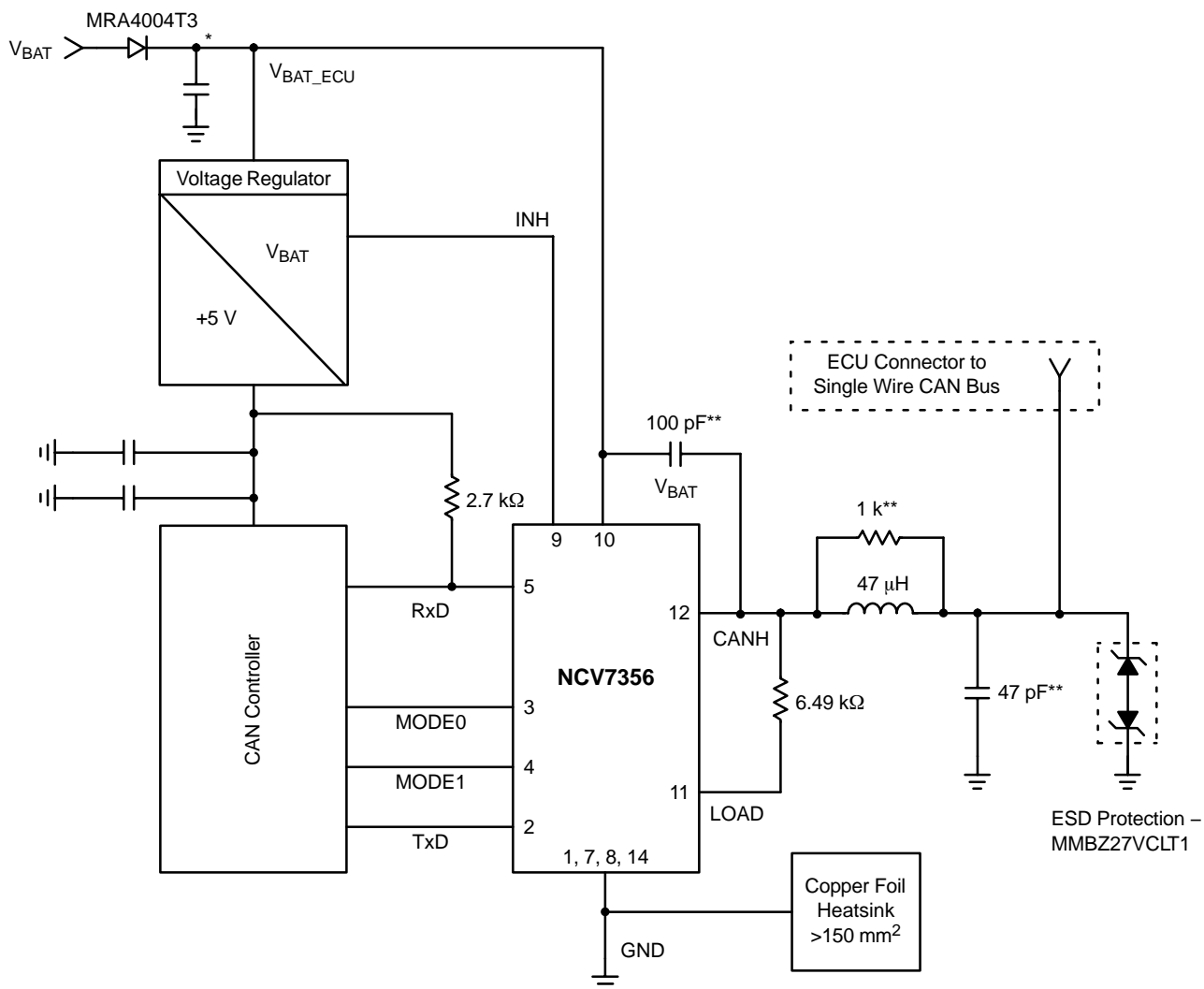


Figure 5. State Diagram

NCV7356



*Recommended capacitance at $V_{BAT_ECU} > 1.0 \mu F$ (immunity to ISO7637/1 test pulses)

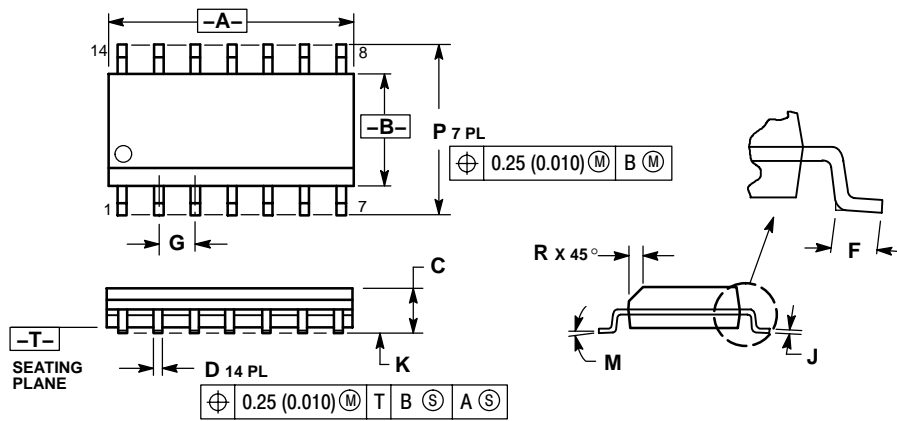
** Components to reduce EMC.

Figure 6. Application Circuitry

NCV7356

PACKAGE DIMENSIONS


SOIC-14
D SUFFIX
CASE 751A-03
ISSUE G



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.