General Description

The PMB 2306, PMB 2307 PLL are high speed CMOS ICs are especially designed for use in battery-powered radio equipment and mobile telephones. The intended application will be in GSM, PCN, DECT and other digital mobile systems. The wide range of dividing ratios also allows application in analog systems.

The circuit consists of a reference-, A- and N-counter, a dual-modulus-control logic, a phase detector with charge pump and a serial control logic. The setting of the operating mode and the selection of the counter ratios is done serially at the ports CLK, DA and EN.

The operating modes allow the selection of single or dual operation, asynchronous or synchronous data acquisition, 4 different antibacklash-impulse times, 8 different PD-output current modes, polarity setting of the PD-output signal, adjustment of the trigger-edge of the MOD-output signal, 2 standby modes and the control of the multifunction outputs MFO1 and MFO2.

The reference frequency is applied at the RI input and scaled down by the R-counter. Its maximum value is 50 MHz. The VCO frequency is applied at the FI input and scaled down by the N- or N/A-counter according to single or dual-mode operation. The maximum value at FI is 220 MHz at single-, and 65 MHz at dual-mode operation.

The phase detector is frequency and phase sensitive. It produces a phase detector signal with adjustable anti-backlash impulses in order to prevent a dead zone at very small phase deviations. Phase differences smaller than 100 ps can therefore be resolved.

Programming of the IC is done by a serial data control. The contents of the messages are assigned to the functional units according to the destination address. Single or dual-mode operation as well as asynchronous or synchronous data acquisition is set by status 2 and should therefore precede the programming of the counters.

The PMB 2306/PMB 2307 offer the possibility of synchronous data acquisition to avoid error signals at the phase detector due to non-corresponding dividing factors in the counters produced by asynchronous loading.

Synchronous programming guarantees control during changes of frequency or channel. That means that the state of the phase detector or the phase difference is kept maintained, and in case of “lock in”, the control process starts with the phase difference “zero”.

Synchronous transmission is particularly advantageous when large transfers in channel are to be made in a specific short transient recovery time. For this purpose a larger reference frequency is switched to in order to achieve rapid-“rough”-transient response, increasing the bandwidth of the loop at the time. When reaching the “quasi lock-in” state, the reference frequency is switched back to its original values.

Type	Package
PMB 2306-T	P-DSO-14-1 (SMD)
PMB 2306-R	P-TSSOP-16-1 (Shrink, SMD)
PMB 2307-R	P-TSSOP-16-1 (Shrink, SMD)

Adjustment to the “actual” value then takes place with the usual transient response as for small transfers in channel. The synchronous transmission ensures that no additional phase errors arise due to the change of reference frequencies.

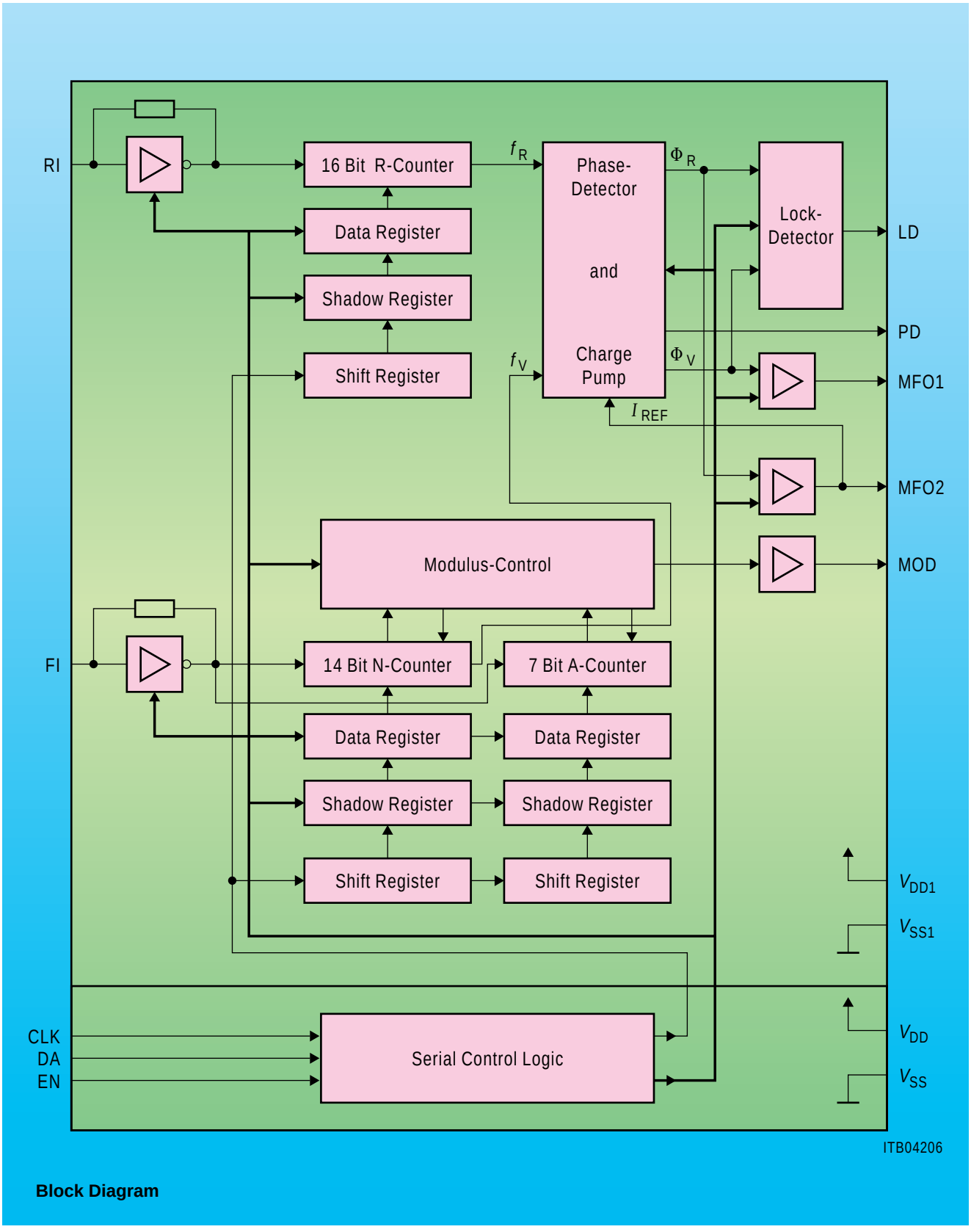
The PMB 2306/2307 has two standby modes (standby1, 2) to reduce the current consumption.

- Standby1 switches off the whole circuit, the current consumption is reduced to below 1 µA.
- Standby2 switches off the counters, the charge pump and the outputs, only the preamplifiers stay active.

The standby modes do not affect the port output signal. For the influence on the other output signals see standby table.

Features

- Low operating current consumption
- Low operating voltage
  PMB 2306: 3 V to 5.5 V
  PMB 2307: 2.7 V to 5.5 V
- High input sensitivity, high input frequencies (220 MHz)
- Extremely fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Synchronous programming of the counters (N-, N/A-, R-counters) and system parameters
- Fast modulus switchover for 65-MHz operation
- Switchable modulus trigger edge
- Large dividing ratios for small channel spacing
  – A-scaler 0 to 127
  – N-scaler 3 to 16380
  – R-scaler 3 to 65535
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 5 MHz)
- Switchable polarity and rate of trimming rise of the phase detector
- 2 multifunction outputs
- Digital phase detector output signals (e.g. for external charge pump)
- f_{rn}, f_{yn} outputs of the R- and N-scalers
- Port 1 output (e.g. for standby of the prescaler)
- External current setting for PD output
- Lock detect output with gated antibacklash pulse (quasi digital lock detect)



Block Diagram