Si3232PPT0-EVB

EVALUATION BOARD FOR THE Si3232 DUAL PROSLIC

Description

This document describes the operation of the Silicon Laboratories Si3232 Dual ProSLIC™ device evaluation platform. The Dual ProSLIC evaluation platform is designed to provide observation of the ProSLIC's functionality. The Dual ProSLIC platform consists of a ProSLIC motherboard, an Si3232 daughter card (Si3232DC0-EVB), and the ProSLIC LINC™ software. The ProSLIC LINC software is a GUI-based program that can run in Microsoft Windows® environments.

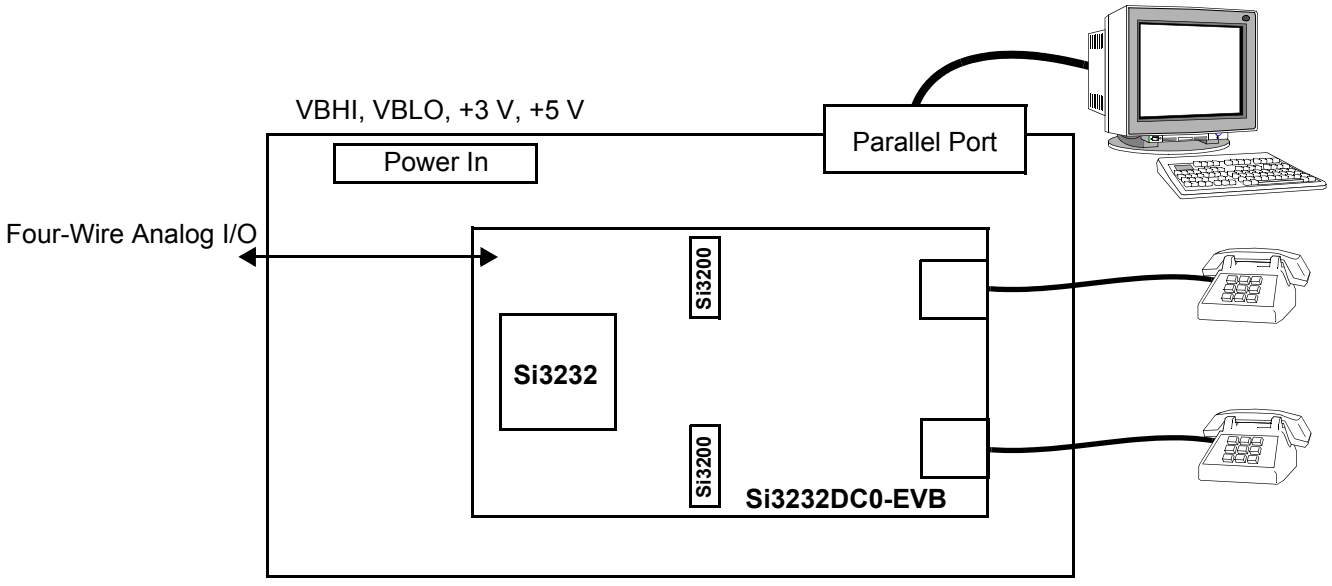
Equipment requirements:

- PC running Windows 95, 98, ME, NT, or 2000
- 5 V, 1 A power supply
- 3 V, 1 A power supply (optional)
- –24 V, 0.5 A power supply
- –75 V, 0.5 A power supply
- Balanced audio generator and analyzer (optional)
  (e.g., Audio Precision System 2 and/or HP TIMS set and/or Wandel and Goltermann PCM-4)

Features

- Silicon Laboratories Dual ProSLIC device
- All components necessary for linecard implementation
- Layout for optional secondary protections
- Control I/O through standard parallel port
- On-board oscillator for stand-alone operation
- PCM I/O set up for Audio Precision System 2 or Wandel and Goltermann PCM-4
- Full access to PCM highway
- Daisy-chain connection for multiple boards
- Si3232 power selection for 3 or 5 V operation

Functional Block Diagram



ProSLIC LINC Evaluation Software

The ProSLIC LINC software is an executable program that allows control and monitoring of the ProSLIC. It utilizes the primary LPT port of a standard PC to communicate to the ProSLIC's SPI port.

To install the software, insert the Silicon Laboratories ProSLIC CD into the computer. The setup routine can be invoked by running the setup.exe program in the root directory of the CD.

Invoking the ProSLIC LINC is achieved by double clicking the ProSLIC LINC icon. Refer to the ProSLIC LINC User Guide for software operation.

Si3232PPT0-EVB Dual ProSLIC Evaluation Board Description

The schematics for the Dual ProSLIC evaluation daughter card are shown in Figures 1 through 3. The schematic in Figure 1 shows the Dual ProSLIC linecard implementation. All circuitry pertaining to the telephony function of the Dual ProSLIC is found here. Four-wire analog is present on JP3 and JP4. Figure 2 contains a number of options for secondary fault protection. Secondary protection components can be selected for a given level of protection against expected faults. Figure 3 is the schematic that describes the serial control interface, daisy chain ports, and power supply filtering and connections. These schematics represent typical linefeed components for the ProSLIC.

The layout of the Dual ProSLIC evaluation daughter card is found in Figures 4–8. Figure 4 shows the component placement while Figures 5 and 8 show the two layers of component interconnect. Figures 6 and 7 show the inner ground and VDD planes. The signal flow is four-wire analog on the left to two-wire analog on the right.

Signal requirements for ProSLIC operation are PCLK (PCM clock), FS (frame sync), and Serial IO. The ProSLIC motherboard has a local oscillator with a programmable logic device to provide the ProSLIC PCLK and FS signals. The DIP switch (S2) sets the PCLK frequency and controls the FS enable. See Table 1 for S2 settings. JP3 and JP4 select this internal clock source or an external PCM clock source. The ProSLIC motherboard has been designed with digital PCM interfaces (P2, P3, J8, and J11). These connections are not used with the Si3232 Dual ProSLIC. J9 and J10 allow access to the ProSLIC's clock inputs for connection to an actual telephone system's clocks. TIP and RING of the two-wire analog interface is present at the RJ-11 connectors, J1 and J11 of the Dual ProSLIC daughter card.

The schematics of the ProSLIC motherboard are found in Figures 9, 10, and 11. Figure 9 shows the connections from the motherboard to the daughter card. Figure 10 illustrates the LPT port connection to the SPI drivers. The PCM highway and LED indicators are shown in Figure 11.

The ProSLIC evaluation board is voltage programmable with specific jumper settings. JP1 selects 3 V for ProSLIC operation. JP2 selects 3 V or 5 V PCM source level compatibility. These should be placed on the expected setting.

Power is connected to the ProSLIC at J2, J3 and J4. The 5 V is always required for the buffers, U2 and U3, to interface to the parallel port. The ProSLIC can be powered from 5 V or 3 V with the placement of a jumper on JP1. The Protection Return connections on J6 should be connected to an appropriate ground for TIP/RING fault testing. This return is tied to signal ground on-board though it has a dedicated trace for high current conditions. Serial control of the ProSLIC is achieved by toggling select bits of a standard parallel port. The parallel port connection is available at P1 and J1.

Multiple dual ProSLIC cards can be daisy-chained by stacking the cards. Stack up to eight cards by aligning JS1–JS5 and pressing together. The ProSLIC LINC Software allows channel selection for RAM and register manipulation.

Si3232PPT0-EVB Dual ProSLIC Evaluation Platform Setup

To prepare the Dual ProSLIC evaluation platform for use, perform the following steps:

1. Set power supplies to 3.3 V, 5 V, –24 V, and –75 V.
2. With these supplies off, connect them to J2, J3, and J4 corresponding to the silk screen designators.
3. Connect the PC's parallel port (LPT1) to P1 (or J1) using a 25 pin D male-to-male cable.
4. Select the on-board clock source or external clock source with JP3 and JP4.
5. TIP/RING connection can be made from the RJ-11s to a phone or telephony test equipment.
6. Invoke the ProSLIC LINC software.
7. Turn the power supplies on and press the ProSLIC motherboard reset button (S1).
8. Click the "Reinitialize" button in the ProSLIC LINC software panel.

The Dual ProSLIC is now ready to perform its linecard function.

To achieve an end-to-end connection with 600 Ω:

1. Verify that R11 is shorted.
2. Click RESET.
3. Click REINITIALIZE.
4. Click REGISTER SET.
5. Click Broadcast box.
6. Write "1" to LINEFEED register.

This connects the evaluation platform end-to-end per daughter card RF-11 connector pairs.

Table 1. On-Board PCLK Settings (S2)

S2-1,2,3	S2-4	S2-5	S2-6	S2-7	S2-8
PCLK frequency	unused	unused	unused	unused	FS enable
0,0,0 = 8.192 MHz 0,0,1 = 4.096 MHz 0,1,0 = 2.048 MHz 0,1,1 = 1.024 MHz 1,x,x = 512 kHz	x	x	x	x	0 = FS disabled 1 = FS enabled
Note: 1 = on.					

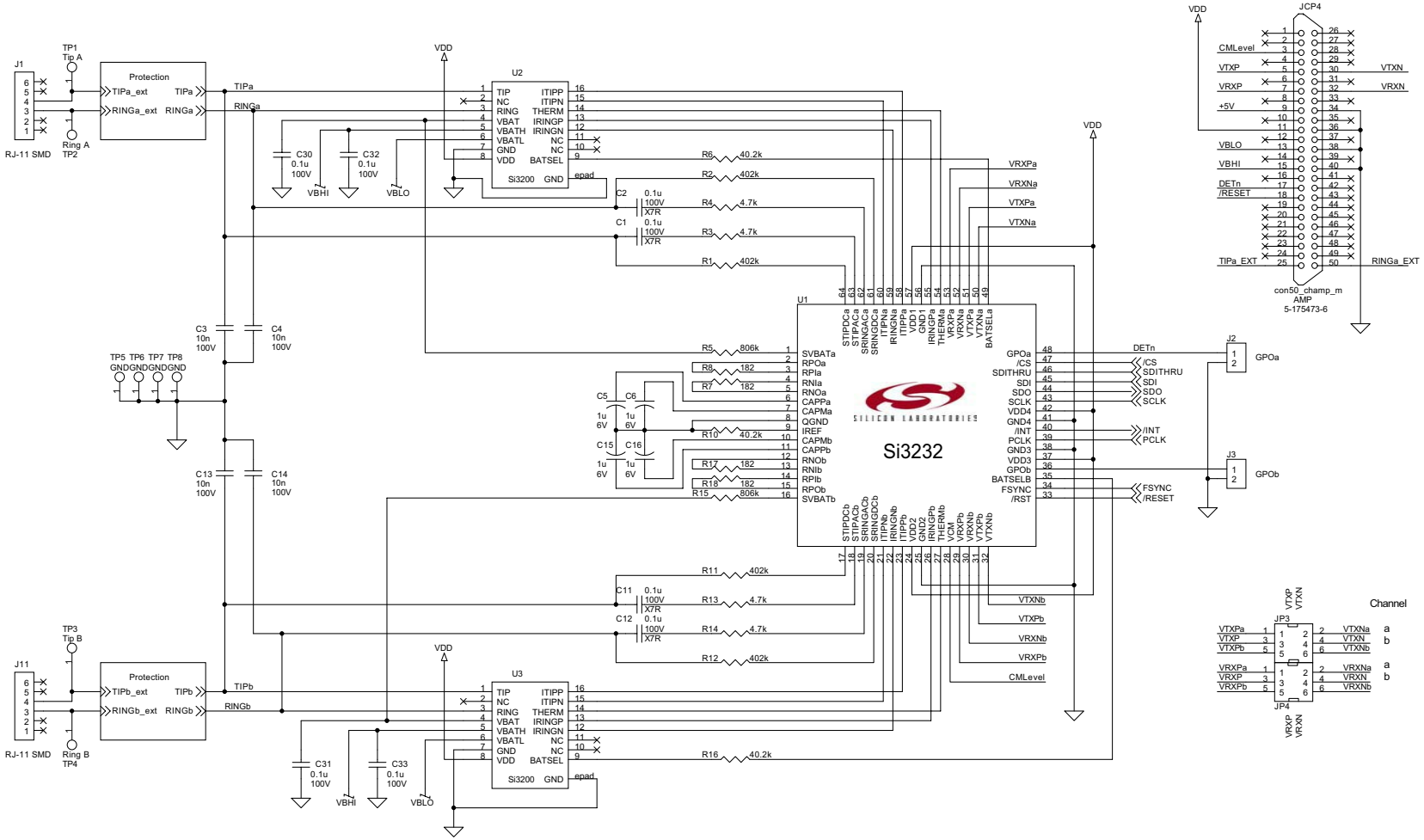


Figure 1. Si3232DC0-EVB Evaluation Circuit (1 of 3)

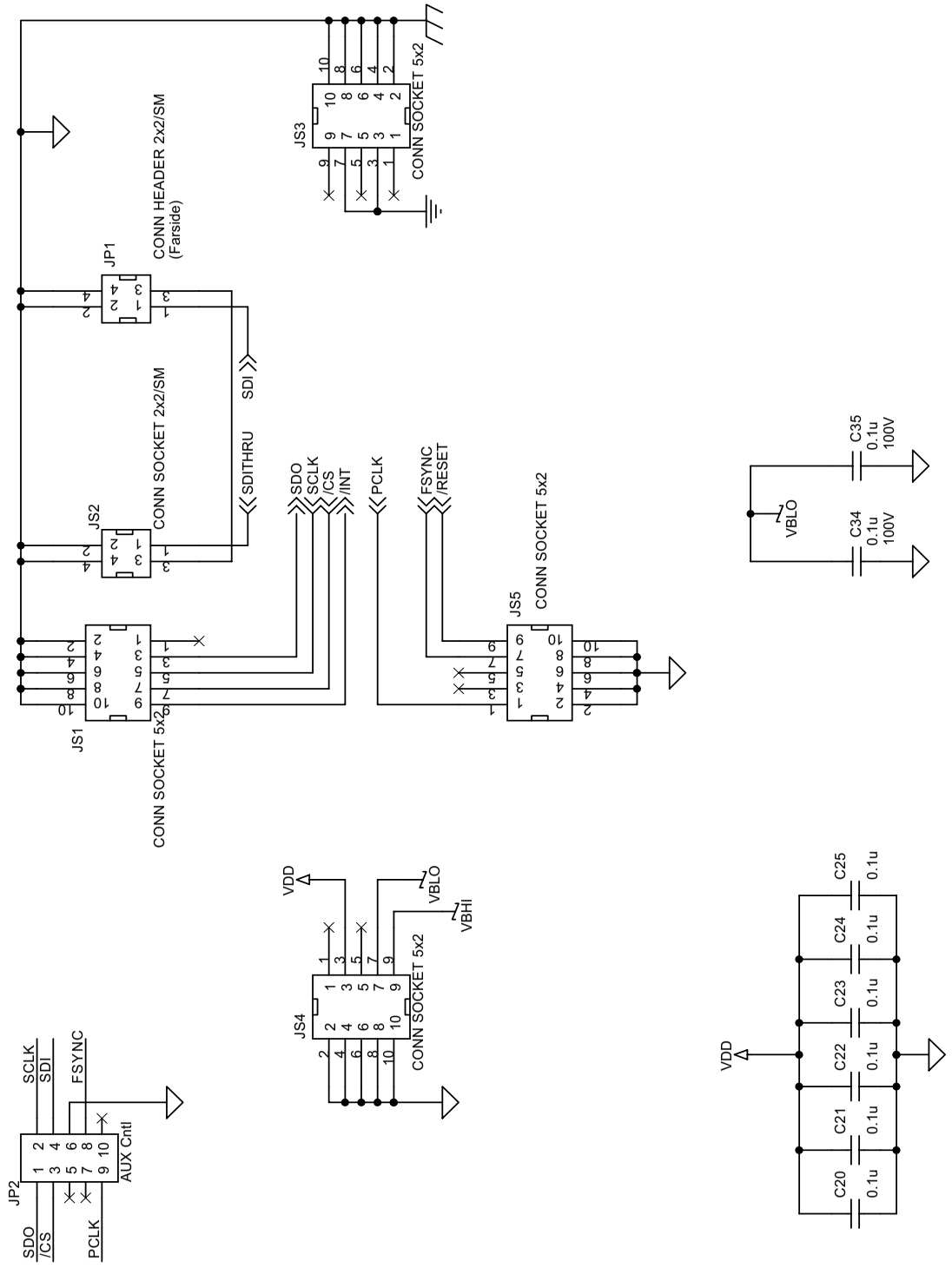
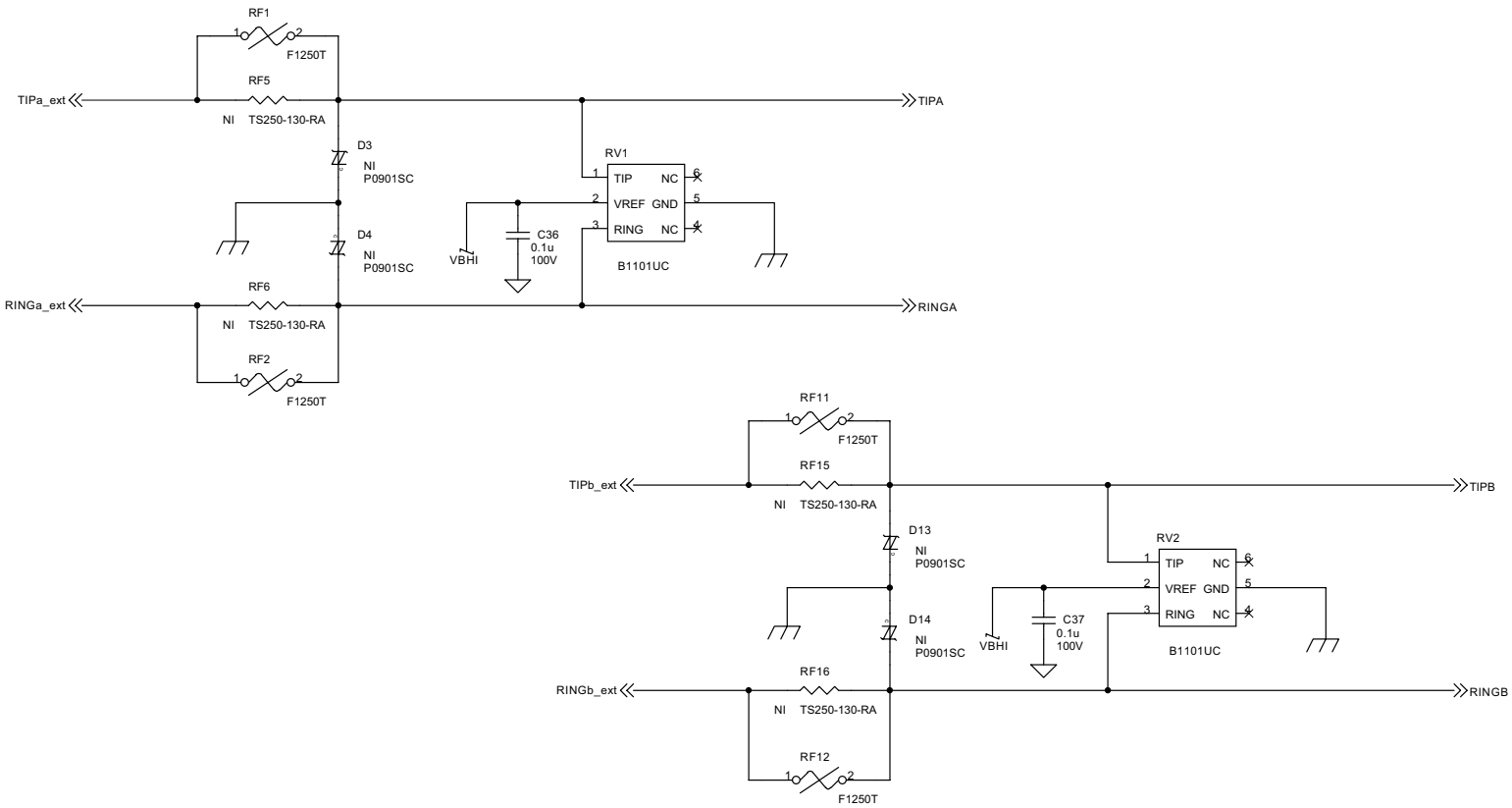


Figure 2. Si3232DC0-EVB Evaluation Circuit (interconnect) (2 of 3)



* Optional protection devices:
Battery tracking over voltage protection devices are required when using maximum battery voltage on Si3200.
Fixed voltage thyristor protection devices, D3, D4, D13, D14 can be used in certain cases. The selection of the thyristor device voltage depends on the required battery voltage for ringing. The maximum clamp voltage for the device must be under the Si3200 maximum voltage. The minimum clamping voltage of the device must be above the maximum battery voltage. For example, the Teccor P0901SC is shown for applications that operate from a maximum negative battery of -72V.
Over current devices should be selected for application requirements and over voltage protection device current limitations.

Figure 3. Si3232DC0-EVB Evaluation Circuit (protection) (3 of 3)

Bill of Materials

Table 2. Si3232DC0-EVB Application Circuit

Component(s)	Value	Function
C1, C2, C11, C12	100 nF, 100 V, X7R, ±20%	Filter capacitors for TIP, RING ac sensing inputs.
C3, C4, C13, C14	10 nF, 100 V, X7R, ±20%	TIP/RING compensation capacitors.
C5, C15	1 μF, 6.3 V, X7R, ±20%	Low pass filter capacitors to stabilize common mode SLIC feedback loops.
C6, C16	1 μF, 6.3 V, X7R, ±20%	Low pass filter capacitors to stabilize differential SLIC feedback loops.
C30–C33	0.1 μF, 100 V, Y5V	Decoupling for battery voltage supply pins.
C20–C25	0.1 μF, 10 V, Y5V	Decoupling for analog and digital chip supply pins.
R1, R2, R11, R12	402 kΩ, 1/10 W, ±1%	Sense resistors for TIP and RING voltage sensing nodes.
R3, R4, R13, R14	4.7 kΩ, 1/10 W, ±1%	Sense resistors for TIP, RING ac sensing inputs.
R5, R15	806 kΩ, 1/10 W, ±1%	Sense resistor for battery voltage sensing nodes.
R6, R16	40.2 kΩ, 1/10 W, ±5%	Sets bias current for battery switching circuit.
R7, R8, R17, R18	182 Ω, 1/10 W, ±1%	Bias resistors for internal transconductance amplifier.
R10	40.2 kΩ, 1/10 W, ±1%	Generates a high accuracy reference current.

Table 3. Si3232DC0-EVB Protection Circuit

Component(s)	Description	Function/Comments
C36, C37	0.1 μF, 100 V, Y5V	Decoupling for B1101UC.
D3, D4, D13, D14*	Teccor P0721SC transient voltage suppressor	Overvoltage protection (optional).
RF1, RF2, RF11, RF12	Teccor F1250T, 250 V/1.25 A, TeleLink® fuse	Overcurrent protection.
RF5, RF6, RF15, RF16*	Raychem TS-250-130-RA resettable fuse	Overcurrent protection PTC (optional).
RV1, RV2	Teccor B1101UC Dual Negative BATTRAX® SLIC Protector or Bourns TISP61089B	Battery-tracking overvoltage protection.
***Note:** Optional protection components not used on Si3232DC0-EVB. Usage depends on application.		

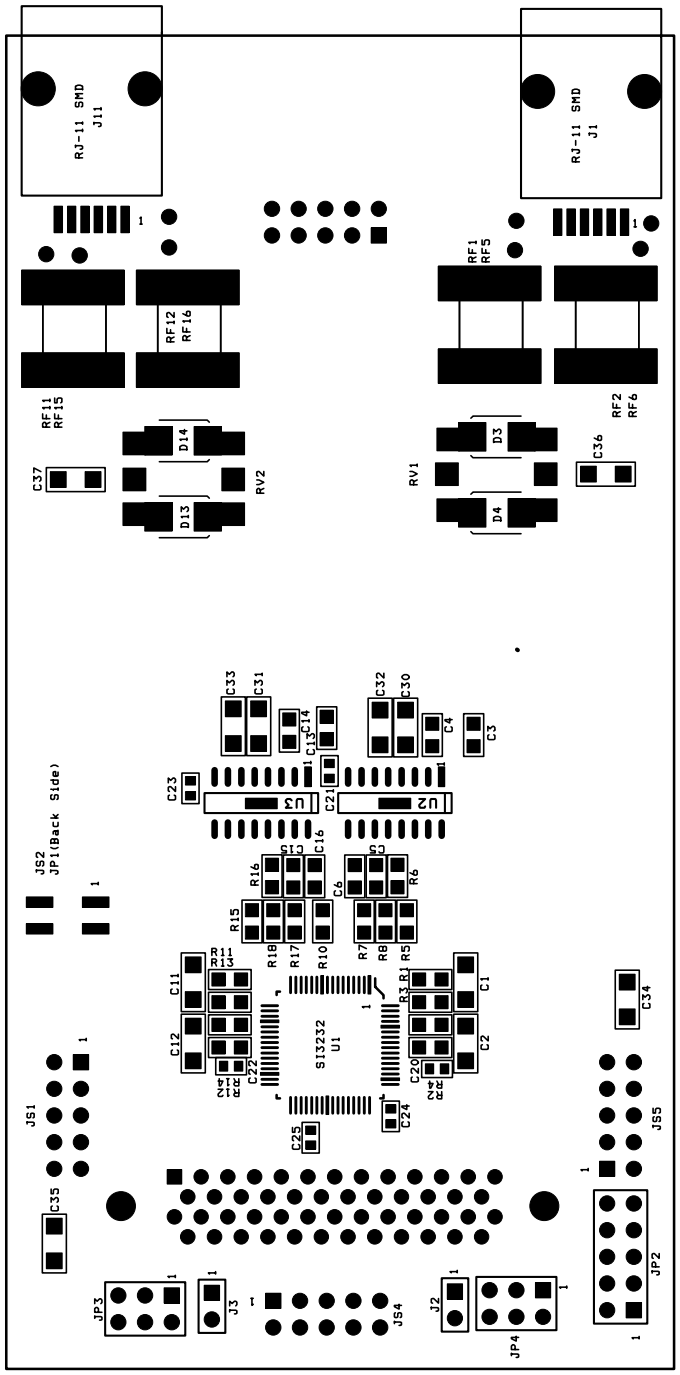


Figure 4. Si3232DC0-EVB Silkscreen

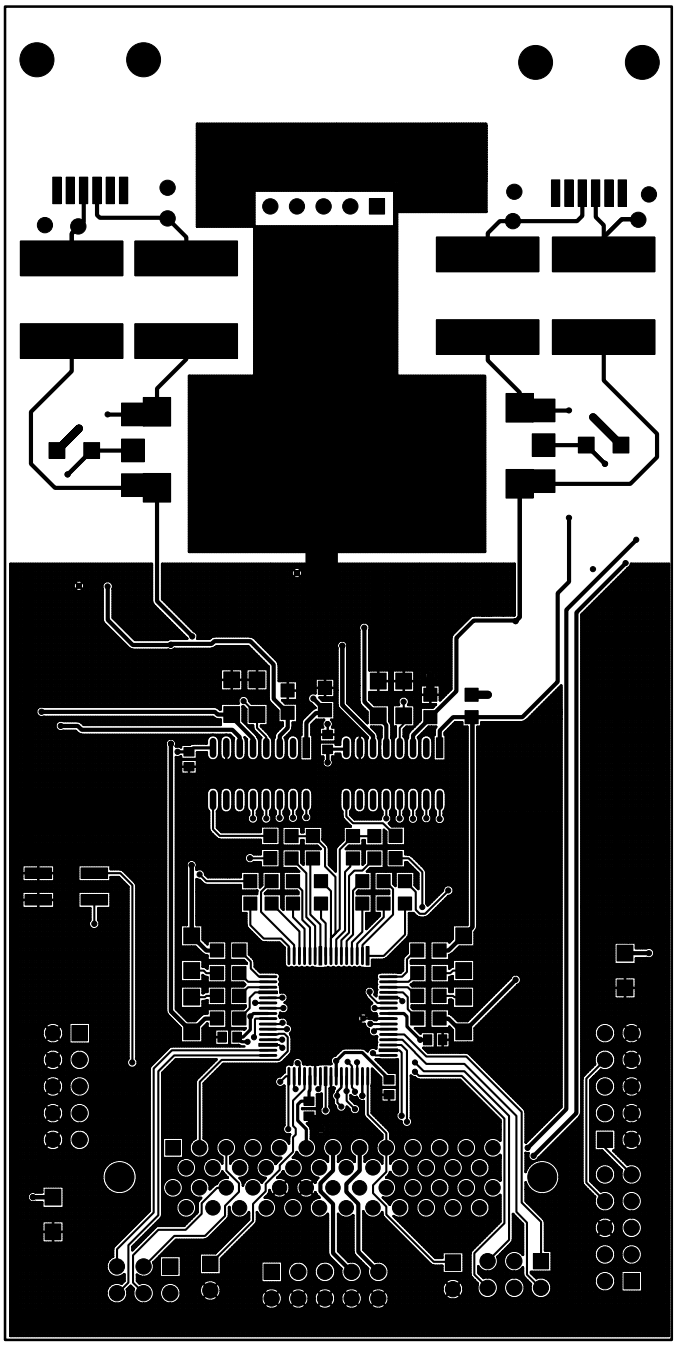


Figure 5. Si3232DC0-EVB Component Side

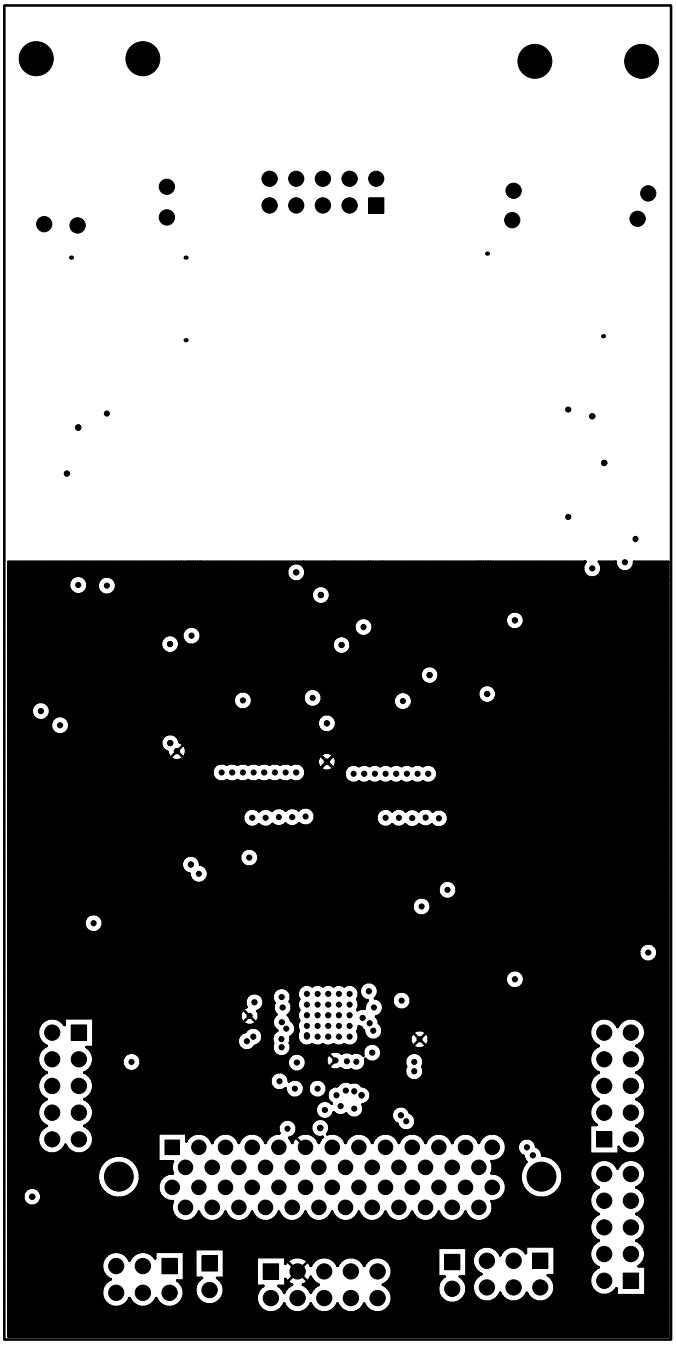


Figure 6. Si3232DC0-EVB Power

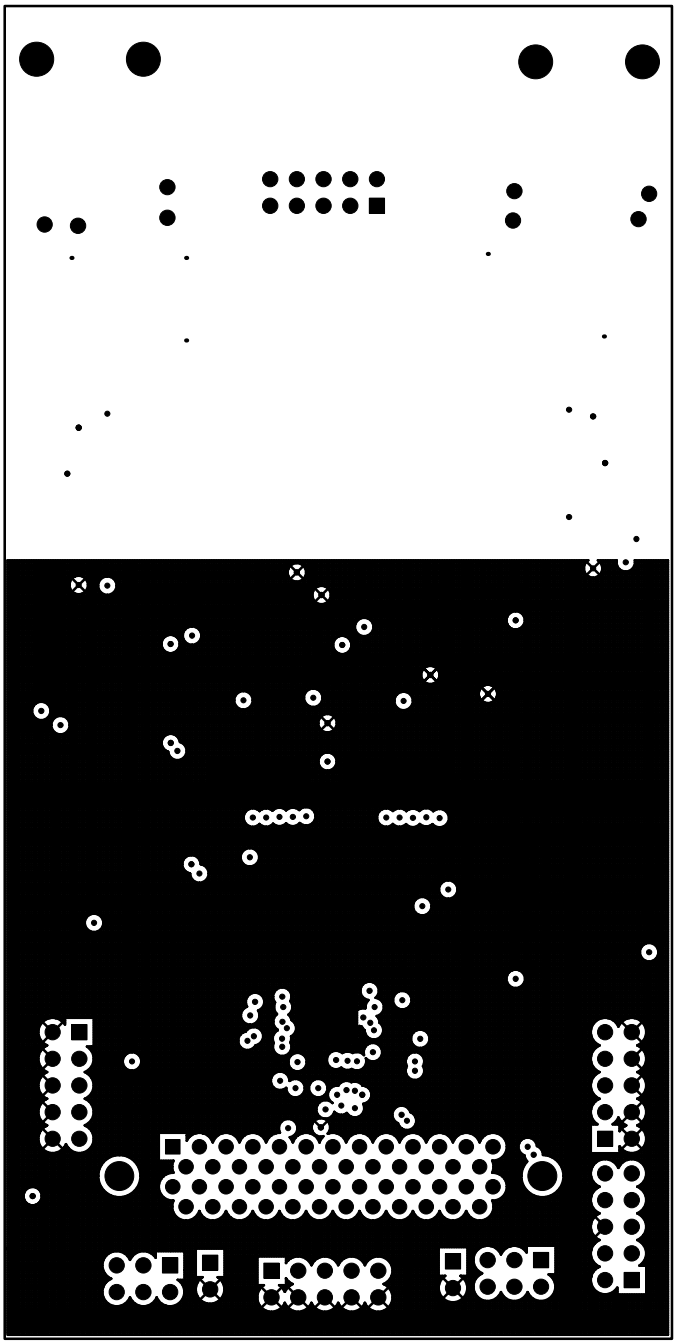


Figure 7. Si3232DC0-EVB Ground

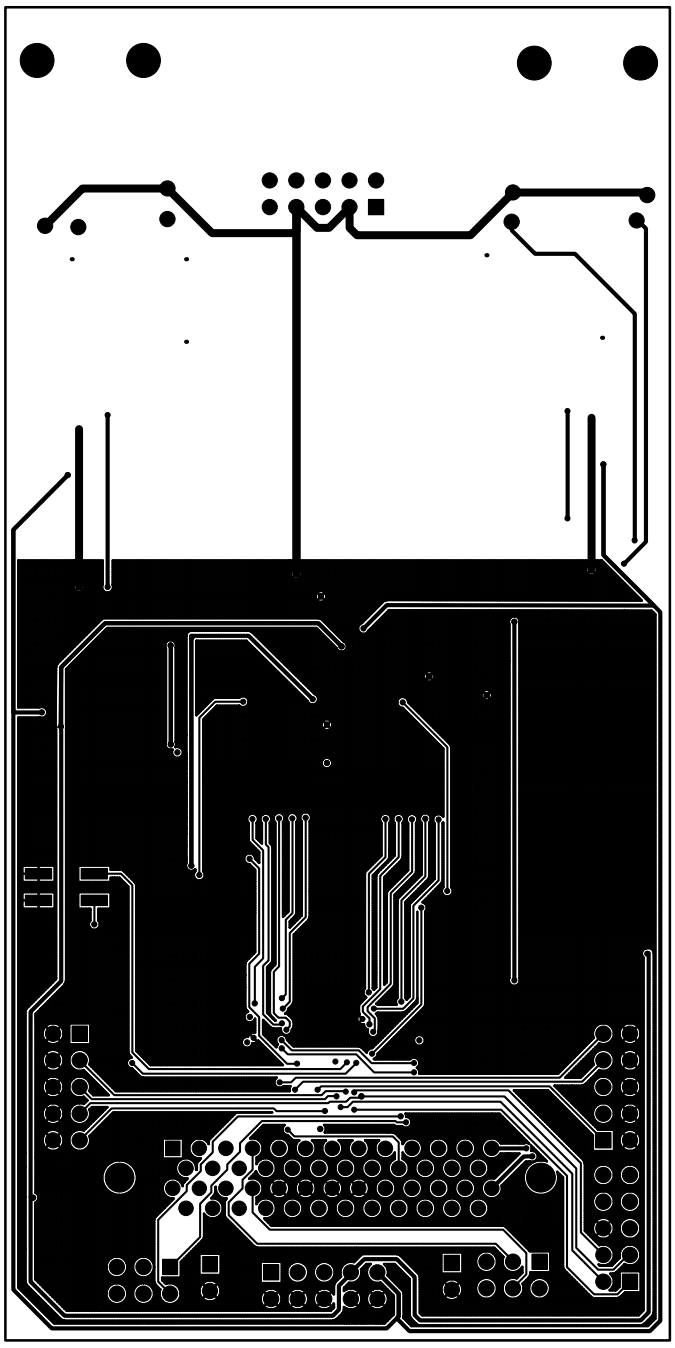


Figure 8. Si3232DC0-EVB Solder Side

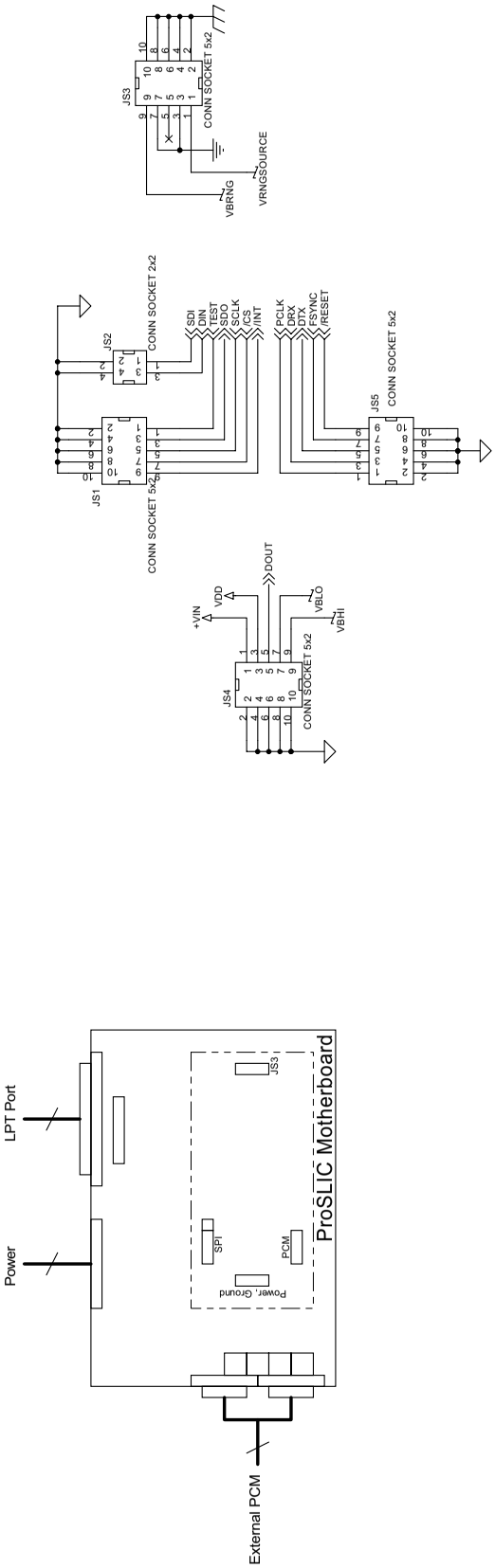


Figure 9. ProSLIC Motherboard (ProSLIC IF)

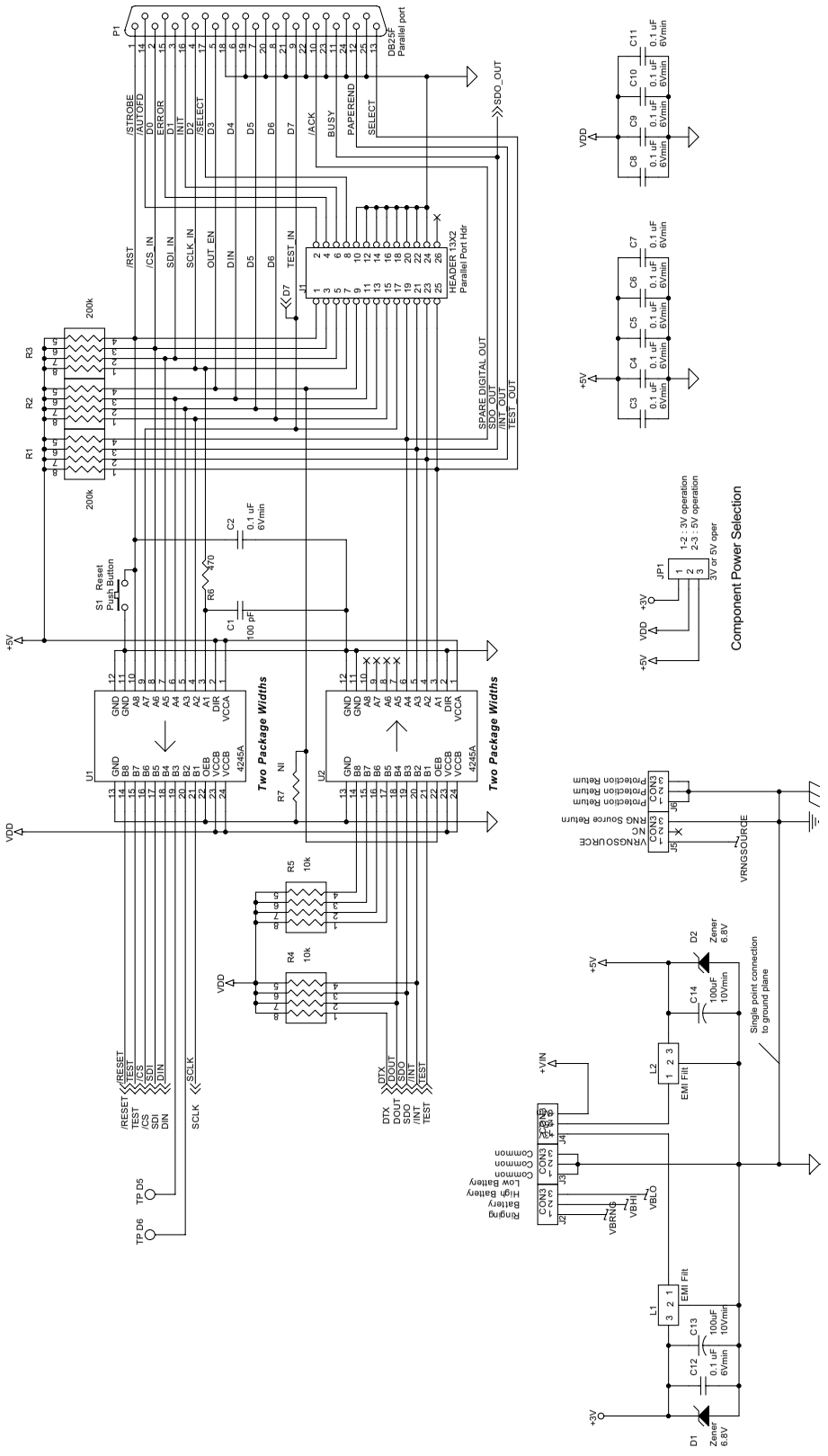


Figure 10. ProSLIC Motherboard (LPT to SPI)

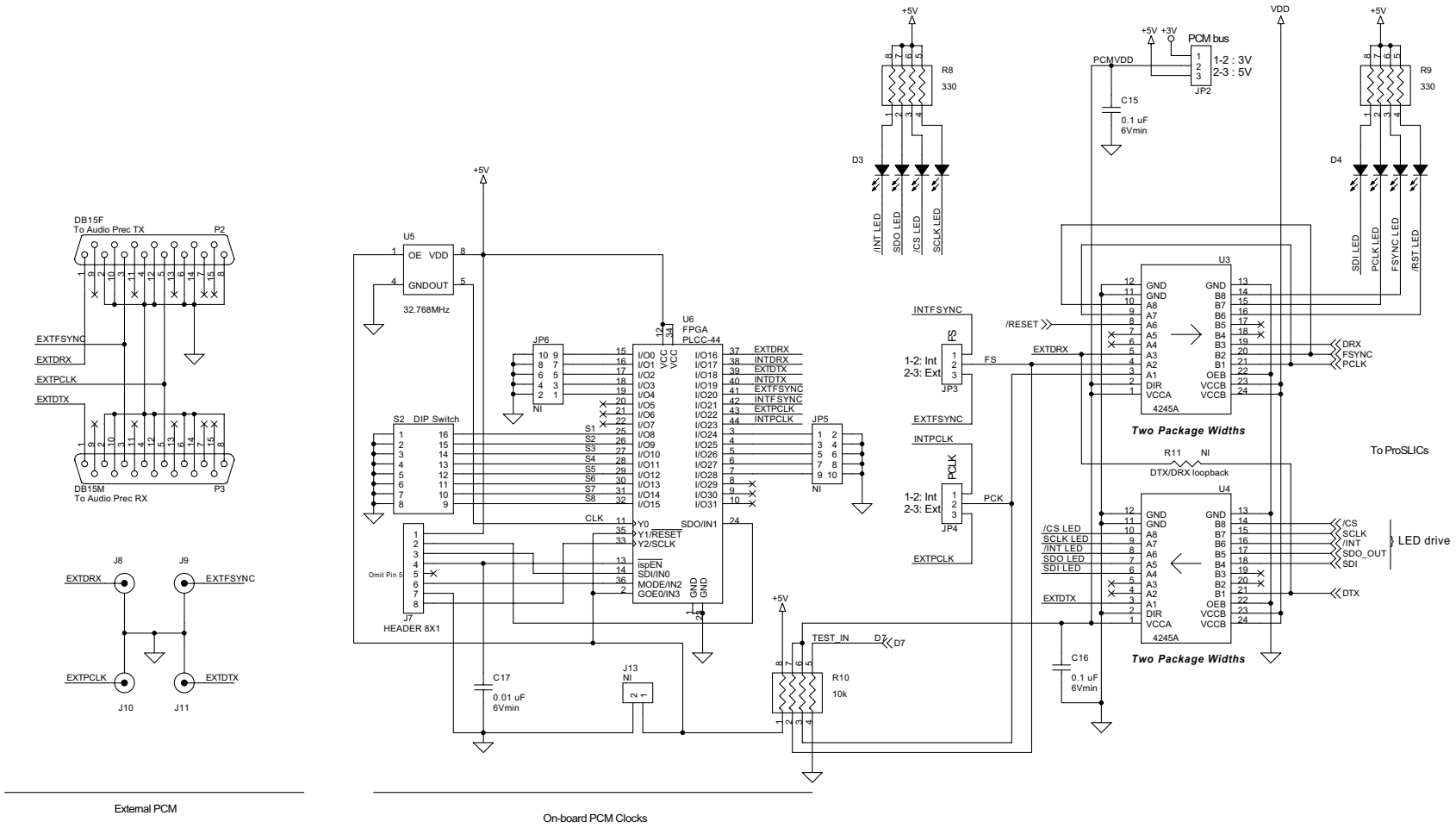


Figure 11. ProSLIC Motherboard (PCM)

Document Change List

Revision 0.92 to Revision 1.0

- "Functional Block Diagram" on page 1 updated.
- "Si3232PPT0-EVB Dual ProSLIC Evaluation Board Description" on page 2 updated.
- Figures 1 through 11 updated.

Notes:

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