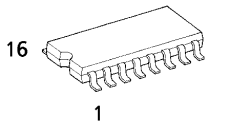
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC175F, TC74VHC175FN, TC74VHC175FT

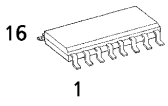
QUAD D-TYPE FLIP-FLOP WITH CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

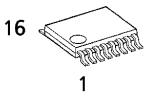
The TC74VHC175 is an advanced high speed CMOS QUAD D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
These four flip-flops are controlled by a clock input (CK) and a clear input ($\overline{CLR}$).
The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and $\overline{Q}$1 thru $\overline{Q}$4) on the positive-going edge of the clock pulse.
When the $\overline{CLR}$ input is held low, the Q outputs are at the low logic level and the $\overline{Q}$ outputs are at the high logic level, regardless of other input conditions.
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

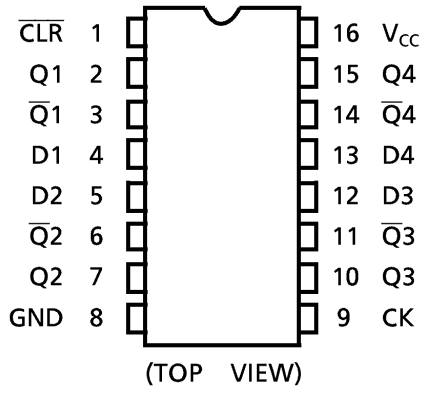


FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

FEATURES:

- High Speed ····· f_{MAX} = 210MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V~5.5V
- Low Noise ····· V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74 ALS175

PIN ASSIGNMENT



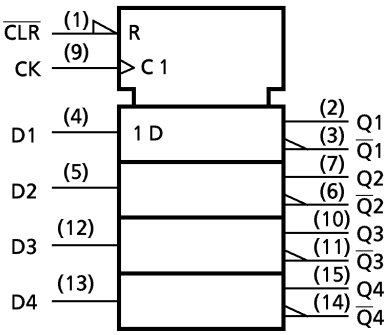
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLR}$	D	CK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

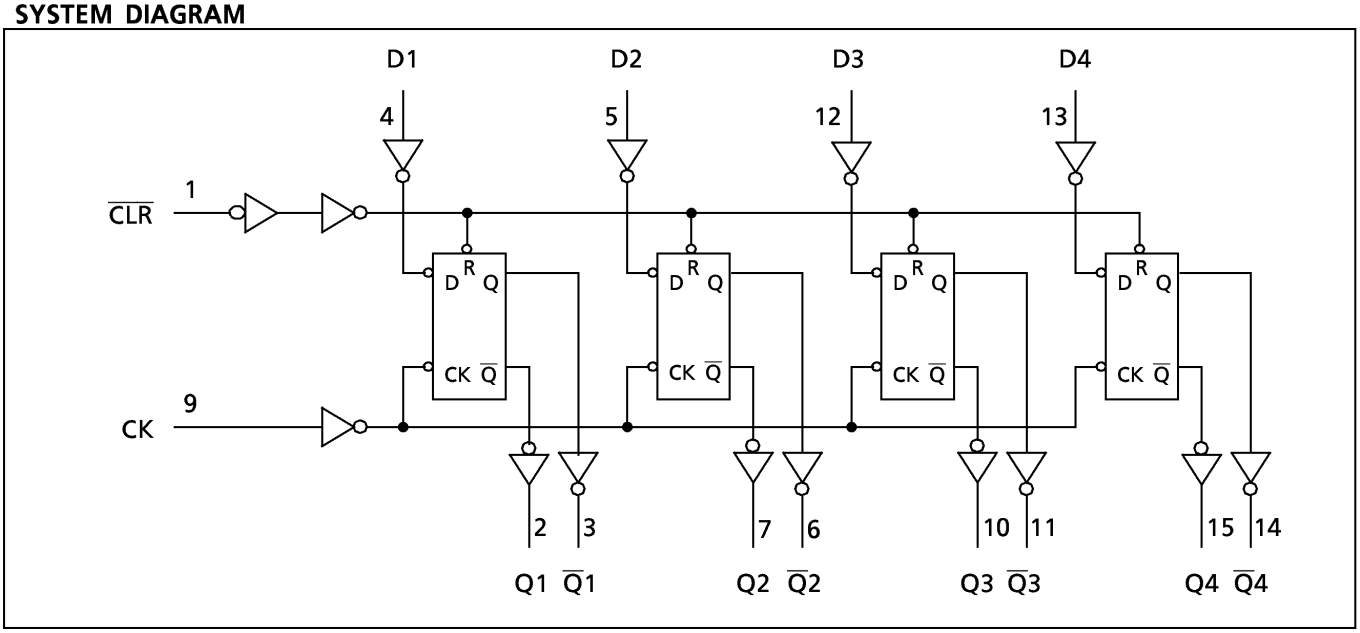
X : Don't Care

IEC LOGIC SYMBOL



980910EBA2

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	$V_{CC}\times0.7$	—	—	$V_{CC}\times0.7$	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	$V_{CC}\times0.3$	—	$V_{CC}\times0.3$	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = −40~85°C	UNIT
				TYP .	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3 ± 0.3	—	5.0	5.0	ns
	$t_{W(H)}$		5.0 ± 0.5	—	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	
Minimum Set - up Time	t_s		3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	4.0	4.0	
Minimum Hold Time	t_h		3.3 ± 0.3	—	1.0	1.0	
			5.0 ± 0.5	—	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3 ± 0.3	—	5.0	5.0	
			5.0 ± 0.5	—	5.0	5.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q,$\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	7.5	11.5	1.0	13.5	ns
				50	−	10.0	15.0	1.0	17.0	
			5.0 ± 0.5	15	−	4.8	7.3	1.0	8.5	
				50	−	6.3	9.3	1.0	10.5	
Propagation Delay Time ($\overline{CLR}$-Q,$\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	−	6.3	10.1	1.0	12.0	
				50	−	8.8	13.6	1.0	15.5	
			5.0 ± 0.5	15	−	4.3	6.4	1.0	7.5	
				50	−	5.8	8.4	1.0	9.5	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	90	140	−	75	−	MHZ
				50	50	75	−	45	−	
			5.0 ± 0.5	15	150	210	−	125	−	
				50	85	115	−	75	−	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	−	−	1.5	−	1.5	ns
			5.0 ± 0.5	50	−	−	1.0	−	1.0	
Input Capacitance	C_{IN}				−	4	10	−	10	pF
Pwer Dissipation Capacitance	C_{PD}	(Note 2)			−	44	−	−	−	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per bit)}$$

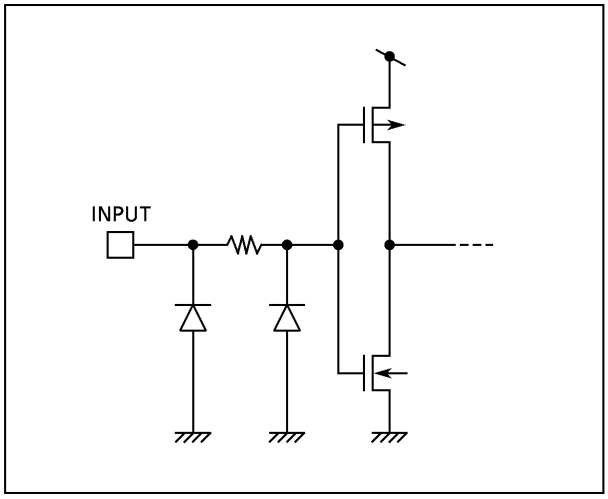
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation:

$$C_{PD} \text{ (total)} = 30 + 14 \cdot n$$

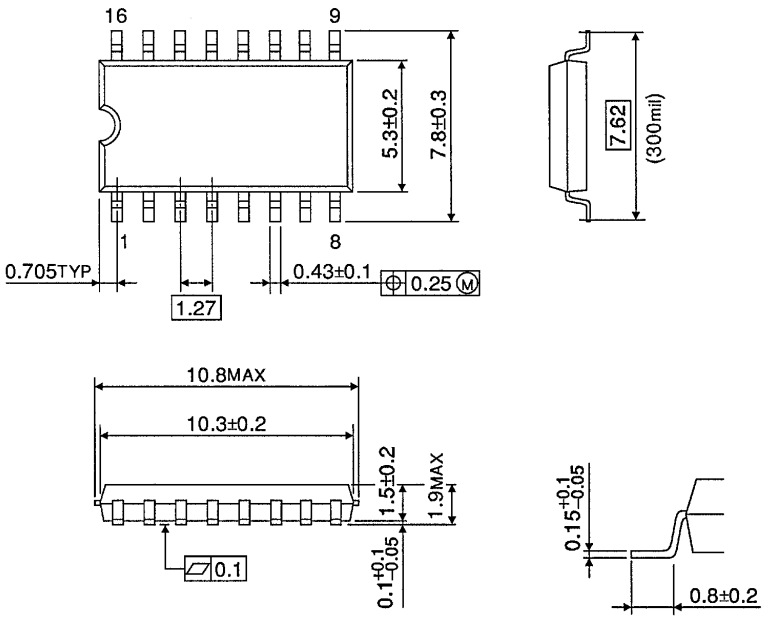
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	C_L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	C_L = 50pF	5.0	−0.4	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	C_L = 50pF	5.0	−	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	C_L = 50pF	5.0	−	1.5	V

INPUT EQUIVALENT CIRCUIT



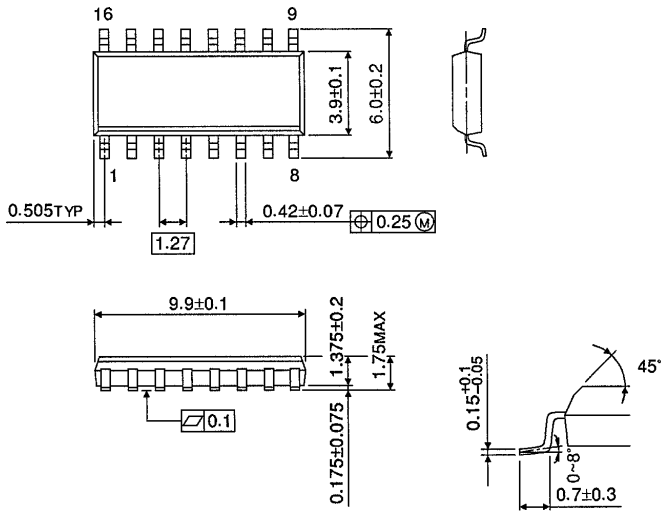
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

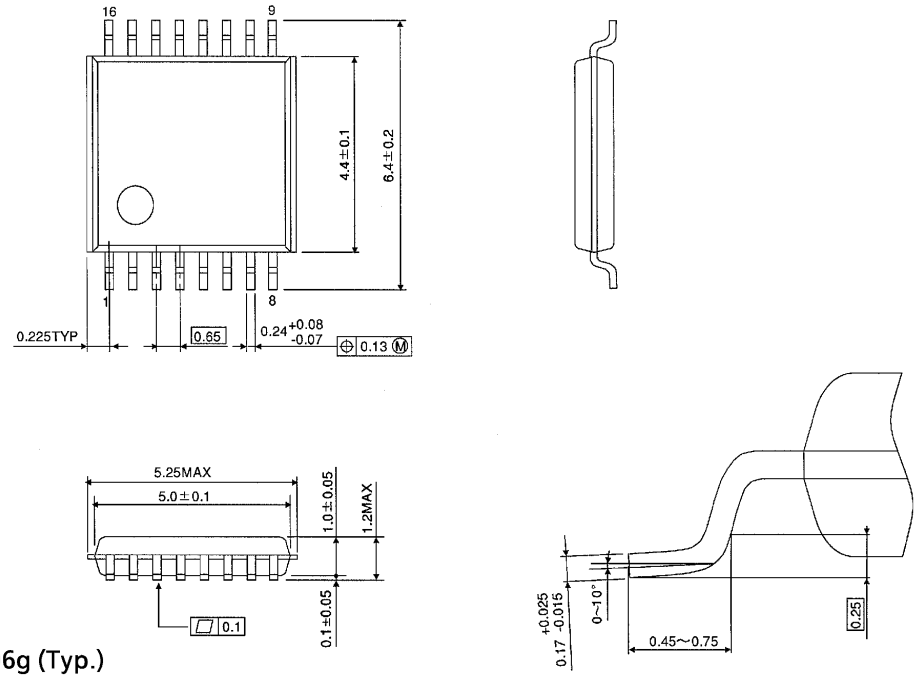
SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)