# PM73122

# SBI™ Configuration Between PM73122 AAL1gator™-32 and PM8315 TEMUX™

# Application Note

**Preliminary**

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PMC-2001770, (P1)

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## References

- PMC-1981419 "ATM Adaptation Layer 1 Segmentation and Reassembly Processor-32 Data Sheet", Issue 5, May 4, 2000.
- PMC-2000421 "PM73122 AAL1gator-32 Revision A Device Errata Sheet", Issue 3, November 2000.
- PMC-1991820 "32/8/4 Link CES/DBCES AA1 SAR Programmer's Guide", Issue 1, January, 2000.
- PMC-1981125 "High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer Telecom Standard Product Data Sheet", Issue 5, January 2000.
- PMC-1990495 "High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer Telecom Standard Product Register Descriptions", Issue 3, December 1999.

- PMC-1990677 “PM8315 TEMUX Datasheet/Register Description Errata”, Issue 7, July, 2000.
- PMC-1991268 “TEMUX Programmer’s Guide”, Issue 1, April 2000.

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# 1 Introduction

This application note serves as a reference aid for engineers developing software for the Scaleable Bandwidth Interconnect (SBI™) bus. The SBI bus is one way of interconnecting the PM73122 AAL1gator™-32 to the PM8315 TEMUX™ or the PM5365 TEMAP.

## 1.1 Device Definitions

- The PM73122 AAL1gator™-32 is a single-chip device used to carry constant bit rate (CBR) or "circuit" traffic over ATM networks.
- The PM8315 TEMUX is an integrated circuit that combines 28 T1 framers, 21 E1 framers, a SONET/SDH VT1.5/V2/TU-11/TU-12 bit asynchronous mapper, and a full-featured M13 multiplexer with DS3 framer.
- The PM5365 TEMAP is a high density VT/TU mapper with integrated T1/J1/E1 performance monitoring.

  Note: With the exception of the sections describing structured and synchronous configurations, TEMUX and TEMAP are interchangeable.

- The SBI bus is a synchronous time-division multiplexed bus that is designed to transfer data from the SBI line interface of the AAL1gator-32 to the TEMUX or TEMAP chips in a pin-efficient manner. The data belongs to a number of independently timed links of varying bandwidth.

## 1.2 Objectives of this Application Note

This application note provides a sample scenario describing in detail how SBI configuration is done using three AAL1gator-32s and three TEMUXs for 84 unstructured T1s. It provides scripts that can be used for this configuration. The scripts also serve as a reference for other configurations, which data is provided for.

The main objectives of this document are as follows:

- To describe in detail the SBI configuration of three TEMUXs to three AAL1gator-32s using 84 unstructured T1s.
- To describe the various SBI configurations between the AAL1gator-32 and TEMUX.
- To describe how AAL1gator-32 SBI mapping works.
- To provide various SBI mapping and control RAM configurations.
- To provide additional reference material for SBI mapping.

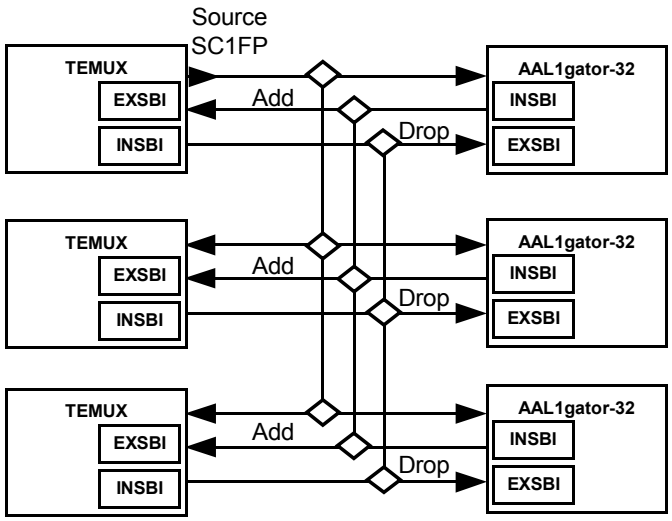
# 2 Example Configuration Scenario

In this example configuration, three PM73122 AAL1gator-32s and three PM8315 TEMUXs are configured to pass 84 unstructured T1s across an SBI bus. The setup procedures for SBI mapping described in Sections 4 and 5 are based on the scenario as described below.

In the add direction, data is being placed onto the SBI bus by the AAL1gator-32. The AAL1gator-32 is the SBI clock master. It uses its internal T1 clock synthesizer to produce a clock at either a nominal rate or at a rate controlled by an SRTS or adaptive clocking mechanism. The TEMUX is the SBI clock slave.

In the drop direction, data is being extracted from the SBI bus by the AAL1gator-32. The TEMUX is the SBI clock master and the AAL1gator-32 is the SBI clock slave. Refer to Figure 1.

**Figure 1 SBI Bus Interconnection between Three AAL1gator-32s and Three TEMUXs**




Both the TEMUX extract SBI block (EXSBI) and the AAL1gator-32 EXSBI use the clock rate (ClkRate) and the phase field of the SBI link rate octet (V4) to reconstruct the T1 clocks. The SBI bus communicates the TEMUX link rate to the AAL1gator-32 by sending a measurement of the clock ticks and clock phase between the T1, the internal reference clock, and the frame pulse of the C1 octet (C1FP). The clock rate field measures clock ticks by counting the number of rising clock edges between two C1FP pulses. The phase field counts the number of rising clock edges between the last C1FP pulse and the T1 clock using a 19.44 MHz SBI clock to detect and measure any clock phase that may occur.

Figure 1 shows that one of the TEMUXs is configured to source the SBI C1FP signal (SC1FP). This SC1FP signal indicates the first C1 octet on the SBI bus, and also provides multiframe alignment to the other two TEMUXs and to the three AAL1gator-32s. The TEMUX and AAL1gator-32 insert SBI blocks (INSBIs) are configured to generate odd SBI parity, and the TEMUX and AAL1gator-32 EXSBIs are configured to check odd parity.

# 3 SBI Mapping Overview

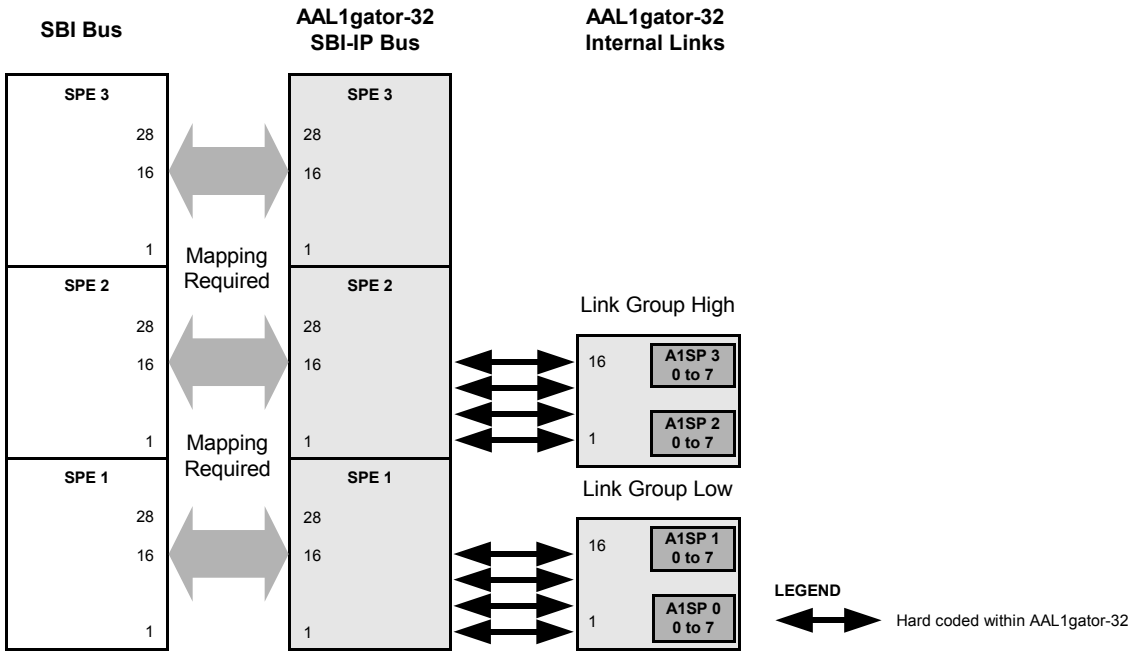
Three components are required for SBI mapping:

- 84 external SBI bus tributaries
- 84 internal parallel AAL1gator-32 SBI (SBI-IP) bus tributaries
- 32 internal AAL1gator-32 links to the AAL1 segmentation and reassembly (SAR) processors (A1SP)

Figure 2 shows how these components are related.

Note: This SBI mapping scheme applies only to the AAL1gator-32, not to the TEMUX. The TEMUX does not map tributaries; the TEMUX INSBI simply drives all 28 T1s or 21 E1s onto *one* of the three SPEs of the Drop bus and extracts all 28 T1s or 21 E1s from *one* of the three SPEs of the Add bus.

**Figure 2 Components for SBI Mapping**




Both the external SBI bus and the AAL1gator-32 SBI-IP bus carry three synchronized payload envelopes (SPEs). Each SPE contains 28 tributaries meaning that each bus has 84 tributaries to map. However, only 32 of the 84 SBI-IP bus tributaries are considered enabled. These SBI-IP tributaries are hard coded to the 32 A1SP links inside the AAL1gator-32. The objective of SBI mapping is to connect the 84 SBI tributaries to the appropriate SBI-IP tributaries by properly writing the AAL1gator-32's SBI mapping RAM.

Once configured, when the AAL1gator-32 EXSBI receives the SPEs from the Drop bus, it selects the appropriate 32 SBI-IP tributaries to link to. Similarly, once configured, when the INSBI of the AAL1gator-32 receives data from its A1SPs, it selects the appropriate 32 SBI-IP tributaries to connect to.

## 3.1 About SBI Tributary Mapping

Each SBI bus tributary is allocated one mapping RAM location in the AAL1gator-32. This location defines the mapping between each SBI bus tributary and an SBI-IP bus tributary.

As shown in Figure 2, 32 SBI-IP tributaries are hard coded to the A1SP processors. These are considered "enabled." The remaining 52 SBI-IP tributaries are not connected to anything in the AAL1gator-32, *but they must still be mapped to the external SBI bus tributaries* in order for the SBI bus to function properly.

For example, even if your configuration of the AAL1gator-32 does not require any SBI bus tributaries to be mapped to the SBI-IP bus SPE 3, you must still map the unused SBI bus tributaries to SBI-IP bus SPE 3.

To indicate a particular SPE on the SBI-IP bus, use the data in Table 1:

**Table 1 SPE Link Group Mapping Scheme**

| SPE to Indicate | LINK_GRP_HIGH | LINK_GRP_LOW |
|---|---|---|
| SPE 1 | SBI-IP SPE[1] = 0 | SBI-IP SPE[0] = 1 |
| SPE 2 | SBI-IP SPE[1] = 1 | SBI-IP SPE[0] = 0 |
| SPE 3 | SBI-IP SPE[1] = 1 | SBI-IP SPE[0] = 1 |

**Note**

1. The configuration terminology "link group" used in the register descriptions (0x80405 and 0x80505) of the AAL1gator-32 Data Sheet (PMC-1981419) for the A1SP link groups should not be used when SBI mapping is performed. This terminology should be replaced with the following "SBI-IP" terminology:

   ```
   LINK_GRP_HIGH = SBI-IP SPE[1]
   LINK_GRP_LOW  = SBI-IP SPE[0]
   ```

   However, the A1SP internal links 0 to 31 can still be labeled as Link Group Low (A1SP0 links 0 to 7 and A1SP1 links 0 to 7) and Link Group High (A1SP2 links 0 to 7 and A1SP3 links 0 to 7) as illustrated in Figure 2.

Note that different tributary labeling conventions are used for each of the TEMUX and the AAL1gator-32 devices. Table 2, which shows a complete table for 28 unstructured T1s from a DS3, illustrates how both the TEMUX and the AAL1gator-32 SBI tributaries are labeled from 1 to 28, while the AAL1gator-32 AISP links are labeled from 0 to 31. (Note that Table 2 shows AAL1gator-32 line numbers on a per A1SP and per chip basis.)

Table 2 also provides information for setting AAL1gator-32 virtual channel identifiers (VCI) in the TX_HEAD fields of the transmit queue tables (T_QUEUE_TBL). Each transmit queue table must have its TX_HEAD field set to a different value, as shown in the AAL1gator-32 VCI column.

**Table 2 TEMUX/AAL1gator-32 Tributary Correspondence and VCI fields for 28 T1s**

| TEMUX Framer | TEMUX SBI Bus[1] | AAL1gator-32 SBI Bus | AAL1gator-32 A1SP | AAL1gator-32 VCI |
|---|---|---|---|---|
| N=1 | trib=1 | trib=1 | line=0 | x0100 |
| N=2 | trib=2 | trib=2 | line=1 | x0120 |
| N=3 | trib=3 | trib=3 | line=2 | x0140 |
| N=4 | trib=4 | trib=4 | line=3 | x0160 |
| N=5 | trib=5 | trib=5 | line=4 | x0180 |
| N=6 | trib=6 | trib=6 | line=5 | x01A0 |
| N=7 | trib=7 | trib=7 | line=6 | x01C0 |
| N=8 | trib=8 | trib=8 | line=7 | x01E0 |
| N=9 | trib=9 | trib=9 | line=0/8[2] | x0300 |
| N=10 | trib=10 | trib=10 | line=1/9 | x0320 |
| N=11 | trib=11 | trib=11 | line=2/10 | x0340 |
| N=12 | trib=12 | trib=12 | line=3/11 | x0360 |
| N=13 | trib=13 | trib=13 | line=4/12 | x0380 |
| N=14 | trib=14 | trib=14 | line=5/13 | x03A0 |
| N=15 | trib=15 | trib=15 | line=6/14 | x03C0 |
| N=16 | trib=16 | trib=16 | line=7/15 | x03E0 |
| N=17 | trib=17 | trib=17 | line=0/16 | x0500 |
| N=18 | trib=18 | trib=18 | line=1/17 | x0520 |
| N=19 | trib=19 | trib=19 | line=2/18 | x0540 |
| N=20 | trib=20 | trib=20 | line=3/19 | x0560 |
| N=21 | trib=21 | trib=21 | line=4/20 | x0580 |
| N=22 | trib=22 | trib=22 | line=5/21 | x05A0 |
| N=23 | trib=23 | trib=23 | line=6/22 | x05C0 |
| N=24 | trib=24 | trib=24 | line=7/23 | x05E0 |
| N=25 | trib=25 | trib=25 | line=0/24 | x0700 |
| N=26 | trib=26 | trib=26 | line=1/25 | x0720 |
| N=27 | trib=27 | trib=27 | line=2/26 | x0740 |
| N=28 | trib=28 | trib=28 | line=3/27 | x0760 |

**Note**

1. The tributary labels for the TEMUX SBI tributaries and the AAL1gator-32 SBI tributaries cannot be different.
2. Each A1SP group is labeled from 0 to 7. “0/8” refers to the first link in the A1SP2 group, effectively link “8” of the “27” links that correspond to the TEMUX and AAL1gator-32 tributaries shown in the table. “0/16” refers to the first link in the A1SP3 group, otherwise known as link 16 of the 27 links that correspond to the TEMUX and AAL1gator-32 tributaries.

## 3.2 Default (1:1) Mapping between the TEMUX and the AAL1gator-32

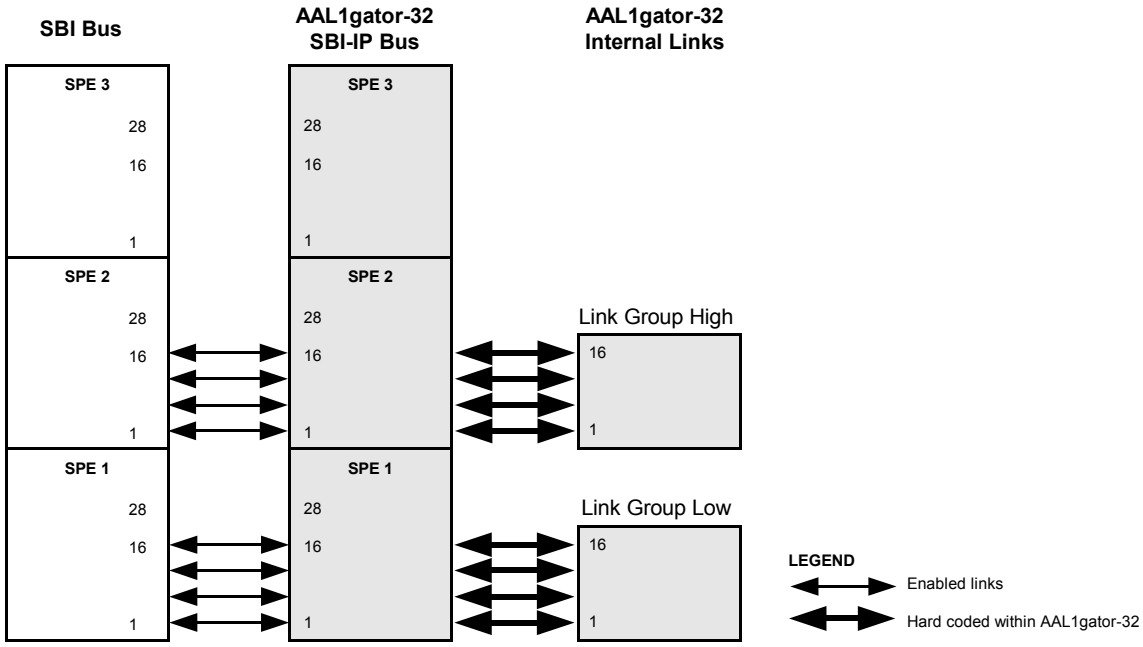
The time switch enable bit (TS_EN) in the SBI Configuration register (0x80300) is disabled when set to "0" and enabled when set to "1".

As a default, SBI mapping is disabled in the AAL1gator-32.

Figure 3 shows the default disabled mapping scheme. In this configuration, the AAL1gator-32 can process one of the following:

- 32 T1 or E1 tributaries — the lowest 16 tributaries in SPE 1 and the lowest 16 tributaries in SPE 2, or
- Two DS3 tributaries, one in each SPE 1 and SPE 2

**Figure 3 Default (1:1) Mapping**




## 3.3 SBI Mapping Between the TEMUX and the AAL1gator-32

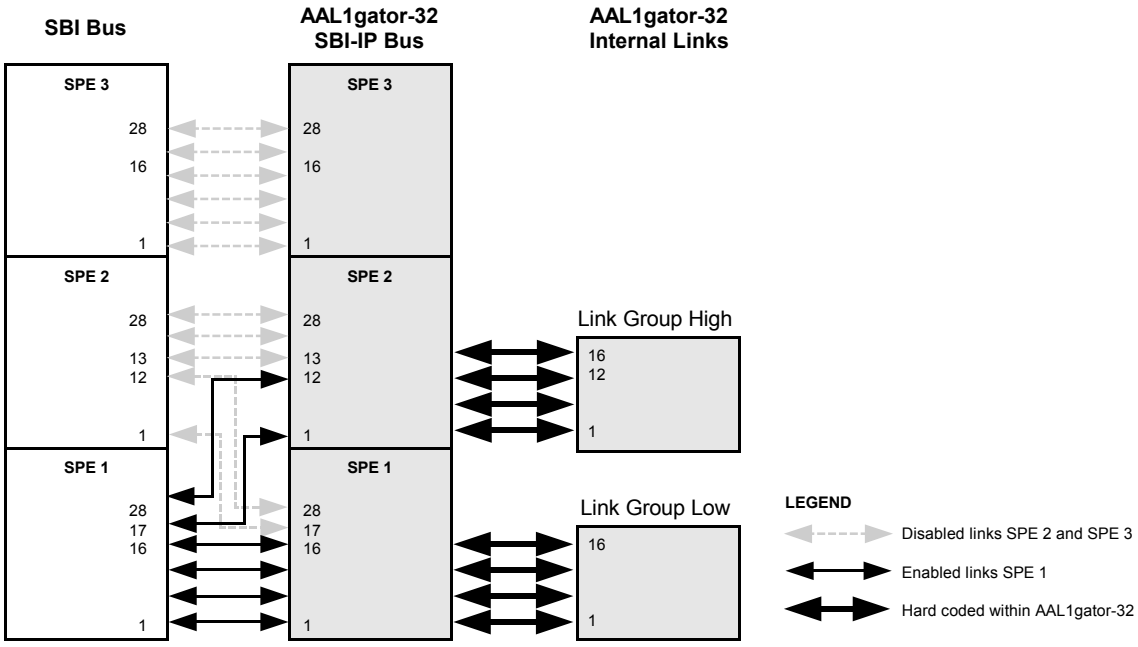
Mapping in the AAL1gator-32 can be enabled by setting the global TS_EN (time switch enable) bits in the SBI Bus Configuration register (0x80300) and the EXSBI/INSBI Control registers (0x80400/0x80500) to "1".

Once enabled, mapping can be done on a tributary by tributary basis by configuring the tributary control RAMs and enabling the SPEs in the SBI Bus Configuration register (0x80300).

Remember that even if only one tributary requires mapping, all tributaries must be mapped for proper operation.

The following figures show an example of how channelized DS3s are mapped from the TEMUX to the AAL1gator-32 SPEs. Table 3 on page 18 summarizes the channelized DS3 mapping scheme shown in the figures.

**Figure 4 TEMUX/AAL1gator-32 Mapping Using SPE 1**




In Figure 4, the enabled SBI SPE 1 tributaries 1 through 28 are mapped into the enabled SBI-IP bus tributaries. Remember, the enabled tributaries are the ones that are directly connected to the A1SP internal links.

Note how the unused SBI bus tributaries are mapped into unused SBI-IP bus tributaries. Unused SBI SPE 2 tributaries 1 through 12 are mapped down into the top 12 unused tributaries on the SBI-IP bus for SPE 1. Unused SBI SPE 2 tributaries 13 through 28 are mapped 1:1 into the top 13 through 28 tributaries on the SBI-IP bus for SPE 2. Unused SBI SPE 3 tributaries 1 through 28 are mapped 1:1 into all the tributaries on the SBI-IP bus for SPE 3.

**Figure 5 TEMUX/AAL1gator-32 Mapping Using SPE 2**

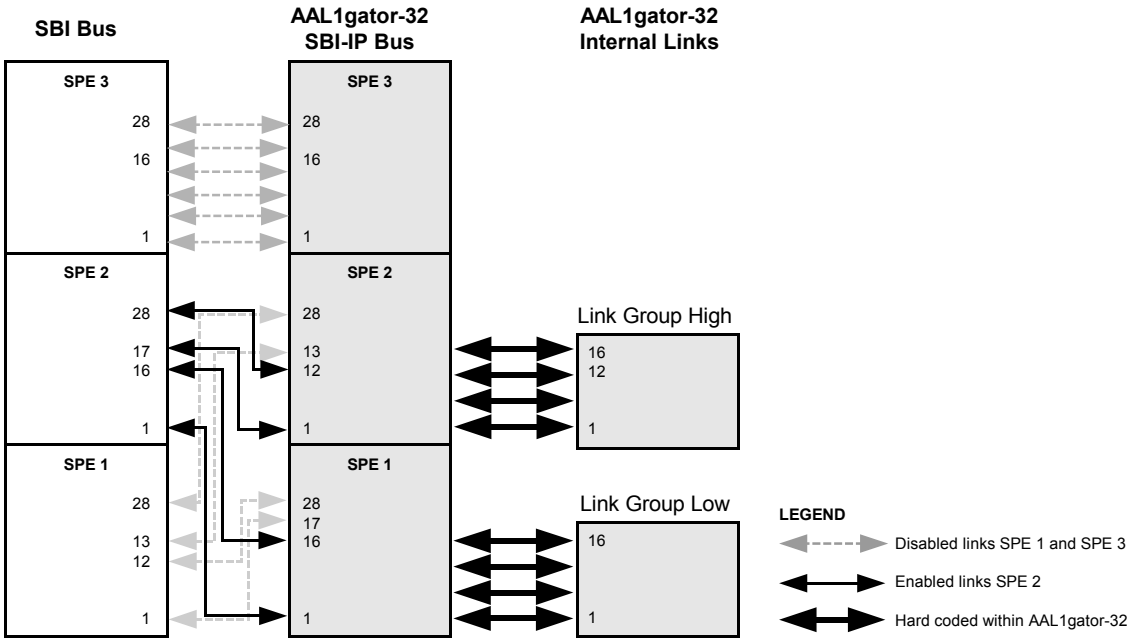



Figure 5 shows the mapping scheme for the second SPE in the scenario. Here, the SBI SPE 2 tributaries are enabled.

SBI SPE 2 tributaries 1 through 16 are mapped to the SBI-IP bus SPE 1 tributaries 1 through 16 and SBI SPE 2 tributaries 17 through 28 are mapped to the first 12 tributaries on the SBI-IP bus SPE 2.

The disabled SBI SPE 1 tributaries 1 through 12 are mapped to the upper 12 tributaries of the SBI-IP bus SPE 1 and SBI SPE 1 tributaries 13 through 28 are mapped to the upper 16 tributaries of the SBI-IP bus, SPE 2. The disabled SBI SPE 3 tributaries are mapped 1:1 to the SBI-IP tributaries for SPE 3.

**Figure 6 TEMUX/AAL1gator-32 Mapping Using SPE 3**

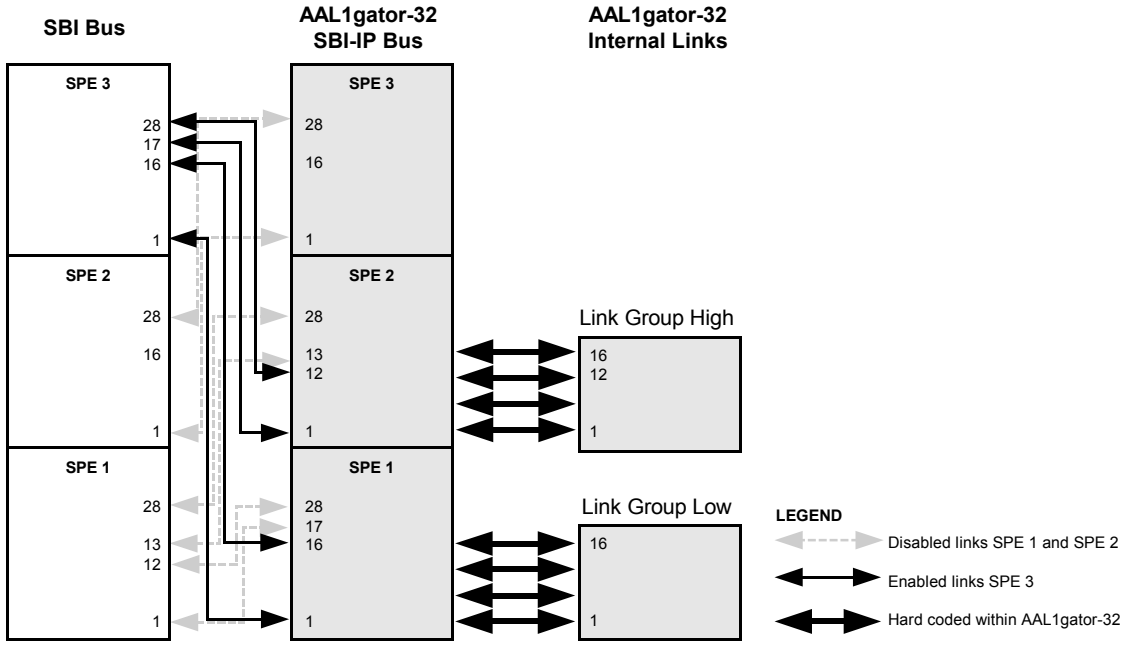



Figure 6 shows the mapping scheme for the third SPE in the scenario.

Table 3 summarizes the channelized DS3 mapping scheme shown in Figure 4, Figure 5, and Figure 6. You can use this table to configure the 84 mapping entries for each AAL1gator-32 chip. Note that each SBI tributary appears in the table exactly once, and each SBI-IP bus tributary appears in the table exactly once.

**Table 3 Channelized DS3 Mapping Summary**

| A32# | SBI SPE # | Tributary # | SBI-IP SPE # | SBI-IP Tributary # | TRIB_ENBL |
|---|---|---|---|---|---|
| 1 | 1 | 1–16 | SPE 1 | 1–16 | enabled |
| | | 17–28 | SPE 2 | 1–12 | enabled |
| | 2 | 1–12 | SPE 1 | 17–28 | disabled |
| | | 13–28 | SPE 2 | 13–28 | disabled |
| | 3 | 1–28 | SPE 3 | 1–28 | disabled |
| 2 | 1 | 1–12 | SPE 1 | 17–28 | disabled |
| | | 13–28 | SPE 2 | 13–28 | disabled |
| | 2 | 1–16 | SPE 1 | 1–16 | enabled |
| | | 17–28 | SPE 2 | 1–12 | enabled |
| | 3 | 1–28 | SPE 3 | 1–28 | disabled |
| 3 | 1 | 1–12 | SPE 1 | 17–28 | disabled |
| | | 13–28 | SPE 2 | 13–28 | disabled |
| | 2 | 1–28 | SPE 3 | 1–28 | disabled |
| | 3 | 1–16 | SPE 1 | 1–16 | enabled |
| | | 17–28 | SPE 2 | 1–12 | enabled |

Sections 4 and 5 provide the setup procedures for TEMUX and AAL1gator-32 using the mapping example provided here.

These setup procedures may be used as a template for the mapping configuration data provided in the rest of the application note.

For further information on SBI mapping, consult the following sources:

- Section 8.4.1 “Programming the SBI Interface” of the AAL1gator-32 Programmer’s Guide provides general configuration rules.
- Section 8.4.3.2.1 “SBI Extract Tributary Mapping Configuration” of the AAL1gator-32 Programmer’s Guide gives more details on configuring tributary mapping RAMs.
- Section 8.4.4.2.2 “SBI Insert Tributary Control Configuration” of the AAL1gator-32 Programmer’s Guide gives more details on configuring the tributary control RAMs.

# 4 Sample TEMUX Setup

Use the following procedure to configure the SBI bus for each of the three TEMUXs. Refer to Section 14 of the TEMUX Programmer's Guide for further information.

Note: Only one of the three TEMUXs should be designated to source the SC1FP signal (SC1FPMSTR).

1. Reset the SBI logic:

```
wr 0x1700 0x00
wr 0x1700 0x01
wr 0x1700 0x00
```

2. Disable the SBI interrupts:

```
wr 0x1710 0x41 ; disable EXSBI interrupts and check odd parity
wr 0x1720 0x41 ; disable INSBI interrupts and generate odd parity
```

3. Configure the SBI top-level registers:

```
wr 0x1701 0xC5 ; c1fpmaster, add/drop spe=1
wr 0x1702 0x00 ; busmaster off
```

4. Configure the INSBI: 28 indirect writes to INSBI control RAM: (0x1726):

```
iwr INSBI $dropspe=1 $trib=1-28 0x09; Unframed, enabled.
```

   Note: iwr is a PMC-Sierra indirect write command. To configure your indirect write for the TEMUX INSBI, use the following script:

```
rd 0x1724 ; poll BUSY bit (bit 7) until it clears
wr 0x1723 0x21 ; address (indicates SPE 1, tributary 1)
wr 0x1726 0x09 ; data (Unframed tributary, enabled)
wr 0x1724 0x00 ; initiate write access to INSBI Control RAM
rd 0x1724 ; poll BUSY bit (bit 7) until it clears.
```

5. Configure the EXSBI: 28 indirect writes to EXSBI control RAM (0x1716):

```
iwr EXSBI $addspe=1 $trib=1-28 0x49; Unframed, clk_slave, Phase
```

# 5 Sample AAL1gator-32 Setup

Use the following procedure to configure the SBI bus for the three AAL1gator-32s. Refer to Section 8.4.1 of the AAL1gator-32 Programmer's Guide for the general configuration rules.

1. Use the following script for the initial SBI configuration:

```
wr 0x80300 0x0000 ; all spes disabled, spe type = t1
wr 0x80400 0x0001 ; page 0, dc dis, map dis, check odd parity
wr 0x80500 0x0001 ; page 0, dc dis, map dis, gen odd parity
wr 0x80301 0x0000 ; t1 link types
wr 0x80302 0x0000 ; enable links
wr 0x80303 0x0000 ; enable links
wr 0x80304 0x0000 ; no sync links
wr 0x80305 0x0000 ; no sync links
```

2. Write the SBI EXSBI and INSBI mapping RAMs. Refer to Section 6 for the actual configurations.

   Note: A valid 19.44 MHz REFCLK and C1FP pulse must be present before attempting to configure the AAL1gator-32 SBI registers. If either of the BUSY bits (0x80404 or 0x80504, bit 7) does not clear, verify that a valid C1FP signal is present.

   Note: Use the following sample AAL1gator-32 INSBI script to configure your indirect writes:

```
rd 0x80404 ; poll BUSY bit (bit 7) until it clears
wr 0x80403 0x21 ; address (indicates SPE 1, tributary 1)
wr 0x80406 0x19 ; data
wr 0x80404 0x00 ; initiates write
rd 0x80404 ; poll BUSY bit (bit 7) until it clears
```

3. Set the global time space enable bits (TS_EN) in the SBI Bus Configuration register (0x80300) and the EXSBI/INSBI Control registers (0x80400/0x80500) to "1".

4. Write the SBI EXSBI and INSBI control RAMs. Refer to Section 6 for the actual configurations.

5. Enable SBI mapping:

```
wr 0x80300 0x2000 ; enable EXSBI/INSBI mapping
wr 0x80400 0x0004 ; enable EXSBI mapping
wr 0x80500 0x0004 ; enable INSBI mapping
```

6. Enable the SPEs by setting the SPEn_ENBL bits:

```
wr 0x80300 0x2040 ; A32 #1 using SPE 1
wr 0x80300 0x2080 ; A32 #2 using SPE 2
wr 0x80300 0x2100 ; A32 #3 using SPE 3
```

# 6 AAL1gator-32 SBI Mapping and Control RAM Configurations

This section provides data for four possible configurations:

- 84 T1s for a three-TEMUX three-AAL1gator-32 configuration
- 63 E1s for a three-TEMUX three-AAL1gator-32 configuration
- 63 E1s for a three-TEMUX two-AAL1gator-32 configuration
- 32 E1s for 1:1 mapping in a three-TEMUX two-AAL1gator-32 configuration

## 6.1 How to Use this Section

Each sub section of Section 6 contains configuration information: the sequence of operations for configuring the SBI bus registers, summaries of the required mapping steps, and detailed mapping and control RAM configuration tables. The mapping and control RAM configuration tables contain data for both the EXSBI and the INSBI. Refer to Section 8.4.1 "Programming the SBI Interface" of the AAL1gator-32 Programmer's Guide for the general configuration rules.

To map your particular TEMUX/AAL1gator-32 configuration, use the data provided in the appropriate section and follow the steps below for each tributary:

1. Write the SBI bus tributary number and select the mapping RAM in the indirect address register:

```
0x80403=0x00A1 ; EXSBI (example shows SPE=1, trib=1)
0x80503=0x00A1 ; INSBI (example shows SPE=1, trib=1)
```

2. Write the corresponding SBI-IP bus tributary number into the mapping RAM indirect data register:

```
0x80405=0x0021 ; EXSBI (example shows SPE=1 trib=1)
0x80505=0x0021 ; INSBI (example shows SPE=1 trib 1)
```

3. Initiate the write access to page 0 of the mapping RAM:

```
0x80404=0x000 ; EXSBI RWB=0 and Page 0
0x80504=0x000 ; INSBI RWB=0 and Page 0
```

4. Poll the BUSY bit, bit 7, until it reads "0":

```
read 0x80404 until it reads back EXSBI BUSY(bit 7)=0
read 0x80504 until it reads back INSBI BUSY(bit7)=0
```

5. Repeat the procedure until all 84(T1) or 63(E1) mapping RAM locations are written for both EXSBI and INSBI.

## 6.2 Configuring 84 T1s For Three TEMUXs and Three AAL1gator-32s

### 6.2.1 Configuring the SBI bus registers

Use the sequence below to configure the SBI bus registers for 84 T1s.

To configure the first AAL1gator-32 SBI bus:

1. Prepare the SBI bus registers for mapping:

```
wr 0x80300 0x0000 ; set SPEx_TYP=T1; keep SPEs disabled
wr 0x80400 0x0041 ; default
wr 0x80500 0x0041 ; default

wr 0x80301 0x0000 ; set LINK_TYPx=T1
wr 0x80302 0x0000 ; set LINK_DISx=0
wr 0x80303 0x0000 ; set LINK_DISx=0
wr 0x80304 0x0000 ; set SYNC_LINKx=0
wr 0x80305 0x0000 ; set SYNC_LINKx=0
```

2. Load the mapping and control RAMs:

   Note: Insert the specified mapping and control RAM writes here.

```
; load SBI EXSBI Mapping RAM for A32 #1
; load SBI INSBI Mapping RAM for A32 #1
; load SBI EXSBI Control RAM for A32 #1
; load SBI INSBI Control RAM for A32 #1
```

3. After you have configured the RAMs, enable mapping:

```
wr 0x80300 0x2000 ; set global ts_en=1
wr 0x80400 0x0045 ; set exsbi ts_en=1 to enable exsbi mapping
wr 0x80500 0x0045 ; set insbi ts_en=1 to enable insbi mapping
```

4. Enable the SPEs:

```
wr 0x80300 0x2040 ; enable SPE 1 on A32 #1
```

To configure the second AAL1gator-32 SBI bus:

1. Prepare the SBI bus registers for mapping:

```
wr 0x80300 0x0000 ; set SPEx_TYP=T1; keep SPEs disabled
wr 0x80400 0x0041 ; default
wr 0x80500 0x0041 ; default

wr 0x80301 0x0000 ; set LINK_TYPx=T1
wr 0x80302 0x0000 ; set LINK_DISx=0
wr 0x80303 0x0000 ; set LINK_DISx=0
wr 0x80304 0x0000 ; set SYNC_LINKx=0
wr 0x80305 0x0000 ; set SYNC_LINKx=0
```

2. Load the mapping and control RAMs:

   Note: Insert the specified mapping and control RAM writes here.

```
; load SBI EXSBI Mapping RAM for A32 #2
; load SBI INSBI Mapping RAM for A32 #2
; load SBI EXSBI Control RAM for A32 #2
; load SBI INSBI Control RAM for A32 #2
```

3. After the RAMs have been configured, enable mapping:

```
wr 0x80300 0x2000 ; set global ts_en=1
wr 0x80400 0x0045 ; set exsbi ts_en=1 to enable exsbi mapping
wr 0x80500 0x0045 ; set insbi ts_en=1 to enable insbi mapping
```

4. Enable the SPEs:

```
wr 0x80300 0x2080 ; enable SPE 2 on A32 #2
```

To configure the third AAL1gator-32 SBI bus:

1. Prepare the SBI bus registers for mapping:

```
wr 0x80300 0x0000 ; set SPEx_TYP=T1; keep SPEs disabled
wr 0x80400 0x0041 ; default
wr 0x80500 0x0041 ; default

wr 0x80301 0x0000 ; set LINK_TYPx=T1
wr 0x80302 0x0000 ; set LINK_DISx=0
wr 0x80303 0x0000 ; set LINK_DISx=0
wr 0x80304 0x0000 ; set SYNC_LINKx=0
```

```
wr 0x80305 0x0000 ; set SYNC_LINKx=0
```

2. Load the mapping and control RAMs:

   Note: Insert specified mapping and control RAM writes here.

```
; load SBI EXSBI Mapping RAM for A32 #3
; load SBI INSBI Mapping RAM for A32 #3
; load SBI EXSBI Control RAM for A32 #3
; load SBI INSBI Control RAM for A32 #3
```

3. After the RAMs have been configured, enable mapping:

```
wr 0x80300 0x2000 ; set global ts_en=1
wr 0x80400 0x0045 ; set exsbi ts_en=1 to enable exsbi mapping
wr 0x80500 0x0045 ; set insbi ts_en=1 to enable insbi mapping
```

4. After mapping is enabled, enable the SPEs:

```
wr 0x80300 0x2100 ; enable SPE 3 on A32 #3
```

### 6.2.2 Mapping Summary

Table 4, Table 5, and Table 6 provide summaries of the mapping that should be done for each of the three AAL1gator-32s when configuring 84 T1s.

**Table 4 Summary Table for AAL1gator-32 #1 Channelized DS3 Mapping**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | TRIB_ENBL |
|---|---|---|---|---|---|
| 1 | 1–16 | 1 | SPE 1 | 1–16 | enabled |
| | 17–28 | | SPE 2 | 1–12 | enabled |
| 2 | 1–12 | | SPE 1 | 17–28 | disabled |
| | 13–28 | | SPE 2 | 13–28 | disabled |
| 3 | 1–28 | | SPE 3 | 1–28 | disabled |

**Table 5 Summary Table for AAL1gator-32 #2 Channelized DS3 Mapping**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | TRIB_ENBL |
|---|---|---|---|---|---|
| 1 | 1–12 | 2 | SPE 1 | 17–28 | disabled |
| | 13–28 | | SPE 2 | 13–28 | disabled |
| 2 | 1–16 | | SPE 1 | 1–16 | enabled |
| | 17–28 | | SPE 2 | 1–12 | enabled |
| 3 | 1–28 | | SPE 3 | 1–28 | disabled |

**Table 6 Summary Table for AAL1gator-32 #3 Channelized DS3 Mapping**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | TRIB_ENBL |
|---|---|---|---|---|---|
| 1 | 1–12 | 3 | SPE 1 | 17–28 | disabled |
| | 13–28 | | SPE 2 | 13–28 | disabled |
| 2 | 1–28 | | SPE 3 | 1–28 | disabled |
| 3 | 1–16 | | SPE 1 | 1–16 | enabled |
| | 17–28 | | SPE 2 | 1–12 | enabled |

### 6.2.3 Detailed Mapping RAM for AAL1gator-32 #1

Table 7, Table 8, and Table 9 contain the detailed mapping RAM configuration data for the first AAL1gator-32.

**Table 7 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #1 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0021 | 1/1 | 1/1 | enabled |
| 0x00A2 | 0x0022 | 1/2 | 1/2 | enabled |
| 0x00A3 | 0x0023 | 1/3 | 1/3 | enabled |
| 0x00A4 | 0x0024 | 1/4 | 1/4 | enabled |
| 0x00A5 | 0x0025 | 1/5 | 1/5 | enabled |
| 0x00A6 | 0x0026 | 1/6 | 1/6 | enabled |
| 0x00A7 | 0x0027 | 1/7 | 1/7 | enabled |
| 0x00A8 | 0x0028 | 1/8 | 1/8 | enabled |
| 0x00A9 | 0x0029 | 1/9 | 1/9 | enabled |
| 0x00AA | 0x002A | 1/10 | 1/10 | enabled |
| 0x00AB | 0x002B | 1/11 | 1/11 | enabled |
| 0x00AC | 0x002C | 1/12 | 1/12 | enabled |
| 0x00AD | 0x002D | 1/13 | 1/13 | enabled |
| 0x00AE | 0x002E | 1/14 | 1/14 | enabled |
| 0x00AF | 0x002F | 1/15 | 1/15 | enabled |
| 0x00B0 | 0x0030 | 1/16 | 1/16 | enabled |
| 0x00B1 | 0x0041 | 1/17 | 2/1 | enabled |
| 0x00B2 | 0x0042 | 1/18 | 2/2 | enabled |
| 0x00B3 | 0x0043 | 1/19 | 2/3 | enabled |
| 0x00B4 | 0x0044 | 1/20 | 2/4 | enabled |
| 0x00B5 | 0x0045 | 1/21 | 2/5 | enabled |
| 0x00B6 | 0x0046 | 1/22 | 2/6 | enabled |
| 0x00B7 | 0x0047 | 1/23 | 2/7 | enabled |
| 0x00B8 | 0x0048 | 1/24 | 2/8 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00B9 | 0x0049 | 1/25 | 2/9 | enabled |
| 0x00BA | 0x004A | 1/26 | 2/10 | enabled |
| 0x00BB | 0x004B | 1/27 | 2/11 | enabled |
| 0x00BC | 0x004C | 1/28 | 2/12 | enabled |

**Table 8 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #1 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0031 | 2/1 | 1/17 | disabled |
| 0x00C2 | 0x0032 | 2/2 | 1/18 | disabled |
| 0x00C3 | 0x0033 | 2/3 | 1/19 | disabled |
| 0x00C4 | 0x0034 | 2/4 | 1/20 | disabled |
| 0x00C5 | 0x0035 | 2/5 | 1/21 | disabled |
| 0x00C6 | 0x0036 | 2/6 | 1/22 | disabled |
| 0x00C7 | 0x0037 | 2/7 | 1/23 | disabled |
| 0x00C8 | 0x0038 | 2/8 | 1/24 | disabled |
| 0x00C9 | 0x0039 | 2/9 | 1/25 | disabled |
| 0x00CA | 0x003A | 2/10 | 1/26 | disabled |
| 0x00CB | 0x003B | 2/11 | 1/27 | disabled |
| 0x00CC | 0x003C | 2/12 | 1/28 | disabled |
| 0x00CD | 0x004D | 2/13 | 2/13 | disabled |
| 0x00CE | 0x004E | 2/14 | 2/14 | disabled |
| 0x00CF | 0x004F | 2/15 | 2/15 | disabled |
| 0x00D0 | 0x0050 | 2/16 | 2/16 | disabled |
| 0x00D1 | 0x0051 | 2/17 | 2/17 | disabled |
| 0x00D2 | 0x0052 | 2/18 | 2/18 | disabled |
| 0x00D3 | 0x0053 | 2/19 | 2/19 | disabled |
| 0x00D4 | 0x0054 | 2/20 | 2/20 | disabled |
| 0x00D5 | 0x0055 | 2/21 | 2/21 | disabled |
| 0x00D6 | 0x0056 | 2/22 | 2/22 | disabled |
| 0x00D7 | 0x0057 | 2/23 | 2/23 | disabled |
| 0x00D8 | 0x0058 | 2/24 | 2/24 | disabled |
| 0x00D9 | 0x0059 | 2/25 | 2/25 | disabled |
| 0x00DA | 0x005A | 2/26 | 2/26 | disabled |
| 0x00DB | 0x005B | 2/27 | 2/27 | disabled |
| 0x00DC | 0x005C | 2/28 | 2/28 | disabled |

**Table 9 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #1 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0061 | 3/1 | 3/1 | disabled |
| 0x00E2 | 0x0062 | 3/2 | 3/2 | disabled |
| 0x00E3 | 0x0063 | 3/3 | 3/3 | disabled |
| 0x00E4 | 0x0064 | 3/4 | 3/4 | disabled |
| 0x00E5 | 0x0065 | 3/5 | 3/5 | disabled |
| 0x00E6 | 0x0066 | 3/6 | 3/6 | disabled |
| 0x00E7 | 0x0067 | 3/7 | 3/7 | disabled |
| 0x00E8 | 0x0068 | 3/8 | 3/8 | disabled |
| 0x00E9 | 0x0069 | 3/9 | 3/9 | disabled |
| 0x00EA | 0x006A | 3/10 | 3/10 | disabled |
| 0x00EB | 0x006B | 3/11 | 3/11 | disabled |
| 0x00EC | 0x006C | 3/12 | 3/12 | disabled |
| 0x00ED | 0x006D | 3/13 | 3/13 | disabled |
| 0x00EE | 0x006E | 3/14 | 3/14 | disabled |
| 0x00EF | 0x006F | 3/15 | 3/15 | disabled |
| 0x00F0 | 0x0070 | 3/16 | 3/16 | disabled |
| 0x00F1 | 0x0071 | 3/17 | 3/17 | disabled |
| 0x00F2 | 0x0072 | 3/18 | 3/18 | disabled |
| 0x00F3 | 0x0073 | 3/19 | 3/19 | disabled |
| 0x00F4 | 0x0074 | 3/20 | 3/20 | disabled |
| 0x00F5 | 0x0075 | 3/21 | 3/21 | disabled |
| 0x00F6 | 0x0076 | 3/22 | 3/22 | disabled |
| 0x00F7 | 0x0077 | 3/23 | 3/23 | disabled |
| 0x00F8 | 0x0078 | 3/24 | 3/24 | disabled |
| 0x00F9 | 0x0079 | 3/25 | 3/25 | disabled |
| 0x00FA | 0x007A | 3/26 | 3/26 | disabled |
| 0x00FB | 0x007B | 3/27 | 3/27 | disabled |
| 0x00FC | 0x007C | 3/28 | 3/28 | disabled |

### 6.2.4 Detailed Mapping RAM for AAL1gator-32 #2

Table 10, Table 11, and Table 12 contain the detailed mapping RAM configuration data for the second AAL1gator-32.

**Table 10 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #2 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0031 | 1/1 | 1/17 | disabled |
| 0x00A2 | 0x0032 | 1/2 | 1/18 | disabled |
| 0x00A3 | 0x0033 | 1/3 | 1/19 | disabled |
| 0x00A4 | 0x0034 | 1/4 | 1/20 | disabled |
| 0x00A5 | 0x0035 | 1/5 | 1/21 | disabled |
| 0x00A6 | 0x0036 | 1/6 | 1/22 | disabled |
| 0x00A7 | 0x0037 | 1/7 | 1/23 | disabled |
| 0x00A8 | 0x0038 | 1/8 | 1/24 | disabled |
| 0x00A9 | 0x0039 | 1/9 | 1/25 | disabled |
| 0x00AA | 0x003A | 1/10 | 1/26 | disabled |
| 0x00AB | 0x003B | 1/11 | 1/27 | disabled |
| 0x00AC | 0x003C | 1/12 | 1/28 | disabled |
| 0x00AD | 0x004D | 1/13 | 2/13 | disabled |
| 0x00AE | 0x004E | 1/14 | 2/14 | disabled |
| 0x00AF | 0x004F | 1/15 | 2/15 | disabled |
| 0x00B0 | 0x0050 | 1/16 | 2/16 | disabled |
| 0x00B1 | 0x0051 | 1/17 | 2/17 | disabled |
| 0x00B2 | 0x0052 | 1/18 | 2/18 | disabled |
| 0x00B3 | 0x0053 | 1/19 | 2/19 | disabled |
| 0x00B4 | 0x0054 | 1/20 | 2/20 | disabled |
| 0x00B5 | 0x0055 | 1/21 | 2/21 | disabled |
| 0x00B6 | 0x0056 | 1/22 | 2/22 | disabled |
| 0x00B7 | 0x0057 | 1/23 | 2/23 | disabled |
| 0x00B8 | 0x0058 | 1/24 | 2/24 | disabled |
| 0x00B9 | 0x0059 | 1/25 | 2/25 | disabled |
| 0x00BA | 0x005A | 1/26 | 2/26 | disabled |
| 0x00BB | 0x005B | 1/27 | 2/27 | disabled |
| 0x00BC | 0x005C | 1/28 | 2/28 | disabled |

**Table 11 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #2 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0021 | 2/1 | 1/1 | enabled |
| 0x00C2 | 0x0022 | 2/2 | 1/2 | enabled |
| 0x00C3 | 0x0023 | 2/3 | 1/3 | enabled |
| 0x00C4 | 0x0024 | 2/4 | 1/4 | enabled |
| 0x00C5 | 0x0025 | 2/5 | 1/5 | enabled |
| 0x00C6 | 0x0026 | 2/6 | 1/6 | enabled |
| 0x00C7 | 0x0027 | 2/7 | 1/7 | enabled |
| 0x00C8 | 0x0028 | 2/8 | 1/8 | enabled |
| 0x00C9 | 0x0029 | 2/9 | 1/9 | enabled |
| 0x00CA | 0x002A | 2/10 | 1/10 | enabled |
| 0x00CB | 0x002B | 2/11 | 1/11 | enabled |
| 0x00CC | 0x002C | 2/12 | 1/12 | enabled |
| 0x00CD | 0x002D | 2/13 | 1/13 | enabled |
| 0x00CE | 0x002E | 2/14 | 1/14 | enabled |
| 0x00CF | 0x002F | 2/15 | 1/15 | enabled |
| 0x00D0 | 0x0030 | 2/16 | 1/16 | enabled |
| 0x00D1 | 0x0041 | 2/17 | 2/1 | enabled |
| 0x00D2 | 0x0042 | 2/18 | 2/2 | enabled |
| 0x00D3 | 0x0043 | 2/19 | 2/3 | enabled |
| 0x00D4 | 0x0044 | 2/20 | 2/4 | enabled |
| 0x00D5 | 0x0045 | 2/21 | 2/5 | enabled |
| 0x00D6 | 0x0046 | 2/22 | 2/6 | enabled |
| 0x00D7 | 0x0047 | 2/23 | 2/7 | enabled |
| 0x00D8 | 0x0048 | 2/24 | 2/8 | enabled |
| 0x00D9 | 0x0049 | 2/25 | 2/9 | enabled |
| 0x00DA | 0x004A | 2/26 | 2/10 | enabled |
| 0x00DB | 0x004B | 2/27 | 2/11 | enabled |
| 0x00DC | 0x004C | 2/28 | 2/12 | enabled |

**Table 12 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #2 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0061 | 3/1 | 3/1 | disabled |
| 0x00E2 | 0x0062 | 3/2 | 3/2 | disabled |
| 0x00E3 | 0x0063 | 3/3 | 3/3 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E4 | 0x0064 | 3/4 | 3/4 | disabled |
| 0x00E5 | 0x0065 | 3/5 | 3/5 | disabled |
| 0x00E6 | 0x0066 | 3/6 | 3/6 | disabled |
| 0x00E7 | 0x0067 | 3/7 | 3/7 | disabled |
| 0x00E8 | 0x0068 | 3/8 | 3/8 | disabled |
| 0x00E9 | 0x0069 | 3/9 | 3/9 | disabled |
| 0x00EA | 0x006A | 3/10 | 3/10 | disabled |
| 0x00EB | 0x006B | 3/11 | 3/11 | disabled |
| 0x00EC | 0x006C | 3/12 | 3/12 | disabled |
| 0x00ED | 0x006D | 3/13 | 3/13 | disabled |
| 0x00EE | 0x006E | 3/14 | 3/14 | disabled |
| 0x00EF | 0x006F | 3/15 | 3/15 | disabled |
| 0x00F0 | 0x0070 | 3/16 | 3/16 | disabled |
| 0x00F1 | 0x0071 | 3/17 | 3/17 | disabled |
| 0x00F2 | 0x0072 | 3/18 | 3/18 | disabled |
| 0x00F3 | 0x0073 | 3/19 | 3/19 | disabled |
| 0x00F4 | 0x0074 | 3/20 | 3/20 | disabled |
| 0x00F5 | 0x0075 | 3/21 | 3/21 | disabled |
| 0x00F6 | 0x0076 | 3/22 | 3/22 | disabled |
| 0x00F7 | 0x0077 | 3/23 | 3/23 | disabled |
| 0x00F8 | 0x0078 | 3/24 | 3/24 | disabled |
| 0x00F9 | 0x0079 | 3/25 | 3/25 | disabled |
| 0x00FA | 0x007A | 3/26 | 3/26 | disabled |
| 0x00FB | 0x007B | 3/27 | 3/27 | disabled |
| 0x00FC | 0x007C | 3/28 | 3/28 | disabled |

### 6.2.5 Detailed Mapping RAM for AAL1gator-32 #3

Table 13, Table 14, and Table 15 contain the detailed mapping RAM configuration data for the third AAL1gator-32.

**Table 13 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #3 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0031 | 1/1 | 1/17 | disabled |
| 0x00A2 | 0x0032 | 1/2 | 1/18 | disabled |
| 0x00A3 | 0x0033 | 1/3 | 1/19 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A4 | 0x0034 | 1/4 | 1/20 | disabled |
| 0x00A5 | 0x0035 | 1/5 | 1/21 | disabled |
| 0x00A6 | 0x0036 | 1/6 | 1/22 | disabled |
| 0x00A7 | 0x0037 | 1/7 | 1/23 | disabled |
| 0x00A8 | 0x0038 | 1/8 | 1/24 | disabled |
| 0x00A9 | 0x0039 | 1/9 | 1/25 | disabled |
| 0x00AA | 0x003A | 1/10 | 1/26 | disabled |
| 0x00AB | 0x003B | 1/11 | 1/27 | disabled |
| 0x00AC | 0x003C | 1/12 | 1/28 | disabled |
| 0x00AD | 0x004D | 1/13 | 2/13 | disabled |
| 0x00AE | 0x004E | 1/14 | 2/14 | disabled |
| 0x00AF | 0x004F | 1/15 | 2/15 | disabled |
| 0x00B0 | 0x0050 | 1/16 | 2/16 | disabled |
| 0x00B1 | 0x0051 | 1/17 | 2/17 | disabled |
| 0x00B2 | 0x0052 | 1/18 | 2/18 | disabled |
| 0x00B3 | 0x0053 | 1/19 | 2/19 | disabled |
| 0x00B4 | 0x0054 | 1/20 | 2/20 | disabled |
| 0x00B5 | 0x0055 | 1/21 | 2/21 | disabled |
| 0x00B6 | 0x0056 | 1/22 | 2/22 | disabled |
| 0x00B7 | 0x0057 | 1/23 | 2/23 | disabled |
| 0x00B8 | 0x0058 | 1/24 | 2/24 | disabled |
| 0x00B9 | 0x0059 | 1/25 | 2/25 | disabled |
| 0x00BA | 0x005A | 1/26 | 2/26 | disabled |
| 0x00BB | 0x005B | 1/27 | 2/27 | disabled |
| 0x00BC | 0x005C | 1/28 | 2/28 | disabled |

**Table 14 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #3 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0061 | 2/1 | 3/1 | disabled |
| 0x00C2 | 0x0062 | 2/2 | 3/2 | disabled |
| 0x00C3 | 0x0063 | 2/3 | 3/3 | disabled |
| 0x00C4 | 0x0064 | 2/4 | 3/4 | disabled |
| 0x00C5 | 0x0065 | 2/5 | 3/5 | disabled |
| 0x00C6 | 0x0066 | 2/6 | 3/6 | disabled |
| 0x00C7 | 0x0067 | 2/7 | 3/7 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C8 | 0x0068 | 2/8 | 3/8 | disabled |
| 0x00C9 | 0x0069 | 2/9 | 3/9 | disabled |
| 0x00CA | 0x006A | 2/10 | 3/10 | disabled |
| 0x00CB | 0x006B | 2/11 | 3/11 | disabled |
| 0x00CC | 0x006C | 2/12 | 3/12 | disabled |
| 0x00CD | 0x006D | 2/13 | 3/13 | disabled |
| 0x00CE | 0x006E | 2/14 | 3/14 | disabled |
| 0x00CF | 0x006F | 2/15 | 3/15 | disabled |
| 0x00D0 | 0x0070 | 2/16 | 3/16 | disabled |
| 0x00D1 | 0x0071 | 2/17 | 3/17 | disabled |
| 0x00D2 | 0x0072 | 2/18 | 3/18 | disabled |
| 0x00D3 | 0x0073 | 2/19 | 3/19 | disabled |
| 0x00D4 | 0x0074 | 2/20 | 3/20 | disabled |
| 0x00D5 | 0x0075 | 2/21 | 3/21 | disabled |
| 0x00D6 | 0x0076 | 2/22 | 3/22 | disabled |
| 0x00D7 | 0x0077 | 2/23 | 3/23 | disabled |
| 0x00D8 | 0x0078 | 2/24 | 3/24 | disabled |
| 0x00D9 | 0x0079 | 2/25 | 3/25 | disabled |
| 0x00DA | 0x007A | 2/26 | 3/26 | disabled |
| 0x00DB | 0x007B | 2/27 | 3/27 | disabled |
| 0x00DC | 0x007C | 2/28 | 3/28 | disabled |

**Table 15 Detailed DS3 Mapping RAM Configuration for AAL1gator-32 #3 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0021 | 3/1 | 1/1 | enabled |
| 0x00E2 | 0x0022 | 3/2 | 1/2 | enabled |
| 0x00E3 | 0x0023 | 3/3 | 1/3 | enabled |
| 0x00E4 | 0x0024 | 3/4 | 1/4 | enabled |
| 0x00E5 | 0x0025 | 3/5 | 1/5 | enabled |
| 0x00E6 | 0x0026 | 3/6 | 1/6 | enabled |
| 0x00E7 | 0x0027 | 3/7 | 1/7 | enabled |
| 0x00E8 | 0x0028 | 3/8 | 1/8 | enabled |
| 0x00E9 | 0x0029 | 3/9 | 1/9 | enabled |
| 0x00EA | 0x002A | 3/10 | 1/10 | enabled |
| 0x00EB | 0x002B | 3/11 | 1/11 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00EC | 0x002C | 3/12 | 1/12 | enabled |
| 0x00ED | 0x002D | 3/13 | 1/13 | enabled |
| 0x00EE | 0x002E | 3/14 | 1/14 | enabled |
| 0x00EF | 0x002F | 3/15 | 1/15 | enabled |
| 0x00F0 | 0x0030 | 3/16 | 1/16 | enabled |
| 0x00F1 | 0x0041 | 3/17 | 2/1 | enabled |
| 0x00F2 | 0x0042 | 3/18 | 2/2 | enabled |
| 0x00F3 | 0x0043 | 3/19 | 2/3 | enabled |
| 0x00F4 | 0x0044 | 3/20 | 2/4 | enabled |
| 0x00F5 | 0x0045 | 3/21 | 2/5 | enabled |
| 0x00F6 | 0x0046 | 3/22 | 2/6 | enabled |
| 0x00F7 | 0x0047 | 3/23 | 2/7 | enabled |
| 0x00F8 | 0x0048 | 3/24 | 2/8 | enabled |
| 0x00F9 | 0x0049 | 3/25 | 2/9 | enabled |
| 0x00FA | 0x004A | 3/26 | 2/10 | enabled |
| 0x00FB | 0x004B | 3/27 | 2/11 | enabled |
| 0x00FC | 0x004C | 3/28 | 2/12 | enabled |

## 6.3 Configuring 63 E1s For Three TEMUXs and Three AAL1gator-32s

In E1 mode, each SPE carries only 21 tributaries. It is important not to set a control or mapping address greater than 21. Doing so sets the HST_ADDR_ERR bit, which indicates that the access has failed. The hardware will refuse to honor the access and the RAM will not be written at the locations. The HST_ADDR_ERR bit is found in the Extract Tributary RAM Indirect Access Control register (EXT_TRIAC) (0x80404) and in the Insert Tributary RAM Indirect Access Control register (INS_TRIAC) (0x80504).

### 6.3.1 Configuring the SBI bus registers

Use the SBI configuration sequence shown in Section 6.2 to configure 63 E1s. Be sure to specify the type (TYP) as E1.

### 6.3.2 Mapping Summary

Table 16, Table 17, and Table 18 provide summaries of the mapping that should be done for each AAL1gator-32.

**Table 16 AAL1gator-32 #1 Mapping Summary for 21 E2s per SPE**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | Enabled |
|---|---|---|---|---|---|
| SPE 1 | 1–16 | 1 | SPE 1 | 1–16 | enabled |
| | 17–21 | | SPE 2 | 1–5 | enabled |
| SPE 2 | 1–5 | | SPE 1 | 17–21 | disabled |
| | 6–21 | | SPE 2 | 6–21 | disabled |
| SPE 3 | 1–21 | | SPE 3 | 1–21 | disabled |

**Table 17 AAL1gator-32 #2 Mapping Summary For 21 E2s Per SPE**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | Enabled |
|---|---|---|---|---|---|
| SPE 1 | 1–5 | 2 | SPE 1 | 17–21 | disabled |
| | 6–21 | | SPE 2 | 6–21 | disabled |
| SPE 2 | 1–16 | | SPE 1 | 1–16 | enabled |
| | 17–21 | | SPE 2 | 1–5 | enabled |
| SPE 3 | 1–21 | | SPE 3 | 1–21 | disabled |

**Table 18 AAL1gator-32 #3 Mapping Summary For 21 E2s Per SPE**

| SBI SPE # | Tributary # | A32 Link Group # | SBI-IP SPE # | SBI-IP Tributary # | Enabled |
|---|---|---|---|---|---|
| 1 | 1–5 | 3 | SPE 1 | 17–21 | disabled |
| | 6–21 | | SPE 2 | 6–21 | disabled |
| 2 | 1–21 | | SPE 3 | 1–21 | disabled |
| 3 | 1–16 | | SPE 1 | 1–16 | enabled |
| | 17–21 | 3 | SPE 2 | 1–5 | Yes |

### 6.3.3 Detailed Mapping RAM for AAL1gator-32 #1

Note: Detailed mapping RAM configurations tables are provided only for the first AAL1gator-32.

Table 19 contains the detailed mapping RAM configuration data for SPE 1 of the first AAL1gator-32.

**Table 19 Detailed 21 E2s Mapping RAM Configuration for AAL1gator-32 #1 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0021 | 1/1 | 1/1 | enabled |
| 0x00A2 | 0x0022 | 1/2 | 1/2 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A3 | 0x0023 | 1/3 | 1/3 | enabled |
| 0x00A4 | 0x0024 | 1/4 | 1/4 | enabled |
| 0x00A5 | 0x0025 | 1/5 | 1/5 | enabled |
| 0x00A6 | 0x0026 | 1/6 | 1/6 | enabled |
| 0x00A7 | 0x0027 | 1/7 | 1/7 | enabled |
| 0x00A8 | 0x0028 | 1/8 | 1/8 | enabled |
| 0x00A9 | 0x0029 | 1/9 | 1/9 | enabled |
| 0x00AA | 0x002A | 1/10 | 1/10 | enabled |
| 0x00AB | 0x002B | 1/11 | 1/11 | enabled |
| 0x00AC | 0x002C | 1/12 | 1/12 | enabled |
| 0x00AD | 0x002D | 1/13 | 1/13 | enabled |
| 0x00AE | 0x002E | 1/14 | 1/14 | enabled |
| 0x00AF | 0x002F | 1/15 | 1/15 | enabled |
| 0x00B0 | 0x0030 | 1/16 | 1/16 | enabled |
| 0x00B1 | 0x0041 | 1/17 | 2/1 | enabled |
| 0x00B2 | 0x0042 | 1/18 | 2/2 | enabled |
| 0x00B3 | 0x0043 | 1/19 | 2/3 | enabled |
| 0x00B4 | 0x0044 | 1/20 | 2/4 | enabled |
| 0x00B5 | 0x0045 | 1/21 | 2/5 | enabled |

Table 20 contains the detailed mapping RAM configuration data for SPE 2 of the first AAL1gator-32.

**Table 20 Detailed 21 E2s Mapping RAM Configuration for AAL1gator-32 #1 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0031 | 2/1 | 1/17 | disabled |
| 0x00C2 | 0x0032 | 2/2 | 1/18 | disabled |
| 0x00C3 | 0x0033 | 2/3 | 1/19 | disabled |
| 0x00C4 | 0x0034 | 2/4 | 1/20 | disabled |
| 0x00C5 | 0x0035 | 2/5 | 1/21 | disabled |
| 0x00C6 | 0x0046 | 2/6 | 2/6 | disabled |
| 0x00C7 | 0x0047 | 2/7 | 2/7 | disabled |
| 0x00C8 | 0x0048 | 2/8 | 2/8 | disabled |
| 0x00C9 | 0x0049 | 2/9 | 2/9 | disabled |
| 0x00CA | 0x004A | 2/10 | 2/10 | disabled |
| 0x00CB | 0x004B | 2/11 | 2/11 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00CC | 0x004C | 2/12 | 2/12 | disabled |
| 0x00CD | 0x004D | 2/13 | 2/13 | disabled |
| 0x00CE | 0x004E | 2/14 | 2/14 | disabled |
| 0x00CF | 0x004F | 2/15 | 2/15 | disabled |
| 0x00D0 | 0x0050 | 2/16 | 2/16 | disabled |
| 0x00D1 | 0x0051 | 2/17 | 2/17 | disabled |
| 0x00D2 | 0x0052 | 2/18 | 2/18 | disabled |
| 0x00D3 | 0x0053 | 2/19 | 2/19 | disabled |
| 0x00D4 | 0x0054 | 2/20 | 2/20 | disabled |
| 0x00D5 | 0x0055 | 2/21 | 2/21 | disabled |

Table 21 contains the detailed mapping RAM configuration data for SPE 3 of the first AAL1gator-32.

**Table 21 Detailed 21 E2s Mapping RAM Configuration for AAL1gator-32 #1 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0061 | 3/1 | 3/1 | disabled |
| 0x00E2 | 0x0062 | 3/2 | 3/2 | disabled |
| 0x00E3 | 0x0063 | 3/3 | 3/3 | disabled |
| 0x00E4 | 0x0064 | 3/4 | 3/4 | disabled |
| 0x00E5 | 0x0065 | 3/5 | 3/5 | disabled |
| 0x00E6 | 0x0066 | 3/6 | 3/6 | disabled |
| 0x00E7 | 0x0067 | 3/7 | 3/7 | disabled |
| 0x00E8 | 0x0068 | 3/8 | 3/8 | disabled |
| 0x00E9 | 0x0069 | 3/9 | 3/9 | disabled |
| 0x00EA | 0x006A | 3/10 | 3/10 | disabled |
| 0x00EB | 0x006B | 3/11 | 3/11 | disabled |
| 0x00EC | 0x006C | 3/12 | 3/12 | disabled |
| 0x00ED | 0x006D | 3/13 | 3/13 | disabled |
| 0x00EE | 0x006E | 3/14 | 3/14 | disabled |
| 0x00EF | 0x006F | 3/15 | 3/15 | disabled |
| 0x00F0 | 0x0070 | 3/16 | 3/16 | disabled |
| 0x00F1 | 0x0071 | 3/17 | 3/17 | disabled |
| 0x00F2 | 0x0072 | 3/18 | 3/18 | disabled |
| 0x00F3 | 0x0073 | 3/19 | 3/19 | disabled |
| 0x00F4 | 0x0074 | 3/20 | 3/20 | disabled |

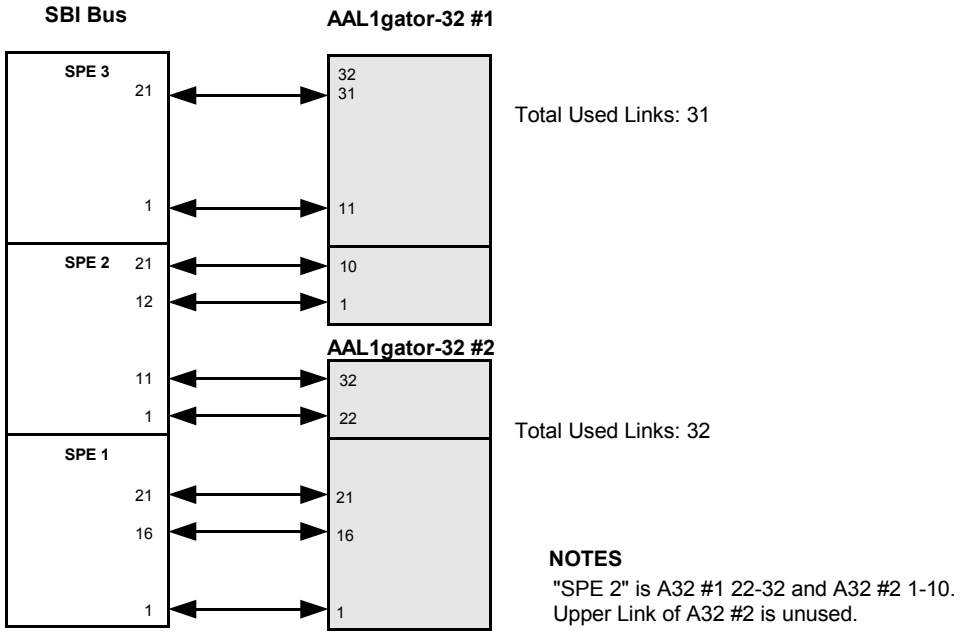
| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00F5 | 0x0075 | 3/21 | 3/21 | disabled |

## 6.4 Configuring 63 E1s For Three TEMUXs and Two AAL1gator-32s

A three-TEMUX/two-AAL1gator-32 configuration is a more efficient way of configuring 63 E1s. T1 support is not required in this instance.

Figure 7 illustrates the mapping that needs to be done when using two AAL1gator-32s instead of three for 63 (21x3) E1s.

**Figure 7 Mapping 63 E1s to Two AAL1gator-32s**




SPE 1 is mapped directly into the lowest 21 links of AAL1gator-32#1. SPE 2 is split between the remaining upper 11 links of AAL1gator-32#1, and the lower 10 links of AAL1gator-32#2. SPE 3 is mapped directly into the next upper 21 links of AAL1gator-32#2, with link #32 of AAL1gator-32#2 remaining unused.

### 6.4.1 Configuring the SBI bus Registers

Use the following sequence to configure the SBI bus registers for 63 E1s for efficient mapping.

To configure the first AAL1gator-32:

1. Prepare the SBI bus registers for mapping:

```
wr 0x80300 0x0015 ; set SPEx_TYP=E1; keep SPEs disabled
wr 0x80400 0x0041 ; default
wr 0x80500 0x0041 ; default
wr 0x80301 0x0101 ; set LINK_TYPx=E1
wr 0x80302 0x0000 ; set LINK_DISx=0
wr 0x80303 0x0000 ; set LINK_DISx=0
wr 0x80304 0x0000 ; set SYNC_LINKx=0
wr 0x80305 0x0000 ; set SYNC_LINKx=0
```

2. Load the mapping and control RAMs:

   Note: Insert the specified mapping and control RAM writes here.

```
; load SBI EXSBI Mapping RAM for A32 #1
; load SBI INSBI Mapping RAM for A32 #1
; load SBI EXSBI Control RAM for A32 #1
; load SBI INSBI Control RAM for A32 #1
```

3. After the RAMs have been configured, enable mapping:

```
wr 0x80300 0x2015 ; set global ts_en=1
wr 0x80400 0x0045 ; set exsbi ts_en=1 to enable exsbi mapping
wr 0x80500 0x0045 ; set insbi ts_en=1 to enable insbi mapping
```

4. After the mapping is enabled, enable the SPEs:

```
wr 0x80300 0x20D5 ; enable SPE 1 and SPE 2 on A32 #1
```

To configure the second AAL1gator-32:

1. Prepare the SBI bus registers for mapping:

```
wr 0x80300 0x0015 ; set SPEx_TYP=E1; keep SPEs disabled
wr 0x80400 0x0041 ; default
wr 0x80500 0x0041 ; default

wr 0x80301 0x0101 ; set LINK_TYPx=E1
wr 0x80302 0x0000 ; set LINK_DISx=0
```

```
wr 0x80303 0x0000 ; set LINK_DISx=0
wr 0x80304 0x0000 ; set SYNC_LINKx=0
wr 0x80305 0x0000 ; set SYNC_LINKx=0
```

2. Load the mapping and control RAMs:

   Note: Insert the specified mapping and control RAM writes here.

```
; load SBI EXSBI Mapping RAM for A32 #2
; load SBI INSBI Mapping RAM for A32 #2
; load SBI EXSBI Control RAM for A32 #2
; load SBI INSBI Control RAM for A32 #2
```

3. After the RAMs have been configured, enable mapping:

```
wr 0x80300 0x2015 ; set global ts_en=1
wr 0x80400 0x0045 ; set exsbi ts_en=1 to enable exsbi mapping
wr 0x80500 0x0045 ; set insbi ts_en=1 to enable insbi mapping
```

4. After mapping is enabled, enable the SPEs:

```
wr 0x80300 0x2195 ; enable SPE 2 and SPE 3 on A32 #1
```

### 6.4.2 Mapping Summary

Table 22 and Table 23 provide summaries of the mapping that should be done for each of the two AAL1gator-32s when configuring for 21x3 E1s. For the first AAL1gator-32, map the 32 (21+11) SBI bus tributaries into all 32 of the AAL1gator-32 A1SP links. For the second AAL1gator-32, map 31 (10+21) SBI bus tributaries into the upper 31 AAL1gator-32 A1SP links.

**Table 22 AAL1gator-32 #1 Mapping Summary for 63 E1s**

| SBI SPE # | Mapping from SBI SPE Tributary | SBI-IP SPE # | Mapping to SBI-IP SPE Tributary | TRIB_ENBL |
|---|---|---|---|---|
| SPE 1 | 1–16 | SPE 1 | 1–16 | enabled |
| | 17–21 | SPE 2 | 1–5 | enabled |
| SPE 2 | 1–11 | SPE 2 | 6–16 | enabled |
| | 12–16 | SPE 1 | 17–21 | disabled |
| | 17–21 | SPE 2 | 17–21 | disabled |
| SPE 3 | 1–21 | SPE 3 | 1–21 | disabled |

**Table 23 AAL1gator-32 #2 Mapping Summary for 63 E1s**

| SBI SPE # | Mapping from SBI SPE Tributary | SBI-IP SPE # | Mapping to SBI-IP SPE Tributary | TRIB_ENBL |
|---|---|---|---|---|
| SPE 1 | 1–21 | SPE 3 | 1–21 | disabled |
| SPE 2 | 1–5 | SPE 1 | 17–21 | disabled |
| | 6–11 | SPE 2 | 16–21 | disabled |
| | 12–21 | SPE 1 | 1–10 | enabled |
| SPE 3 | 1–6 | SPE 1 | 11–16 | enabled |
| | 7–21 | SPE 2 | 1–15 | enabled |

### 6.4.3 Detailed Mapping and Control RAM for AAL1gator-32 #1

Table 24 contains the detailed mapping RAM configuration data for SPE 1 of the first AAL1gator-32.

**Table 24 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #1 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0021 | 1/1 | 1/1 | enabled |
| 0x00A2 | 0x0022 | 1/2 | 1/2 | enabled |
| 0x00A3 | 0x0023 | 1/3 | 1/3 | enabled |
| 0x00A4 | 0x0024 | 1/4 | 1/4 | enabled |
| 0x00A5 | 0x0025 | 1/5 | 1/5 | enabled |
| 0x00A6 | 0x0026 | 1/6 | 1/6 | enabled |
| 0x00A7 | 0x0027 | 1/7 | 1/7 | enabled |
| 0x00A8 | 0x0028 | 1/8 | 1/8 | enabled |
| 0x00A9 | 0x0029 | 1/9 | 1/9 | enabled |
| 0x00AA | 0x002A | 1/10 | 1/10 | enabled |
| 0x00AB | 0x002B | 1/11 | 1/11 | enabled |
| 0x00AC | 0x002C | 1/12 | 1/12 | enabled |
| 0x00AD | 0x002D | 1/13 | 1/13 | enabled |
| 0x00AE | 0x002E | 1/14 | 1/14 | enabled |
| 0x00AF | 0x002F | 1/15 | 1/15 | enabled |
| 0x00B0 | 0x0030 | 1/16 | 1/16 | enabled |
| 0x00B1 | 0x0041 | 1/17 | 2/1 | enabled |
| 0x00B2 | 0x0042 | 1/18 | 2/2 | enabled |
| 0x00B3 | 0x0043 | 1/19 | 2/3 | enabled |
| 0x00B4 | 0x0044 | 1/20 | 2/4 | enabled |
| 0x00B5 | 0x0045 | 1/21 | 2/5 | enabled |

Table 25 contains the detailed mapping RAM configuration data for SPE 2 of the first AAL1gator-32.

**Table 25 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #1 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0046 | 2/1 | 2/6 | enabled |
| 0x00C2 | 0x0047 | 2/2 | 2/7 | enabled |
| 0x00C3 | 0x0048 | 2/3 | 2/8 | enabled |
| 0x00C4 | 0x0049 | 2/4 | 2/9 | enabled |
| 0x00C5 | 0x004A | 2/5 | 2/10 | enabled |
| 0x00C6 | 0x004B | 2/6 | 2/11 | enabled |
| 0x00C7 | 0x004C | 2/7 | 2/12 | enabled |
| 0x00C8 | 0x004D | 2/8 | 2/13 | enabled |
| 0x00C9 | 0x004E | 2/9 | 2/14 | enabled |
| 0x00CA | 0x004F | 2/10 | 2/15 | enabled |
| 0x00CB | 0x0050 | 2/11 | 2/16 | enabled |
| 0x00CC | 0x0031 | 2/12 | 1/17 | disabled |
| 0x00CD | 0x0032 | 2/13 | 1/18 | disabled |
| 0x00CE | 0x0033 | 2/14 | 1/19 | disabled |
| 0x00CF | 0x0034 | 2/15 | 1/20 | disabled |
| 0x00D0 | 0x0035 | 2/16 | 1/21 | disabled |
| 0x00D1 | 0x0051 | 2/17 | 2/17 | disabled |
| 0x00D2 | 0x0052 | 2/18 | 2/18 | disabled |
| 0x00D3 | 0x0053 | 2/19 | 2/19 | disabled |
| 0x00D4 | 0x0054 | 2/20 | 2/20 | disabled |
| 0x00D5 | 0x0055 | 2/21 | 2/21 | disabled |

Table 26 contains the detailed mapping RAM configuration data for SPE 3 of the first AAL1gator-32.

**Table 26 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #1 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0061 | 3/1 | 3/1 | disabled |
| 0x00E2 | 0x0062 | 3/2 | 3/2 | disabled |
| 0x00E3 | 0x0063 | 3/3 | 3/3 | disabled |
| 0x00E4 | 0x0064 | 3/4 | 3/4 | disabled |
| 0x00E5 | 0x0065 | 3/5 | 3/5 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E6 | 0x0066 | 3/6 | 3/6 | disabled |
| 0x00E7 | 0x0067 | 3/7 | 3/7 | disabled |
| 0x00E8 | 0x0068 | 3/8 | 3/8 | disabled |
| 0x00E9 | 0x0069 | 3/9 | 3/9 | disabled |
| 0x00EA | 0x006A | 3/10 | 3/10 | disabled |
| 0x00EB | 0x006B | 3/11 | 3/11 | disabled |
| 0x00EC | 0x006C | 3/12 | 3/12 | disabled |
| 0x00ED | 0x006D | 3/13 | 3/13 | disabled |
| 0x00EE | 0x006E | 3/14 | 3/14 | disabled |
| 0x00EF | 0x006F | 3/15 | 3/15 | disabled |
| 0x00F0 | 0x0070 | 3/16 | 3/16 | disabled |
| 0x00F1 | 0x0071 | 3/17 | 3/17 | disabled |
| 0x00F2 | 0x0072 | 3/18 | 3/18 | disabled |
| 0x00F3 | 0x0073 | 3/19 | 3/19 | disabled |
| 0x00F4 | 0x0074 | 3/20 | 3/20 | disabled |
| 0x00F5 | 0x0075 | 3/21 | 3/21 | disabled |

Table 27 contains the control RAM mapping settings.

Writing to 0x0049 sets the EXSBI “use only phase field of EXT_LINKRATE”, the unstructured tributaries, and the tributary enabled bits. Writing to 0x0019 sets the INSBI as clock master, and the INSBI unstructured tributaries and tributary enabled bits. Writing to the Insert Tributary Control register enables the INSBI to take tributary data from an SBI tributary and transmit it to the local link mapped to that tributary.

Writing to 0x0048 sets the same EXSBI bits as 0x0049 except the tributary is disabled. Writing to 0x0018 is the same.

**Table 27 AAL1gator-32 #1 Control RAM (E1 unstructured, INSBI clock master) for SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0021 | 0x0049/0x0019 | enabled |
| 0x0022 | 0x0049/0x0019 | enabled |
| 0x0023 | 0x0049/0x0019 | enabled |
| 0x0024 | 0x0049/0x0019 | enabled |
| 0x0025 | 0x0049/0x0019 | enabled |
| 0x0026 | 0x0049/0x0019 | enabled |
| 0x0027 | 0x0049/0x0019 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0028 | 0x0049/0x0019 | enabled |
| 0x0029 | 0x0049/0x0019 | enabled |
| 0x002A | 0x0049/0x0019 | enabled |
| 0x002B | 0x0049/0x0019 | enabled |
| 0x002C | 0x0049/0x0019 | enabled |
| 0x002D | 0x0049/0x0019 | enabled |
| 0x002E | 0x0049/0x0019 | enabled |
| 0x002F | 0x0049/0x0019 | enabled |
| 0x0030 | 0x0049/0x0019 | enabled |
| 0x0031 | 0x0049/0x0019 | enabled |
| 0x0032 | 0x0049/0x0019 | enabled |
| 0x0033 | 0x0049/0x0019 | enabled |
| 0x0034 | 0x0049/0x0019 | enabled |
| 0x0035 | 0x0049/0x0019 | enabled |

**Table 28 AAL1gator-32 #1 Control RAM (E1 unstructured, INSBI clock master) for SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0041 | 0x0049/0x0019 | enabled |
| 0x0042 | 0x0049/0x0019 | enabled |
| 0x0043 | 0x0049/0x0019 | enabled |
| 0x0044 | 0x0049/0x0019 | enabled |
| 0x0045 | 0x0049/0x0019 | enabled |
| 0x0046 | 0x0049/0x0019 | enabled |
| 0x0047 | 0x0049/0x0019 | enabled |
| 0x0048 | 0x0049/0x0019 | enabled |
| 0x0049 | 0x0049/0x0019 | enabled |
| 0x004A | 0x0049/0x0019 | enabled |
| 0x004B | 0x0049/0x0019 | enabled |
| 0x004C | 0x0048/0x0018 | disabled |
| 0x004D | 0x0048/0x0018 | disabled |
| 0x004E | 0x0048/0x0018 | disabled |
| 0x004F | 0x0048/0x0018 | disabled |
| 0x0050 | 0x0048/0x0018 | disabled |
| 0x0051 | 0x0048/0x0018 | disabled |
| 0x0052 | 0x0048/0x0018 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0053 | 0x0048/0x0018 | disabled |
| 0x0054 | 0x0048/0x0018 | disabled |
| 0x0055 | 0x0048/0x0018 | disabled |

**Table 29 AAL1gator-32 #1 Control RAM (E1 unstructured, INSBI clock master) for SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0061 | 0x0048/0x0018 | disabled |
| 0x0062 | 0x0048/0x0018 | disabled |
| 0x0063 | 0x0048/0x0018 | disabled |
| 0x0064 | 0x0048/0x0018 | disabled |
| 0x0065 | 0x0048/0x0018 | disabled |
| 0x0066 | 0x0048/0x0018 | disabled |
| 0x0067 | 0x0048/0x0018 | disabled |
| 0x0068 | 0x0048/0x0018 | disabled |
| 0x0069 | 0x0048/0x0018 | disabled |
| 0x006A | 0x0048/0x0018 | disabled |
| 0x006B | 0x0048/0x0018 | disabled |
| 0x006C | 0x0048/0x0018 | disabled |
| 0x006D | 0x0048/0x0018 | disabled |
| 0x006E | 0x0048/0x0018 | disabled |
| 0x006F | 0x0048/0x0018 | disabled |
| 0x0070 | 0x0048/0x0018 | disabled |
| 0x0071 | 0x0048/0x0018 | disabled |
| 0x0072 | 0x0048/0x0018 | disabled |
| 0x0073 | 0x0048/0x0018 | disabled |
| 0x0074 | 0x0048/0x0018 | disabled |
| 0x0075 | 0x0048/0x0018 | disabled |

### 6.4.4 Detailed Mapping and Control RAM for AAL1gator-32 #2

Table 30 contains the detailed mapping RAM configuration data for SPE 1 of the second AAL1gator-32.

**Table 30 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #2 SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0061 | 1/1 | 3/1 | disabled |
| 0x00A2 | 0x0062 | 1/2 | 3/2 | disabled |
| 0x00A3 | 0x0063 | 1/3 | 3/3 | disabled |
| 0x00A4 | 0x0064 | 1/4 | 3/4 | disabled |
| 0x00A5 | 0x0065 | 1/5 | 3/5 | disabled |
| 0x00A6 | 0x0066 | 1/6 | 3/6 | disabled |
| 0x00A7 | 0x0067 | 1/7 | 3/7 | disabled |
| 0x00A8 | 0x0068 | 1/8 | 3/8 | disabled |
| 0x00A9 | 0x0069 | 1/9 | 3/9 | disabled |
| 0x00AA | 0x006A | 1/10 | 3/10 | disabled |
| 0x00AB | 0x006B | 1/11 | 3/11 | disabled |
| 0x00AC | 0x006C | 1/12 | 3/12 | disabled |
| 0x00AD | 0x006D | 1/13 | 3/13 | disabled |
| 0x00AE | 0x006E | 1/14 | 3/14 | disabled |
| 0x00AF | 0x006F | 1/15 | 3/15 | disabled |
| 0x00B0 | 0x0070 | 1/16 | 3/16 | disabled |
| 0x00B1 | 0x0071 | 1/17 | 3/17 | disabled |
| 0x00B2 | 0x0072 | 1/18 | 3/18 | disabled |
| 0x00B3 | 0x0073 | 1/19 | 3/19 | disabled |
| 0x00B4 | 0x0074 | 1/20 | 3/20 | disabled |
| 0x00B5 | 0x0075 | 1/21 | 3/21 | disabled |

Table 31 contains the detailed mapping RAM configuration data for SPE 2 of the second AAL1gator-32.

**Table 31 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #2 SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0031 | 2/1 | 1/17 | disabled |
| 0x00C2 | 0x0032 | 2/2 | 1/18 | disabled |
| 0x00C3 | 0x0033 | 2/3 | 1/19 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C4 | 0x0034 | 2/4 | 1/20 | disabled |
| 0x00C5 | 0x0035 | 2/5 | 1/21 | disabled |
| 0x00C6 | 0x0050 | 2/6 | 2/16 | enabled (but unused) |
| 0x00C7 | 0x0051 | 2/7 | 2/17 | disabled |
| 0x00C8 | 0x0052 | 2/8 | 2/18 | disabled |
| 0x00C9 | 0x0053 | 2/9 | 2/19 | disabled |
| 0x00CA | 0x0054 | 2/10 | 2/20 | disabled |
| 0x00CB | 0x0055 | 2/11 | 2/21 | disabled |
| 0x00CC | 0x0021 | 2/12 | 1/1 | enabled |
| 0x00CD | 0x0022 | 2/13 | 1/2 | enabled |
| 0x00CE | 0x0023 | 2/14 | 1/3 | enabled |
| 0x00CF | 0x0024 | 2/15 | 1/4 | enabled |
| 0x00D0 | 0x0025 | 2/16 | 1/5 | enabled |
| 0x00D1 | 0x0026 | 2/17 | 1/6 | enabled |
| 0x00D2 | 0x0027 | 2/18 | 1/7 | enabled |
| 0x00D3 | 0x0028 | 2/19 | 1/8 | enabled |
| 0x00D4 | 0x0029 | 2/20 | 1/9 | enabled |
| 0x00D5 | 0x002A | 2/21 | 1/10 | enabled |

Table 32 contains the detailed mapping RAM configuration data for SPE 3 of the second AAL1gator-32.

**Table 32 Detailed 63 E1s Mapping RAM Configuration for AAL1gator-32 #2 SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x002B | 3/1 | 1/11 | enabled |
| 0x00E2 | 0x002C | 3/2 | 1/12 | enabled |
| 0x00E3 | 0x002D | 3/3 | 1/13 | enabled |
| 0x00E4 | 0x002E | 3/4 | 1/14 | enabled |
| 0x00E5 | 0x002F | 3/5 | 1/15 | enabled |
| 0x00E6 | 0x0030 | 3/6 | 1/16 | enabled |
| 0x00E7 | 0x0041 | 3/7 | 2/1 | enabled |
| 0x00E8 | 0x0042 | 3/8 | 2/2 | enabled |
| 0x00E9 | 0x0043 | 3/9 | 2/3 | enabled |
| 0x00EA | 0x0044 | 3/10 | 2/4 | enabled |
| 0x00EB | 0x0045 | 3/11 | 2/5 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00EC | 0x0046 | 3/12 | 2/6 | enabled |
| 0x00ED | 0x0047 | 3/13 | 2/7 | enabled |
| 0x00EE | 0x0048 | 3/14 | 2/8 | enabled |
| 0x00EF | 0x0049 | 3/15 | 2/9 | enabled |
| 0x00F0 | 0x004A | 3/16 | 2/10 | enabled |
| 0x00F1 | 0x004B | 3/17 | 2/11 | enabled |
| 0x00F2 | 0x004C | 3/18 | 2/12 | enabled |
| 0x00F3 | 0x004D | 3/19 | 2/13 | enabled |
| 0x00F4 | 0x004E | 3/20 | 2/14 | enabled |
| 0x00F5 | 0x004F | 3/21 | 2/15 | enabled |

Table 33 shows the detailed control RAM configuration.

Writing to 0x0048 sets the EXSBI “use only phase field of EXT_LINKRATE”, the unstructured tributaries, and the tributary disabled bits. Writing to 0x0018 sets the INSBI as clock master, and the INSBI unstructured tributaries and tributary disabled bits. Writing to the Insert Tributary Control register enables the INSBI to take tributary data from an SBI tributary and transmit it to the local link mapped to that tributary.

**Table 33 AAL1gator-32 #2 Control RAM (E1 unstructured, INSBI clock master) for SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0021 | 0x0048/0x0018 | disabled |
| 0x0022 | 0x0048/0x0018 | disabled |
| 0x0023 | 0x0048/0x0018 | disabled |
| 0x0024 | 0x0048/0x0018 | disabled |
| 0x0025 | 0x0048/0x0018 | disabled |
| 0x0026 | 0x0048/0x0018 | disabled |
| 0x0027 | 0x0048/0x0018 | disabled |
| 0x0028 | 0x0048/0x0018 | disabled |
| 0x0029 | 0x0048/0x0018 | disabled |
| 0x002A | 0x0048/0x0018 | disabled |
| 0x002B | 0x0048/0x0018 | disabled |
| 0x002C | 0x0048/0x0018 | disabled |
| 0x002D | 0x0048/0x0018 | disabled |
| 0x002E | 0x0048/0x0018 | disabled |
| 0x002F | 0x0048/0x0018 | disabled |
| 0x0030 | 0x0048/0x0018 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0031 | 0x0048/0x0018 | disabled |
| 0x0032 | 0x0048/0x0018 | disabled |
| 0x0033 | 0x0048/0x0018 | disabled |
| 0x0034 | 0x0048/0x0018 | disabled |
| 0x0035 | 0x0048/0x0018 | disabled |

**Table 34 AAL1gator-32 #2 Control RAM (E1 unstructured, INSBI clock master) for SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0041 | 0x0048/0x0018 | disabled |
| 0x0042 | 0x0048/0x0018 | disabled |
| 0x0043 | 0x0048/0x0018 | disabled |
| 0x0044 | 0x0048/0x0018 | disabled |
| 0x0045 | 0x0048/0x0018 | disabled |
| 0x0046 | 0x0048/0x0018 | disabled |
| 0x0047 | 0x0048/0x0018 | disabled |
| 0x0048 | 0x0048/0x0018 | disabled |
| 0x0049 | 0x0048/0x0018 | disabled |
| 0x004A | 0x0048/0x0018 | disabled |
| 0x004B | 0x0048/0x0018 | disabled |
| 0x004C | 0x0049/0x0019 | enabled |
| 0x004D | 0x0049/0x0019 | enabled |
| 0x004E | 0x0049/0x0019 | enabled |
| 0x004F | 0x0049/0x0019 | enabled |
| 0x0050 | 0x0049/0x0019 | enabled |
| 0x0051 | 0x0049/0x0019 | enabled |
| 0x0052 | 0x0049/0x0019 | enabled |
| 0x0053 | 0x0049/0x0019 | enabled |
| 0x0054 | 0x0049/0x0019 | enabled |
| 0x0055 | 0x0049/0x0019 | enabled |

**Table 35 AAL1gator-32 #2 Control RAM (E1 unstructured, INSBI clock master) for SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0061 | 0x0049/0x0019 | enabled |
| 0x0062 | 0x0049/0x0019 | enabled |
| 0x0063 | 0x0049/0x0019 | enabled |
| 0x0064 | 0x0049/0x0019 | enabled |
| 0x0065 | 0x0049/0x0019 | enabled |
| 0x0066 | 0x0049/0x0019 | enabled |
| 0x0067 | 0x0049/0x0019 | enabled |
| 0x0068 | 0x0049/0x0019 | enabled |
| 0x0069 | 0x0049/0x0019 | enabled |
| 0x006A | 0x0049/0x0019 | enabled |
| 0x006B | 0x0049/0x0019 | enabled |
| 0x006C | 0x0049/0x0019 | enabled |
| 0x006D | 0x0049/0x0019 | enabled |
| 0x006E | 0x0049/0x0019 | enabled |
| 0x006F | 0x0049/0x0019 | enabled |
| 0x0070 | 0x0049/0x0019 | enabled |
| 0x0071 | 0x0049/0x0019 | enabled |
| 0x0072 | 0x0049/0x0019 | enabled |
| 0x0073 | 0x0049/0x0019 | enabled |
| 0x0074 | 0x0049/0x0019 | enabled |
| 0x0075 | 0x0049/0x0019 | enabled |

## 6.5 Configuring 32 E1s for Debugging Purposes

This configuration is used for 1:1 mapping between three TEMUXs and two AAL1gator-32s. 1:1 mapping for E1 is functionally equivalent to disabling mapping and is therefore, a useful debugging tool.

### 6.5.1 Configuring the SBI bus registers

Use the standard configuration sequence shown in Section 6.4 to configure 32 E1s.

### 6.5.2 Detailed Mapping and Control RAM for AAL1gator-32 #1

Note: The detailed mapping RAM configuration is only shown for the first AAL1gator-32.

Table 36 contains the detailed mapping RAM configuration data for SPE 1 for configuring 32 E1s.

**Table 36 Detailed Mapping RAM Configuration for SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00A1 | 0x0021 | 1/1 | 1/1 | enabled |
| 0x00A2 | 0x0022 | 1/2 | 1/2 | enabled |
| 0x00A3 | 0x0023 | 1/3 | 1/3 | enabled |
| 0x00A4 | 0x0024 | 1/4 | 1/4 | enabled |
| 0x00A5 | 0x0025 | 1/5 | 1/5 | enabled |
| 0x00A6 | 0x0026 | 1/6 | 1/6 | enabled |
| 0x00A7 | 0x0027 | 1/7 | 1/7 | enabled |
| 0x00A8 | 0x0028 | 1/8 | 1/8 | enabled |
| 0x00A9 | 0x0029 | 1/9 | 1/9 | enabled |
| 0x00AA | 0x002A | 1/10 | 1/10 | enabled |
| 0x00AB | 0x002B | 1/11 | 1/11 | enabled |
| 0x00AC | 0x002C | 1/12 | 1/12 | enabled |
| 0x00AD | 0x002D | 1/13 | 1/13 | enabled |
| 0x00AE | 0x002E | 1/14 | 1/14 | enabled |
| 0x00AF | 0x002F | 1/15 | 1/15 | enabled |
| 0x00B0 | 0x0030 | 1/16 | 1/16 | enabled |
| 0x00B1 | 0x0031 | 1/17 | 1/17 | disabled |
| 0x00B2 | 0x0032 | 1/18 | 1/18 | disabled |
| 0x00B3 | 0x0033 | 1/19 | 1/19 | disabled |
| 0x00B4 | 0x0034 | 1/20 | 1/20 | disabled |
| 0x00B5 | 0x0035 | 1/21 | 1/21 | disabled |

Table 37 contains the detailed mapping RAM configuration data for SPE 2 for configuring 32 E1s.

**Table 37 Detailed Mapping RAM Configuration for SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C1 | 0x0041 | 2/1 | 2/1 | enabled |
| 0x00C2 | 0x0042 | 2/2 | 2/2 | enabled |
| 0x00C3 | 0x0043 | 2/3 | 2/3 | enabled |
| 0x00C4 | 0x0044 | 2/4 | 2/4 | enabled |
| 0x00C5 | 0x0045 | 2/5 | 2/5 | enabled |
| 0x00C6 | 0x0046 | 2/6 | 2/6 | enabled |
| 0x00C7 | 0x0047 | 2/7 | 2/7 | enabled |
| 0x00C8 | 0x0048 | 2/8 | 2/8 | enabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00C9 | 0x0049 | 2/9 | 2/9 | enabled |
| 0x00CA | 0x004A | 2/10 | 2/10 | enabled |
| 0x00CB | 0x004B | 2/11 | 2/11 | enabled |
| 0x00CC | 0x004C | 2/12 | 2/12 | enabled |
| 0x00CD | 0x004D | 2/13 | 2/13 | enabled |
| 0x00CE | 0x004E | 2/14 | 2/14 | enabled |
| 0x00CF | 0x004F | 2/15 | 2/15 | enabled |
| 0x00D0 | 0x0050 | 2/16 | 2/16 | enabled |
| 0x00D1 | 0x0051 | 2/17 | 2/17 | disabled |
| 0x00D2 | 0x0052 | 2/18 | 2/18 | disabled |
| 0x00D3 | 0x0053 | 2/19 | 2/19 | disabled |
| 0x00D4 | 0x0054 | 2/20 | 2/20 | disabled |
| 0x00D5 | 0x0055 | 2/21 | 2/21 | disabled |

Table 38 contains the detailed mapping RAM configuration data for SPE 3 for configuring 32 E1s.

**Table 38 Detailed Mapping RAM Configuration for SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00E1 | 0x0061 | 3/1 | 3/1 | disabled |
| 0x00E2 | 0x0062 | 3/2 | 3/2 | disabled |
| 0x00E3 | 0x0063 | 3/3 | 3/3 | disabled |
| 0x00E4 | 0x0064 | 3/4 | 3/4 | disabled |
| 0x00E5 | 0x0065 | 3/5 | 3/5 | disabled |
| 0x00E6 | 0x0066 | 3/6 | 3/6 | disabled |
| 0x00E7 | 0x0067 | 3/7 | 3/7 | disabled |
| 0x00E8 | 0x0068 | 3/8 | 3/8 | disabled |
| 0x00E9 | 0x0069 | 3/9 | 3/9 | disabled |
| 0x00EA | 0x006A | 3/10 | 3/10 | disabled |
| 0x00EB | 0x006B | 3/11 | 3/11 | disabled |
| 0x00EC | 0x006C | 3/12 | 3/12 | disabled |
| 0x00ED | 0x006D | 3/13 | 3/13 | disabled |
| 0x00EE | 0x006E | 3/14 | 3/14 | disabled |
| 0x00EF | 0x006F | 3/15 | 3/15 | disabled |
| 0x00F0 | 0x0070 | 3/16 | 3/16 | disabled |
| 0x00F1 | 0x0071 | 3/17 | 3/17 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | map_RAM data Registers EXSBI (0x80405) and INSBI (0x80505) | Mapping from SBI SPE/ Tributary | Mapping to SBI-IP SPE/ Tributary | TRIB_ENBL |
|---|---|---|---|---|
| 0x00F2 | 0x0072 | 3/18 | 3/18 | disabled |
| 0x00F3 | 0x0073 | 3/19 | 3/19 | disabled |
| 0x00F4 | 0x0074 | 3/20 | 3/20 | disabled |
| 0x00F5 | 0x0075 | 3/21 | 3/21 | disabled |

Table 39, Table 40, Table 41 contain data to configure the control RAM (E1 unstructured, INSBI clock master) for the first AAL1gator-32.

Writing to 0x0049 sets the EXSBI “use only phase field of EXT_LINKRATE”, the unstructured tributaries, and the tributary enabled bits. Writing to 0x0019 sets the INSBI as clock master, and the INSBI unstructured tributaries and tributary enabled bits. Writing to the Insert Tributary Control register enables the INSBI to take tributary data from an SBI tributary and transmit it to the local link mapped to that tributary.

**Table 39 AAL1gator-32 #1 Control RAM for SPE 1**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0021 | 0x0049/0x0019 | enabled 1 |
| 0x0022 | 0x0049/0x0019 | enabled |
| 0x0023 | 0x0049/0x0019 | enabled |
| 0x0024 | 0x0049/0x0019 | enabled |
| 0x0025 | 0x0049/0x0019 | enabled |
| 0x0026 | 0x0049/0x0019 | enabled |
| 0x0027 | 0x0049/0x0019 | enabled |
| 0x0028 | 0x0049/0x0019 | enabled 8 |
| 0x0029 | 0x0049/0x0019 | enabled |
| 0x002A | 0x0049/0x0019 | enabled |
| 0x002B | 0x0049/0x0019 | enabled |
| 0x002C | 0x0049/0x0019 | enabled |
| 0x002D | 0x0049/0x0019 | enabled |
| 0x002E | 0x0049/0x0019 | enabled |
| 0x002F | 0x0049/0x0019 | enabled |
| 0x0030 | 0x0049/0x0019 | enabled 16 |
| 0x0031 | 0x0048/0x0018 | disabled |
| 0x0032 | 0x0048/0x0018 | disabled |
| 0x0033 | 0x0048/0x0018 | disabled |
| 0x0034 | 0x0048/0x0018 | disabled |
| 0x0035 | 0x0048/0x0018 | disabled 21 |

**Table 40 AAL1gator-32 #1 Control RAM for SPE 2**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0041 | 0x0049/0x0019 | enabled 1 |
| 0x0042 | 0x0049/0x0019 | enabled |
| 0x0043 | 0x0049/0x0019 | enabled |
| 0x0044 | 0x0049/0x0019 | enabled |
| 0x0045 | 0x0049/0x0019 | enabled |
| 0x0046 | 0x0049/0x0019 | enabled |
| 0x0047 | 0x0049/0x0019 | enabled |
| 0x0048 | 0x0049/0x0019 | enabled 8 |
| 0x0049 | 0x0049/0x0019 | enabled |
| 0x004A | 0x0049/0x0019 | enabled |
| 0x004B | 0x0049/0x0019 | enabled |
| 0x004C | 0x0049/0x0019 | enabled |
| 0x004D | 0x0049/0x0019 | enabled |
| 0x004E | 0x0049/0x0019 | enabled |
| 0x004F | 0x0049/0x0019 | enabled |
| 0x0050 | 0x0049/0x0019 | enabled 16 |
| 0x0051 | 0x0048/0x0018 | disabled |
| 0x0052 | 0x0048/0x0018 | disabled |
| 0x0053 | 0x0048/0x0018 | disabled |
| 0x0054 | 0x0048/0x0018 | disabled |
| 0x0055 | 0x0048/0x0018 | disabled 21 |

**Table 41 AAL1gator-32 #1 Control RAM for SPE 3**

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x0061 | 0x0048/0x0018 | disabled 1 |
| 0x0062 | 0x0048/0x0018 | disabled |
| 0x0063 | 0x0048/0x0018 | disabled |
| 0x0064 | 0x0048/0x0018 | disabled |
| 0x0065 | 0x0048/0x0018 | disabled |
| 0x0066 | 0x0048/0x0018 | disabled |
| 0x0067 | 0x0048/0x0018 | disabled |
| 0x0068 | 0x0048/0x0018 | disabled 8 |
| 0x0069 | 0x0048/0x0018 | disabled |
| 0x006A | 0x0048/0x0018 | disabled |

| Indirect Address Registers EXSBI (0x80403) and INSBI (0x80503) | Extract Tributary Control RAM (0x80406) and Insert Tributary Control RAM (0x80506) Indirect Access Data Registers | TRIB_ENBL |
|---|---|---|
| 0x006B | 0x0048/0x0018 | disabled |
| 0x006C | 0x0048/0x0018 | disabled |
| 0x006D | 0x0048/0x0018 | disabled |
| 0x006E | 0x0048/0x0018 | disabled |
| 0x006F | 0x0048/0x0018 | disabled |
| 0x0070 | 0x0048/0x0018 | disabled 16 |
| 0x0071 | 0x0048/0x0018 | disabled |
| 0x0072 | 0x0048/0x0018 | disabled |
| 0x0073 | 0x0048/0x0018 | disabled |
| 0x0074 | 0x0048/0x0018 | disabled |
| 0x0075 | 0x0048/0x0018 | disabled 21 |

# 7 AAL1gator-32 Queue Tables

After performing SBI configuration, you may wish to define the receive and transmit queue tables for the AAL1gator-32 A1SP. This section contains information for configuring queue tables for:

- Unstructured lines
- T1 SDF-FR lines
- T1 SDF-MF lines
- E1 SDF-FR lines
- E1 SDF-MF lines
- E1 single-DS0-with-no-pointer queues

## 7.1 Unstructured Lines

When configuring AAL1gator-32 queue tables for unstructured lines, make sure your transmit and receive queue tables (T_QUEUE_TBL and R_QUEUE_TBL) match the tables shown in the code below.

```
A32 t_queue_tbl(0) for udf-ml (t1, e1, or j2)
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; set tx_enabled
02008:  0000 1000 0000 0178 8178 0000 FFFF FFFF ; set vci(8:0)=x100
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable

A32 r_queue_tbl(0) for udf-ml (t1, e1, or j2)
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ; set r_cdvt=4, mxbuf=18
0A008:  0000 0000 0000 0000 0000 0000 FFFF FFFF ;
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ;
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
```

Note: To enable T1 unstructured lines for this configuration, the FR_STRUCT bit must be set to "10" in the LIN_STR_MODE memory register.

### 7.1.1 Debugging information

Use the information below to debug your queue tables.

- The T1 udf-ml cell rate is (1.544M/47*8)=4106.383 cells/sec. The time between cells: 47*8=376 T1 bits *(1/1.544 µs /bit)= 244 µs.
- The E1 udf-ml cell rate is (2.048M/47*8)=5446.809 cells/sec. The time between cells: 47*8=376 E1 bits *(1/2.048 µs/bit)= 184 µs.
- The J2/DS2 udf-ml cell rate is (6.312M/47*8)=16787.23 cells/sec. The time between cells: 47*8=376 j2/ds2 bits *(1/6.312 µs/bit)= 60 µs.
    - T1: 1 ppm = 1.544 Hz, 50 ppm=77.2 Hz.

- E1: 1 ppm = 2.048 Hz, 50 ppm=102.4 Hz.

## 7.2 T1 SDF-FR Lines, 24 Channels Allocated

When configuring AAL1gator-32 queue tables for T1 SDF-FR lines, make sure your transmit and receive queue tables match the tables shown in the code below.

```
A32 t_queue_tbl(0) for sdf-fr (t1) all channels alloc'ed
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; f/cell=3, b/cell=47
02008:  0000 1000 0000 0177 6177 0000 FFFF 00FF ; num_chan=24
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable

A32 r_queue_tbl(0) for sdf-fr (t1) all channels alloc'ed
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ; set r_cdvt=4, mxbuf=18
0A008:  0000 0017 1700 0000 0000 0000 FFFF 00FF ; tot_size=24-1=23=0x17
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ; last_chan=23
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
; each arriving cell carries at most 1.96 t1 frames
```

Note: To enable SDF-FR and T1 for this configuration, the FR_STRUCT bit must be set to “01” and the T1_MODE bit must be set to “1” in the LIN_STR_MODE memory register.

## 7.3 T1 SDF-MF Lines, 24 Channels Allocated

When configuring AAL1gator-32 queue tables for T1 SDF-MF lines, make sure your transmit and receive queue tables match the tables shown in the code below.

```
A32 t_queue_tbl(0) for sdf-mf (t1) all channels alloc'ed
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; f/cell=3, b/cell=47
02008:  0000 1000 0000 0177 6177 0000 FFFF 00FF ; num_chan=24
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable

A32 r_queue_tbl(0) for sdf-mf (t1) all channels alloc'ed
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ; set r_cdvt=4, mxbuf=18
0A008:  0000 024B 170B 0000 0000 0000 FFFF 00FF ;
tot_size=588-1=587=0x24B
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ;
last_chan=23, r_dat_last=xB
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
; each arriving cell carries at most 1.96 t1 frames
```

Note: To enable SDF-MF and T1 for this configuration, the FR_STRUCT bit must be set to “11” and the T1_MODE bit must be set to “1” in the LIN_STR_MODE memory register.

## 7.4 E1 SDF-FR Lines, 31 Channels Allocated

When configuring AAL1gator-32 queue tables for E1 SDF-FR lines, make sure your transmit and receive queue tables match the tables shown in the code below.

```
A32 t_queue_tbl(0) for sdf-fr (e1) 31 channels alloc'ed
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; f/cell=3, b/cell=47
02008:  0000 1000 0000 0177 7D77 0000 FFFE FFFF ; num_chan=31
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable

A32 r_queue_tbl(0) for sdf-fr (e1) 31 channels alloc'ed
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ; set r_cdvt=4, mxbuf=18
0A008:  0000 001E 1F00 0000 0000 0000 FFFE FFFF ; tot_size=31-1=30=0x1E
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ; last_chan=x1F
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
; each arriving cell carries at most 1.516 e1 frames
```

Note: To enable SDF-FR and T1 for this configuration, the FR_STRUCT bit must be set “01” and the T1_MODE bit must be set to “0“ in the LIN_STR_MODE memory register.

## 7.5 E1 SDF-MF Lines, 30 Channels Allocated

When configuring AAL1gator-32 queue tables for E1 SDF-MF lines, make sure your transmit and receive queue tables match the tables shown in the code below.

```
A32 t_queue_tbl(0) for sdf-mf (e1) 30 channels alloc'ed
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; f/cell=3, b/cell=47
02008:  0000 1000 0000 0177 7977 0000 FFFE FFFE ; num_chan=30
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable.

A32 r_queue_tbl(0) for sdf-mf (e1) 30 channels alloc'ed
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ; set r_cdvt=4, mxbuf=18
0A008:  0000 01EE 1F0E 0000 0000 0000 FFFE FFFE ;
tot_size=495-1=494=0x1EE
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ;
last_chan=31, r_dat_last=15-1=xE
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
; each arriving cell carries at most 1.567 e1 frames
```

Note: To enable SDF-MF and E1 for this configuration, the FR_STRUCT bit must be set to “11” and the T1_MODE bit must be set to “0” in the LIN_STR_MODE memory register.

## 7.6 E1 Single DS0 with No Pointer Queues

When configuring AAL1gator-32 queue tables for E1 Single DS0, make sure your transmit and receive queue tables match the tables shown in the code below.

```
A32 t_queue_tbl(0) for sdf-fr (t1) single ds0 no/ptr, chan#5

02000:  FFFF 0000 0000 0000 0000 0000 786F 000C;
02008:  0000 1000 0000 0178 0578 0000 0000 0020;

02010:  0000 0000 0000 0000 0000 0000 0000 0000;

f/cell=1mf+24frames, set t_chan_unstruct

que_cr=avg_sub_valu=47x8(dec)=x178(hex)


A32 r_queue_tbl(0) for sdf-fr (t1) single ds0 no/ptr, chan#5

0A000:  0000 5E05 0000 9000 8038 0000 0000 0000;

0A008:  0000 0000 0500 0000 0000 0000 0000 0020; r_chan_unstruct

0A010:  0000 0000 0000 0000 0000 0000 0000 0000;

0A018:  0000 0000 0000 0000 0000 0000 0000 0000;

47 bytes/cell, r_cdvt=5, maxbuf=56(dec)

; (each arriving cell brings 47 frames, so r_max_buf s/b >= (r_cdvt +
fr/cell)=5+47=52=x34)
```

Note: to enable SDF-FR for this configuration, the FR_STRUCT bit must be set to “01” in the LIN_STR_MODE memory register.

# 8 SBI Synchronous Tributary Configurations

The following procedures show how to configure SBI synchronous tributaries. Synchronous tributaries are required for transporting channel associated signaling (CAS) across the SBI bus. T1 or E1 timing is not transported across the SBI bus for these synchronous tributaries and the T1 or E1 tributary rate will be the SBI nominal T1 or E1 rate. For T1 this rate is [193 T1 bits/(270*9) SREFCLK cycles] * SREFCLK frequency, which is 1.544 Mbit/s, if SREFCLK is 19.44 MHz. All T1s or E1s that are configured as SBI synchronous tributaries will have the same SBI nominal T1 or E1 timing.

If any one of the 32 links is configured as synchronous, then the depth check enable bits (DC_EN and DC_INT_EN) in the Extract and Insert Control registers (0x84000/0x85000) must first be cleared. This is required because the Depth Check logic does not support synchronous tributaries.

If any SBI tributary is configured as synchronous, then the C1FP pulses must *not* be 500 µs apart (2 KHz rate) but rather 6 ms apart (once every 48 SBI frames). This C1FP rate is configured in the TEMUX by setting the MFSC1FP bit in the SBI Master Configuration register (0x1701) for whichever TEMUX, if any, is configured to source the SC1FP signal (SC1FPMSTR).

For SBI synchronous tributaries, it is irrelevant whether the EXSBI or its corresponding INSBI controls rate justifications across the SBI bus. That is, it is irrelevant which side is clock master, because rate justifications do not occur. For SBI synchronous tributaries, the serial-in to parallel-out (SIPO) block uses a T1 or E1 clock passed to it from the INSBI. The INSBI derives this T1 or E1 clock from the 19.44 MHz REFCLK. The EXSBI has no concept of a synchronous tributary and just follows the V5 octet, which does not move. This ensures that the parallel-in to serial-out (PISO) synthesized clock is locked to the SIPO clock on the INSBI side, regardless of which PISO clock synthesis method is used (phase field, clock field, or data arrival rate).

## 8.1 TEMUX SBI Initialization

Use the following procedure to initialize the TEMUX SBI for synchronous tributaries. The procedure is based on the following assumptions:

- SPE 1 on Add and Drop busses
- TEMUX is SC1FP master (SC1FPMSTR)

To initialize the TEMUX SBI:

1. Toggle the SBI reset bit in the SBI Master Reset/Bus Signal Monitor register (0x1700) to get a clean start.

2. Set the INSBI and EXSBI Control registers (0x1710 and 0x1720) to 0x41 to enable the DC_RSTEN and SBI_PAR_CTL bits:

```
0x1710 = x041
0x1720 = x041
```

3. Set the SBI Master Configuration register (0x1701) to 0x45 to enable the SC1FPMSTR bit and set SDROPSEL[1:0] and SADDSEL[1:0] bits to SPE 1.

4. Set the SBI Master Configuration register (0x1702) to 0x00 to disable the BUSMASTER bit.

5. Configure the tributaries first for the non-synchronous, framed without CAS mode:

```
insbi spe=1 trib control RAM's=0x05 ; frmd w/o cas
exsbi spe=1 trib control RAM's=0x45 ; clk_slv frmd w/o cas,Phase
```

6. Set the SBI Master Configuration register (0x1701) to 0x65 to set the MFSC1FP bit for SBI CAS alignment.

7. Reconfigure the INSBI bus tributaries by setting the SYNCH_TRIB bits:

```
insbi spe=1 trib control RAM's=0x25 ; set SYNCH_TRIB
```

8. Set the SYNCSBI bits in the T1 or E1 Receive Options register (x002+x80*N):

```
0x002+x80*N = 0x08 ; set SYNCSBI=1
```

9. Reconfigure the tributaries for the framed with CAS mode. Note: This will also reset the tributaries.

```
insbi spe=1 trib control RAM's=0x21 ; trib_typ=framed w/cas
exsbi spe=1 trib control RAM's=0x41 ; trib_typ=framed w/cas
```

10. Rewrite register SBI Master Configuration register (0x1701) to 0x65. Note: This function may reset all of the tributaries.

## 8.2 AAL1gator-32 Initialization

Use the following procedure to initialize the AAL1gator-32 SBI for synchronous tributaries. The procedure is based on the following assumptions:

- SPE 1 on Add and Drop busses.
- Default 1:1 SBI mapping, so only the lowest 16 T1s on SPE 1 will work.

Note: The first seven steps are the basic configuration.

To initialize the AAL1gator-32:

1. Decrease the INSBI T1 maximum threshold from xE to xA to avoid overflow:

```
al3w 0x81 0x80509 0x006a
```

2. Set the LINK_TYPL and LINK_TYPH bits to T1:

```
al3w 0x81 0x80301 0x0000
```

3. Clear all the LINK_DIS bits:

```
al3w 0x81 0x80302 0x0000
```

```
al3w 0x81 0x80303 0x0000
```

4. Set all the SYNC_LINK bits:

```
al3w 0x81 0x80304 0xffff
al3w 0x81 0x80305 0xffff
```

5. Clear all the SBI insert alarms:

```
al3w 0x81 0x8030c 0x0000
al3w 0x81 0x8030d 0x0000
```

6. Clear the depth check enable bits (DC_EN) in the EXSBI and INSBI Control registers:

```
al3w 0x81 0x80400 0x0000
al3w 0x81 0x80500 0x0000
```

7. Write the INSBI and EXSBI tributary control RAMs:

```
insbi = clk_mster, synch_trib, struc w/cas
insbi spe=1 trib:1-16 control RAM's=0x31
insbi spe=1 trib:17-28 control RAM's=0x00; trib disabled
exsbi = clk_slave, phase, struc w/cas
exsbi spe=1 trib:1-16 control RAM's=0x41
exsbi spe=1 trib:17-28 control RAM's=0x00; trib disabled
```

8. Enable SPE 1 and SPE 2 for T1:

```
0x80300=0x00c0
```

9. Set the LIN_STR_MODE bits for all A1SPs:

```
LIN_STR_MODE = 0x2073 ; for all sdf-mf lines
LIN_STR_MODE = 0x2071 ; for all sdf-fr lines
```

10. Set the AN_CMDREG_ATTN bits for all A1SPs:

```
al3w 0x81 0x80010 0x8
al3w 0x81 0x80011 0x8
al3w 0x81 0x80012 0x8
al3w 0x81 0x80013 0x8
```

# 9 Changing a Tributary from Unstructured to Structured

Use the following procedure to change an unstructured tributary to a structured tributary.

1. Set the EXSBI and INSBI control RAMs for 21 enabled tributaries:

```
x0005; enable struc w/o cas trib, clock slave
x0015; enable struc w/o cas trib, clock master
```

2. Set the LIN_STR_MODE bit: Tx clk=synthesized (E1 nominal) by AAL1gator-32, SDF-FR. Repeat for all 21 lines:

```
x0.0000 = x0021 ; line 0
```

3. Load the 21 transmit queue tables (T_QUEUE_TBL). Note: Do not set the internal cell loopback if you are using Revision A of the AAL1gator-32 as the loopback FIFO will overflow when many queues are enabled.

```
A32 t_queue_tbl(0) for sdf-fr (e1)
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; set tx_enabled
02000:  0000 1000 0000 0177 8177 0000 FFFF FFFF ; set vci(8:0)=x100
02000:  FFFF FFFF 0000 0000 0000 0000 0000 0000 ;
don't set loopback_enable in rev A, if more than four queues are
sending cells
```

4. Load the 21 receive queue tables (R_QUEUE_TBL):

```
A32 r_queue_tbl(0) for sdf-fr (e1)
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ;
set r_cdvt=4, mxbuf=18
0A000:  0000 001F 1F00 0000 0000 0000 FFFF FFFF ;
rtotsize=31,lastchan=31.
0A000:  0000 0000 0000 0000 0000 0000 0000 0000 ;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000 ;
r_cdvt=4, maxbuf=18, r_tot_size=31, lastchan=31
```

# 10 Unchannelized DS3 over SBI

Use the following data to configure an unchannelized DS3 signal over the SBI bus.

## 10.1 TEMUX Configuration

To configure the TEMUX devices that have been setup for unchannelized DS3 over SBI, use the script below.

```
wr tm1 0x0001 0x0b ; DS3 framer-only, SBI system-i/f
wr tm1 0x1001 0x06 ; Egress Clock Master, Bypass DS3 Tran
wr 0x1002 0x14 ; TXMFPI=RXMFPO=1 (required, even for SBI)

# reset the sbi logic
wr 0x1700 0x00 ; Read: verify  C1FP and SBI Add bus signal activity.
wr 0x1700 0x01 ;
wr 0x1700 0x00 ;

wr 0x1701 0x45 ; SPE=1, C1FP Master
wr 0x1702 0x01 ; BUSMASTER=1 - TEMUX always drives SBI bus
# exsbi(this is an indirect write – use the proper procedure)
wr 0x1716 0x19 ; Clock Master, Unframed Trib, Trib Enabled
wr 0x1713 0x21 ; Address: Trib 1:1
wr 0x1714 0x00 ; Write
# insbi(this is an indirect write – use the proper procedure)
wr tm1 0x1726 0x09 ; Unframed Trib, Trib Enabled
wr tm1 0x1723 0x21 ; Address: Trib 1:1
wr tm1 0x1724 0x00 ; Write
```

## 10.2 AAL1gator-32 Configuration

To configure the AAL1gator-32 devices that have been setup for unchannelized DS3 over SBI, use the script below.

```
wr 0x80000 0x30 ; clear sw_reset
wr 0x80100 0x01 ; set ZBT SSRAM (if using ZBT SSRAM)
; note: the following two writes are indirect: use the proper procedure
iwr 0x81 insbi spe=1 trib=1 0x19; clk_mstr, unstructured trib, enabled
iwr 0x81 exsbi spe=1 trib=1 0x19; clk_mstr, unstructured trib, enabled
wr 0x00001 0x04 ; set UDF_HS
; note: the following write is a block write to 0x0010-0x0017
```

```
blockwr 0x00010 0x2011; write lin_str_mode0 through lin_str_mode7
wr 0x00010 0x200a ; t1_mode, clk_source_tx=000, clk_source_rx=1

# sbi
wr 0x80300 0x42 ; Enable SPE 1 for DS3
wr 0x80301 0x02 ; Link Type Low=DS3
wr 0x80302 0xfffe ; disable all except link 0
wr 0x80303 0xffff ; disable all
```

Hardware Note: (ground RL_CLK1-7 inputs)

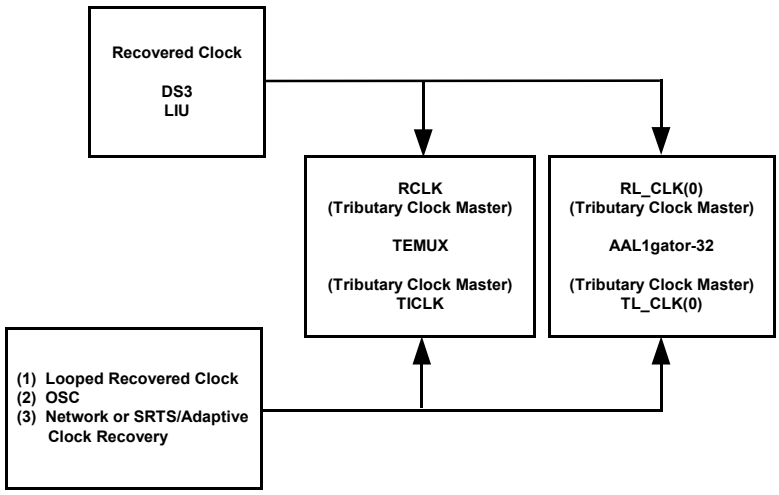
Load the T_QUEUE_TBLs and R_QUEUE_TBLs:

```
A32 t_queue_tbl(0) for udf-hs
02000:  FFFF 0000 0000 0000 0000 0000 4000 0000 ; set tx_enabled
02000:  0000 1000 0000 0000 0000 0000 0000 0000 ; set vci(8:0)=x100
02000:  0000 0000 4000 0000 0000 0000 0000 0000
; set loopback_enable, if desired

A32 r_queue_tbl(0) for udf-hs
0A000:  0000 5E0C 0000 0000 0012 0000 0000 0000;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000
;set r_cdvt=12, mxbuf=18

wr 0x80010 0x28 ; set cmd_reg attn
* Note: read cmdreg_attn here, to verify that it cleared
wr 0x80010 0x0 ; clear a1sp sw_reset
wr 0x80020 0x0 ; start VC
*Note: Should read add-queue-FIFO empty bit here, to verify that queue
was added*
```

## 10.3 DS3 Clock Setup

Figure 8 illustrates the clocking required for transporting DS3 signals between the TEMUX and AAL1gator-32 across the SBI bus.

**Figure 8 DS3 Clock Setup**




In the receive direction, the 44.736 MHz clock recovered by the DS3 line interface unit (LIU) should be routed directly to both the TEMUX RCLK input pin and the AAL1gator-32 RL_CLK(0) input pin. Then, the TEMUX INSBI will be the SBI tributary clock master. (This is a default setting—no configuration is required.) The AAL1gator-32 EXSBI should also be configured to be the SBI tributary clock master. Both INSBI and EXSBI can be clock masters in this configuration as they both use the same clock, so rate justifications across the SBI bus are unnecessary and can be ignored by the AAL1gator-32 EXSBI.

In the transmit direction, the nominal 44.736 MHz clock source can be derived using one or more of the following methods:

- Looped DS3 LIU recovered clock
- Local on-board 44.736 MHz oscillator
- Network-locked on-board 44.736 MHz oscillator
- AAL1 SRTS clock recovery (external FPGA/DAC/VCx0)
- AAL1 Adaptive clock recovery (external FPGA/DAC/VCx0)

The clock generated by one or more of these methods should be routed directly to both the AAL1gator-32 TL_CLK(0) input pin and the TEMUX TICLK input pin. Again, both the AAL1gator-32 INSBI and the TEMUX EXSBI should be configured as the SBI tributary clock master. Again, in the transmit direction, any rate justifications issued across the SBI bus by the AAL1gator-32 can be ignored by the TEMUX as both sides are running at the same rate.

## 10.4 DS3 Debugging information

Use the following debugging information to debug any DS3 CES connection.

- DS3 udf-hs cell rate is (44.736 M/47*8)=118.9787 k cells/sec. Time between cells: 47*8=376 DS3 bits *(1/44.736 µs/bit)= 8.4 µs
- E3 udf-hs cell rate is (34.368 M/47*8)=91.40426 cells/sec. Time between cells: 47*8=376 E3 bits *(1/34.368 µs/bit)= 11 µs
- DS3: 1 ppm = 44.736 Hz, 20 ppm=894.72 Hz

# 11 Generic SBI Debugging Procedure

Below is the procedure for generic SBI debugging. Before starting the procedure, download the TEMAP/AAL1gator-32 errata documents and note the possible erroneous SBI INSBI/EXSBI FIFO underrun/overrun indications based on a microprocessor interface bug described there.

This procedure is based on the following assumption: TEMAP is sourcing the SC1FP signal to all devices on the SBI bus.

To debug the SBI:

1. Configure your TEMUX/AAL1gator-32 SBI register to look like the example detailed below. Make sure you correctly read the four indirect RAMs present in the TEMUX INSBI and EXSBI control RAMs and the AAL1gator-32 INSBI and EXSBI control RAM registers:

```
TEMUX:
x1700: 7C 45 00 -- -- -- -- -- ; SPE 1, c1fp master, busmaster=0
x1708: -- -- -- -- -- -- -- -- ;
x1710: 41 VV 40 21 3E -- 29 VV ;
t1 trib#1 unframed, clk slave, VV=various
x1718: -- -- -- -- -- -- VV 40 ;
x1720: 41 40 40 21 22 -- 09 -- ; t1 trib#1 unframed
x1728: -- -- -- -- -- -- -- -- ;
x1730: -- 40 40 -- -- -- -- -- ;


A32 general:
x80300: C0 00 00 00 00 00 00 00 ; SPE 1 enabled (and SPE 2), t1 trib
x80308: 00 00 00 00 00 00 00 00 ;
A32 exsbi:
x80400: 40 95 40 21 22 51 49 43 ;
unstruc trib, clk slave, clk_mode=phase
x80408: 77 FE 2D 2D 4C 4C 95 00 ;
A32 insbi:
x80500: 40 40 40 21 22 51 19 77 ;
unstruc trib, clk master (see clk_source_tx!)
x80508: DC 6E 2E 86 A6 EF E5 B4 ;
x80510: -- 40 40 -- -- -- -- -- ;
```

2. Choose an AAL1gator-32 clock mode appropriate to your test setup. For example, one reasonable setup is to put the tester in looped/recovered clock mode and let the AAL1gator-32 integral T1 clock synthesizer be the single clock source in the loop. This requires that the AAL1gator-32 SYSCLK is 38.88 MHz:

```
A32 LIN_STR_MODE_0: x00010 = x2022;
clk_source_rx=0, clk_source_tx=0-5, udf-ml
```

3. Make sure you are using the following AAL1gator-32 control tables for unstructured T1s. This facilitates an internal ATM cell loopback from AAL1gator-32 EXSBI to AAL1gator-32 INSBI:

```
A32 t_queue_tbl(0) for udf-ml (t1, e1, or j2)
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; set tx_enabled
02008:  0000 1000 0000 0178 8178 0000 FFFF FFFF ; set vci(8:0)=x100
02010:  0000 0000 4000 0000 0000 0000 0000 0000 ;
set loopback_enable


A32 r_queue_tbl(0) for udf-ml (t1, e1, or j2)
0A000:  0000 5E04 0000 9000 0012 0000 0000 0000 ;
set r_cdvt=4, mxbuf=18
0A008:  0000 0000 0000 0000 0000 0000 FFFF FFFF ;
0A010:  0000 0000 0000 0000 0000 0000 0000 0000 ;
0A018:  0000 0000 0000 0000 0000 0000 0000 0000 ;
```

4. Start cell generation by writing the Add Queue FIFO.

5. Read the AAL1gator-32 transmit data buffer (T_DATA_BUFFER) to verify that your pattern has made it from the tester to the buffer by reading AAL1gator-32 0x04000 to 0x047FF. Verify that you see your pattern.

6. Read the AAL1gator-32 register 0x02007 (T_CELL_CNT) several times. Verify that you see the transmit cell count incrementing.

7. Read the AAL1gator-32 0x0A007 (R_CELL_CNT) several times. Verify that you see the receive cell count incrementing.

8. Clear the sticky bits at AAL1gator-32 0x0A008. Read them back a few times and verify that they are correct (=x4000).

9. Read the AAL1gator-32 receive data buffer (R_DATA_BUFFER) to verify that your pattern has made it from the tester to the buffer by reading AAL1gator-32 0x10000 to 0x11FFF. Verify that you see your pattern.

10. After you have verified the specified data in steps 1 through 9, then repeat the procedure to get the lowest 16 AAL1gator-32 lines working.

11. After the lowest 16 lines are working, repeat steps 1 through 10, but use the following mapping programming to get all 28 T1s from the tester looping.

# 12 AAL1gator-32 Complete Initialization Sequence

Use the following procedure to initialize the AAL1gator-32.

## 12.1 21 x E1 / SBI SPE 1 Setup Start

This initialization setup sequence is based on the following assumptions:

- 21 unstructured E1 lines
- SBI SPE 1 is only used
- AAL1gator-32 is the clock source via its 21 internal E1 clock synthesizers (Test Equipment should be loop-timed)
- AAL1gator-32 internal cell loopback
- AAL1gator-32 using pipelined single-cycle deselect SSRAM
- AAL1gator-32 mapping as shown in Section 6.3

### 12.1.1 Global Setup

To set up the SBI bus for SPE 1:

1. Verify that the SYSCLK DLL has locked:

```
x8.4003 = (read until bit 0 = 1)
```

2. Clear the global software reset (SW_RESET):

```
x8.0000 = x0000
```

3. Choose the Pipelined Single-Cycle Deselect SSRAM:

```
x8.0100 = x0000 ; odd parity
```

### 12.1.2 AAL1gator-32 SBI Setup

Use the setup sequence described in Section 5.

### 12.1.3 AAL1gator-32 A1SP Setup

Use the following setup sequence to initialize the AAL1gator-32 A1SPs. This setup assumes that 21 unstructured E1 signals are mapped to the A1SP links 0 to 20.

1. Set the LIN_STR_MODE: Tx clk=synthesized (E1 nominal) by AAL1gator-32:

```
--a1sp0--------
0x0.0000 = 0x0022 ; line 0
0x0.0001 = 0x0022 ; line 1
0x0.0002 = 0x0022 ; line 2
```

```
0x0.0003 = 0x0022 ; line 3
0x0.0004 = 0x0022 ; line 4
0x0.0005 = 0x0022 ; line 5
0x0.0006 = 0x0022 ; line 6
0x0.0007 = 0x0022 ; line 7
--a1sp1--------
0x2.0000 = 0x0022 ; line 8
0x2.0001 = 0x0022 ; line 9
0x2.0002 = 0x0022 ; line 10
0x2.0003 = 0x0022 ; line 11
0x2.0004 = 0x0022 ; line 12
0x2.0005 = 0x0022 ; line 13
0x2.0006 = 0x0022 ; line 14
0x2.0007 = 0x0022 ; line 15
--a1sp2--------
0x4.0000 = 0x0022 ; line 16
0x4.0001 = 0x0022 ; line 17
0x4.0002 = 0x0022 ; line 18
0x4.0003 = 0x0022 ; line 19
0x4.0004 = 0x0022 ; line 20
```

2. Load the transmit sequential numbering table (T_SEQNUM_TBL).

3. Load the 21 transmit queue tables (T_QUEUE_TBL) and set them for internal cell loopback.

4. Change each table's VCI(15:0) to route the cells to the proper receive queue table (r_queue_tbl). Refer to the VCI mapping table, Table 42.

```
A32 t_queue_tbl(0) for udf-ml (t1, e1, or j2)
02000:  FFFF 0000 0000 0000 0000 0000 432F 0000 ; set tx_enabled
02000:  0000 1000 0000 0178 8178 0000 FFFF FFFF ; set vci(8:0)=x100
02000:  0000 0000 4000 0000 0000 0000 0000 0000 ; set loopback_enable
```

Use the following addresses:

```
--a1sp0--------
0x0.2000 ; line 0
0x0.2400 ; line 1
0x0.2800 ; line 2
0x0.2C00 ; line 3
0x0.3000 ; line 4
0x0.3400 ; line 5
0x0.3800 ; line 6
```

```
0x0.3C00 ; line 7
--a1sp1--------
0x2.2000 ; line 8
0x2.2400 ; line 9
0x2.2800 ; line 10
0x2.2C00 ; line 11
0x2.3000 ; line 12
0x2.3400 ; line 13
0x2.3800 ; line 14
0x2.3C00 ; line 15
--a1sp2--------
0x4.2000 ; line 16
0x4.2400 ; line 17
0x4.2800 ; line 18
0x4.2C00 ; line 19
0x4.3000 ; line 20
```

**Table 42 VCI(15:0) Mapping Table**

| TEMUX Framer | TEMUX SBI | A32 SBI | A32 A1SP | A32 VCI |
|---|---|---|---|---|
| N=1 | trib=1 | trib=1 | line=0 | x0100 |
| N=2 | trib=2 | trib=2 | line=1 | x0120 |
| N=3 | trib=3 | trib=3 | line=2 | x0140 |
| N=4 | trib=4 | trib=4 | line=3 | x0160 |
| N=5 | trib=5 | trib=5 | line=4 | x0180 |
| N=6 | trib=6 | trib=6 | line=5 | x01A0 |
| N=7 | trib=7 | trib=7 | line=6 | x01C0 |
| N=8 | trib=8 | trib=8 | line=7 | x01E0 |
| N=9 | trib=9 | trib=9 | line=0/8 | x0300 |
| N=10 | trib=10 | trib=10 | line=1/9 | x0320 |
| N=11 | trib=11 | trib=11 | line=2/10 | x0340 |
| N=12 | trib=12 | trib=12 | line=3/11 | x0360 |
| N=13 | trib=13 | trib=13 | line=4/12 | x0380 |
| N=14 | trib=14 | trib=14 | line=5/13 | x03A0 |
| N=15 | trib=15 | trib=15 | line=6/14 | x03C0 |
| N=16 | trib=16 | trib=16 | line=7/15 | x03E0 |
| N=17 | trib=17 | Trib=17 | line=0/16 | x0500 |
| N=18 | trib=18 | Trib=18 | line=1/17 | x0520 |
| N=19 | trib=19 | Trib=19 | line=2/18 | x0540 |
| N=20 | trib=20 | Trib=20 | line=3/19 | x0560 |
| N=21 | trib=21 | Trib=21 | line=4/20 | x0580 |

5. Load the receive cyclic redundancy check syndrome (R_CRC_SYNDROME) table.

6. Load the 21 receive queue tables (R_QUEUE_TBL):

```
A32 r_queue_tbl(0) for udf-ml (t1, e1, or j2)
0A000:  0000 5E04 0000 8000 0012 0000 0000 0000 ;
set r_cdvt=4, mxbuf=18
0A000:  0000 0000 0000 0000 0000 0000 FFFF FFFF ;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000 ;
0A000:  0000 0000 0000 0000 0000 0000 0000 0000 ;
```

Use the following addresses:

```
--a1sp0--------
0x0.A000 ; line 0
0x0.A400 ; line 1
0x0.A800 ; line 2
0x0.AC00 ; line 3
0x0.B000 ; line 4
0x0.B400 ; line 5
0x0.B800 ; line 6
0x0.BC00 ; line 7
--a1sp1--------
0x2.A000 ; line 8
0x2.A400 ; line 9
0x2.A800 ; line 10
0x2.AC00 ; line 11
0x2.B000 ; line 12
0x2.B400 ; line 13
0x2.B800 ; line 14
0x2.BC00 ; line 15
--a1sp2--------
0x4.A000 ; line 16
0x4.A400 ; line 17
0x4.A800 ; line 18
0x4.AC00 ; line 19
0x4.B000 ; line 20
```

7. Load the 21 receive change to queue (R_CH_TO_QUEUE) tables:

```
-- a1sp 0 (lines 0-7)-------------
for line_offset=0 to x70, step x10:
  for chan_pair_addr_offset=0 to 15:
```

```
    x0.8200 + line_offset + chan_pair_addr_offset = x0000;
  end for;
end for;
-- a1sp 1 (lines 8-15)-------------
for line_offset=0 to x70, step x10:
  for chan_pair_addr_offset=0 to 15:
    x2.8200 + line_offset + chan_pair_addr_offset = x0000;
  end for;
end for;
-- a1sp 2 (lines 16-20)------------
for line_offset=0 to x40, step x10:
  for chan_pair_addr_offset=0 to 15:
    x4.8200 + line_offset + chan_pair_addr_offset = x0000;
  end for;
end for;
```

8. Set the CMD_REG_ATTN bit and then read to verify that it cleared:

```
0x8.0010 = 0x0028; a1sp0, leave sw_reset bit set
0x8.0011 = 0x0028; a1sp1, leave sw_reset bit set
0x8.0012 = 0x0028; a1sp2, leave sw_reset bit set
```

9. Enable the UTOPIA bus:

```
0x8.80120 = 0x0001 ; Set UTOP_EN bit
```

10. Clear the A1SP software resets (sw_resets):

```
0x8.0010 = 0x0000; a1sp0
0x8.0011 = 0x0000; a1sp1
0x8.0012 = 0x0000; a1sp2
```

11. Start the ATM virtual channels and start ATM cell generation:

```
--a1sp0--------
0x8.0020 = 0x0000 ; start queue 0 (from line 0)
0x8.0020 = 0x0020 ; start queue 32 (from line 1)
0x8.0020 = 0x0040 ; start queue 64 (from line 2)
0x8.0020 = 0x0060 ; start queue 96 (from line 3)
0x8.0020 = 0x0080 ; start queue 128 (from line 4)
0x8.0020 = 0x00A0 ; start queue 160 (from line 5)
0x8.0020 = 0x00C0 ; start queue 192 (from line 6)
0x8.0020 = 0x00E0 ; start queue 224 (from line 7)
```

```
--a1sp1--------
0x8.0021 = 0x0000 ; start queue 0 (from line 8)
0x8.0021 = 0x0020 ; start queue 32 (from line 9)
0x8.0021 = 0x0040 ; start queue 64 (from line 10)
0x8.0021 = 0x0060 ; start queue 96 (from line 11)
0x8.0021 = 0x0080 ; start queue 128 (from line 12)
0x8.0021 = 0x00A0 ; start queue 160 (from line 13)
0x8.0021 = 0x00C0 ; start queue 192 (from line 14)
0x8.0021 = 0x00E0 ; start queue 224 (from line 15)
--a1sp2--------
0x8.0022 = 0x0000 ; start queue 0 (from line 16)
0x8.0022 = 0x0020 ; start queue 32 (from line 17)
0x8.0022 = 0x0040 ; start queue 64 (from line 18)
0x8.0022 = 0x0060 ; start queue 96 (from line 19)
0x8.0022 = 0x0080 ; start queue 128 (from line 20)
```

# 13 Tributaries with Channel Associated Signaling (CAS)

To support T1 or E1s with CAS across the SBI bus, the SBI tributary must be configured as "synchronous". Refer to Section 8 for details on synchronous configurations.

# 14 Miscellaneous FAQ

This section contains miscellaneous FAQ, which you may find helpful for your configuration.

### Q1) What are the valid LINK_DIS and TRIB_ENBL settings, and what do these bits actually do?

A1) Setting LINK_DIS(x) to "1" grounds the clocks from the SIPO or PISO to the A1SP. Note: This setting can potentially decrease the power dissipation by a small amount. Setting TRIB_ENBL(y) to "0" prevents data from passing between the SBI bus and the A1SP internal links.

The valid settings are:

- For an enabled A1SP link x, set LINK_DIS(x)=0 and TRIB_ENBL(trib->x)=1
- For a disabled A1SP link y, set LINK_DIS(y)=1 and TRIB_ENBL(trib->y)=0
- For the unused 52 (52=84-32) SBI tributaries z, set TRIB_ENBL(trib->z)=0.

### Q2) What is the difference between the granularity and range of the three SBI bus clock reconstruction methods: data arrival rate, V4 octet clock field and the V4 octet phase field?

A2) The information below pertains to serial clock reconstruction methods in the AAL1gator-32 EXSBI/PISO. Note: This actually occurs in PISO, which contains the serial clock synthesizers.

The Data Arrival Rate Method (EXT CLK CNTL) is capable of signaling the serial clock to change by eight cycles (one octet) per 500 µs because the SBI tributary can transport one extra, or one less octet of tributary data per 500 µs SBI frame (by using the V3 octet to carry an extra data octet, or by stuffing the octet following the V3 octet with a dummy octet). This tells you both the granularity (eight clock cyles per 500 µs maximum) and the range of frequency change (eight clock cycles more or less, per 500 µs maximum).

The V4 Octet Clock Field Method is capable of signaling the serial clock to change by a maximum of two T1 clock cycles per 500 µs. This is because the AAL1gator-32 receives a V4 octet once per 500 µs and the V4 octet tells the serial clock synthesizer whether to use 771, 772, or 773 T1 clock cycles per 500 µs time-period. So the granularity increased (from eight T1 or E1 clock cycles to one or two T1 or E1 clock cycles), but the frequency range decreased.

The V4 Octet Phase Field Method is capable of signaling the serial clock to change by a maximum of one 19.44 MHz SREFCLK clock cycle per 500 µs. This ensures the granularity is at a maximum, but range of frequency (tolerance) is at a minimum.

### Q3) When should an SPE be enabled?

A3) Do not enable an SPE that does not have any tributaries enabled on it. The SPE should always be enabled last after its tributaries are enabled *and* after all SBI configuration is complete. An SPE should be disabled first before its tributaries are disabled.

### Q4) When does an AAL1gator-32 drive its AACTIVE output?

A4) An AAL1gator-32 drives its AACTIVE output only when the tributaries and their corresponding SPEs are enabled (TRIB_ENBL=1 and SPE_ENBL=1).

### Q5) How can I generate configuration resets for all tributaries within an SPE?

A5) Changing the SPE enabled bit (SPE_ENBL) generates configuration resets for all tributaries within the SPE.

### Q6) What is the difference between an SBI synchronous tributary and an SBI asynchronous tributary?

A6) An SBI synchronous tributary means that T1 or E1 timing is not passed through the SBI bus. It is assumed that the SBI nominal T1 rate is equal to the incoming nominal T1 rate. All T1s operating in synchronous mode across the SBI bus are restricted to have the same timing (the SBI nominal T1 rate). A typical application is a voice or DS0 cross-connect.

An SBI asynchronous tributary means that T1 or E1 timing *is* passed through the SBI bus. The incoming T1 rate can be different from the SBI nominal T1 rate. All T1s operating in an asynchronous (floating) mode across the SBI bus can have independent timing. A typical application is multiple independent private line services such as ATM circuit emulation service (CES) or inverse multiplexer for ATM (IMA) service.

### Q7) For an SBI synchronous tributary, what is the nominal T1 rate?

A7) The nominal T1 rate depends on the frequency of SREFCLK:

193 T1 bits/(270 columns * 9 rows=2430 SREFCLK cycles)* 19.44 M SREFCLK cycles/sec = 1.544 Mbit/s.

If SREFCLK is +50 ppm, the T1 nominal rate becomes 1.544077.2 Mbit/s or 1.544 Mbit/s +50 ppm.

### Q8) How do I fix a data corruption problem caused by a misconfigured TEMUX RJAT?

A8) Data corruption can be avoided by enabling synchronization (SYNC=1) in the TEMUX RJAT block.

# List of Acronyms and Terms

AACTIVE: Nomenclature for “add bus enabled”

AAL1gator-32: PMC-Sierra’s mnemonic for the PM73122 32 Link CES/DBCES ATM AAL1 SA containing four SAR processors

ADD: Direction where data is placed onto the SBI bus

A1SP: ATM Adaptation Layer Type 1 (AAL1) Segmentation and Reassembly (SAR) Processor

API: Application programming interface

DROP: The direction where data is being extracted from the SBI bus

CAS: Channel associated signaling

C1FP: An externally generated signal that indicates the first C1 octet on the SBI bus and multiframe alignment

DS3: Digital signal, level 3, 45 Mbit/s

E1: 2.048 Mbit/s, 30 user channels

EXSBI: Extract SBI block

FIFO: First in, first out

IMA: Inverse multiplexing over ATM

INSBI: Insert SBI block

LINK: A link that has been multiplexed on the SBI bus

LIU: Line interface unit

PISO: Parallel-in-to-serial-out converter

RECEIVE: Direction from the external line interface to the local links

SAR: Segmentation and reassembly

SBI: Scaleable Bandwidth Interconnect — PMC-Sierra’s mnemonic for a high-density 8-bit parallel bus used to connect synchronous and asynchronous link layer devices

SBI-IP: SBI internal parallel bus

| | |
|---|---|
| SC1FP: | SBI C1 frame pulse |
| SDF-FR: | Structured data format, frame-based |
| SDF-MF: | Structured data format, multiframe-based |
| SIPO: | Serial-in-to-parallel-out converter |
| SPE: | Synchronous payload envelope |
| TEMAP: | PMC-Sierra's mnemonic for the PM5365 — a high density VT/TU Mapper and M13 Multiplexer |
| TEMUX: | PMC-Sierra's mnemonic for the PM8315 High Density T1 or E1 Framer with Integrated VT/TU Mapper and M13 Multiplexer |
| T1: | 1.544 Mbit/s, 24 user channels |
| TRANSMIT: | Direction from the local links to the external line interface |
| TRIBUTARY: | Individual data stream within the SBI interface |
| VCI: | Virtual channel identifier |

# Notes