# SGS-THOMSON MICROELECTRONICS

## M28F256

## 256K (32K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 90ns
- LOW POWER CONSUMPTION
  - Standby Current: 100μA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10μs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
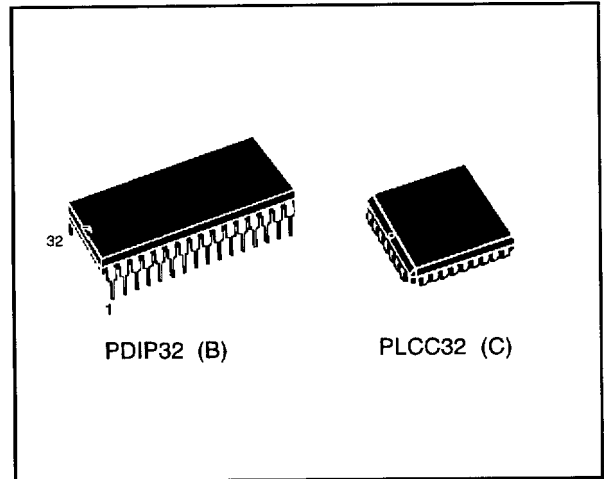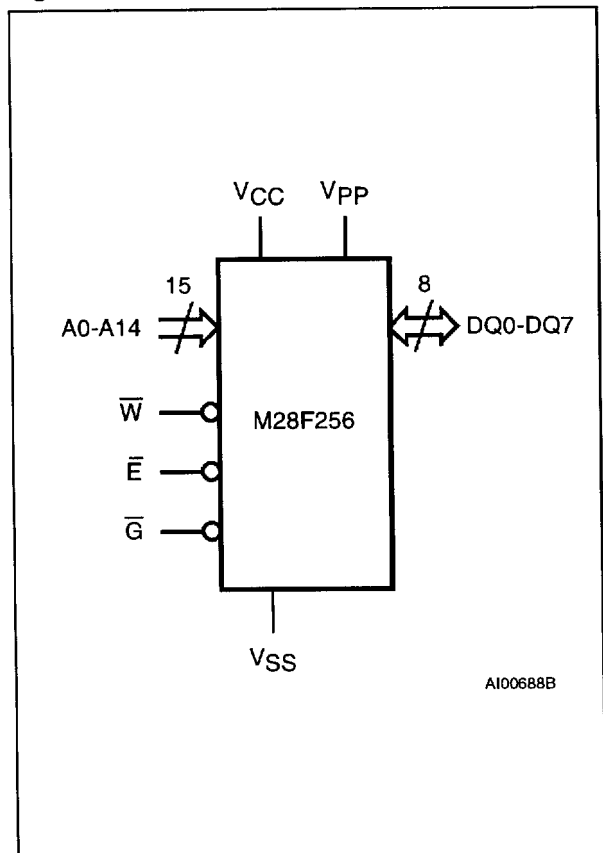- INTEGRATED ERASE/PROGRAM STOP TIMER
- EXTENDED TEMPERATURE RANGES



PDIP32 (B)          PLCC32 (C)

## DESCRIPTION

The M28F256 FLASH Memory Is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface The M28F256 FLASH Memory is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

**Figure 1. Logic Diagram**



AI00688B

## Table 1. Signal Names

| A0 - A14 | Address Inputs |
|---|---|
| DQ0 - DQ7 | Data Inputs / Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{PP}$ | Program Supply |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

## Figure 2A. DIP Pin Connections



```
        VPP  [ 1      ᴗ    32 ]  VCC
         NC  [ 2            31 ]  W̄
         NC  [ 3            30 ]  NC
        A12  [ 4            29 ]  A14
         A7  [ 5            28 ]  A13
         A6  [ 6            27 ]  A8
         A5  [ 7            26 ]  A9
         A4  [ 8   M28F256  25 ]  A11
         A3  [ 9            24 ]  Ḡ
         A2  [ 10           23 ]  A10
         A1  [ 11           22 ]  Ē
         A0  [ 12           21 ]  DQ7
        DQ0  [ 13           20 ]  DQ6
        DQ1  [ 14           19 ]  DQ5
        DQ2  [ 15           18 ]  DQ4
        VSS  [ 16           17 ]  DQ3
```
AI00689
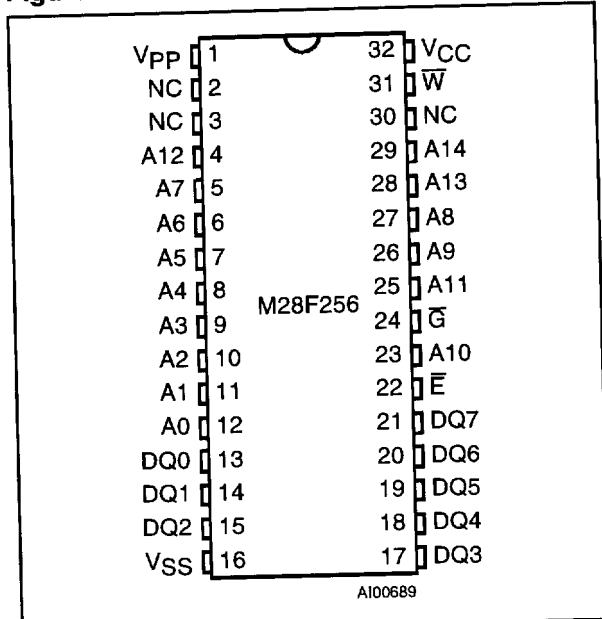
**Warning:** NC = Not Connected

## Figure 2B. LCC Pin Connections



AI00690
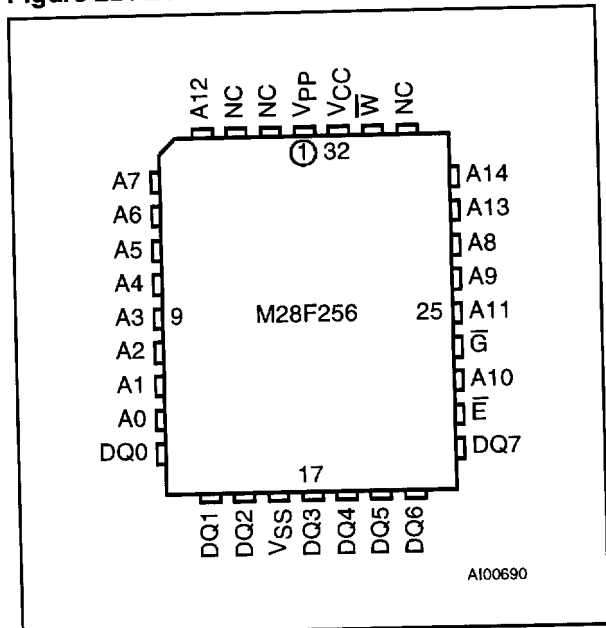
**Warning:** NC = Not Connected

## Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $T_A$ | Ambient Operating Temperature | –40 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ | Input or Output Voltages | –0.6 to 7 | V |
| $V_{CC}$ | Supply Voltage | –0.6 to 7 | V |
| $V_{A9}$ | A9 Voltage | –0.6 to 13.5 | V |
| $V_{PP}$ | Program Supply Voltage, during Erase or Programming | –0.6 to 14 | V |

**Note:** Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

## DEVICE OPERATION

The M28F256 FLASH Memory employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the VPP, program voltage, input. When VPP is less than or equal to 6.5V, the command register is disabled and M28F256 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When VPP is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

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**Table 3. Operations** [1]

| | V$_{PP}$ | Operation | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | A9 | DQ0 - DQ7 |
|---|---|---|---|---|---|---|---|
| Read Only | V$_{PPL}$ | Read | V$_{IL}$ | V$_{IL}$ | V$_{IH}$ | A9 | Data Output |
| | | Output Disable | V$_{IL}$ | V$_{IH}$ | V$_{IH}$ | X | Hi-Z |
| | | Standby | V$_{IH}$ | X | X | X | Hi-Z |
| | | Electronic Signature | V$_{IL}$ | V$_{IL}$ | V$_{IH}$ | V$_{ID}$ | Codes |
| Read/Write [2] | V$_{PPH}$ | Read | V$_{IL}$ | V$_{IL}$ | V$_{IH}$ | A9 | Data Output |
| | | Write | V$_{IL}$ | V$_{IH}$ | V$_{IL}$ Pulse | A9 | Data Input |
| | | Output Disable | V$_{IL}$ | V$_{IH}$ | V$_{IH}$ | X | Hi-Z |
| | | Standby | V$_{IH}$ | X | X | X | Hi-Z |

**Notes:** 1  X = V$_{IL}$ or V$_{IH}$
2  Refer also to the Command Table

**Table 4. Electronic Signature**

| Identifier | A0 | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | V$_{IL}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | V$_{IH}$ | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0A8h |

## READ ONLY MODES, V$_{PP}$ ≤ 6.5V

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

**Read Mode.** The M28F256 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

**Standby Mode.** In the Standby Mode the maximum supply current is reduced to 100μA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

**Output Disable Mode.** When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

**Electronic Signature Mode.** This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

## READ/WRITE MODES, 11.4V ≤ V$_{PP}$ ≤ 12.6V

When V$_{PP}$ is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2

**Table 5. Commands** [(1)]

| Command | Cycles | 1st Cycle | | | 2nd Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Operation | A0-A14 | DQ0-DQ7 | Operation | A0-A14 | DQ0-DQ7 |
| Read | 1 | Write | X | 00h | | | |
| Electronic Signature | 2 | Write | X | 90h | Read | 0000h | 20h |
| | | | | | Read | 0001h | 0A8h |
| Setup Erase/ Erase | 2 | Write | X | 20h | | | |
| | | | | | Write | X | 20h |
| Erase Verify | 2 | Write | A0-A14 | 0A0h | Read | X | Data Output |
| Setup Program/ Program | 2 | Write | X | 40h | | | |
| | | | | | Write | A0-A14 | Data Input |
| Program Verify | 2 | Write | X | 0C0h | Read | X | Data Output |
| Reset | 2 | Write | X | 0FFh | Write | X | 0FFh |

**Note:** 1  X = $V_{IL}$ or $V_{IH}$

## READ/WRITE MODES (cont'd)

cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage $V_{CC}$ and the program voltage $V_{PP}$ can be applied in any order. When the device is powered up or when $V_{PP}$ is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may choose to provide a constant high $V_{PP}$ and use the register commands for all operations, or to switch the $V_{PP}$ from low to high only when needing to erase or program the memory. All command register access is inhibited when $V_{CC}$ falls below the Erase/Write Lockout Voltage ($V_{LKO}$) at 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

**Read Mode.** The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

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## AC MEASUREMENT CONDITIONS

| | |
|---|---|
| Input Rise and Fall Times | $\leq$ 10ns |
| Input Pulse Voltages | 0.45V to 2.4V |
| Input and Output Timing Ref. Voltages | 0.8V to 2V |

Note that Output Hi-Z is defined as the point where data is no longer driven.
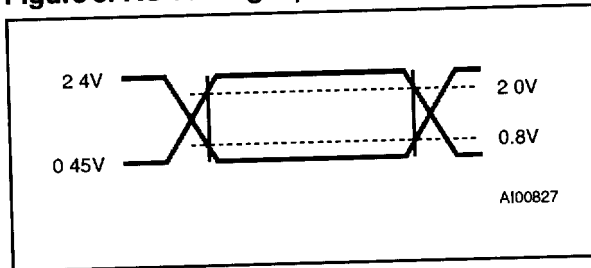
### Figure 3. AC Testing Input Output Waveforms
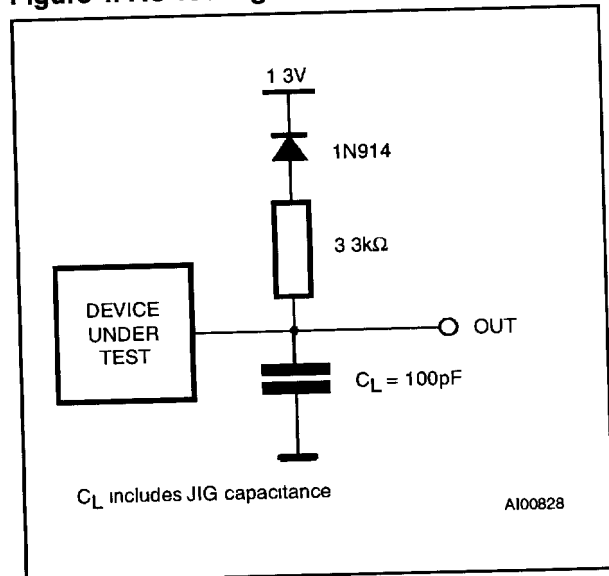


### Figure 4. AC Testing Load Circuit



$C_L$ includes JIG capacitance

### Table 6. Capacitance[1] ($T_A = 25\ °C$, f = 1 MHz )

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | | 12 | pF |

Note: 1. Sampled only, not 100% tested

**Electronic Signature Mode.** In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

**Erase and Erase Verify Modes.** The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle Erase is

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied; reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

## Table 7. DC Characteristics
$(T_A = 0$ to $70\ °C$, $-40$ to $85\ °C$ or $-40$ to $125\ °C$; $V_{CC} = 5V \pm 5\%$ or $5V \pm 10\%)$

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | | $\pm 1$ | µA |
| $I_{LO}$ | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | $\pm 10$ | µA |
| $I_{CC}$ | Supply Current (Read) | $\overline{E} = V_{IL}$, $f = 6MHz$ | | 30 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | 1 | mA |
| | Supply Current (Standby) CMOS | $\overline{E} = V_{CC} \pm 0.2V$ | | 100 | µA |
| $I_{CC2}$ [1] | Supply Current (Programming) | During Programming | | 10 | mA |
| $I_{CC3}$ [1] | Supply Current (Program Verify) | During Verify | | 10 | mA |
| $I_{CC4}$ [1] | Supply Current (Erase) | During Erasure | | 10 | mA |
| $I_{CC5}$ [1] | Supply Current (Erase Verify) | During Erase Verify | | 10 | mA |
| $I_{LPP}$ | Program Leakage Current | $V_{PP} \leq V_{CC}$ | | $\pm 10$ | µA |
| $I_{PP}$ | Program Current (Read or Standby) | $V_{PP} > V_{CC}$ | | 200 | µA |
| | | $V_{PP} \leq V_{CC}$ | | $\pm 10$ | µA |
| $I_{PP1}$ [1] | Program Current (Programming) | $V_{PP} = V_{PPH}$, During Programming | | 10 | mA |
| $I_{PP2}$ [1] | Program Current (Program Verify) | $V_{PP} = V_{PPH}$, During Verify | | 10 | mA |
| $I_{PP3}$ [1] | Program Current (Erase) | $V_{PP} = V_{PPH}$, During Erase | | 5 | mA |
| $I_{PP4}$ [1] | Program Current (Erase Verify) | $V_{PP} = V_{PPH}$, During Erase Verify | | 5 | mA |
| $V_{IL}$ | Input Low Voltage | | $-0.5$ | 0.8 | V |
| $V_{IH}$ | Input High Voltage TTL | | 2 | $V_{CC} + 0.5$ | V |
| | Input High Voltage CMOS | | $0.7\ V_{CC}$ | $V_{CC} + 0.5$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 5.8mA$ (grade 1) | | 0.45 | V |
| | | $I_{OL} = 2.1mA$ (grade 6) | | 0.45 | V |
| $V_{OH}$ | Output High Voltage CMOS | $I_{OH} = -100µA$ | 4.1 | | V |
| | | $I_{OH} = -1mA$ | $V_{CC} - 0.8$ | | V |
| | | $I_{OH} = -2.5mA$ (grade 1) | $V_{CC} - 0.8$ | | V |
| | Output High Voltage TTL | $I_{OH} = -2.5mA$ | 2.4 | | V |
| $V_{PPL}$ | Program Voltage (Read Operations) | | 0 | 6.5 | V |
| $V_{PPH}$ | Program Voltage (Read/Write Operations) | | 11 4 | 12.6 | V |
| $V_{ID}$ | A9 Voltage (Electronic Signature) | | 11 5 | 13 | V |
| $I_{ID}$ [1] | A9 Current (Electronic Signature) | $A9 = V_{ID}$ | | 200 | µA |
| $V_{LKO}$ | Supply Voltage, Erase/Program Lock-out | | 2 5 | | V |

Note: 1 Not 100% Tested Characterisation Data available

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## Table 8A. Read Only Mode AC Characteristics
($T_A$ = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; 0V ≤ $V_{PP}$ ≤ 6.5V)

| Symbol | Alt | Parameter | Test Condition | M28F256 -90 | | -10 | | -12 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 90 | | 100 | | 120 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | | 90 | | 100 | | 120 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | Chip Enable Low to Output Transition | $\overline{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G} = V_{IL}$ | | 90 | | 100 | | 120 | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable Low to Output Transition | $\overline{E} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E} = V_{IL}$ | | 35 | | 40 | | 50 | ns |
| $t_{EHQZ}$ [1] | | Chip Enable High to Output Hi-Z | $\overline{G} = V_{IL}$ | 0 | 20 | 0 | 30 | 0 | 40 | ns |
| $t_{GHQZ}$ [1] | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E} = V_{IL}$ | 0 | 20 | 0 | 30 | 0 | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

Note: 1 Sampled only, not 100% tested

## Table 8B. Read Only Mode AC Characteristics
(($T_A$ = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; 0V ≤ $V_{PP}$ ≤ 6.5V)

| Symbol | Alt | Parameter | Test Condition | M28F256 -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 150 | | 200 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | | 150 | | 200 | ns |
| $t_{ELQX}$ | $t_{LZ}$ | Chip Enable Low to Output Transition | $\overline{G} = V_{IL}$ | 0 | | 0 | | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G} = V_{IL}$ | | 150 | | 200 | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable Low to Output Transition | $\overline{E} = V_{IL}$ | 0 | | 0 | | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E} = V_{IL}$ | | 55 | | 60 | ns |
| $t_{EHQZ}$ [1] | | Chip Enable High to Output Hi-Z | $\overline{G} = V_{IL}$ | 0 | 55 | 0 | 60 | ns |
| $t_{GHQZ}$ [1] | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E} = V_{IL}$ | 0 | 35 | 0 | 40 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 0 | | 0 | | ns |

Note: 1 Sampled only, not 100% tested

**Figure 5. Read Mode AC Waveforms**



AI00682
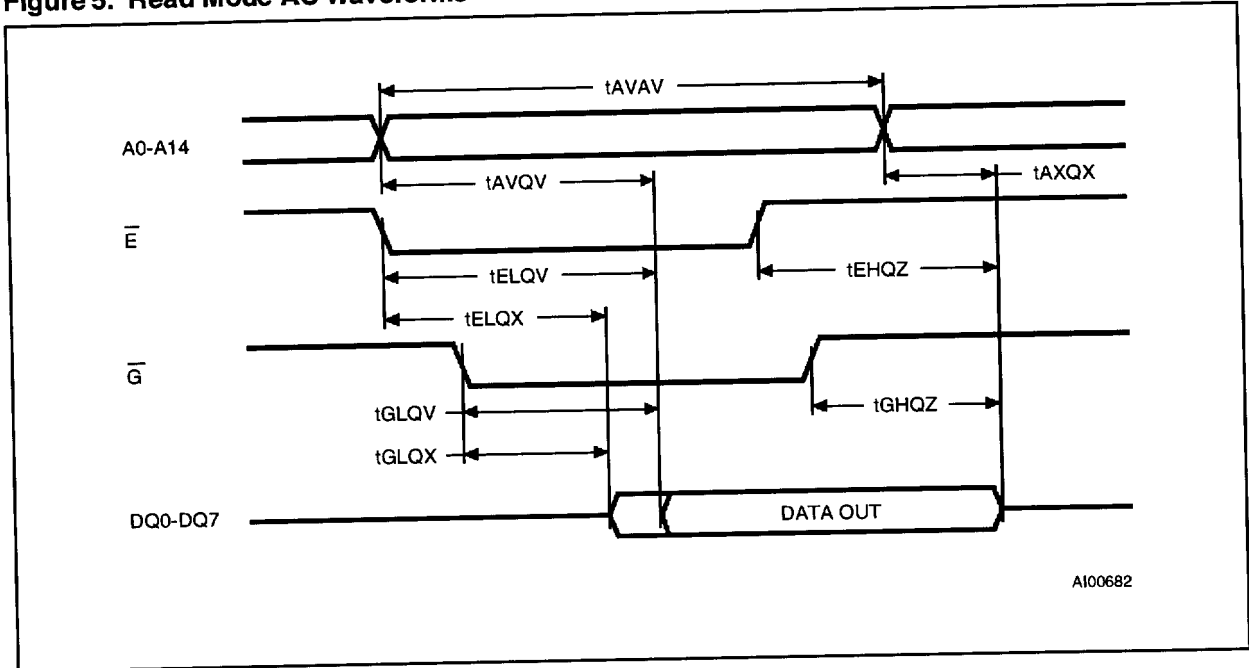
**Figure 6. Read Command Waveforms**



AI00683

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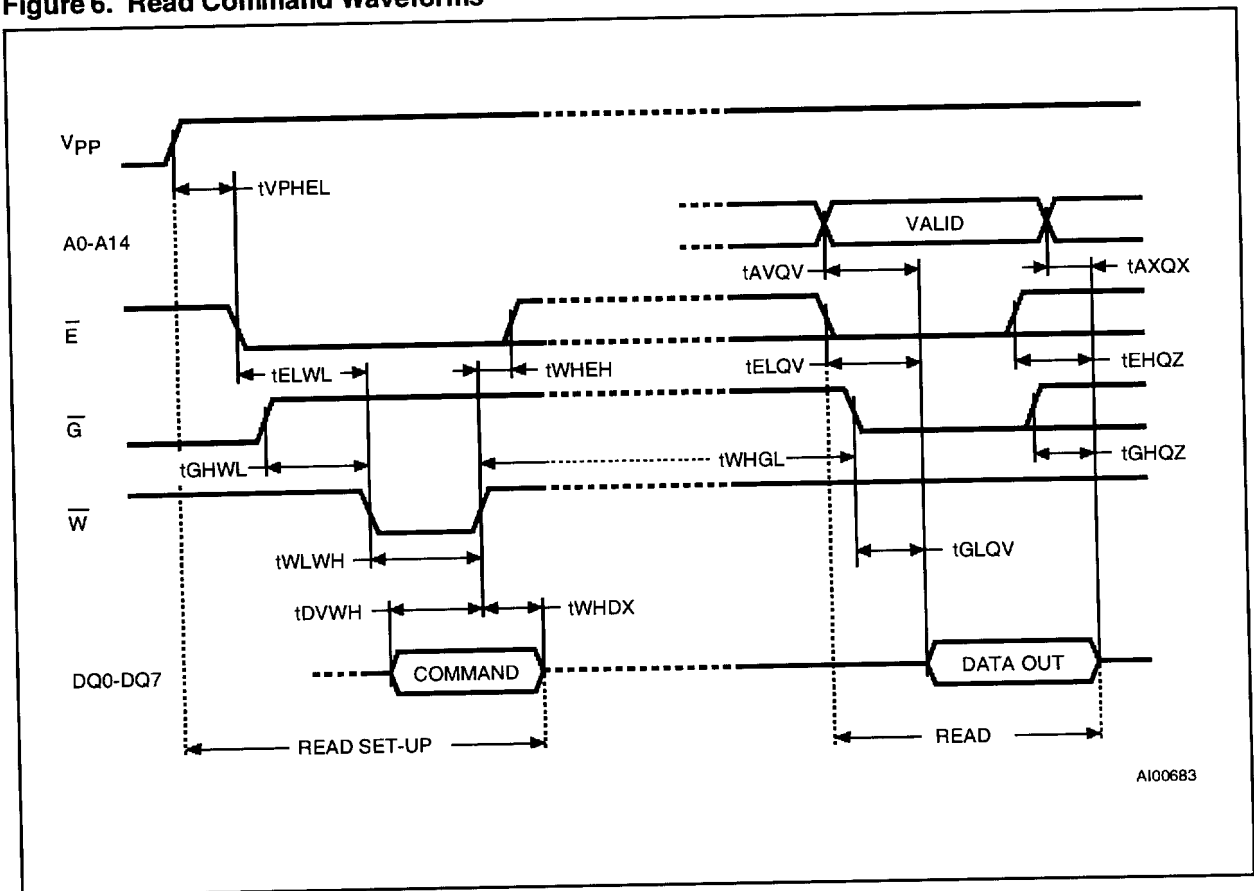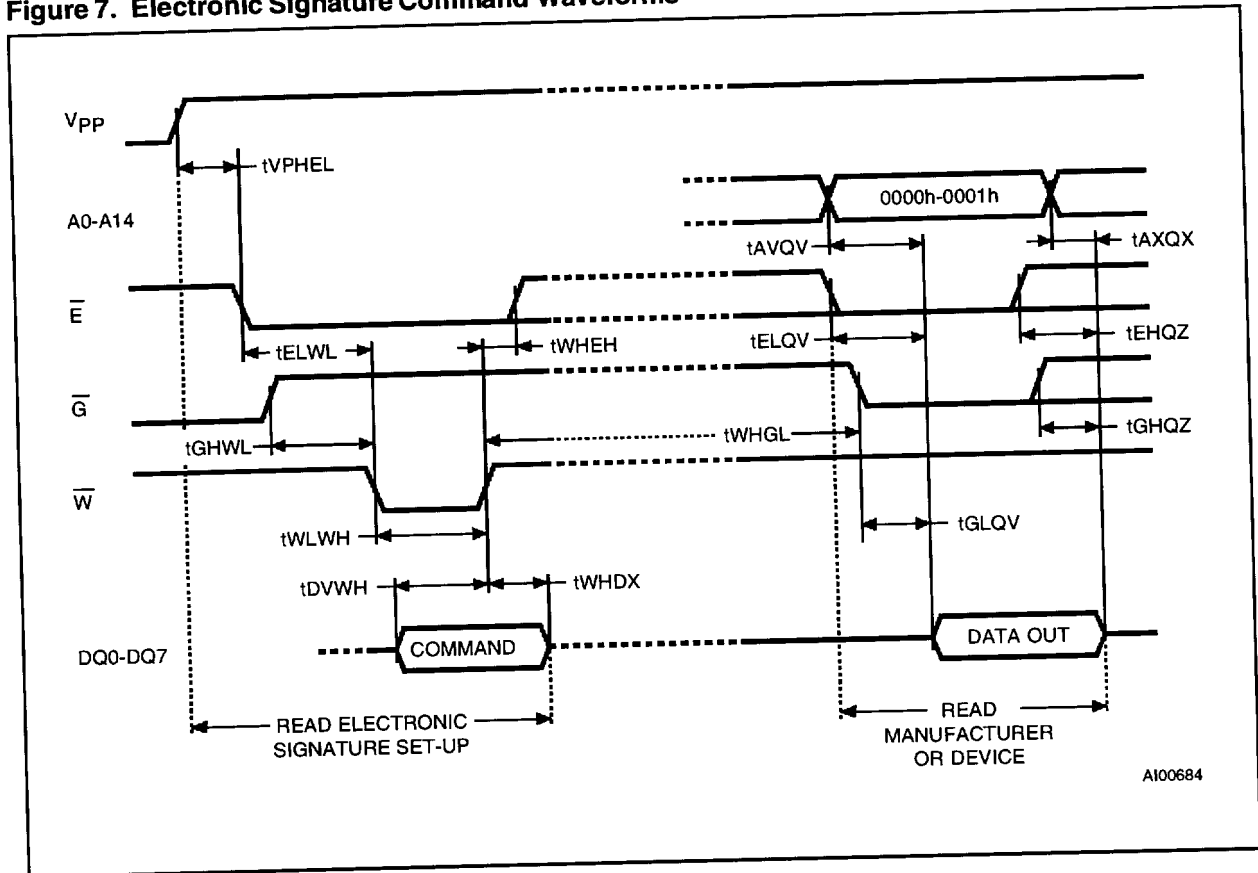
**Figure 7. Electronic Signature Command Waveforms**



**Program and Program Verify Modes.** The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the

Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

**Reset Mode.** This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing 0FFh two times to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

## Table 9A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled

($T_A$ = 0 to 70 °C, −40 to 85 °C or −40 to 125 °C; $V_{CC}$ = 5V ± 5% or 5V ± 10%; $V_{PP}$ = 12V)

| Symbol | Alt | Parameter | M28F256 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -90 | | -10 | | -12 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{VPHEL}$ | | Vpp High to Chip Enable Low | 100 | | 100 | | 100 | | ns |
| $t_{VPHWL}$ | | Vpp High to Write Enable Low | 100 | | 100 | | 100 | | ns |
| $t_{WHWH3}$ | $t_{WC}$ | Write Cycle Time | 90 | | 100 | | 120 | | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Valid to Write Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{AVEL}$ | | Address Valid to Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Write Enable Low to Address Transition | 45 | | 50 | | 60 | | ns |
| $t_{ELAX}$ | | Chip Enable Low to Address Transition | 50 | | 60 | | 80 | | ns |
| $t_{ELWL}$ | $t_{CS}$ | Chip Enable Low to Write Enable Low | 15 | | 15 | | 20 | | ns |
| $t_{WLEL}$ | | Write Enable Low to Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{GHWL}$ | | Output Enable High to Write Enable Low | 0 | | 0 | | 0 | | µs |
| $t_{GHEL}$ | | Output Enable High to Chip Enable Low | 0 | | 0 | | 0 | | µs |
| $t_{DVWH}$ | $t_{DS}$ | Input Valid to Write Enable High | 45 | | 50 | | 50 | | ns |
| $t_{DVEH}$ | | Input Valid to Chip Enable High | 35 | | 40 | | 50 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Enable Low to Write Enable High (Write Pulse) | 45 | | 50 | | 60 | | ns |
| $t_{ELEH}$ | | Chip Enable Low to Chip Enable High (Write Pulse) | 45 | | 45 | | 70 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Write Enable High to Input Transition | 10 | | 10 | | 10 | | ns |
| $t_{EHDX}$ | | Chip Enable High to Input Transition | 10 | | 10 | | 10 | | ns |
| $t_{WHWH1}$ | | Duration of Program Operation | 9.5 | | 9.5 | | 9.5 | | µs |
| $t_{EHEH1}$ | | Duration of Program Operation | 9.5 | | 9.5 | | 9.5 | | µs |
| $t_{WHWH2}$ | | Duration of Erase Operation | 9.5 | | 9.5 | | 9.5 | | ms |
| $t_{WHEH}$ | $t_{CH}$ | Write Enable High to Chip Enable High | 0 | | 0 | | 0 | | ns |
| $t_{EHWH}$ | | Chip Enable High to Write Enable High | 0 | | 0 | | 0 | | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Enable High to Write Enable Low | 20 | | 20 | | 20 | | ns |
| $t_{EHEL}$ | | Chip Enable High to Chip Enable Low | 20 | | 20 | | 20 | | ns |
| $t_{WHGL}$ | | Write Enable High to Output Enable Low | 6 | | 6 | | 6 | | µs |
| $t_{EHGL}$ | | Chip Enable High to Output Enable Low | 6 | | 6 | | 6 | | µs |
| $t_{AVQV}$ | $t_{ACC}$ | Addess Valid to data Output | | 90 | | 100 | | 120 | ns |
| $t_{ELQX}$ [1] | $t_{LZ}$ | Chip Enable Low to Output Transition | 0 | | 0 | | 0 | | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | | 90 | | 100 | | 120 | ns |
| $t_{GLQX}$ [1] | $t_{OLZ}$ | Output Enable Low to Output Transition | 0 | | 0 | | 0 | | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | 35 | | 45 | | 50 | ns |
| $t_{EHQZ}$ [1] | | Chip Enable High to Output Hi-Z | | 20 | | 30 | | 50 | ns |
| $t_{GHQZ}$ [1] | $t_{DF}$ | Output Enable High to Output Hi-Z | | 20 | | 30 | | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | 0 | | 0 | | 0 | | ns |

Notes: 1. Sampled only, not 100% tested
2 A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform

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## Table 9B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled

(T$_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V$_{CC}$ = 5V ± 5% or 5V ± 10%; V$_{PP}$ = 12V)

| Symbol | Alt | Parameter | M28F256 -15 Min | -15 Max | -20 Min | -20 Max | Unit |
|---|---|---|---|---|---|---|---|
| tVPHEL | | Vpp High to Chip Enable Low | 100 | | 100 | | ns |
| tVPHWL | | Vpp High to Write Enable Low | 100 | | 100 | | ns |
| tWHWH3 | twc | Write Cycle Time | 150 | | 200 | | ns |
| tAVWL | tAS | Address Valid to Write Enable Low | 0 | | 0 | | ns |
| tAVEL | | Address Valid to Chip Enable Low | 0 | | 0 | | ns |
| tWLAX | tAH | Write Enable Low to Address Transition | 60 | | 60 | | ns |
| tELAX | | Chip Enable Low to Address Transition | 80 | | 80 | | ns |
| tELWL | tCS | Chip Enable Low to Write Enable Low | 20 | | 20 | | ns |
| tWLEL | | Write Enable Low to Chip Enable Low | 0 | | 0 | | ns |
| tGHWL | | Output Enable High to Write Enable Low | 0 | | 0 | | µs |
| tGHEL | | Output Enable High to Chip Enable Low | 0 | | 0 | | µs |
| tDVWH | tDS | Input Valid to Write Enable High | 50 | | 50 | | ns |
| tDVEH | | Input Valid to Chip Enable High | 50 | | 50 | | ns |
| tWLWH | tWP | Write Enable Low to Write Enable High (Write Pulse) | 60 | | 60 | | ns |
| tELEH | | Chip Enable Low to Chip Enable High (Write Pulse) | 70 | | 70 | | ns |
| tWHDX | tDH | Write Enable High to Input Transition | 10 | | 10 | | ns |
| tEHDX | | Chip Enable High to Input Transition | 10 | | 10 | | ns |
| tWHWH1 | | Duration of Program Operation | 9.5 | | 9.5 | | µs |
| tEHEH1 | | Duration of Program Operation | 9.5 | | 9.5 | | µs |
| tWHWH2 | | Duration of Erase Operation | 9.5 | | 9.5 | | ms |
| tWHEH | tCH | Write Enable High to Chip Enable High | 0 | | 0 | | ns |
| tEHWH | | Chip Enable High to Write Enable High | 0 | | 0 | | ns |
| tWHWL | tWPH | Write Enable High to Write Enable Low | 20 | | 20 | | ns |
| tEHEL | | Chip Enable High to Chip Enable Low | 20 | | 20 | | ns |
| tWHGL | | Write Enable High to Output Enable Low | 6 | | 6 | | µs |
| tEHGL | | Chip Enable High to Output Enable Low | 6 | | 6 | | µs |
| tAVQV | tACC | Address Valid to data Output | | 150 | | 200 | ns |
| tELQX (1) | tLZ | Chip Enable Low to Output Transition | 0 | | 0 | | ns |
| tELQV | tCE | Chip Enable Low to Output Valid | | 150 | | 200 | ns |
| tGLQX (1) | toLZ | Output Enable Low to Output Transition | 0 | | 0 | | ns |
| tGLQV | toE | Output Enable Low to Output Valid | | 55 | | 60 | ns |
| tEHQZ (1) | | Chip Enable High to Output Hi-Z | | 55 | | 60 | ns |
| tGHQZ (1) | tDF | Output Enable High to Output Hi-Z | | 35 | | 40 | ns |
| tAXQX | toH | Address Transition to Output Transition | 0 | | 0 | | ns |

**Notes:** 1 Sampled only, not 100% tested
2 A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform

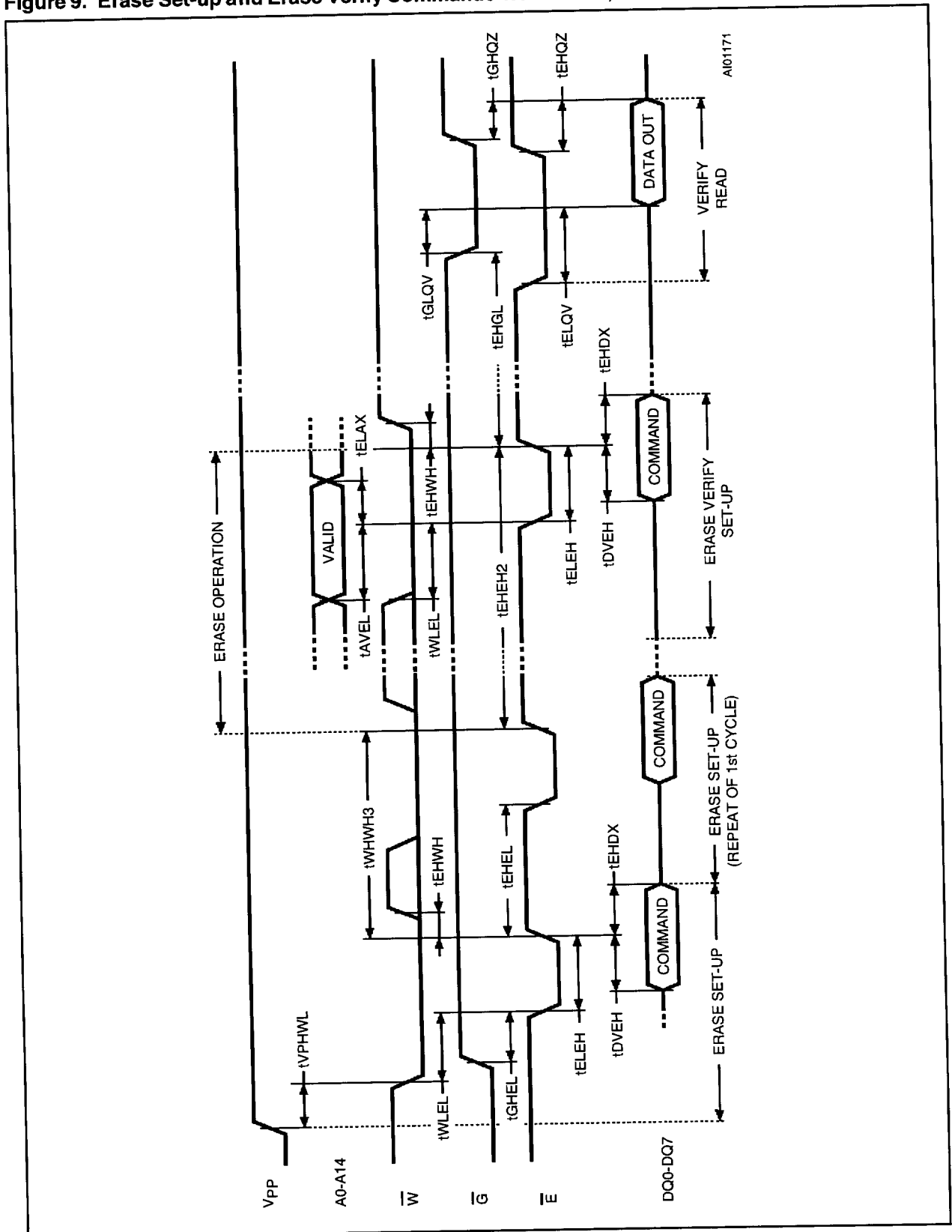**Figure 8. Erase Set-up and Erase Verify Commands Waveforms, W̄ Controlled**

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**Figure 9. Erase Set-up and Erase Verify Commands Waveforms, E Controlled**

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**Figure 10.  Program Set-up and Program Verify Commands Waveforms, $\overline{W}$ Controlled**



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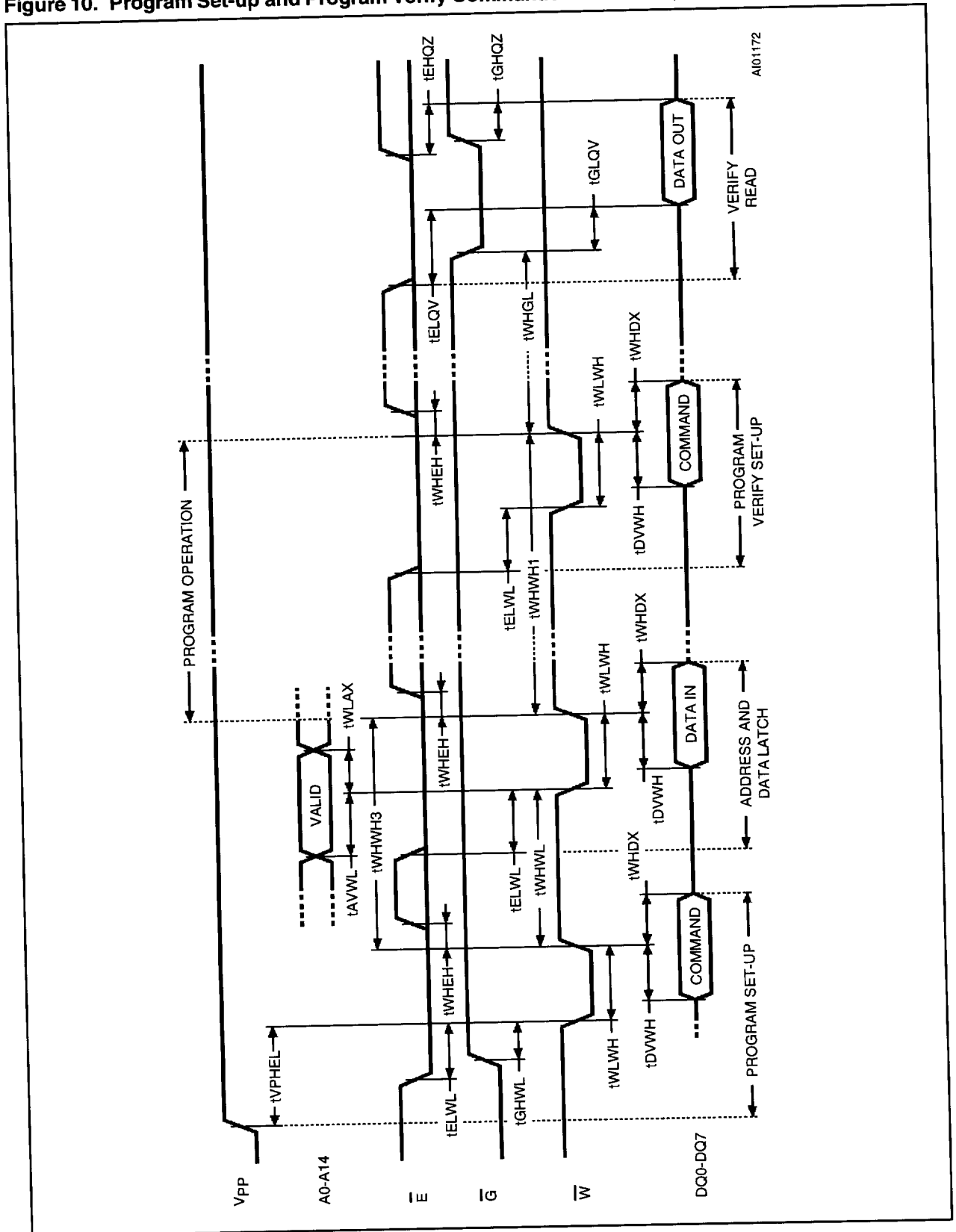
## Figure 12. Erasing Flowchart



Vpp = 12V

PROGRAM ALL
BYTES TO 00h

n=0, Addr=0000h

ERASE SET-UP

Wait 10ms

ERASE VERIFY
Latch Addr

NO

YES ++n
LIMIT

Vpp < 6.5V
FAIL

Wait 6μs

READ DATA OUTPUT

NO Data
OK

Addr++

YES

Last NO
Addr

YES

READ COMMAND

Vpp < 6 5V, PASS

AI00687

## Figure 13. Programming Flowchart



Vpp = 12V

n = 0

PROGRAM SET-UP
Latch Addr, Data

Wait 10μs

NO

YES ++n
= 25

PROGRAM VERIFY

Wait 6μs

Vpp < 6 5V
FAIL

READ DATA OUTPUT

NO Data
OK

Addr++

YES

Last NO
Addr

YES

READ COMMAND

Vpp < 6 5V, PASS

AI00677

## PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

## PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10μs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.
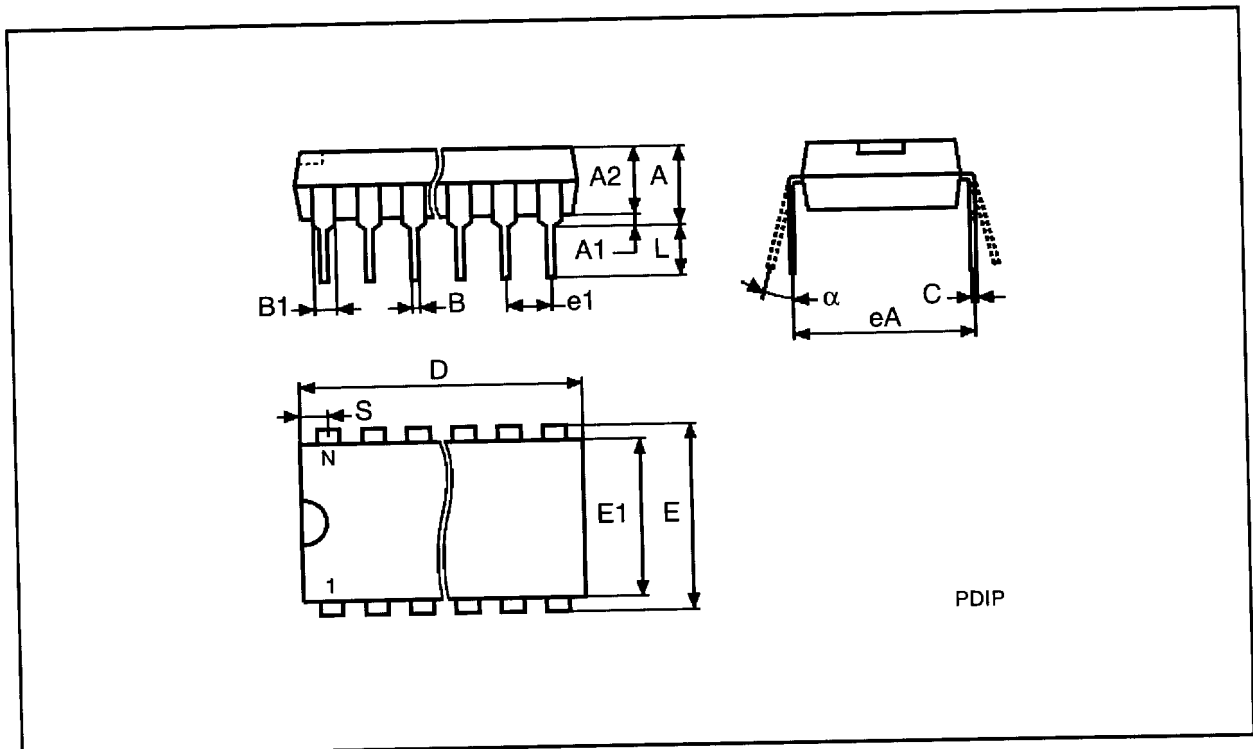
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## ORDERING INFORMATION SCHEME

Example:  M28F256  -12 X B 1 TR

| Speed | | Vcc Tolerance | | Package | | Temp. Range | | Option | |
|---|---|---|---|---|---|---|---|---|---|
| -90 | 90 ns | blank | ± 10% | B | PDIP32 | 1 | 0 to 70 °C | TR | Tape & Reel Packing |
| -10 | 100 ns | X | ± 5% | C | PLCC32 | 3 | –40 to 125 °C | | |
| -12 | 120 ns | | | | | 6 | –40 to 85 °C | | |
| -15 | 150 ns | | | | | | | | |
| -20 | 200 ns | | | | | | | | |
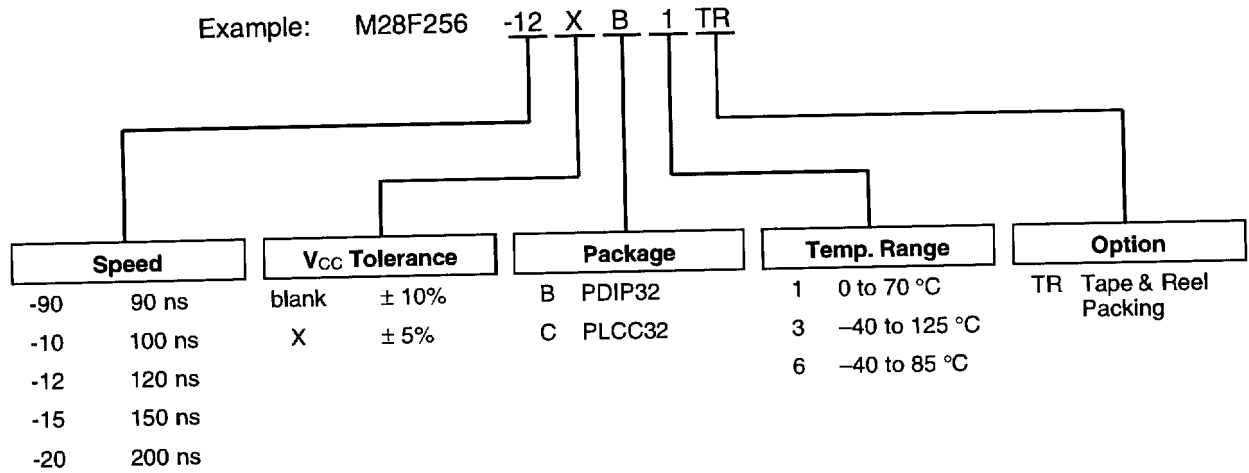
For a list of available options (Speed, Vcc Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

## PDIP32 - 32 pin Plastic DIP, 600 mils width

| Symb | mm | | | inches | | |
|------|-----|-----|-----|--------|-----|-----|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 4.83 | | | 0.190 |
| A1 | | 0.38 | – | | 0.015 | – |
| A2 | – | – | – | – | – | – |
| B | | 0.41 | 0.51 | | 0.016 | 0.020 |
| B1 | | 1.14 | 1.40 | | 0.045 | 0.055 |
| C | | 0.20 | 0 30 | | 0.008 | 0.012 |
| D | | 41.78 | 42.04 | | 1.645 | 1.655 |
| E | | 15.24 | 15.88 | | 0.600 | 0.625 |
| E1 | | 13.46 | 13.97 | | 0.530 | 0.550 |
| e1 | 2.54 | – | – | 0.100 | – | – |
| eA | 15.24 | – | – | 0.600 | – | – |
| L | | 3.18 | 3.43 | | 0.125 | 0.135 |
| S | | 1.78 | 2.03 | | 0.070 | 0.080 |
| α | | 0° | 15° | | 0° | 15° |
| N | 32 | | | 32 | | |

PDIP32



Drawing is not to scale

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## PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

| Symb | mm | | | inches | | |
|------|-----|-----|-----|-----|-----|-----|
|      | Typ | Min | Max | Typ | Min | Max |
| A    |     | 2.54 | 3.56 |     | 0.100 | 0.140 |
| A1   |     | 1.52 | 2.41 |     | 0.060 | 0.095 |
| B    |     | 0.33 | 0.53 |     | 0.013 | 0.021 |
| B1   |     | 0.66 | 0.81 |     | 0.026 | 0.032 |
| D    |     | 12.32 | 12.57 |     | 0.485 | 0.495 |
| D1   |     | 11.35 | 11.56 |     | 0.447 | 0.455 |
| D2   |     | 9.91 | 10.92 |     | 0.390 | 0.430 |
| E    |     | 14.86 | 15.11 |     | 0.585 | 0.595 |
| E1   |     | 13.89 | 14.10 |     | 0.547 | 0.555 |
| E2   |     | 12.45 | 13.46 |     | 0.490 | 0.530 |
| e    | 1.27 | – | – | 0.050 | – | – |
| N    | 32 | | | 32 | | |
| Nd   | 7 | | | 7 | | |
| Ne   | 9 | | | 9 | | |
| CP   |     |     | 0.10 |     |     | 0.004 |

PLCC32



PLCC

Drawing is not to scale

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