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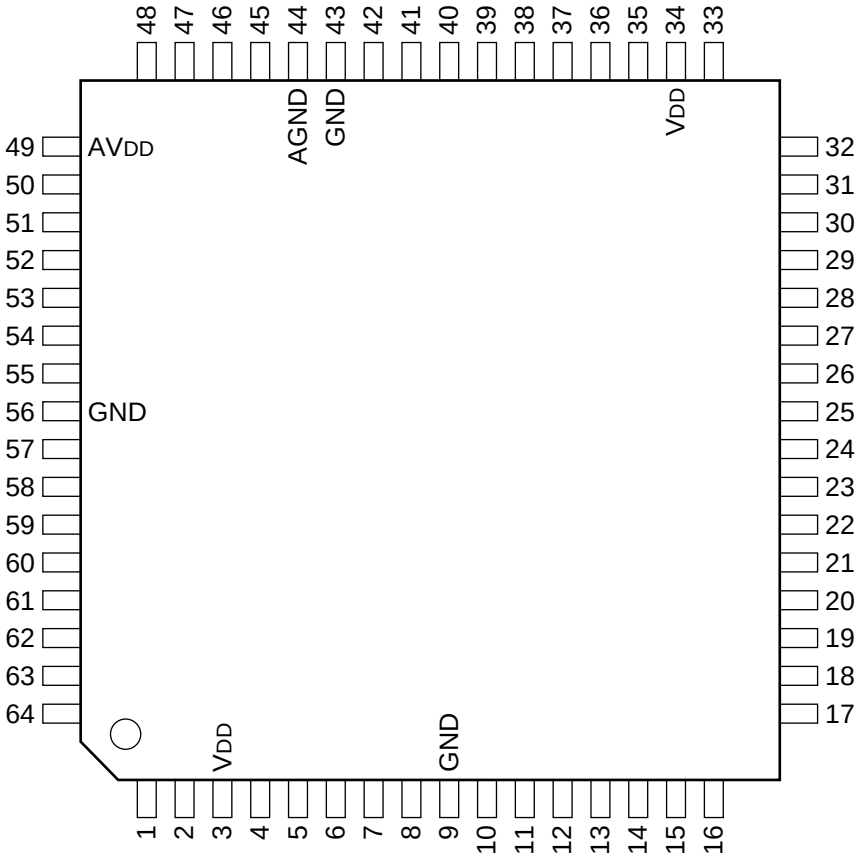
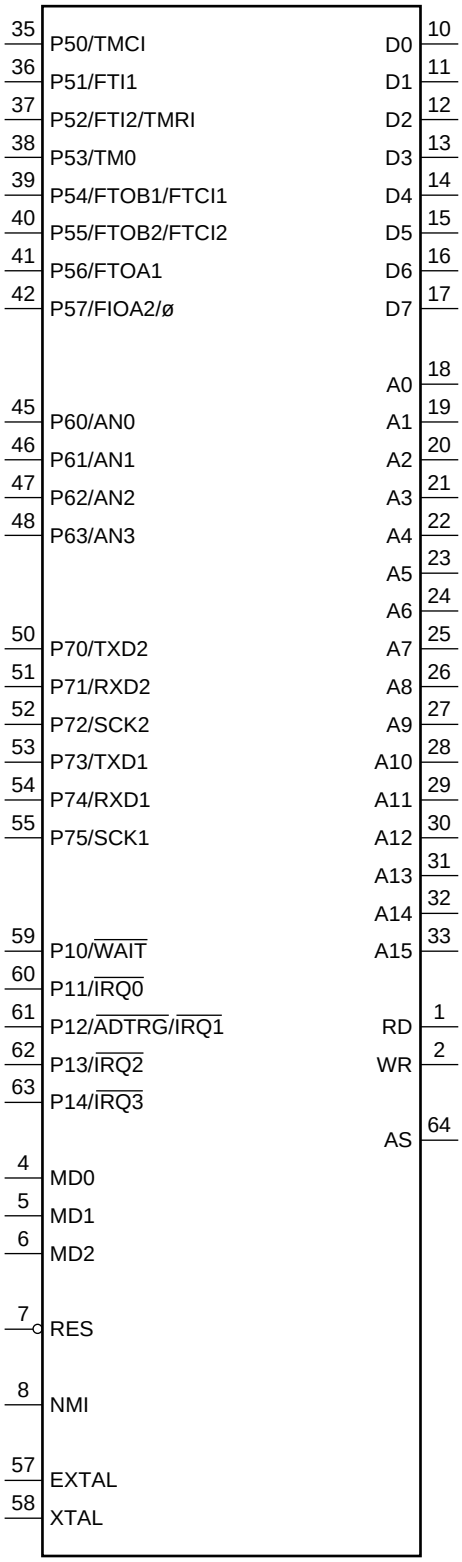
C-MOS MICRO COMPUTER

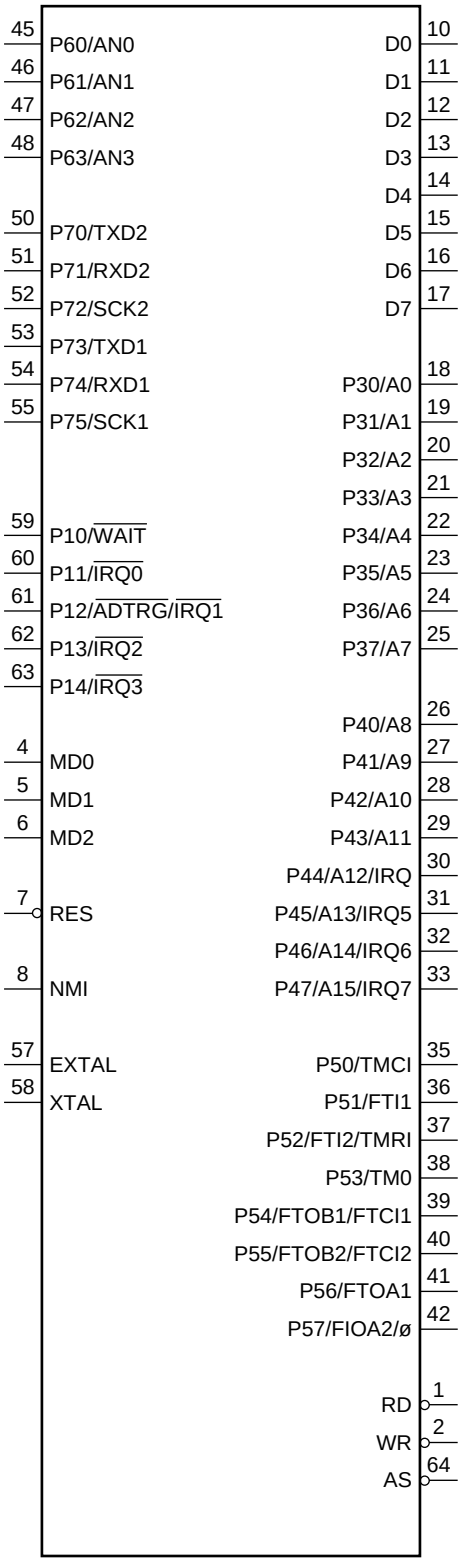
-TOP VIEW-



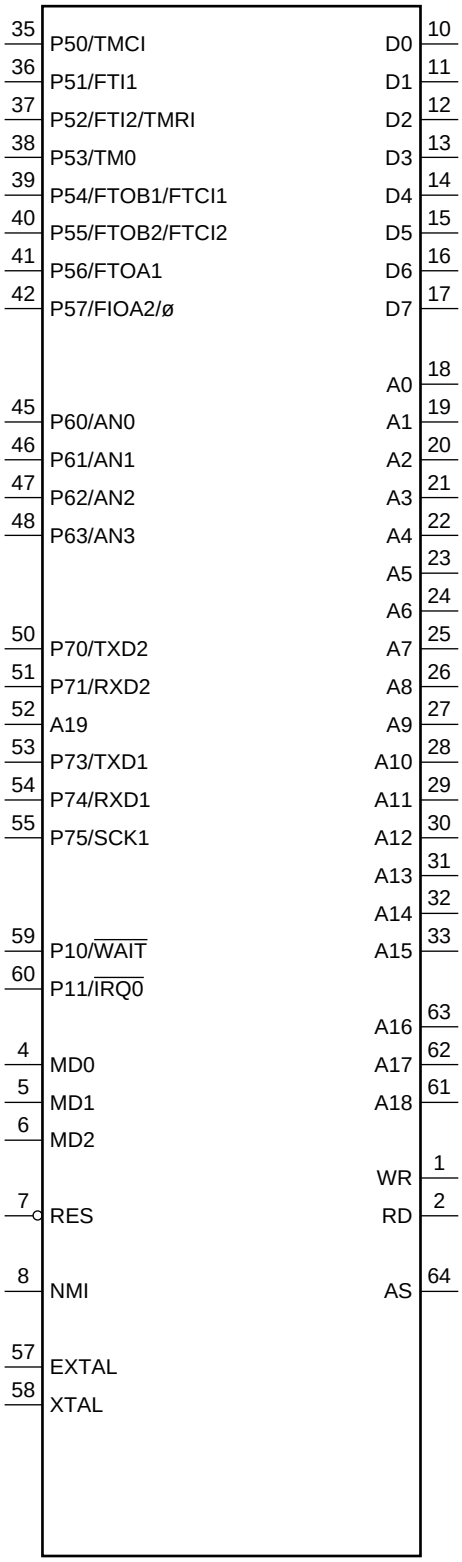
MODE 1


35 P50/TMCI
36 P51/FTI1
37 P52/FTI2/TMRI
38 P53/TM0
39 P54/FTOB1/FTCI1
40 P55/FTOB2/FTCI2
41 P56/FTOA1
42 P57/FIOA2/ø
45 P60/AN0
46 P61/AN1
47 P62/AN2
48 P63/AN3
50 P70/TXD2
51 P71/RXD2
52 P72/SCK2
53 P73/TXD1
54 P74/RXD1
55 P75/SCK1
59 P10/WAIT
60 P11/IRQ0
61 P12/ADTRG/IRQ1
62 P13/IRQ2
63 P14/IRQ3
4 MD0
5 MD1
6 MD2
7 RES
8 NMI
57 EXTAL
58 XTAL
10 D0
11 D1
12 D2
13 D3
14 D4
15 D5
16 D6
17 D7
18 A0
19 A1
20 A2
21 A3
22 A4
23 A5
24 A6
25 A7
26 A8
27 A9
28 A10
29 A11
30 A12
31 A13
32 A14
33 A15
1 RD
2 WR
64 AS

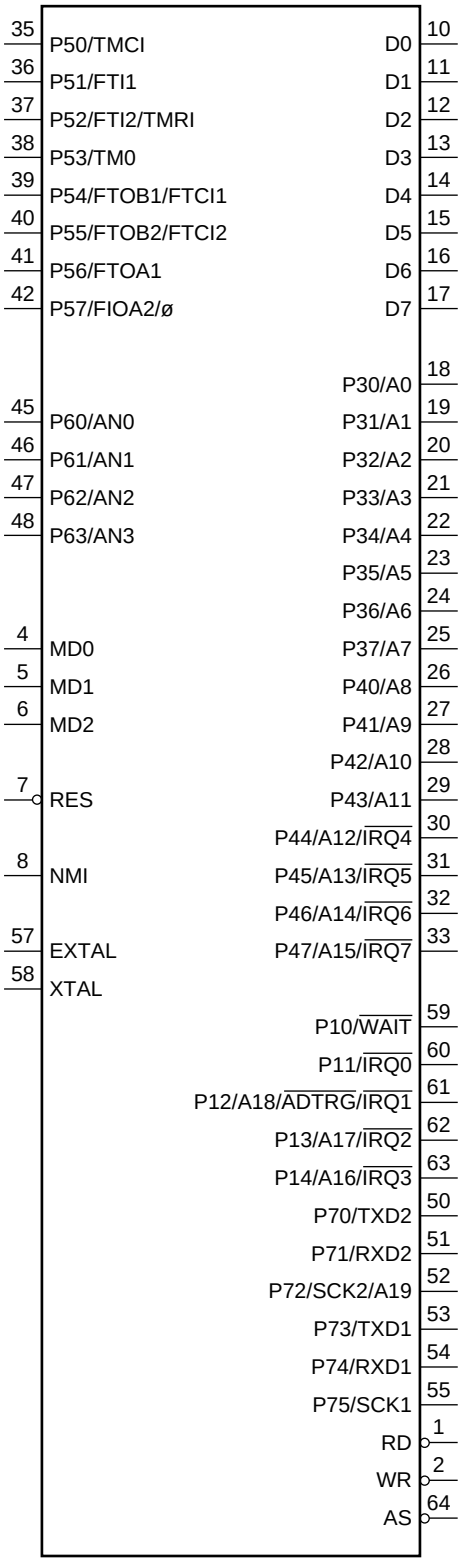
MODE 2


45 P60/AN0
46 P61/AN1
47 P62/AN2
48 P63/AN3
50 P70/TXD2
51 P71/RXD2
52 P72/SCK2
53 P73/TXD1
54 P74/RXD1
55 P75/SCK1
59 P10/WAIT
60 P11/IRQ0
61 P12/ADTRG/IRQ1
62 P13/IRQ2
63 P14/IRQ3
4 MD0
5 MD1
6 MD2
7 RES
8 NMI
57 EXTAL
58 XTAL
10 D0
11 D1
12 D2
13 D3
14 D4
15 D5
16 D6
17 D7
18 P30/A0
19 P31/A1
20 P32/A2
21 P33/A3
22 P34/A4
23 P35/A5
24 P36/A6
25 P37/A7
26 P40/A8
27 P41/A9
28 P42/A10
29 P43/A11
30 P44/A12/IRQ
31 P45/A13/IRQ5
32 P46/A14/IRQ6
33 P47/A15/IRQ7
35 P50/TMCI
36 P51/FTI1
37 P52/FTI2/TMRI
38 P53/TM0
39 P54/FTOB1/FTCI1
40 P55/FTOB2/FTCI2
41 P56/FTOA1
42 P57/FIOA2/ø
1 RD
2 WR
64 AS

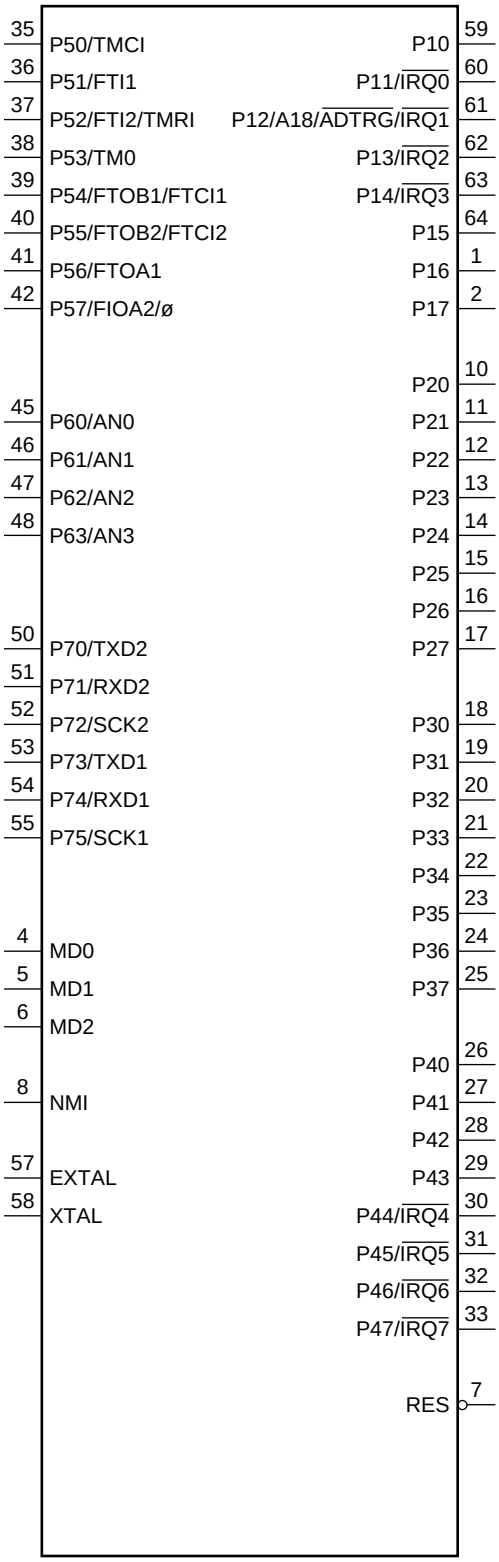
MODE 3


35 P50/TMCI
36 P51/FTI1
37 P52/FTI2/TMRI
38 P53/TM0
39 P54/FTOB1/FTCI1
40 P55/FTOB2/FTCI2
41 P56/FTOA1
42 P57/FIOA2/ø
45 P60/AN0
46 P61/AN1
47 P62/AN2
48 P63/AN3
50 P70/TXD2
51 P71/RXD2
52 A19
53 P73/TXD1
54 P74/RXD1
55 P75/SCK1
59 P10/WAIT
60 P11/IRQ0
4 MD0
5 MD1
6 MD2
7 RES
8 NMI
57 EXTAL
58 XTAL
D0 10
D1 11
D2 12
D3 13
D4 14
D5 15
D6 16
D7 17
A0 18
A1 19
A2 20
A3 21
A4 22
A5 23
A6 24
A7 25
A8 26
A9 27
A10 28
A11 29
A12 30
A13 31
A14 32
A15 33
A16 63
A17 62
A18 61
WR 1
RD 2
AS 64

MODE 4


35 P50/TMCI
36 P51/FTI1
37 P52/FTI2/TMRI
38 P53/TM0
39 P54/FTOB1/FTCI1
40 P55/FTOB2/FTCI2
41 P56/FTOA1
42 P57/FIOA2/ø
45 P60/AN0
46 P61/AN1
47 P62/AN2
48 P63/AN3
4 MD0
5 MD1
6 MD2
7 RES
8 NMI
57 EXTAL
58 XTAL
D0 10
D1 11
D2 12
D3 13
D4 14
D5 15
D6 16
D7 17
P30/A0 18
P31/A1 19
P32/A2 20
P33/A3 21
P34/A4 22
P35/A5 23
P36/A6 24
P37/A7 25
P40/A8 26
P41/A9 27
P42/A10 28
P43/A11 29
P44/A12/IRQ4 30
P45/A13/IRQ5 31
P46/A14/IRQ6 32
P47/A15/IRQ7 33
P10/WAIT 59
P11/IRQ0 60
P12/A18/ADTRG/IRQ1 61
P13/A17/IRQ2 62
P14/A16/IRQ3 63
P70/TXD2 50
P71/RXD2 51
P72/SCK2/A19 52
P73/TXD1 53
P74/RXD1 54
P75/SCK1 55
RD 1
WR 2
AS 64

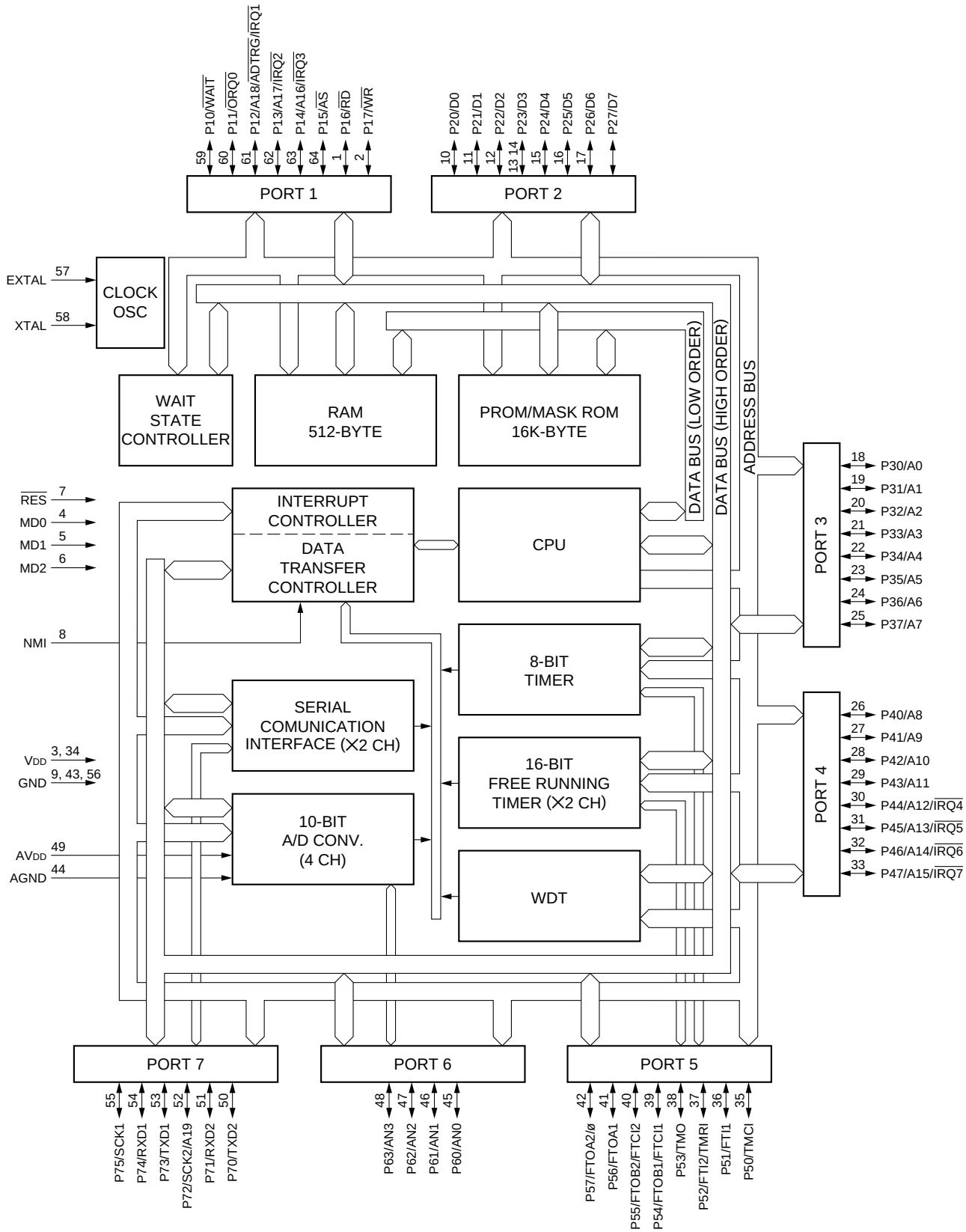
MODE 7



INPUTS			OPERATION MODE	CONTENTS
MD2	MD1	MD0		
0	0	1	MODE 1	EXTENSION MINIMUM MODE (ROM INVALID)
0	1	0	MODE 2	EXTENSION MINIMUM MODE (ROM VALID)
0	1	1	MODE 3	EXTENSION MAXIMUM MODE (ROM INVALID)
1	0	0	MODE 4	EXTENSION MAXIMUM MODE (ROM VALID)
1	1	1	MODE 7	SINGLE CHIP MODE

0; LOW LEVEL

1; HIGH LEVEL


PORT 1
PORT 2
P10/WAIT
P11/ORQ0
P12/A18/ADTRG/IRQ1
P13/A17/IRQ2
P14/A16/IRQ3
P15/AS
P16/RD
P17/WR
P20/D0
P21/D1
P22/D2
P23/D3
P24/D4
P25/D5
P26/D6
P27/D7
EXTAL
XTAL
CLOCK OSC
WAIT STATE CONTROLLER
RAM 512-BYTE
PROM/MASK ROM 16K-BYTE
DATA BUS (LOW ORDER)
DATA BUS (HIGH ORDER)
ADDRESS BUS
RES
MD0
MD1
MD2
INTERRUPT CONTROLLER
DATA TRANSFER CONTROLLER
CPU
NMI
8-BIT TIMER
SERIAL COMUNICATION INTERFACE (×2 CH)
16-BIT FREE RUNNING TIMER (×2 CH)
VDD
GND
10-BIT A/D CONV. (4 CH)
AVDD
AGND
WDT
PORT 3
P30/A0
P31/A1
P32/A2
P33/A3
P34/A4
P35/A5
P36/A6
P37/A7
PORT 4
P40/A8
P41/A9
P42/A10
P43/A11
P44/A12/IRQ4
P45/A13/IRQ5
P46/A14/IRQ6
P47/A15/IRQ7
PORT 7
PORT 6
PORT 5
P75/SCK1
P74/RXD1
P73/TXD1
P72/SCK2/A19
P71/RXD2
P70/TXD2
P63/AN3
P62/AN2
P61/AN1
P60/AN0
P57/FTOA2/ø
P56/FTOA1
P55/FTOB2/FTCI2
P54/FTOB1/FTCI1
P53/TMO
P52/FTI2/TMRI
P51/FTI1
P50/TMCI