

ML6553

Bus Termination Regulator

Features

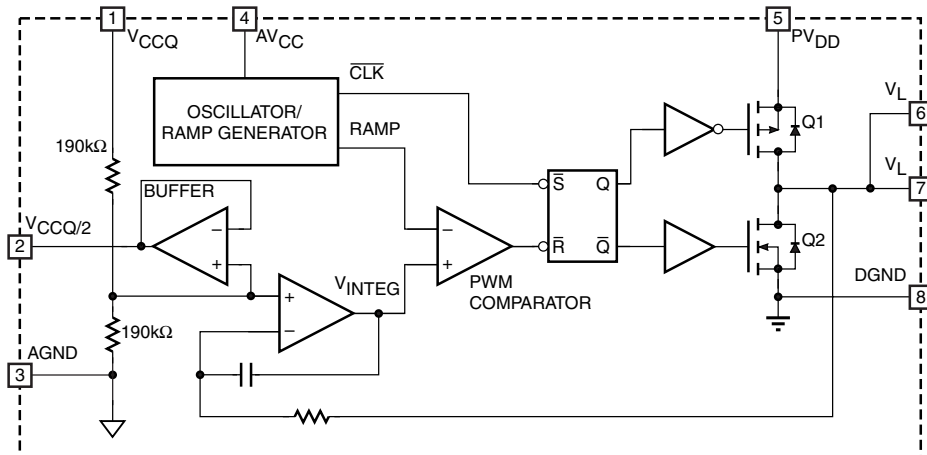
- Can source and sink up to 1A
- Generates termination voltages for DDR SDRAM, SSTL_2 SDRAM, SGRAM, or equivalent memories
- Generates termination voltages for active termination schemes for GTL+, DDR, Rambus™, VME, LV-TTL, PECL and other high speed logic
- V_L regulated to within 3% at 800mA
- Minimum external components. Requires no feedback compensation
- Fixed frequency operation for easier system integration
- Lower power consumption than passive, resistor divider termination, reducing heat by as much as 50%
- Separate voltages for VCCQ and PVDD

General Description

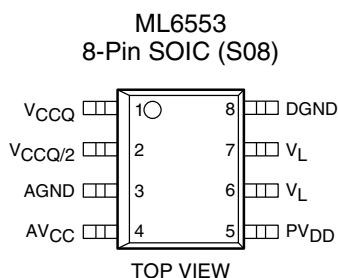
The ML6553 switching regulator is designed to convert voltage supplies ranging from 2.0V to 3.6V into a desired output voltage or termination voltage for various applications. The ML6553 can be implemented to produce regulated output voltages in two different modes. In the default mode, the output is 50% of voltage applied to VCCQ. The switching regulator is capable of sourcing or sinking up to 1A of current.

The ML6553, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed back-plane designs. The voltage output of the regulator can be used as a termination voltage for other bus interface standards such as SSTL, DDR, Rambus™, GTL+, VME, LV-CMOS, LV-TTL, P-ECL, and CMOS.

Block Diagram



Pin Configuration



Pin Description

Pin	Name	Function
1	VCCQ	Voltage supply for internal reference voltage divider
2	VCCQ/2	VREF output is VCCQ/2
3	AGND	Analog signal ground
4	AVCC	Voltage supply for the noise sensitive analog control section.
5	PVDD	Voltage supply for the internal power transistors.
6	VL	Output inductor connection
7	VL	Output inductor connection
8	DGND	Return for the internal power transistors.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Unit
V _{IN}		5	V
Voltage on Any Other Pin	GND – 0.3	V _{IN} + 0.3	V
Peak Switch Current (I _{PEAK})		1	A
Average Switch Current (I _{AVG})		300	mA
Junction Temperature		150	°C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering, 10 sec)		150	°C
Thermal Resistance (θ _{JA})		160	°C/W
Output Current, Source or Sink		1	A

Operating Conditions

Temperature Range	0°C to 70°C
AVCC, PVDD Operating Range	2.0V to 3.6V

Electrical Characteristics

$AV_{CC} = PV_{DD} = 3.3V \pm 10\%$. Unless otherwise specified, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
Switching Regulator							
V_{TT}	Output Voltage, V_{TT} (See Figure 2)	$I_{OUT} = 0$, $V_{REF} = \text{open}$	$V_{CCQ} = 2.3V$	1.12	1.15	1.18	V
			$V_{CCQ} = 2.5V$	1.22	1.25	1.28	V
			$V_{CCQ} = 2.7V$	1.32	1.35	1.38	V
		$I_{OUT} = \pm 1A$, $V_{REF} = \text{open}$ Note 2	$V_{CCQ} = 2.3V$	1.09	1.15	1.21	V
			$V_{CCQ} = 2.5V$	1.19	1.25	1.31	V
			$V_{CCQ} = 2.7V$	1.28	1.35	1.42	V
$V_{CCQ/2}$	Output Voltage, $V_{CCQ/2}$	$V_{CCQ} = 2.3V$	1.139	1.15	1.162	V	
		$V_{CCQ} = 2.5V$	1.238	1.25	1.263	V	
		$V_{CCQ} = 2.7V$	1.337	1.35	1.364	V	
	Source Resistance from V_L			20		m Ω	
	Switching Frequency			650		kHz	
I_{REF}	Output Load Current for $V_{CCQ/2}$ Pin			3		mA	
Supply							
I_Q	Quiescent Current	$I_{OUT} = 0$, no load	I_{VCCQ}		10		μA
			I_{AVCC}	500			μA
			I_{PVDD}	4.5			mA

Notes:

- Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
- Specifications are taken from the application circuit in Figure 2 using the recommended component values.

Functional Description

The ML6553 switching regulator is designed to sink and source 1A load current and maintain a tight output voltage regulation without the need for external feedback. Feedback is accomplished internally by setting the average value of V_L equal to $V_{CCQ}/2$ through a high gain error amp. The ML6553 implements an open loop design that does not require external loop compensation, providing a simplified regulator design that can be used in cost sensitive applications.

Regulator Operation

Refer to the block diagram on the first page of this datasheet. The oscillator/ramp block generates a 650kHz clock pulse that is used to set the flip-flop. It also generates a 650kHz ramp that the PWM comparator uses to reset the flip-flop. When the flip-flop is set, the high side switch (Q1) is turned

on and the low side switch (Q2) is held off. In this state, the voltage at V_L is pulled up to PV_{DD} , which the error amp, integrates and inverts. The resulting output voltage of the error amp will decline until it intersects the rising voltage of the ramp. When this occurs the flip-flop is reset. In the reset state, the high side switch is off, the low side switch is on and V_L is pulled to $DGND$. The flip-flop will remain in the reset state until the next clock pulse. A timing diagram is shown in Figure 1.

In the absence of a load, the duty cycle will be 50% if the PV_{DD} and V_{CCQ} are the same. The average voltage at V_L will be half the voltage applied to V_{CCQ} , and the net current change will be zero. If the ML6553 needs to source current, the duty cycle will increase, resulting in more current being supplied to the load. If the ML6553 needs to sink current, the duty will decrease, resulting in current being pulled from the load and returned back to the PV_{DD} supply.

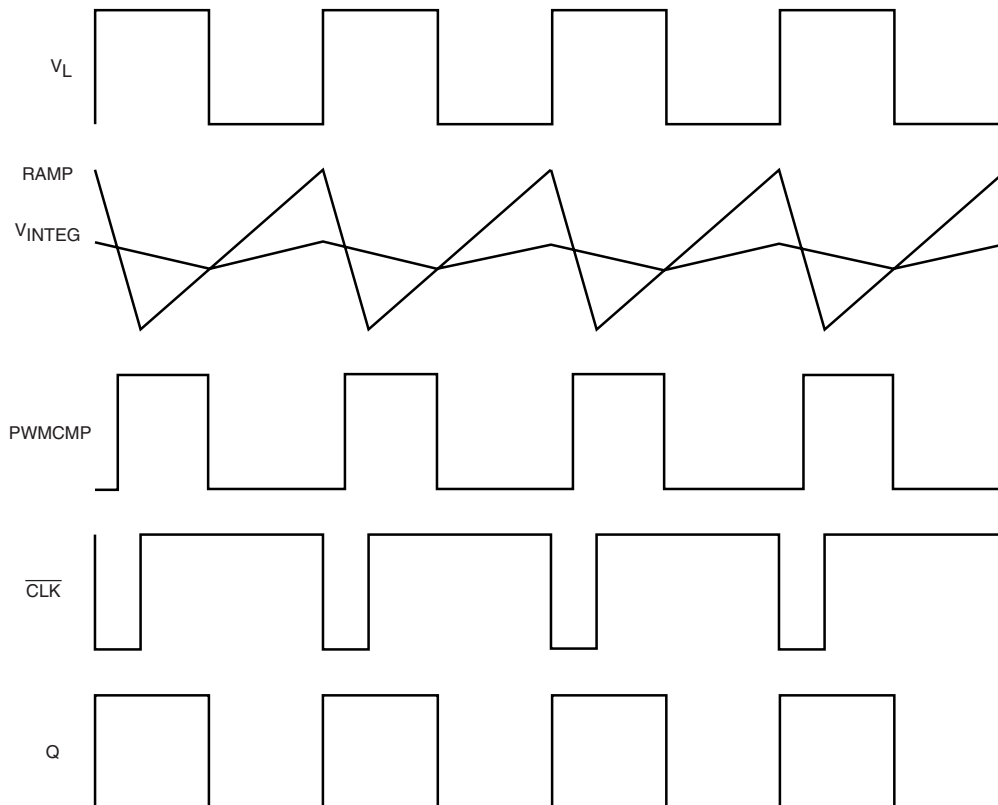


Figure 1. Timing Diagram

Design Consideration

Inductor Selection

The ML6553 requires the selection of an external inductor. A value of 4.7μH is a good choice, but any value between 2.2μH and 10μH is acceptable. Choosing an inductance value of less than 2.2μH will reduce the component’s footprint or the DC resistance, but the output voltage ripple will increase. Conversely, inductance values greater than 10μH will reduce the output ripple, but component size and output regulation become issues.

It is important to use an inductor that is rated to handle 1.5A peak currents without saturating. Also look for an inductor with low winding resistance. An inductor with low winding resistance leads to better regulation and higher output current capability. A good rule of thumb is to use inductors with 20mΩ or less of winding resistance.

The final selection of the inductor will be based on trade-offs between size, cost and performance. Make your selections carefully. Inductor tolerance, core and copper loss will vary with the type of inductor selected and should be evaluated with the ML6553 under worst case conditions to determine its suitability.

Suggested inductor for L1:

Manufacturer	Part No.	Inductance	DC Resistance
Coiltronics	UP3-4R7	4.7μH	0.011Ω

Coiltronics (561) 241-7876

Output Capacitor

The output capacitor filters the pulses of current from the bus terminator regulator as well as lowers the AC output impedance. For the best performance, one 330μF OS-CON decoupling capacitor is recommended.

Note that data transitions on the bus cause fast changes in output current. These fast current changes cause high frequency spikes to appear on the output. To minimize these effects, choose an output capacitor with a combined ESR of less than 50mΩ and use good layout practices to minimize trace inductance from the output capacitors to the termination resistors. In addition, it is also recommended to bypass the termination resistors with 0.01μF ceramic capacitors.

Suitable capacitors can be obtained from the following vendors:

AVX	(207) 282-5111	TPS Series
Sanyo	(619) 661-6835	OS-CON Series

Input Capacitor

It is recommended to de-couple the PVDD input with a 47μF to 100μF capacitor. This provides the benefits of preventing the input ripple from affecting the ML6553 control circuitry, as well as improves the efficiency by reducing the I squared R losses during the charge cycle of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

The AVCC input should be de-coupled with at least a ceramic capacitor but a low pass RC filter is recommended if the supply is particularly noisy. If a RC filter is used, the series resistor value needs to be low enough to prevent excessive voltage drops and high enough to provide effective filtering. Resistor values on the order of 100Ω are acceptable.

The VCCQ pin can also be bypassed with a ceramic capacitor if noise is present. The VCCQ pin can be de-coupled with a low pass RC filter if there is significant noise pickup on its input. If a RC filter is used, resistor values on the order of 1,000Ω are acceptable.

Layout

Good layout practices will ensure the proper operation of the ML6553. Some layout guidelines follow:

- Use adequate ground and power traces or planes.
- Keep the 47μF-100μF input capacitor as close to PVDD and DGND as possible.
- Use short trace lengths from the inductor to the VL pins and from the inductor to the output capacitors.
- Use a separate trace from AGND to DGND, and use DGND as the ground point for all the power components.
- Use additional bypass capacitors at each termination resistor pack.

A typical application circuit schematic is shown in Figure 2, and a sample layout is shown in Figure 3.

$$I_{OUT(MAX)} = \frac{(DESIREDOVA - OUTPUTOVA) \times V_{TT}}{L_{DCR} + 0.020} \quad (1)$$

Where LDCR is the DC resistance of the output inductor, L1 in Figure 2, and 0.020 is the source resistance of the output VL. Both LDCR and 0.020 are in Ohms.

Output Current Capability

The maximum current available at the output of the regulator is related to the DC resistance of the inductor, the source impedance of the ML6553, and the desired regulation. The source impedance of the ML6553 can be estimated at $20\text{m}\Omega$ with an initial output voltage accuracy of $\pm 1\%$. So the maximum output current can be estimated using:

$$I_{\text{OUT(MAX)}} \approx \frac{(\text{DESIRED}_{\text{OVA}} - \text{INITIAL}_{\text{OVA}})}{L_{\text{DCR}} + 0.020} \times V_{\text{TT}}$$

So, for an inductor with $11\text{m}\Omega$ DC resistance, a termination voltage of 1.25V , and a desired output voltage accuracy of 3% :

$$I_{\text{OUT(MAX)}} = \frac{(3\% - 1\%) \times 1.25}{(0.011 + 0.020) \times 100} = 0.806\text{A} \quad (2)$$

This is enough current capability to terminate 50 bus lines, assuming 16mA of drive current per line.

Since the feedback loop is closed internally on the ML6553 the total series resistance of the L/C output filter contributes to increased deviation from no load to full load. The output source impedance of the ML6553 is approximately $20\text{m}\Omega$. A 1A load current yields 11mV (from L1) in output deviation $+20\text{mV}$ from the ML6553. Be sure to factor in the component ESR values when constrained to a particular maximum output deviation. Adequately bypass the VTT output with SMD film capacitors to reduce transients generated by stray lead inductance.

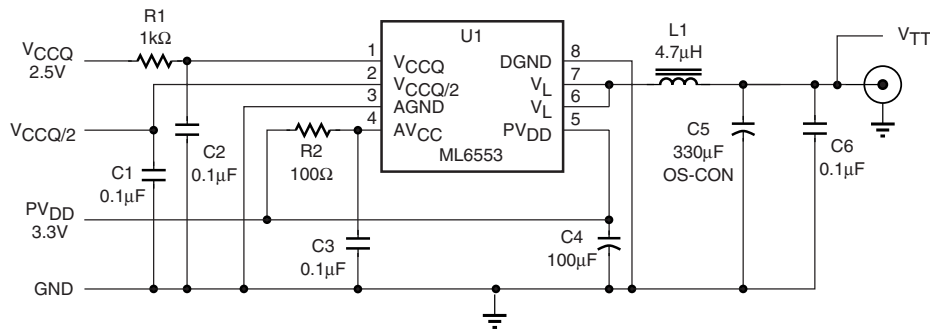


Figure 2. Application Schematic

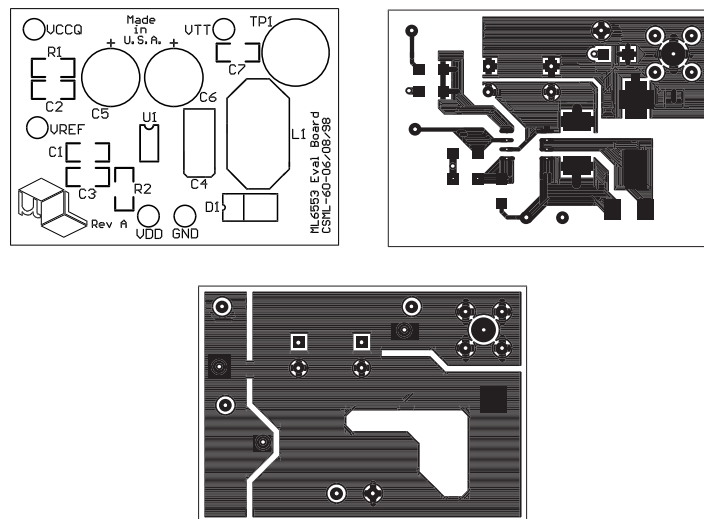
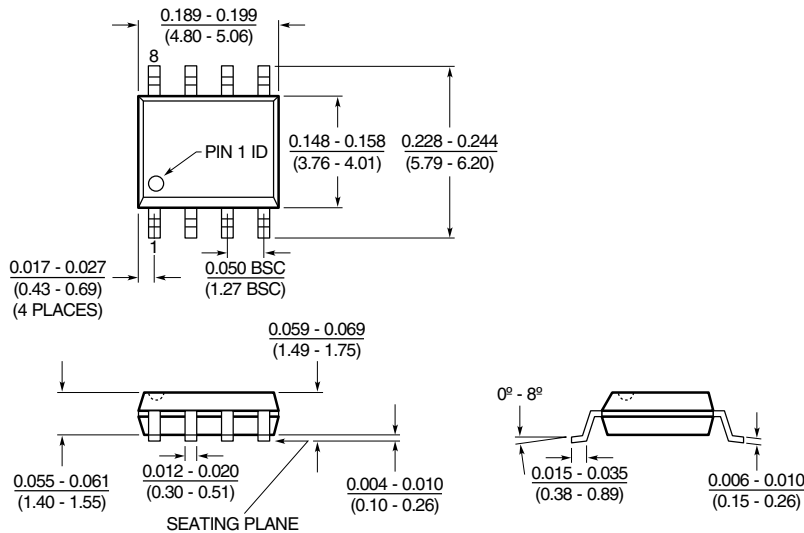


Figure 3. ML6553 Board Layout

Mechanical Dimensions Inches (Millimeters)

S08 8-Pin SOIC



Ordering Information

Part Number	Temperature Range	Package
ML6553CS-1	0°C to 70°C	8-Pin SOIC (S08)

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