



Digital Signal Processor for TV

■ Package

■ General Description

The NJU26102 is a digital signal processor that provides Delay, eala, VIVA2+, PEQ, and AGC.

The NJU26102 is suitable for audio products such as TV, CD radio- cassette, speakers system, and others.



NJU26102FR1

■ Feature

- 3D Sound: eala, BBE VIVA, BBE ViVA+, BBE VIVA2+.
- Sound enhancement: BBE, Mach3Bass.
- 5band - PEQ, Tone Control.
- AGC to control sound-volume difference between channels or programs.

■ Digital Signal Processor Specification

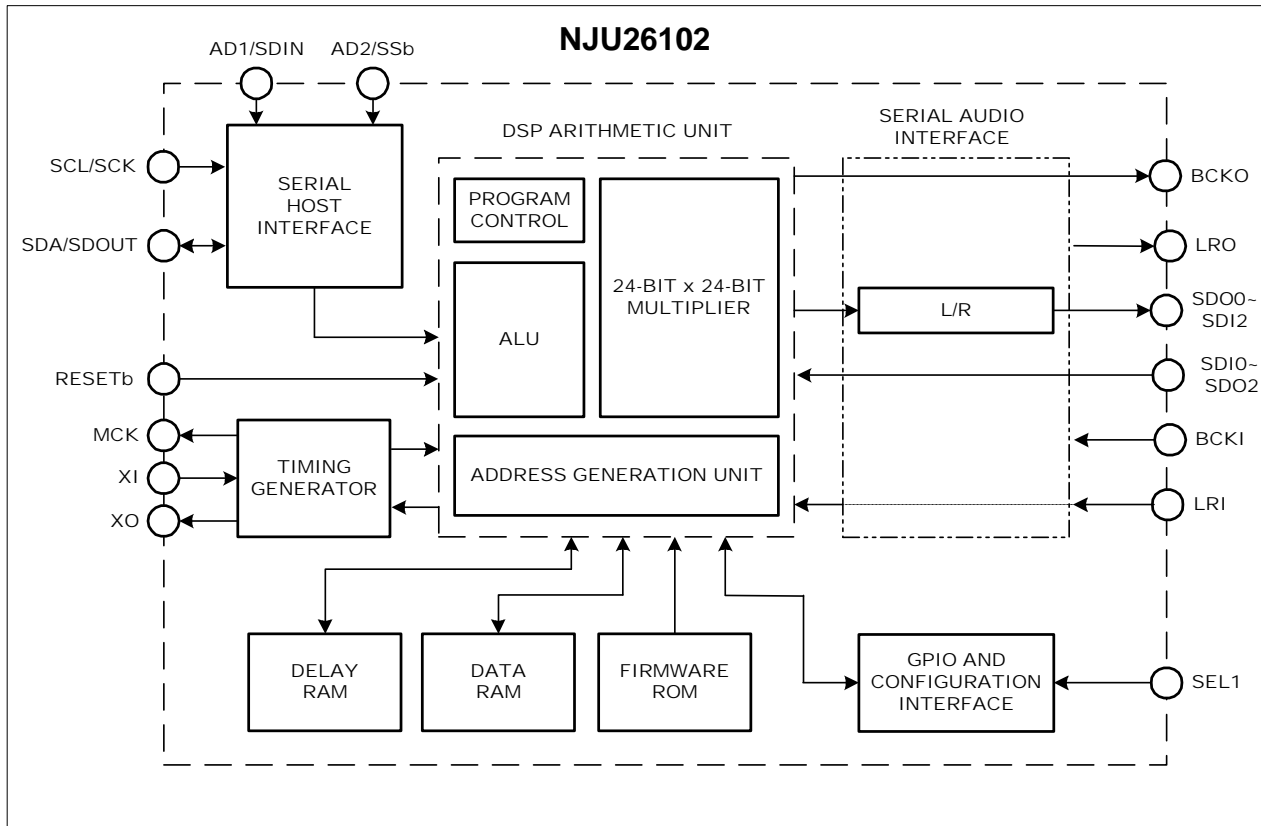
- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Master / Slave Mode
- Master Mode MCK : 1/2 fclk, 1/3 fclk
ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Two kinds of micro computer interface
 - I²C bus (standard-mode/100kbps)
 - Serial interface (4 lines: clock, enable, input data, output data)
- Power Supply : 2.5V (3.3V Input tolerant)
- Package : QFP32-R1

The detail hardware specification of the NJU26102 is described in the “NJU26100 Series Hardware Data Sheet”.

NJU26102

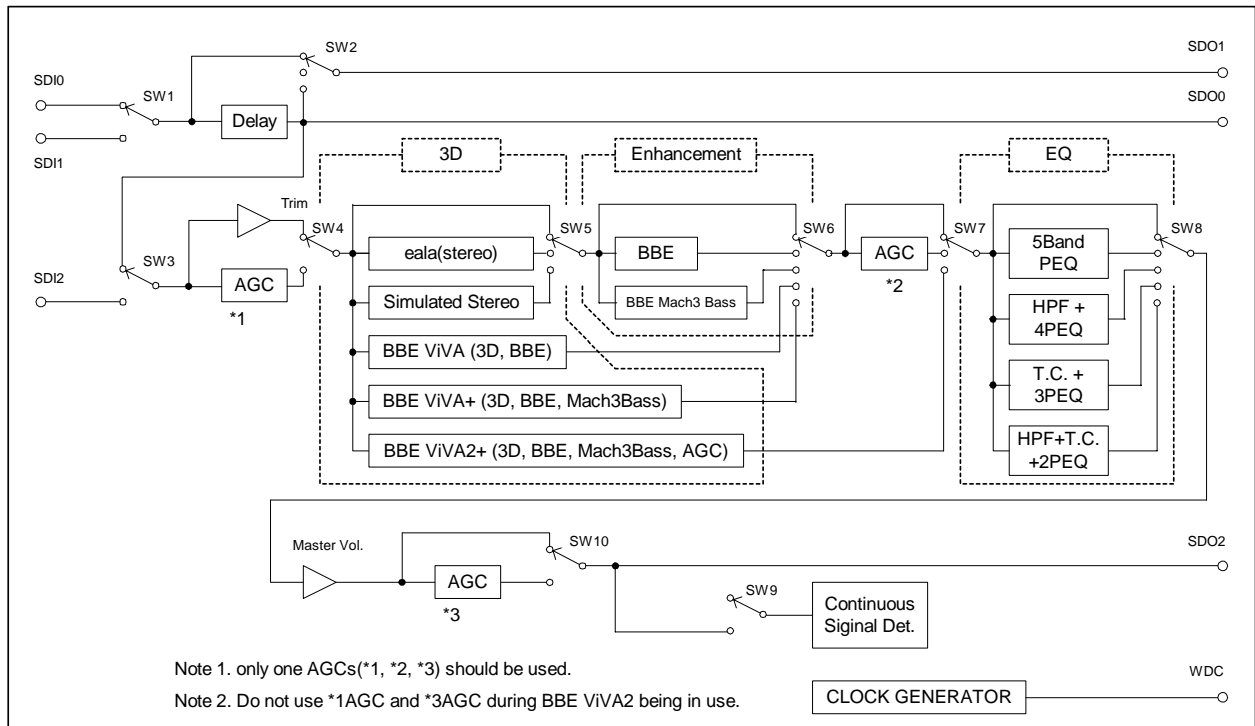
DSP Block Diagram

Fig.1 NJU26102 DSP Block Diagram



Function Block Diagram

Fig.2 NJU26102 Function Block Diagram



Pin Configuration

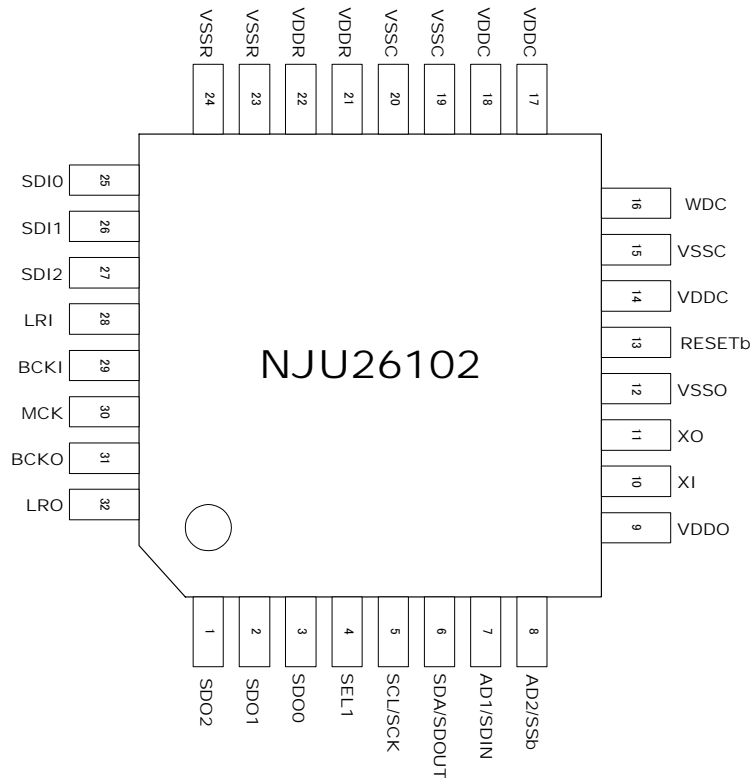


Fig.3 NJU26102 Pin Configuration

Pin Description

Table 1 Pin Description

No.	Symbol	I/O	Description	No.	Symbol	I/O	Description
1	SDO2	O	Audio Data Output 2 L/R	17	VDDC	--	Core Power Supply +2.5V
2	SDO1	O	Audio Data Output 1 L/R	18	VDDC	--	Core Power Supply +2.5V
3	SDO0	O	Audio Data Output 0 L/R	19	VSSC	--	Core GND
4	SEL1	I ^{*2}	Select I ² C or Serial bus	20	VSSC	--	Core GND
5	SCL/SCK	I	I ² C Clock / Serial Clock	21	VDDR	--	I/O Power Supply +2.5V
6	SDA/SDOUT	I/O	I ² C I/O / Serial Output	22	VDDR	--	I/O Power Supply +2.5V
7	AD1/SDIN	I	I ² C Address / Serial Input	23	VSSR	--	I/O GND
8	AD2/SSb	I	I ² C Address / Serial Enable	24	VSSR	--	I/O GND
9	VDDO	--	OSC Power Supply +2.5V	25	SDI0	I	Audio Data Input 0 L/R
10	XI	I	X'tal Clock Input	26	SDI1	I	Audio Data Input 1 L/R
11	XO	O	OSC Output	27	SDI2	I	Audio Data Input 2 L/R
12	VSSO	--	OSC GND	28	LRI	I	LR Clock Input
13	RESETb	I	RESET (active Low)	29	BCKI	I	Bit Clock Input
14	VDDC	--	Core Power Supply +2.5V	30	MCK	O	Master Clock Output
15	VSSC	--	Core GND	31	BCKO	O	Bit Clock Output
16	WDC	O ^{*2}	Clock for Watch Dog Timer	32	LRO	O	LR Clock Output

*1 I : Input, O : Output, I/O : Bi-directional

*2 SEL1 : Input, WDC : Output

■ Audio Interface

The NJU26102 audio interface provides industry serial data formats of I²S, MSB-first left-justified or MSB-first Right-justified. The NJU26102 audio interface provides three data inputs, SDI0, SDI1, and SDI2, and three data outputs, SDO0, SDO1, and SDO3, as shown in table 2 and 3. The input serial data is selected by the firmware command.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description
25	SDI0	Audio Data Input 0 L / R
26	SDI1	Audio Data Input 1 L / R
27	SDI2	Audio Data Input 2 L / R

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
3	SDO0	Audio Data Output 0 L / R
2	SDO1	Audio Data Output 1 L / R
1	SDO2	Audio Data Output 2 L / R

■ Host Interface

The NJU26102 can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : 4-Wire serial bus or I²C bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The detail 4-Wire Serial bus and I²C bus information are described in the “NJU26100 Series Hardware Data Sheet”.

■ I²C address

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. These pins offer additional flexibility to SLAVE address. 4 addresses could be chosen by AD1 and AD2-pin. The AD1 and AD2-pin addresses are decided by the connections of AD1 and AD2-pin. The AD1 and AD2 addresses should be the same level as AD1 and AD2-pin connections.

Table 4 I²C Bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	1	1	1	AD2*	AD1*	R/W

* AD1 or AD2 address is 0 when AD1 or AD2-pin is “L”. AD1 or AD2 address is 1 when AD1 or AD2-pin is “H”.

The detail I²C bus timing of the NJU26102 is described in the “NJU26100 Series Hardware Data Sheet”.

■ Watchdog Clock

NJU26102 outputs clock pulse through WDC (Pin No. 16) during normal operation.

WDC Clock Cycle (L / H) Time	184msec(fs=48kHz)
	200msec(fs=44.1kHz)
	276msec(fs=32kHz)

The NJU26102 generates a clock pulse through the WDC terminal after resetting the NJU26102. The WDC clock is useful to check the status of the NJU26102 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26102. When the WDC clock pulse is lost or not normal clock cycle, the NJU26102 does not operate correctly. Then reset the NJU26102 and set up the NJU26102 again.

■ Firmware Command Table

Host processor can control the NJU26102 via 4-Wire serial bus or I²C bus interface. The following table summarizes the available user commands.

Table 5 NJU26102 Command

No.	Command	Command Description
1	System State	DSP Mode, Data Width, Serial Audio Mode, Audio Clock, MCK clock
2	Firmware Version No. Request	Firmware Version No. Request
3	Firmware Mode Select	eala, BBE, Mach3Bass, VIVA, VIVA+, VIVA2, PEQ, AGC, Signal Detect, Bypass
4	Input Select / Fs Select	Input Select: SDI0, SDI1, SDI2, Delay Input Select Sample Rate: 48, 44.1, 32kHz
5	Input Trim	0 to -31dB
6	Master Volume	0 to -96dB, -Inf (with Smooth Control)
7	Channel Balance	0 to -30dB, -Inf, L/R Select
8	AGC Threshold Level	Threshold Level: -6 to -40dBFS Noise Compressor Threshold Level: -50 to -96dBFS, -Inf Attack Time: 0.1, 0.2, 0.5, 1, 2, 5sec Release Time: 1, 2, 5msec Ratio: 1.5:1, 2:1, 4:1, 8:1, 20:1, -Inf:1 Boost: 0 to +24dB Output Trim: 0 to -31dB Position: forward the 3D, EQ, backward the Master Volume
9	eala Gain	0 to +12dB
10	BBE VIVA / VIVA+ Surround Gain	0 to +6dB
11	BBE	Level: 0 to -15dB HF Adjust: 0 to 15
12	BBE VIVA2+ AGC	Threshold Level: -6 to -26dBFS Attack Time: 0.1, 0.2, 0.5, 1, 2, 5sec Release Time: 1, 2, 5msec Ratio: 2:1, 4:1, 8:1, -Inf:1 Boost: 0 to +24dB Output Trim: 0 to -31dB
13	BBE Mach3Bass	f0: 40 to 150Hz Q: 1.8 to 8.2 Gain: 0 to +12dB
14	EQ Mode	5band PEQ, HPF, Tone Control
15	PEQ f0 /HPF fc	f0: 20 to 20kHz(1/6 octave, 20 points/decade) Q: 0.33 to 8.2 Gain: -12 to +12dB
16	Delay Time	Delay: 0 to 37.5msec (at Fs = 32kHz)
17	Continuous Signal Detect	Continuous Signal Detect
18	NOP	No Operation

In respect to detail command information, request NJR.

■ License Information

1. The NJU26102 is manufactured by New Japan Radio Co.,Ltd. under license from BBE Sound Inc. BBE is a registered trademark of BBE Sound Inc. A license from BBE Sound Inc. must be required before the NJU26102 can be purchased from New Japan Radio Co.,Ltd.

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Version V1.1

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