PA7572 PEEL Array™

Programmable Electrically Erasable Logic Array

Versatile Logic Array Architecture
- 24 I/Os, 14 inputs, 60 registers/latches
- Up to 72 logic cell output functions
- PLA structure with true product-term sharing
- Logic functions and registers can be I/O-buried

High-Speed Commercial and Industrial Versions
- As fast as 13ns/20ns (tpdi/tpdx), 66.6MHz (f_{MAX})
- Industrial grade available for 4.5 to 5.5V V_{CC} and -40 to +85 °C temperatures

Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications
- Integration of multiple PLDs and random logic
- Buried counters, complex state-machines
- Comparators, decoders, other wide-gate functions

CMOS Electrically Erasable Technology
- Reprogrammable in 40-pin DIP, 44-pin PLCC and TQFP packages

Flexible Logic Cell
- Up to 3 output functions per logic cell
- D,T and JK registers with special features
- Independent or global clocks, resets, presets, clock polarity and output enables
- Sum-of-products logic for output enables

Development and Programmer Support
- ICT PLACE Development Software
- Fitters for ABEL, CUPL and other software
- Programming support by popular third-party programmers

General Description

The PA7572 is a member of the Programmable Electrically Erasable Logic (PEEL™) Array family based on Anachip's CMOS EEPROM technology. PEEL™ Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7572 offers a versatile logic array architecture with 24 I/O pins, 14 input pins and 60 registers/latches (24 buried logic cells, 12 input registers/latches, 24 buried I/O registers/latches). Its logic array implements 100 sum-of-products logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available.

The PA7572's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T, and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7572 suitable for a variety of combinatorial, synchronous and asynchronous logic applications. The PA7572 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 66.6MHz (f_{MAX}) at moderate power consumption 140mA (100mA typical). Packaging includes 40-pin DIP and 44-pin PLCC (see Figure 1). Anachip and popular third-party development tool manufacturers provide development and programming support for the PA7572.

Figure 1. Pin Configuration

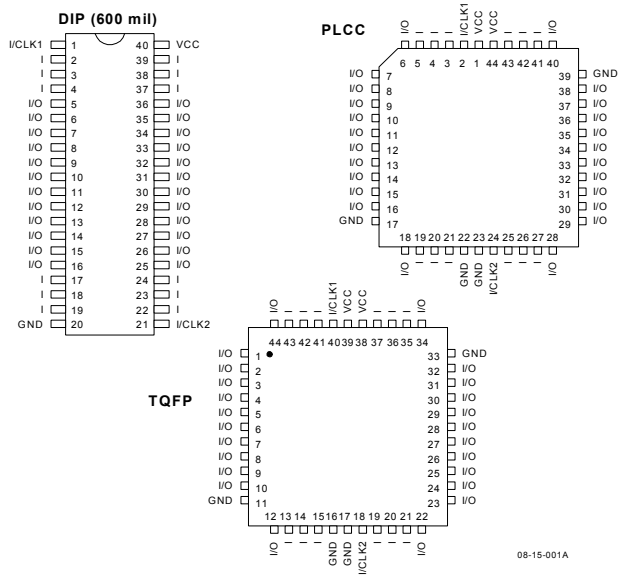
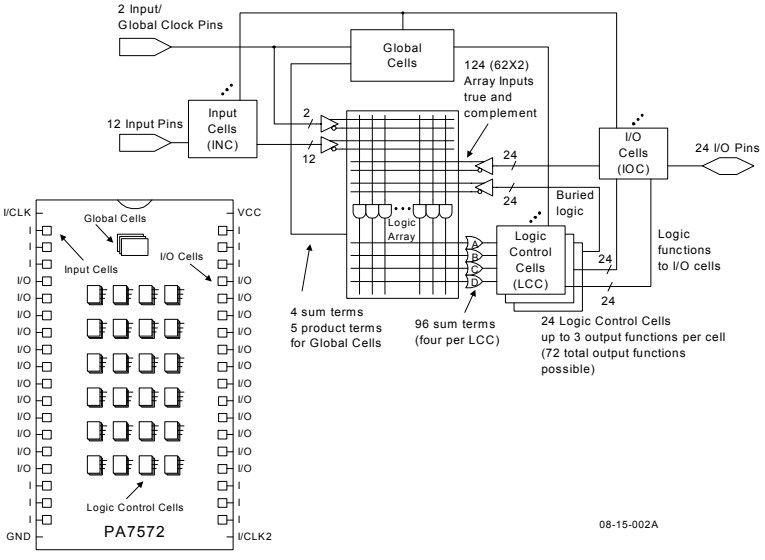


Figure 2. Block Diagram



Inside the Logic Array

The heart of the PEEL™ Array architecture is based on a logic array structure similar to that of a PLA (programmable AND, programmable OR). The logic array implements all logic functions and provides interconnection and control of the cells. In the PA7572 PEEL™ Array, 62 inputs are available into the array from the I/O cells, inputs cells and input/global-clock pins.

All inputs provide both true and complement signals, which can be programmed to any product term in the array. The PA7572 PEEL™ Arrays contains 124 product terms. All product terms (with the exception of certain ones fed to the global cells) can be programmably connected to any of the sum-terms of the logic control cells (four sum-terms per logic control cell). Product-terms and sum-terms are also routed to the global cells for control purposes. Figure 3 shows a detailed view of the logic array structure.

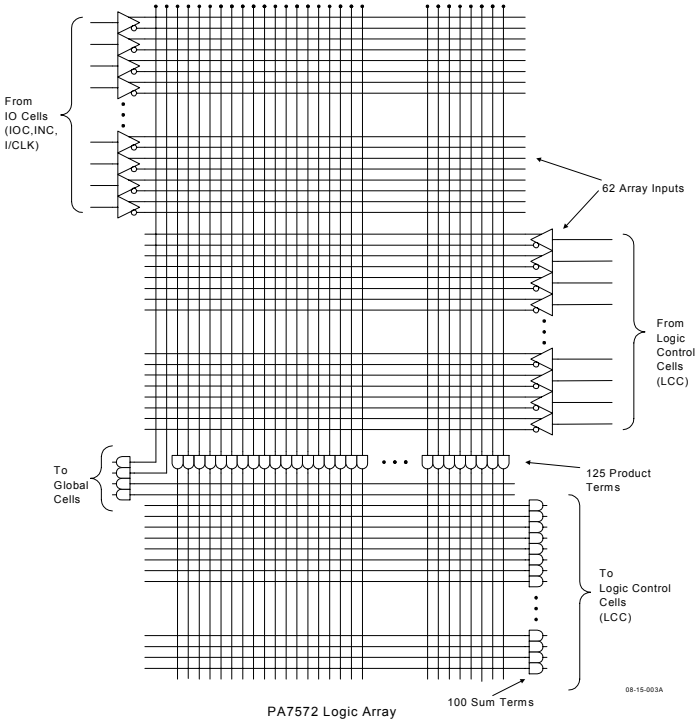


Figure 3. PA7572 Logic Array

True Product-Term Sharing

The PEEL™ logic array provides several advantages over common PLD logic arrays. First, it allows for true product-term sharing, not simply product-term steering, as commonly found in other CPLDs. Product term sharing ensures that product-terms are used where they are needed and not left unutilized or duplicated. Secondly, the sum-of-products functions provided to the logic cells can be used for clocks, resets, presets and output enables instead of just simple product-term control.

The PEEL™ logic array can also implement logic functions with many product terms within a single-level delay. For example a 16-bit comparator needs 32 shared product terms to implement 16 exclusive-OR functions. The PEEL™ logic array easily handles this in a single level delay. Other PLDs/CPLDs either run out of product-terms or require expanders or additional logic levels that often slow performance and skew timing.

Logic Control Cell (LCC)

Logic Control Cells (LCC) are used to allocate and control the logic functions created in the logic array. Each LCC has four primary inputs and three outputs. The inputs to each LCC are complete sum-of-product logic functions from the array, which can be used to implement combinatorial and sequential logic functions, and to control LCC registers and I/O cell output enables.

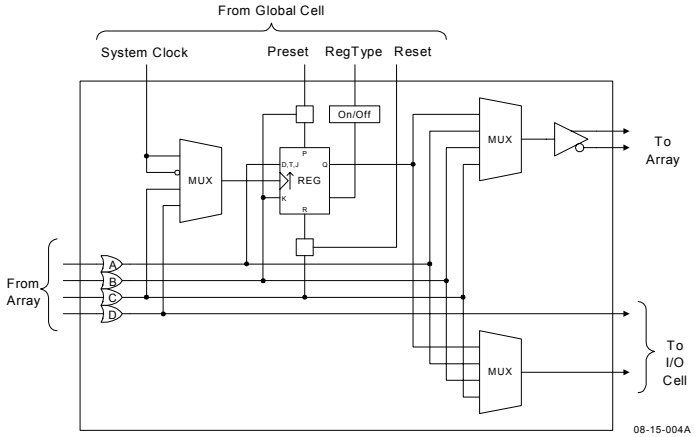


Figure 4. Logic Control Cell Block Diagram

As shown in Figure 4, the LCC is made up of three signal routing multiplexers and a versatile register with synchronous or asynchronous D, T, or JK registers (clocked-SR registers, which are a subset of JK, are also possible). See Figure 5. EEPROM memory cells are used for programming the desired configuration. Four sum-of-product logic functions (SUM terms A, B, C and D) are fed into each LCC from the logic array. Each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
Sum-B = Preset, K or Sum-B
Sum-C = Reset, Clock, Sum-C
Sum-D = Clock, Output Enable, Sum-D

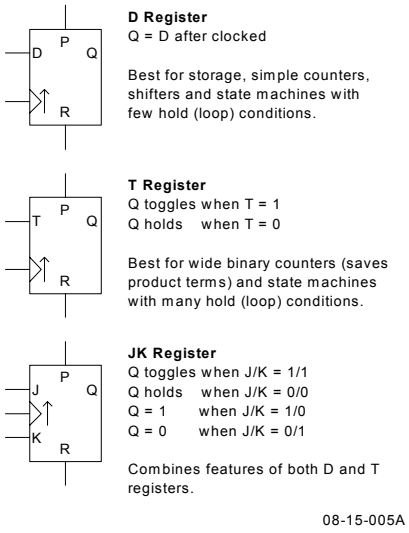


Figure 5. LCC Register Types

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input, or the preset to the register, or a combinatorial path. SUM-C can be the clock, the reset to the register, or a combinatorial path. SUM-D can be the clock to the register, the output enable for the connected I/O cell, or an internal feedback node. Note that the sums controlling clocks, resets, presets and output enables are complete sum-of-product functions, not just product terms as with most other PLDs. This also means that any input or I/O pin can be used as a clock or other control function.

Several signals from the global cell are provided primarily for synchronous (global) register control. The global cell signals are routed to all LCCs. These signals include a high-speed clock of positive or negative polarity, global preset and reset, and a special register-type control that selectively allows dynamic switching of register type. This last feature is especially useful for saving product terms when implementing loadable counters and state machines by dynamically switching from D-type registers to load and T-type registers to count (see Figure 9).

Multiple Outputs Per Logic Cell

An important feature of the logic control cell is its capability to have multiple output functions per cell, each operating independently. As shown in Figure 4, two of the three outputs can select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be registered, one combinatorial and the third, an output enable, or an additional buried logic function. The multi-function PEEL™ Array logic cells are equivalent to two or three macrocells of other PLDs, which have one output per cell. They also allow registers to be truly buried from I/O pins without limiting them to input-only (see Figure 8 & Figure 9).

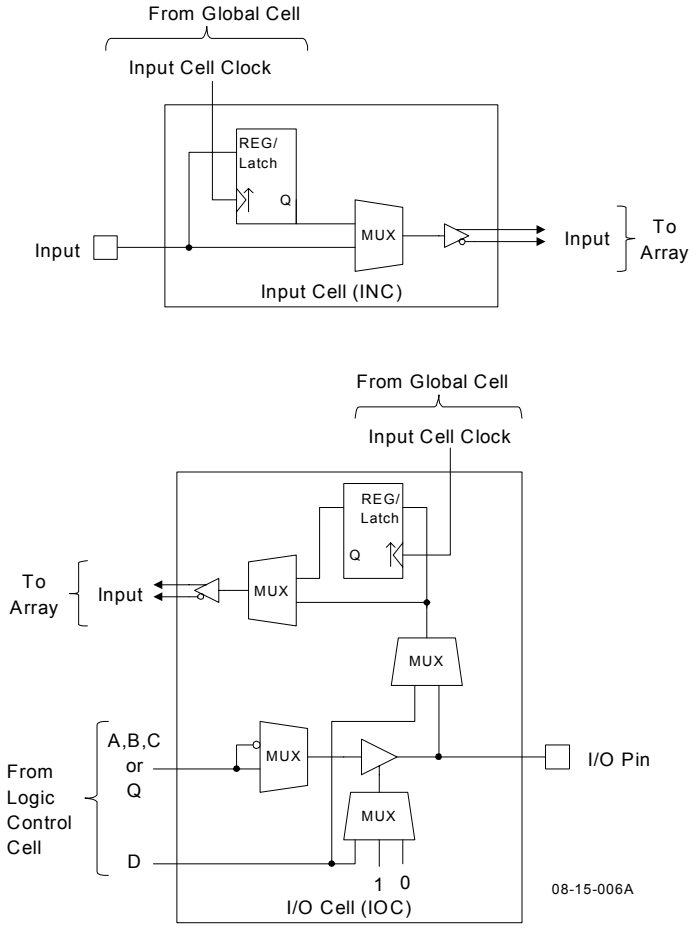


Figure 6. Input and I/O Cell Block Diagrams

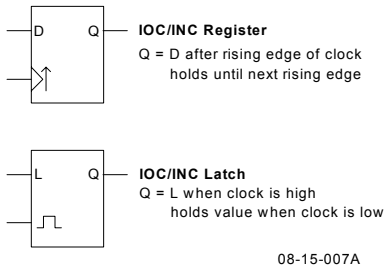


Figure 7. IOC/INC Register Configurations

Input Cells (INC)

Input cells (INC) are included on dedicated input pins. The block diagram of the INC is shown in Figure 6. Each INC consists of a multiplexer and a register/transparent latch, which can be clocked from various sources selected by the global cell (see Figure 7). The register is rising edge clocked. The latch is transparent when the clock is high and latched on the clock's falling edge. The register/ latch can also be bypassed for a non-registered input.

I/O Cell (IOC)

All PEEL™ Arrays have I/O cells (IOC) as shown above in Figure 6. Inputs to the IOCs can be fed from any of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The register/ latch can be clocked from a variety of sources determined by the global cell. It can also be bypassed for a non-registered input. The PA7572 allows the use of SUM-D as a feedback to the array when the I/O pin is a dedicated output. This allows for additional buried registers and logic paths. (See Figure 8 and Figure 9).

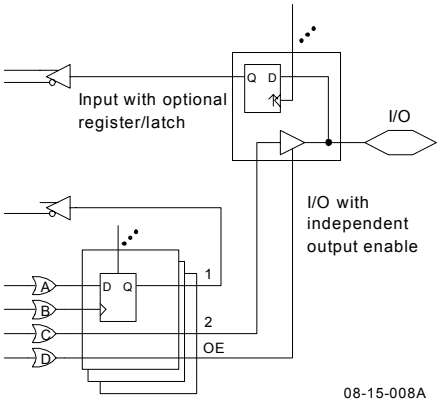


Figure 8. LCC & IOC With Two Outputs

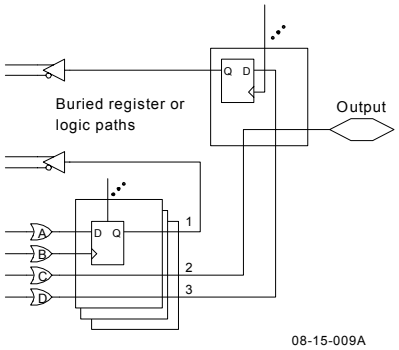


Figure 9. LCC & IOC With Three Outputs

Global Cells

The global cells, shown in Figure 10, are used to direct global clock signals and/or control terms to the LCCs, IOCs and INCs. The global cells allow a clock to be selected from the CLK1 pin, CLK2 pin, or a product term from the logic array (PCLK). They also provide polarity control for INC and IOC clocks enabling rising or falling clock edges for input registers/latches. Note that each individual LCC clock has its own polarity control. The global cell for LCCs includes sum-of-products control terms for global reset and preset, and a fast product term control for LCC register-type, used to save product terms for loadable counters and state machines (see Figure 11). The PA7572 provides two global cells that divide the LCC and IOCs into groups, A and B. Half of the LCCs and IOCs use global cell A, half use global cell B. This means that two high-speed global clocks can be used among the LCCs.

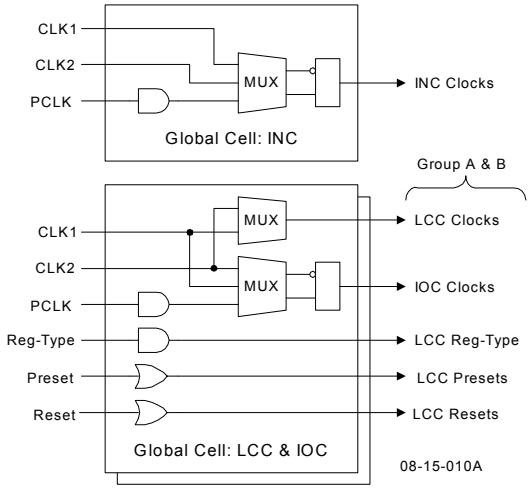


Figure 10. Global Cells

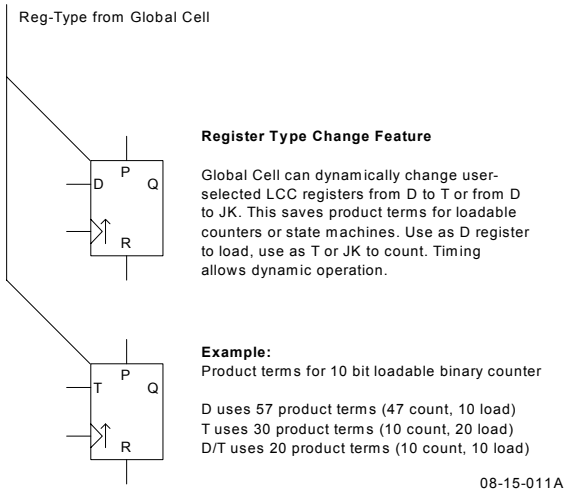


Figure 11. Register Type Change Feature

PEEL™ Array Development Support

Development support for PEEL™ Arrays is provided by Anachip and manufacturers of popular development tools. Anachip offers the powerful PLACE Development Software (free to qualified PLD designers).

The PLACE software includes an architectural editor, logic compiler, waveform simulator, documentation utility and a programmer interface. The PLACE editor graphically illustrates and controls the PEEL™ Array's architecture, making the overall design easy to understand, while allowing the effectiveness of boolean logic equations, state machine design and truth table entry. The PLACE compiler performs logic transformation and reduction, making it possible to specify equations in almost any fashion and fit the most logic possible in every design. PLACE also provides a multi-level logic simulator allowing external and internal signals to be simulated and analyzed via a waveform display.(See Figure 12, Figure 13, Figure 14)

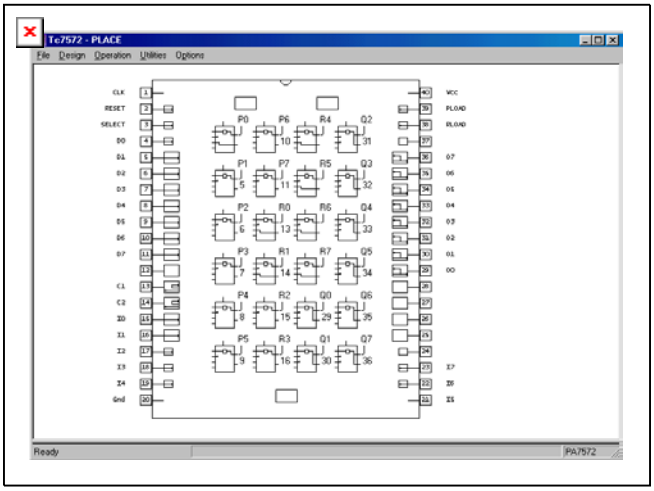


Figure 12. PLACE Architectural Editor

PEEL™ Array development is also supported by popular development tools, such as ABEL and CUPL, via ICT's PEEL™ Array fitters. A special smart translator utility adds the capability to directly convert JEDEC files for other devices into equivalent JEDEC files for pin-compatible PEEL™ Arrays.

Programming

PEEL™ Arrays are EE-reprogrammable in all package types, plastic-DIP, PLCC and SOIC. This makes them an ideal development vehicle for the lab. EE-reprogrammability is also useful for production, allowing unexpected changes to be made quickly and without waste. Programming of PEEL™ Arrays is supported by many popular third party programmers.

Design Security and Signature Word

The PEEL™ Arrays provide a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PEEL™ Arrays cannot be accessed until the entire chip has been electrically erased. Another programming feature, signature word, allows a user-definable code to be programmed into the PEEL™ Array. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed in the device or to record the design revision.

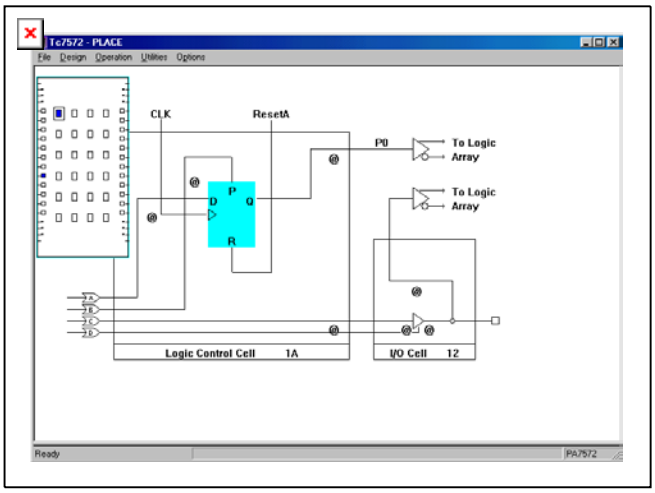


Figure 13. PLACE LCC and IOC Screen

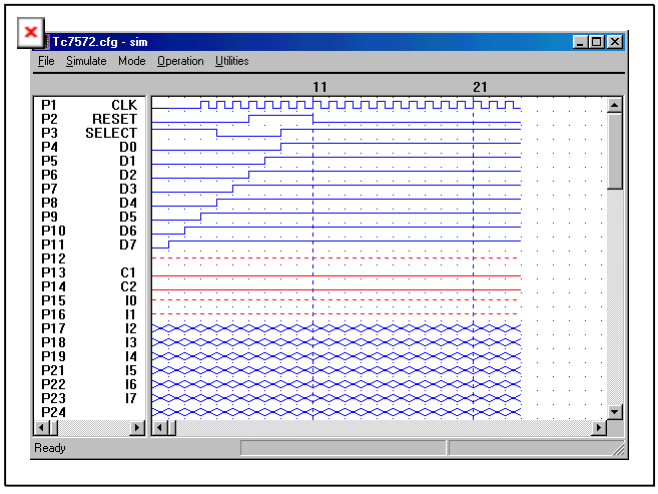


Figure 14. PLACE Simulator Screen

This device has been designed and tested for the specified operating ranges. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to Ground[1]	-0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Table 2. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_R	Clock Rise Time	See Note 2		20	ns
T_F	Clock Fall Time	See Note 2		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 2		250	ms

Table 3. D.C. Electrical Characteristics

Over the Operating Range

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC} = Min, I_{OH} = -10µA		V_{CC} - 0.3		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage - CMOS	V_{CC} = Min, I_{OL} = -10µA			0.15	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			-0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤V_{IN} ≤V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤V_O ≤V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = 5V, V_O = 0.5V, TA= 25°C		-30	-120	mA
I_{CC}[11]	V_{CC} Current	V_{IN} = 0V or V_{CC}[3,11] f = 25MHz All outputs disabled[4]	-20	50 (typ.)[18]	75	mA
			I-20		85	
C_{IN}[7]	Input Capacitance[5]	T_A = 25°C, V_{CC} = 5.0V @ f = 1 MHz			6	pF
C_{OUT}[7]	Output Capacitance[5]				12	pF

Table 4. A.C Electrical Characteristics Combinatorial

Over the Operating Range

Symbol	Parameter[6,12]	-20/I-20		Unit
		Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL} + t_{LC})		13	ns
t_{PDX}	Propagation delay External (t_{IA} + t_{AL} +t_{LC} + t_{LO})		20	ns
t_{IA}	Input or I/O pin to array input		2	ns
t_{AL}	Array input to LCC		12	ns
t_{LC}	LCC input to LCC output[10]		1	ns
t_{LO}	LCC output to output pin		5	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output[7]		5	ns
t_{OX}	Output Disable, Enable from input pin[7]		20	ns

This device has been designed and tested for the recommended operating conditions. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage

Figure 15. Combinatorial Timing - Waveforms and Block Diagram

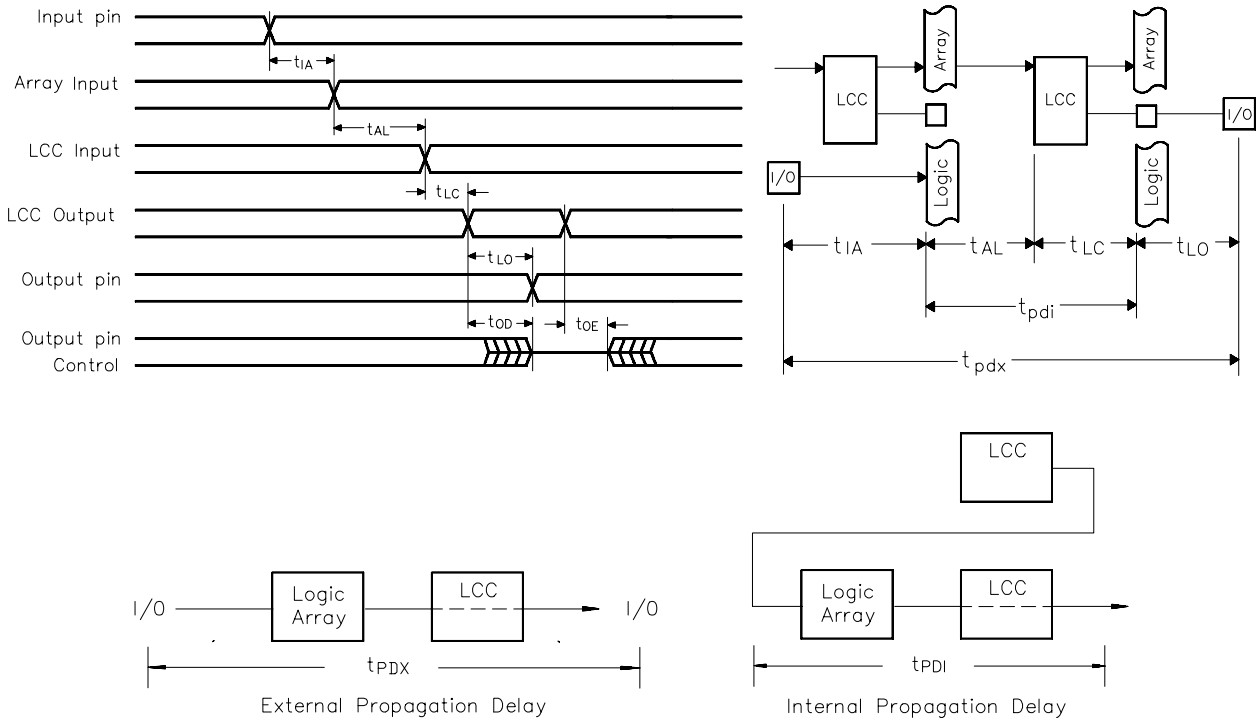
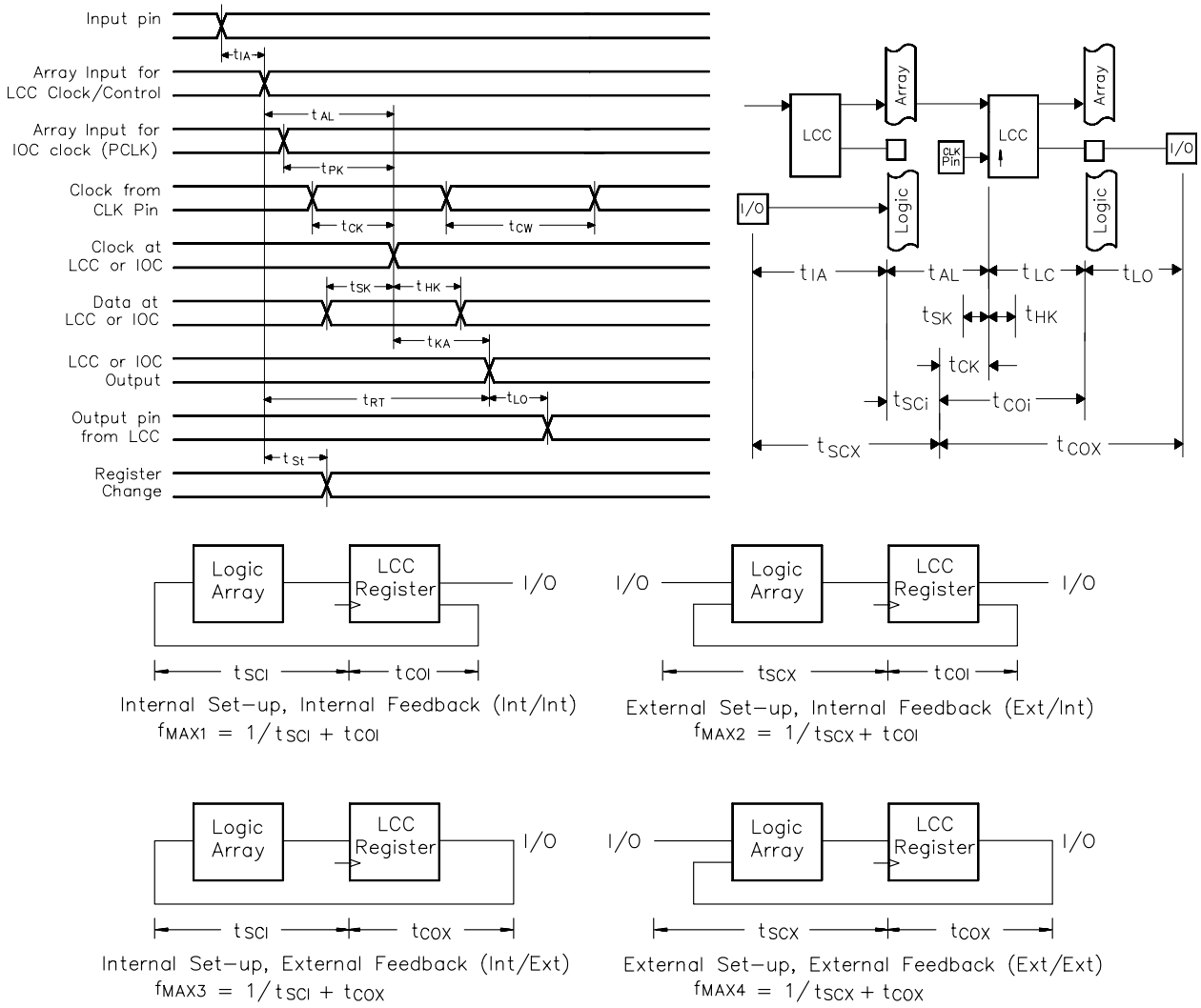


Table 5. A.C. Electrical Characteristics Sequential

Symbol	Parameter[6,1]	-20/I-20		Unit
		Min	Max	
t_{SCI}	Internal set-up to system clock[8] - LCC[14] ($t_{AL} + t_{SK} + t_{LC} - t_{CK}$)	8		ns
t_{SCX}	Input[16] (EXT.) set-up to system clock, - LCC ($t_{IA} + t_{SCI}$)	10		ns
t_{COI}	System-clock to Array Int. - LCC/IOC/INC[14] ($t_{CK} + t_{LC}$)		7	ns
t_{COX}	System-clock to Output Ext. - LCC ($t_{COI} + t_{LO}$)		12	ns
t_{HX}	Input hold time from system clock - LCC	0		ns
t_{SK}	LCC Input set-up to async. clock[13] - LCC	1		ns
t_{AK}	Clock at LCC or IOC - LCC output	1		ns
t_{HK}	LCC input hold time from system clock - LCC	4		ns
t_{SI}	Input set-up to system clock - IOC/INC[14] ($t_{SK} - t_{CK}$)	0		ns
t_{HI}	Input hold time from system clock - IOC/INC ($t_{SK} - t_{CK}$)	5		ns
t_{PK}	Array input to IOC PCLK clock		9	ns
t_{SPI}	Input set-up to PCLK clock[17] - IOC/INC (t_{SK}-t_{PK}-t_{IA})	0		ns
t_{HPI}	Input hold from PCLK clock[17] - IOC/INC (t_{PK}+t_{IA}-t_{SK})	10		ns
t_{SD}	Input set-up to system clock - IOC/INC Sum-D ($t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{CK}$)	10		ns
t_{HD}	Input hold time from system clock - IOC Sum-D	0		ns
t_{SDP}	Input set-up to PCLK clock - IOC Sum-D[15] ($t_{IA} + t_{AL} + t_{LC} + t_{SK} - t_{PK}$)	7		ns
t_{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		ns
t_{CK}	System-clock delay to LCC/IOC/INC		6	ns
t_{CW}	System-clock low or high pulse width	7		ns
f_{MAX1}	Max. system-clock frequency Int/Int $1/(t_{SCI} + t_{COI})$		66.6	MHz
f_{MAX2}	Max. system-clock frequency Ext/Int $1/(t_{SCX} + t_{COI})$		58.8	MHz
f_{MAX3}	Max. system-clock frequency Int/Ext $1/(t_{SCI} + t_{COX})$		50.0	MHz
f_{MAX4}	Max. system-clock frequency Ext/Ext $1/(t_{SCX} + t_{COX})$		45.4	MHz
f_{TGL}	Max. system-clock toggle frequency $1/(t_{CW} + t_{CW})$[9]		71.4	MHz
t_{PR}	LCC presents/reset to LCC output		1	ns
t_{ST}	Input to Global Cell present/reset ($t_{IA} + t_{AL} + t_{PR}$)		15	ns
t_{AW}	Asynch. preset/reset pulse width	8		ns
t_{RT}	Input to LCC Reg-Type (RT)		8	ns
t_{RTV}	LCC Reg-Type to LCC output register change		1	ns
t_{RTC}	Input to Global Cell register-type change ($t_{RT} + t_{RTV}$)		9	ns
t_{RW}	Asynch. Reg-Type pulse width	10		ns
t_{RESET}	Power-on reset time for registers in clear state[2]		5	µs

Figure 16. Sequential Timing – Waveforms and Block Diagram



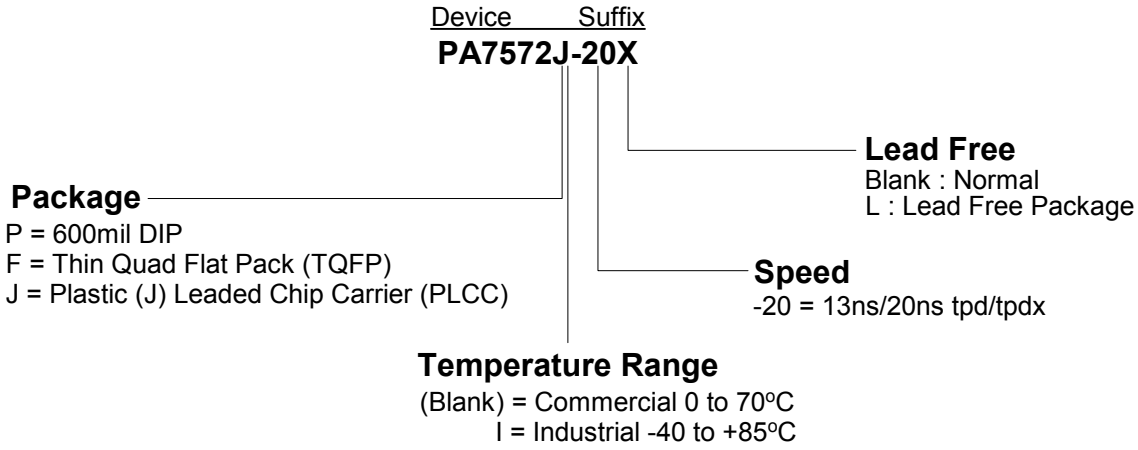
Notes

1. Minimum DC input is -0.5V, however inputs may under-shoot to -2.0V for periods less than 20ns.
2. Test points for Clock and V_{CC} in t_R,t_F,t_{CL},t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
3. I/O pins are 0V or V_{CC}.
4. Test one output at a time for a duration of less than 1 sec.
5. Capacitances are tested on a sample basis.
6. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
7. t_{OE} is measured from input transition to V_{REF} ±0.1V (See test loads at end of Section 6 for V_{REF} value). t_{OD} is measured from input transition to V_{OH} -0.1V or V_{OL} +0.1V.
8. DIP: “System-clock” refers to pin 1/21 high speed clocks. PLCC: “System-clock” refers to pin 2/24 high speed clocks.
9. For T or JK registers in toggle (divide by 2) operation only.
10. For combinatorial and async-clock to LCC output delay.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
12. Test loads are specified in Section 5 of this Data Book.
13. “Async. Clock” refers to the clock from the Sum term (OR gate).
14. The “LCC” term indicates that the timing parameter is applied to the LCC register. The “LCC/IOC” term indicates that the timing parameter is applied to both the LCC and IOC registers. The “LCC/IOC/INC” term indicates that the timing parameter is applied to the LCC, IOC, and INC registers.
15. This refers to the Sum-D gate routed to the IOC register for an additional buried register.
16. The term “input” without any reference to another term refers to an (external) input pin.
17. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} -t_{PK} -t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
18. Typical (typ) ICC is measured at T_A = 25° C, freq = 25MHZ, V_{CC} = 5V

Table 6. Ordering Information

Part Number	Speed	Temperature	Package
PA7572P-20 (L)	13/20ns	C	P40
PA7572F-20 (L)			F44
PA7572J-20 (L)			J44
PA7572PI-20 (L)	13/20ns	I	P40
PA7572FI-20 (L)			F44
PA7572JI-20 (L)			J44

Figure 17. Part Number



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