VGA Port ESD Protection and Termination Network

Features

- Seven channel ESD protection
- ±15 kV ESD protection per channel, connector side (HBM)
- ±8 kV contact, 15 kV air discharge ESD protection per channel, connector side (IEC 61000-4-2 Level 4 standard)
- Low loading capacitance—4.5pF typical
- 16-pin QSOP package

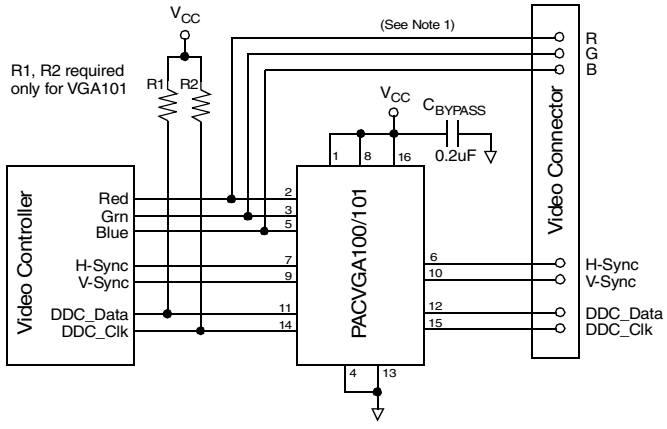
Applications

- ESD protection and termination resistors for VGA (video) port interfaces
- Desktop PCs
- Notebook computers
- LCD monitors

Product Description

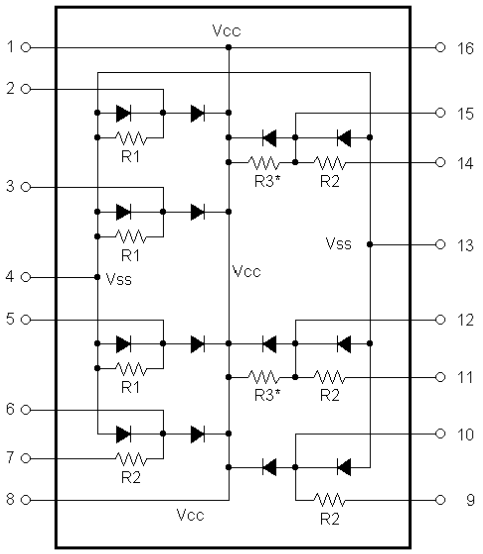
The PACVGA100/101 functions as a transmission line termination and ESD protection device for video applications. It provides 75 ohm parallel terminations for video R, G, and B lines and series terminations for the Horizontal Sync, Vertical Sync and the two DDC lines which serve as Plug and Play logic signals. In addition, all interface lines provide Level 4 ESD protection per the IEC 61000-4-2 contact discharge specification. The PACVGA100 provides internal pull-up resistors (R3) for the two DDC lines whereas the PACVGA101 omits these internal pull-ups so that different pull-up resistor values can be added externally.

Typical Application Circuit



Note 1: For best ESD protection, minimize R/G/B trace lengths between the PACVGA100/101 device and the video connector.

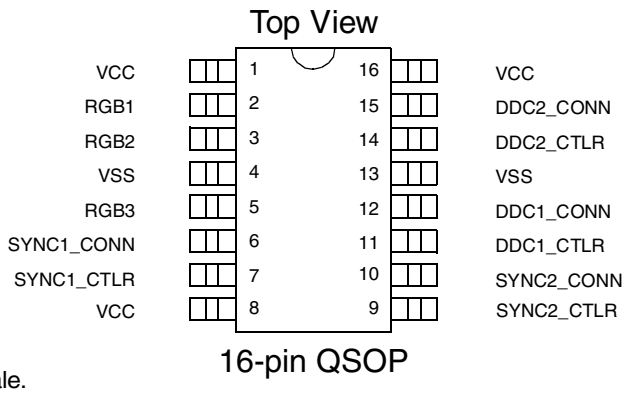
Simplified Electrical Schematic



R1 = 75Ω, R2 = 33Ω
R3 = 2.2KΩ (for PACVGA100 only)

* R3 omitted for PACVGA101

PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD(s)	NAME	DESCRIPTION
1, 8, 16	V_{CC}	Positive voltage supply pins.
2	RGB1	RGB Video Protection Channel 1. Ties to one of the RGB video lines (for example, the Red signal) between the VGA controller device and the video connector.
3	RGB2	RGB Video Protection Channel 2. Ties to one of the RGB video lines (for example, the Blue signal) between the VGA controller device and the video connector.
4, 13	V_{SS}	Ground reference supply pin.
5	RGB3	RGB Video Protection Channel 3. Ties to one of the RGB video lines (for example, the Green signal) between the VGA controller device and the video connector.
6	SYNC1_CONN	Sync Signal Output 1. Ties to the video connector side of one of the sync lines (for example the Horizontal Sync signal).
7	SYNC1_CTLR	Sync Signal Input 1. Connects to the VGA Controller side of one of the sync lines (for example, the Horizontal Sync signal).
9	SYNC2_CTLR	Sync Signal Input 2. Connects to the VGA Controller side of one of the sync lines (for example, the Vertical Sync signal).
10	SYNC2_CONN	Sync Signal Output 2. Connects to the video connector side of one of the sync lines (for example, the Vertical Sync signal).
11	DDC1_CTLR	DDC Signal Input 1. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
12	DDC1_CONN	DDC Signal Output 1. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
14	DDC2_CTLR	DDC Signal Input 2. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Clk).
15	DDC2_CONN	DDC Signal Output 2. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Clk).

Ordering Information

PART NUMBERING INFORMATION			
Pins	**Package**	**Ordering Part Number[1]**	**Part Marking**
16	QSOP	PACVGA100	PACVGA100Q
16	QSOP	PACVGA101	PACVGA101Q

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Supply Voltage (V_{CC} - V_{SS})	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	(V_{SS} - 0.5) to (V_{CC} + 0.5)	V
Package Power Rating	800	mW

Note 1: Only one diode conducting at a time.

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage (V_{CC}- V_{SS}) PACVGA100 PACVGA101	 5.0 3.3 to 5.0	 V V

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS[1]						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TOL_R	Resistor Absolute Tolerance R/G/B Termination Resistor (R1) Series Termination Resistor (R2) DDC Pull-up Resistor (R3)				 ±5 ±5 ±10	 % % %
TCR	Temperature Coefficient of Resistance (TCR)				±200	ppm/°C
V_F	Diode Forward Voltage	I_F = 20mA	0.65		0.95	V
V_{RB}	Diode Reverse Breakdown Voltage Top Diode (Cathode connected to V_{CC}) Bottom Diode (Anode connected to V_{SS})		 17.0 25.0			 V V
I_{LEAK}	Channel Leakage Current			±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance at pins 2, 3, 5, 6, 10, 12 & 15	@ 1 MHz, V_P=5V, V_N=0V, V_{IN}=2.5V; Note 2 applies		4.5	6	pF
V_{ESD}	ESD Protection 1) Peak Discharge Voltage at pins 2, 3, 5, 6 10, 12 & 15, in system a) Human Body Model, MIL-STD-883, Method 3015 b) Contact discharge per IEC 61000-4-2 2) Peak Discharge Voltage at pins 7, 9, 11 & 14 a) Human Body Model, MIL-STD-883, Method 3015	 Note 3 Notes 2,4 Notes 2,5 Note 6 Notes 2,4	 ±15 ±8 ±4			 kV kV kV
V_{CP}	Channel Clamp Voltage at pins 2, 3, 5, 6, 10, 12 & 15 Positive Transients Negative Transients	@15kV ESD HBM; Notes 2 & 4			 V_P + 13.0 V_N - 13.0	 V V

Note 1: All parameters specified at T_A=25°C unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

Note 3: From I/O pins to V_P or V_N only; V_P bypassed to V_N with 0.2µF ceramic capacitor.

Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 5.0V, V_N grounded.

Note 5: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 5.0V, V_N grounded.

Note 6: These pins are not directly connected to the VGA connector and therefore are not subject to direct ESD strikes.

Mechanical Details

QSOP Mechanical Specifications

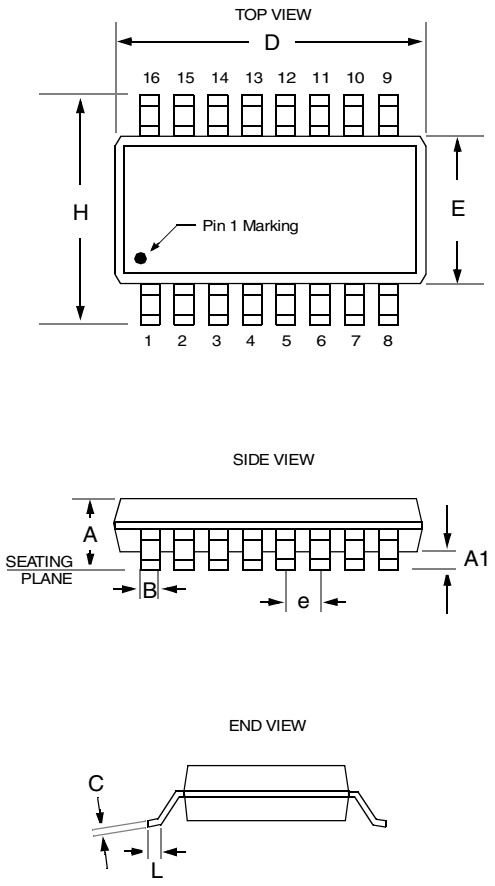
PACVGA100/101 devices are packaged in 16-pin QSOP packages. Dimensions are presented below.

For complete information on the QSOP-16 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	16			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.19	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for QSOP-16