ZL40162



# High Output Current High Speed Dual Operational Amplifier

Data Sheet

April 2003

### Features

- High Output Drive
  - 18.8 Vpp differential output voltage, RL =  $50\Omega$
  - 9.4 Vpp single-ended output voltage, RL =  $25\Omega$
- High Output Current
  - ± 200mA @ Vo = 9.4 Vpp, Vs = 12V
- Low Distortion
  - 83dB SFDR (Spurious Free Dynamic Range) @ 100KHz, Vo = 2Vpp, RL = 25Ω
- High Speed
  - 158MHz 3dB bandwidth (G=2)
- 195V / μs slew rate
- Low Noise
  - 3.8nV / √Hz: input noise voltage
  - 2.7pA /  $\sqrt{Hz}$ : input noise current
- Low supply current: 7mA/amp
- Single-supply operation: 5V to 12V
- High ESD (Electro-Static Discharge) immunity
  - 4kV for Supply and Output pins
- Low differential gain and phase
  - 0.01% and -0.1deg

# Applications

- ADSL PCI modem cards
- xDSL external modem
- Line Driver

### **Ordering Information**

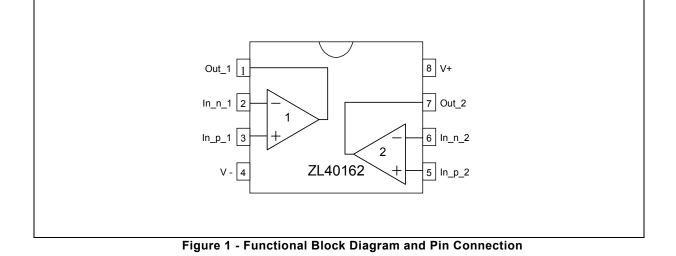
ZL40162/DCA ZL40162/DCB

(tubes) 8 lead SOIC (tape and reel) 8 lead SOIC

#### -40°C to +85°C

### Description

The ZL40162 is a low cost voltage feedback opamp capable of driving signals to within 1V of the power supply rails. It features low noise and low distortion accompanied by a high output current which makes it ideally suited for the application as an xDSL line driver. The dual opamp can be connected as a differential line driver delivering signals up to 18.8Vpp swing into a  $25\Omega$  load, fully supporting the peak upstream power levels for upstream full-rate ADSL (Asymmetrical Digital Subscriber Line).



### **Application Notes**

The ZL40162 is a high speed, high output current, dual operational amplifier with a high slew rate and low distortion. The device uses conventional voltage feedback for ease of use and more flexibility. These characteristics make the ZL40162 ideal for applications where driving low impedances of 25 to  $100\Omega$  such as xDSL and active filters.

The figure below shows a typical ADSL application utilising a 1:2 transformer, the feedback path provides a Gain = +2.

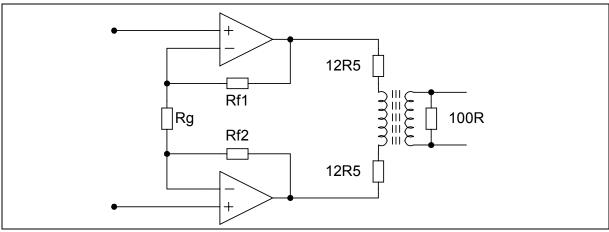


Figure 2 - A Typical ADSL Application

A class AB output stage allows the ZL40162 to deliver high currents to low impedance loads with low distortion while consuming low quiescent current.

# Note: the high ESD immunity figure of 4kV may mean that in some designs fewer additional EMC protection components are needed thus reducing total system costs.

The ZL40162 is not limited to ADSL applications and can be used as a general purpose opamp configured with either inverting or non-inverting feedback. The figure below shows non-inverting feedback arrangement that has typically been used to obtain the data sheet specifications.

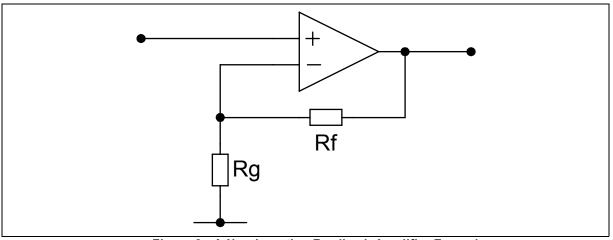


Figure 3 - A Non-Inverting Feedback Amplifier Example

## Absolute Maximum Ratings - (See Note 1)

Parameter	Symbol	Min	Мах	Units
Vin Differential	V <sub>IN</sub>		±1.2	V
Output Short Circuit Protection	V <sub>OS/C</sub>		See Apps Note in this data sheet	
Supply Voltage	V+, V-		±13.2	V
Voltage at Input Pins	V <sub>(+IN)</sub> , V <sub>(-IN)</sub>	(V-) -0.8	(V+) +0.8	V
Voltage at Output Pins	V <sub>O</sub>		±5.5	V
ESD Protection (HBM Human Body Model) (See Note 2)		4	(Note 3)	kV
Storage Temperature		-55	+150	°C
Latch-up test		+/-100mA for 100ms	(Note 4)	
Supply transient test		20% pulse for 100ms	(Note 5)	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.
Note 3: 1.25kV between the pairs of +INA, -INA and +INB, -INB pins only. 4kV between supply pins, OUTA or OUTB pins and any input here.

input pin. +/-100mA applied to input and output pins to force the device to go into "latch-up". The device passes this test to JEDEC spec Note 4: 17

Note 5: Positive and Negative supply transient testing increases the supplies by 20% for 100ms.

# **Operating Ratings - (See Note 1)**

Parameter	Symbol	Min	Max	Units
Supply Voltage	V+, V-	± 2.5	±6.5	V
Junction Temperature Range		-40	150	°C
Junction to Ambient Resistance	Rth(j-a)	150		°C 4 layer FR5 board
Junction to Case Resistance	Rth(j-c)	60		°C 4 layer FR5 board

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

# **Electrical Characteristics -** TA = 25°C, G = +2, Vs = $\pm$ 6V, Rf = Rg = 510 $\Omega$ , RL = 100 $\Omega$ / 2pF; Unless otherwise specified

Symbol	Parameter	Conditions	Min (Note 1)	Typ (Note 2)	Max (Note 3)	Units	Test Type
Dynamic	Performance	L	1	1	1	1	
	-3dB Bandwidth	Vo = 200mVp-p		158		MHz	С
	-0.1dB Bandwidth	Vo = 200mVp-p		17		MHz	С
	Slew Rate	4V Step O/P, 10-90%		195		V/µs	С
	Rise and Fall Time	4V Step O/P, 10-90%		16.4		ns	С
	Rise and Fall Time	200mV Step O/P, 10-90%		2.4		ns	С
	Differential Gain	NTSC, RL = 150Ω		0.01		%	С
	Differential Phase	NTSC, RL = 150Ω		-0.1		deg	С
Distortio	n and Noise Respons	Se					
	2 <sup>nd</sup> Harmonic Distortion	Vo = 8.4Vpp, f =100KHz,RL= 25Ω/2pF		-65.4		dBc	С
		Vo = 8.4Vpp, f =1MHz,RL = 100Ω/2pF		-80.8		dBc	С
		Vo = 2Vpp, f =100kHz,RL= 25Ω/2pF		-93.1		dBc	С
		Vo = 2Vpp, f =1MHz,RL =100Ω/2pF		-85.5		dBc	С
	3 <sup>rd</sup> Harmonic Distortion	Vo = 8.4Vpp, f =100KHz,RL=25Ω/2pF		-69.9		dBc	С
		Vo = 8.4Vpp, f =1MHz,RL =100Ω/2pF		-74.8		dBc	С
		Vo = 2Vpp, f =100KHz,RL=25Ω/2pF		-82.7		dBc	С
		Vo = 2Vpp, f =1MHz,RL=100Ω/2pF		-71.8		dBc	С
MTPR	Multi-Tone Power	47.4375 KHz		-76		dBc	С
	Ratio	69 KHz		-74.5		dBc	С
		90.5625 KHz		-72		dBc	С
		112.125 KHz		-70		dBc	С
	Input Noise Voltage	f = 100KHz		3.8		nV/√Hz	С
	Input Noise Current	f = 100KHz		2.7		pA/√Hz	С
Input Ch	aracteristics	I	1	1	1	1	1
Vos	Input Offset Voltage	Tj = -40°C to 150°C	- 4.2	- 0.3	4.2	mV	Α

Symbol	Parameter	Conditions	Min (Note 1)	Typ (Note 2)	Max (Note 3)	Units	Test Type
lb	Input Bias Current	Tj = -40°C to 150°C		-10	-20	μA	А
los	Input Offset Current	Tj = -40°C to 150°C	-2	-0.2	2	μA	А
CMVR	Common Mode Voltage Range	Tj = -40°C to 150°C	- 4.9		4.9	V	A
CMRR	Common Mode Rejection Ratio	Tj = -40°C to 150°C	70	79		dB	A
Transfer	Characteristics						
Avol	Voltage Gain	RL = 1k, Tj = -40°C to 150°C	4.7	10		V/mV	A
		RL = 25Ω, Tj = -40°C to 150°C	1.6	5.5			A
	Output Swing	RL = 25Ω, Tj = -40°C to 150°C	- 4.5	± 4.7	4.5	V	A
	Output Swing	RL = 1k, Tj = -40°C to 150°C	- 5	± 5.1	5	V	A
lsc	Output Current (Note 3)	Vo = 0, Tj = -40°C to 150°C	570	1000		mA	В
Power S	upply			1			
ls	Supply Current / Amp	Tj = -40°C to 150°C		7	9	mA	A
PSRR	Power Supply Rejection Ratio	Tj = -40°C to 150°C	73	81		dB	A

Note 1: The maximum power dissipation is a function of Tj(max),  $\theta$ JA and TA. The maximum allowable power dissipation at any ambient temperature is PD = (Tj(max) - TA)/ $\theta$ JA. All numbers apply for packages soldered directly onto a PC board.

Note 2: Typical values represent the most likely parametric norm.

Note 3:

Test Types: a. 100% tested at 25°C. Over temperature limits are set by characterisation or simulation. b. Limits set by characterisation or simulation. c. Typical value only for information.

 $\pm$  2.5V Electrical Characteristics - TA = 25°C, G = +2, Vs =  $\pm$  2.5V, Rf = Rg = 510 $\Omega$ , RL = 100 $\Omega$  / 2pF; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 1)	Typ (Note 2)	Max (Note 3)	Units	Test Type
Dynamic	Performance						
	-3dB Bandwidth			152.5		MHz	С
	-0.1dB Bandwidth			19		MHz	С
	Slew Rate	1V Step O/P, 10-90%		171		V/µs	С
	Rise and Fall Time	1V Step O/P, 10-90%		4.67		ns	С
	Rise and Fall Time	200mV Step O/P, 10-90%		2.15		ns	С
Distortio	n and Noise Respons	e					
	2 <sup>nd</sup> Harmonic Distortion	Vo = 2Vpp,f = 100KHz, RL = 25Ω		-92.5		dBc	С
		Vo = 2Vpp, f = 1MHz, RL = 100Ω		-85.4		dBc	С
	3 <sup>rd</sup> Harmonic Distortion	Vo = 2Vpp, f = 100KHz, RL = $25\Omega$		-84.4		dBc	С
		Vo = 2Vpp, f = 1MHz, RL = 100Ω		-72.7		dBc	С
Input Cha	aracteristics		•				
Vos	Input Offset Voltage	Tj = -40°C to 150°C	- 4.2	- 0.3	4.2	mV	В
lb	Input Bias Current	Tj = -40°C to 150°C		- 10	-20	μA	В
CMVR	Common Mode Voltage Range		-1.55		1.55	V	В
CMRR	Common Mode Rejection Ratio	Tj = -40°C to 150°C	70	80		dB	В
Transfer	Characteristics		•				
Avol	Voltage Gain	RL = 1k, Tj = -40°C to 150°C	5.5	10.7		V/mV	В
		RL = 25Ω, Tj = -40°C to 150°C	1.6	6			В
Output C	haracteristics	1		1	<u> </u>		1
	Output Swing	RL = 25Ω, Tj = -40°C to 150°C	-1.4	±1.48	1.4	V	В
		RL = 1k, Tj = -40°C to 150°C	-1.6	±1.65	1.6		В

Symbol	Parameter	Conditions	Min (Note 1)	<b>Typ</b> (Note 2)	Max (Note 3)	Units	Test Type
Power Su	upply						
ls	Supply Current/Amp	Tj = -40°C to 150°C		6.75	8.5	mA	A
PSRR	Power Supply Rejection Ratio	Tj = -40°C to 150°C	73	83		dB	В

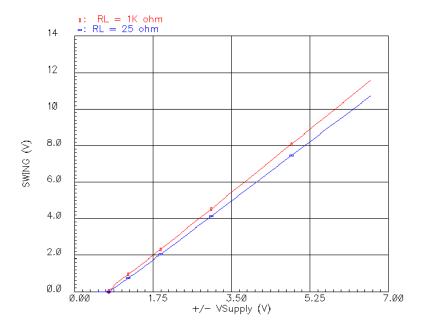
The maximum power dissipation is a function of Tj(max),  $\theta$ JA and TA. The maximum allowable power dissipation at any ambient temperature is PD = (Tj(max) - TA)/ $\theta$ JA. All numbers apply for packages soldered directly onto a PC board. Note 1:

Note 2: Typical values represent the most likely parametric norm.

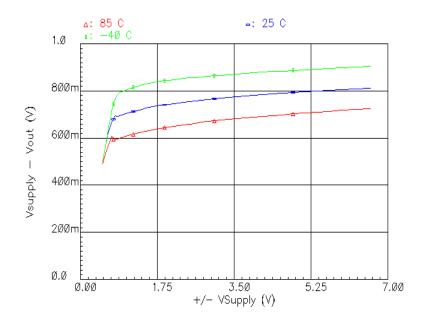
Note 3: Test Types: a. 100% tested at 25°C. Over temperature limits are set by characterisation or simulation. b. Limits set by characterisation or simulation.

c. Typical value only for information.

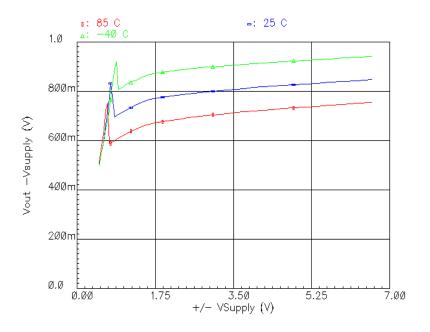
#### **Output Swing**



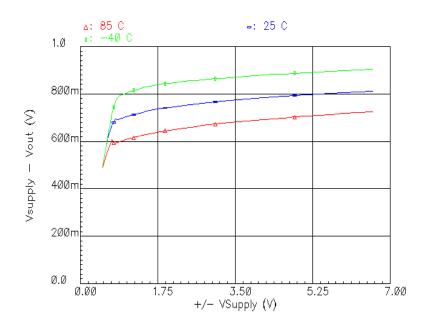
#### Positive Output Swing into $1 \mbox{k} \Omega$



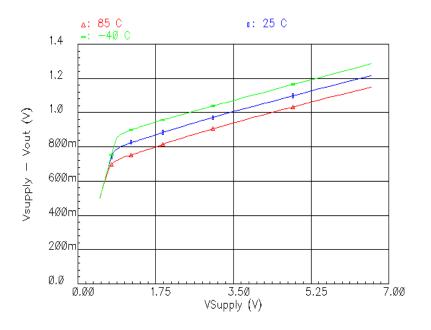
#### Negative Output Swing into 1k $\!\Omega$



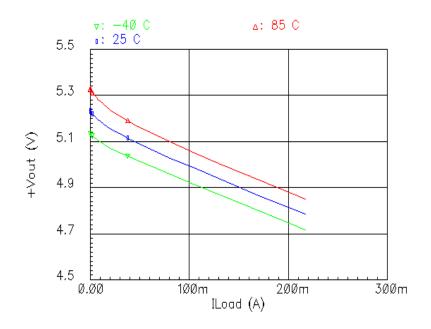
#### Positive Output Swing into $\mathbf{25}\Omega$



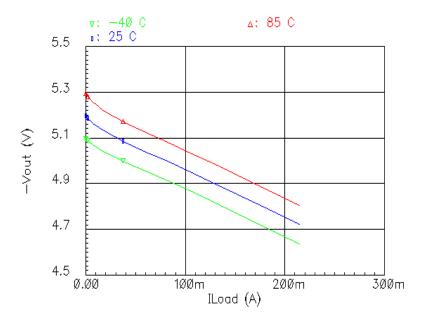
#### Negative Output Swing into $\mathbf{25}\Omega$



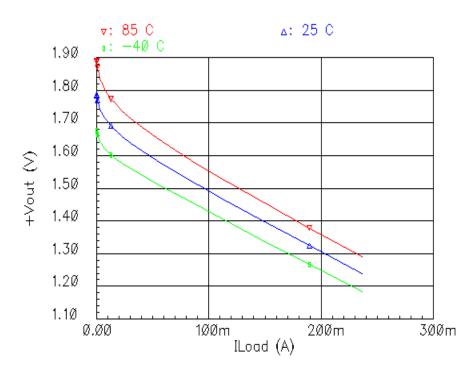
+Vout VS Iload



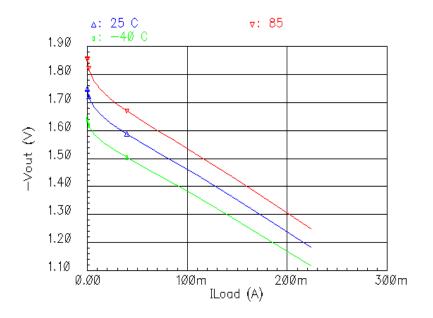
#### -Vout VS ILoad



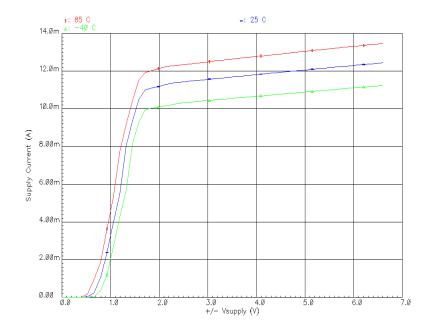


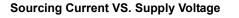


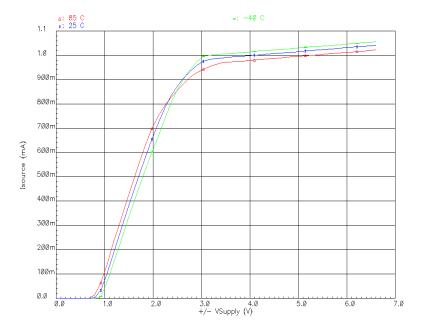
#### -Vout VS ILoad, Vs = ±2.5V



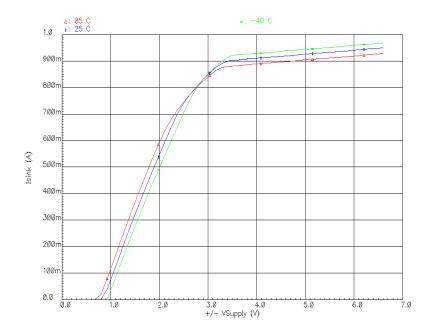
Supply Current VS. Supply Voltage



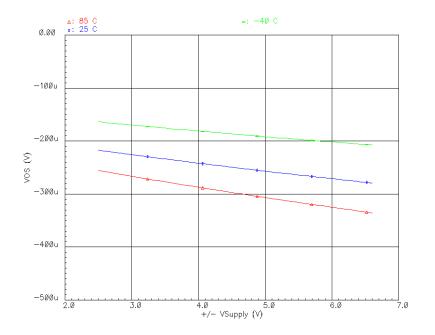




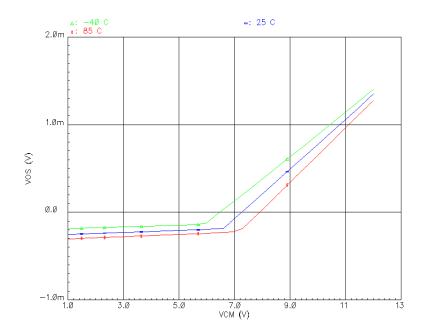
Sinking Current VS. Supply Voltage



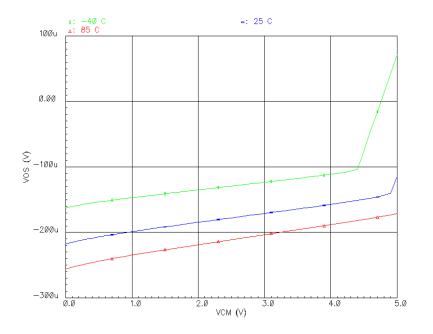
#### Vos VS. Vs



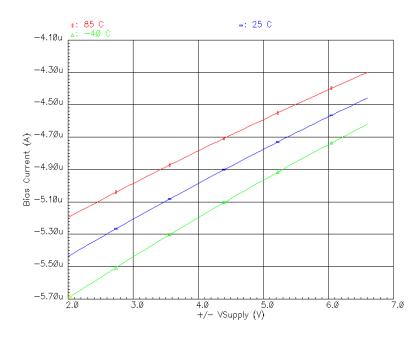
#### Vos VS. Vcm



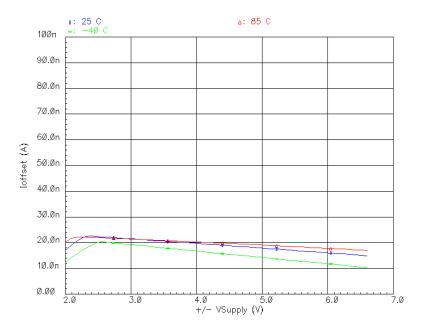
#### Vos VS. Vcm, Vs = ±2.5V



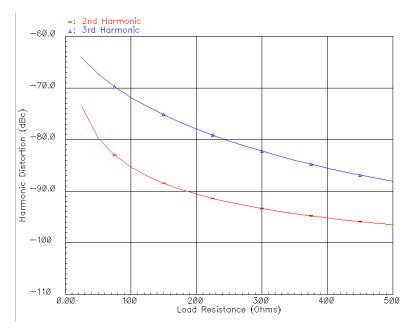
#### **Bias Current VS. Vsupply**

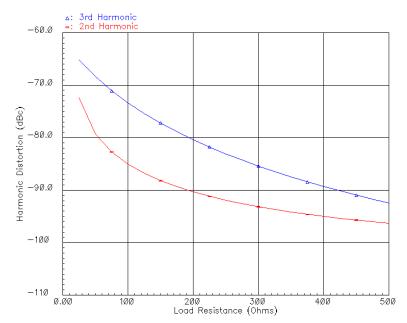


#### **Offset Current VS. Vsupply**



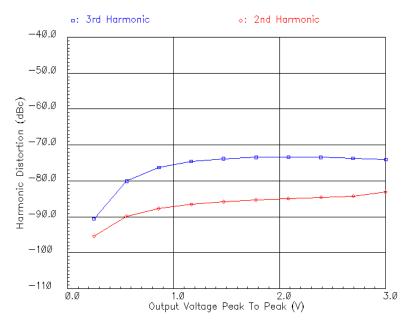
Harmonic Distortion VS. Load F = 1MHZ Vout = 2Vpp



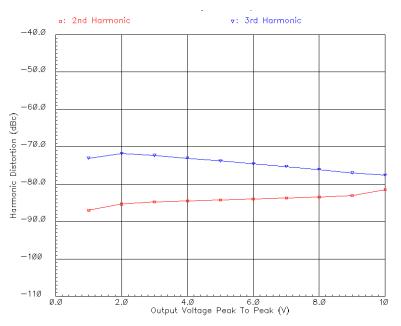


Harmonic Distortion VS. Load Vs = ±2.5V, F = 1MHz, Vout = 2Vpp

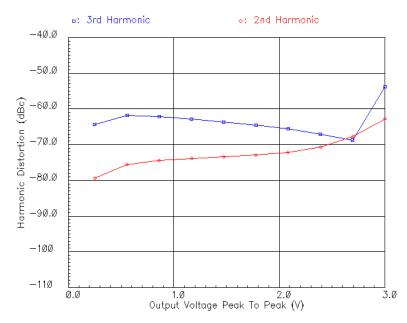
#### Harmonic Distortion VS. Output Voltage Vs = ±2.5V, F = 1MHz



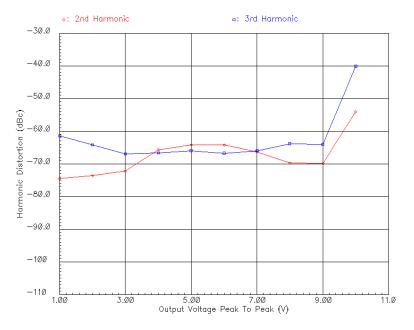




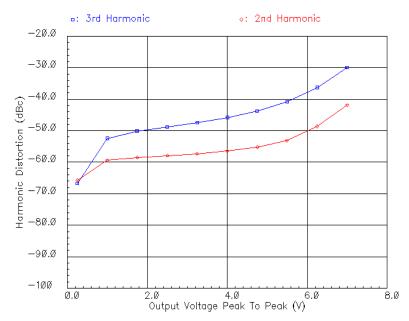
# Harmonic Distortion VS. Output Voltage Vs = $\pm 2.5V$ , F = 1MHz, RL = $25\Omega$



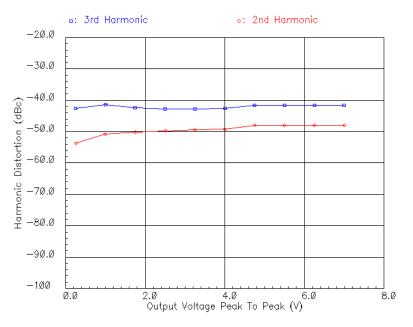
Harmonic Distortion VS. Output Voltage F = 1MHz, RL = 25 $\Omega$ 



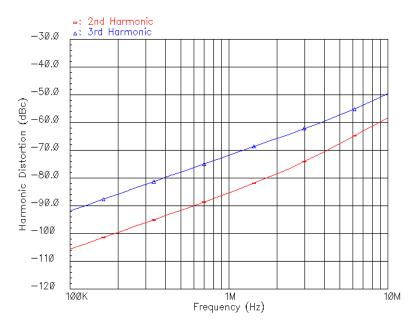
Harmonic Distortion VS. Output Voltage F = 10MHz

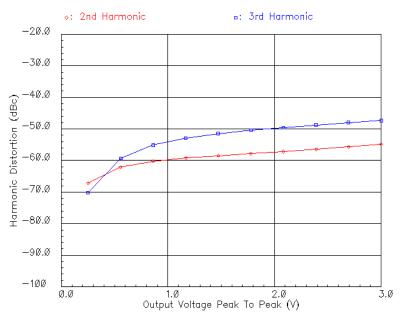


Harmonic Distortion VS. Output Voltage F = 10MHz, RL = 25 $\Omega$ 



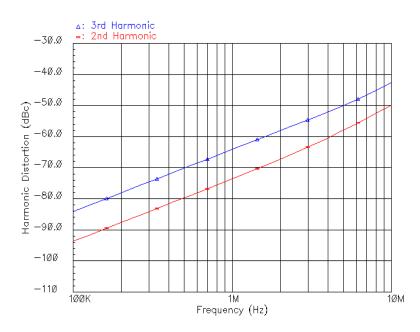
Harmonic Distortion VS. Frequency Vout = 2Vpp

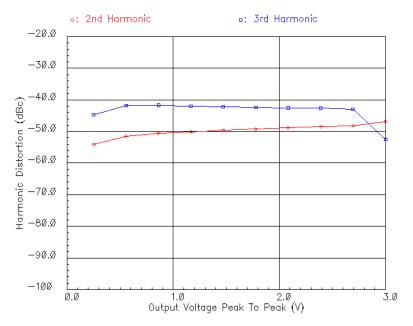




#### Harmonic Distortion VS. Output Voltage Vs =±2.5V, F = 10MHz

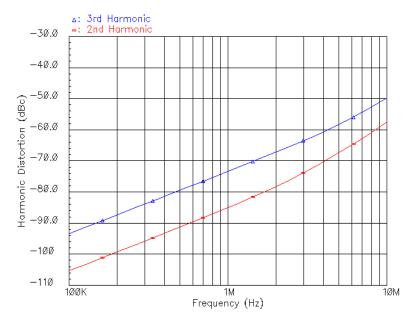
Harmonic Distortion VS. Frequency Vout = 2Vpp, RL =  $25\Omega$ 

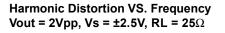


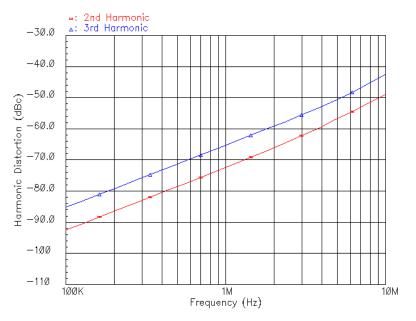


# Harmonic Distortion VS. Output Voltage Vs =±2.5V, F = 10MHz, RL = 25 $\Omega$

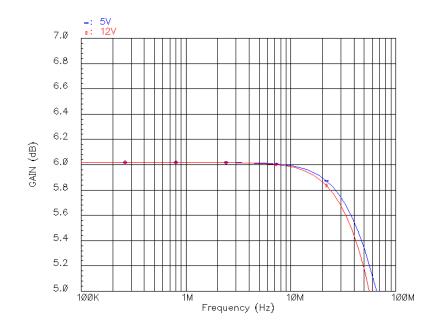
Harmonic Distortion VS. Frequency Vout = 2Vpp, Vs =±2.5V



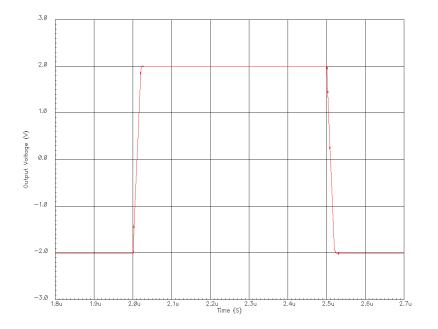




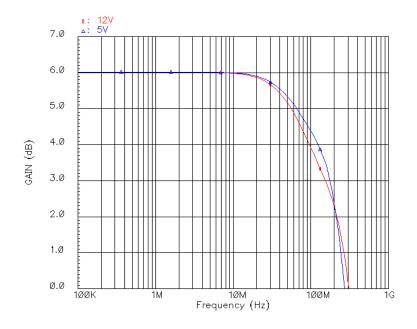
#### **Frequency Response**



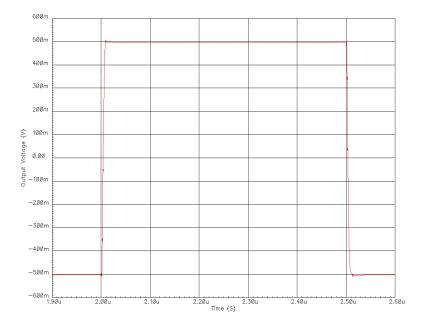
#### **Pulse Response**



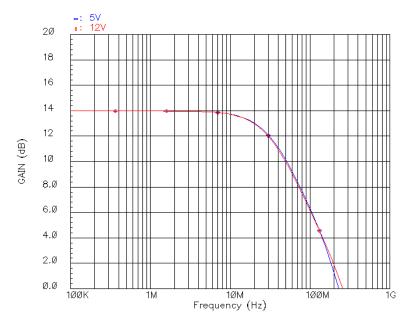
#### **Frequency Response**



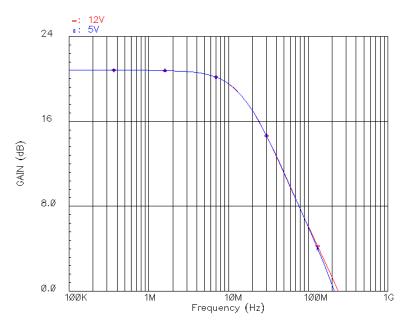
#### Pulse Response, Vs = ±2.5V



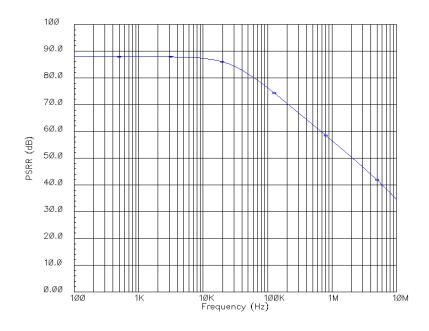
#### Frequency Response Gain = +5



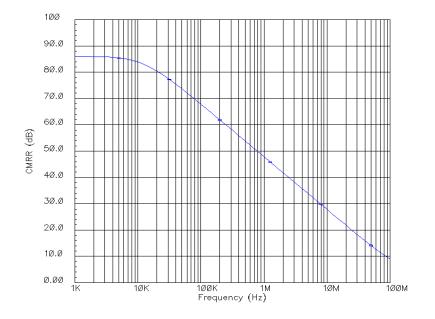
#### Frequency Response Gain = +10

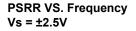


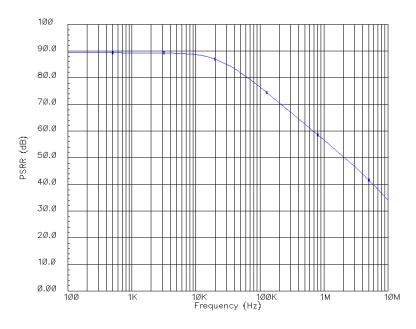
#### **PSRR VS. Frequency**



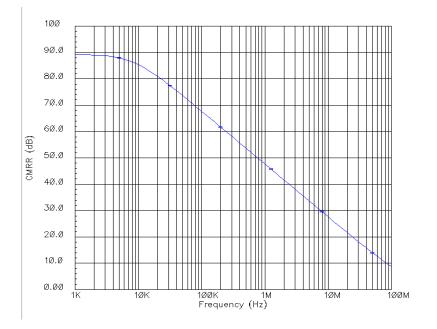
#### **CMRR VS. Frequency**

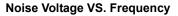


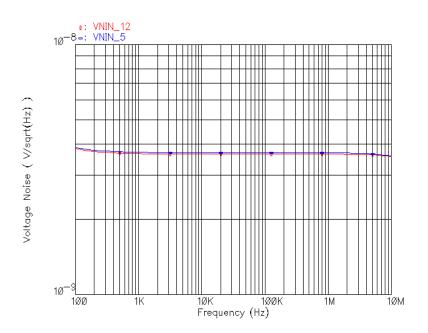




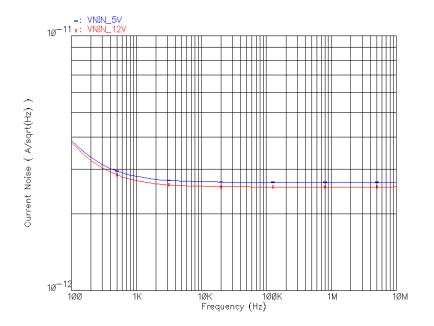
#### CMRR VS. Frequency Vs = ±2.5V

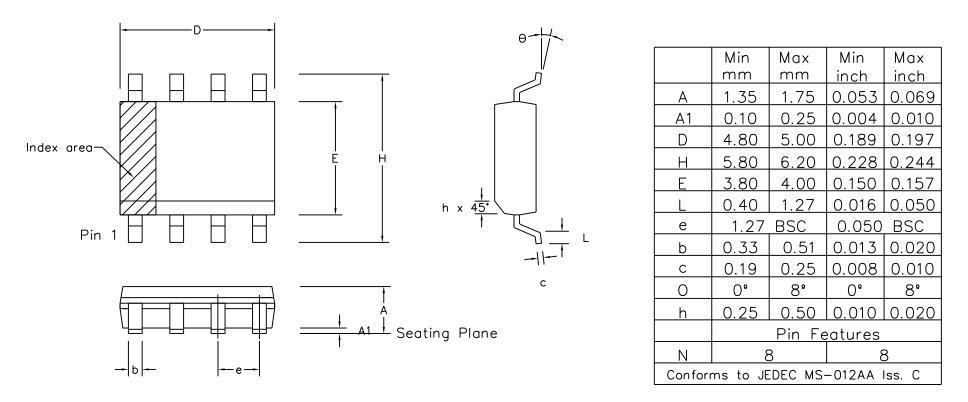






#### **Current Noise VS. Frequency**





#### Notes:

- 1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
- 2. Controlling dimensions are in inches.
- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
- 4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
- 5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	4	5		Previous package codes	Package Outline for
ACN	6745	201936	202595	203705	212424	SEMICONDUCTOR	MP/S	8 lead SOIC (0.150" Body width)
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02			
APPRD.								GPD00010



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