FM4005

Integrated Processor Companion

Features

High Integration Device Replaces Multiple Parts

- Real-time Clock (RTC)
- Low Voltage Reset
- Watchdog Timer
- Early Power-Fail Warning/NMI
- Two 16-bit Event Counters
- Serial Number with Write-lock for Security

Real-Time Clock/Calendar

- Backup Current under 1 µA
- Seconds through Centuries in BCD format
- Tracks Leap Years through 2099
- Uses Standard 32.768 kHz Crystal (6pF)
- Software Calibration
- Calibration Data is Nonvolatile
- Programmed Settings are Nonvolatile
- Supports Battery or Capacitor Backup

Processor Companion

- Active-low Reset Output for V_{DD} and Watchdog
- Programmable Low V_{DD} Reset Thresholds
- Manual Reset Filtered and Debounced
- Programmable Watchdog Timer
- Dual Battery-backed Event Counter Tracks System Intrusions or other Events
- Comparator for Early Power-Fail Interrupt
- 64-bit Programmable Serial Number with Lock

Fast Two-wire Serial Interface

- Up to 1 MHz Maximum Bus Frequency
- Supports Legacy Timing for 100 kHz & 400 kHz

Easy to Use Configurations

- Operates from 2.7 to 5.5V
- Small Footprint 14-pin SOIC (-S)
  - "Green" 14-pin SOIC (-G)
- Low Operating Current
- -40°C to +85°C Operation

Description

The FM4005 is an integrated device that includes the most commonly needed functions for processor-based systems. Major features include real-time clock, low-V_{DD} reset, watchdog timer, battery-backed event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or other purpose. The family operates from 2.7 to 5.5V.

The real-time clock (RTC) provides time and date information in BCD format. It can be permanently powered from external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low VDD condition or a watchdog timeout. /RST goes active when VDD drops below a programmable threshold and remains active for 100 ms after VDD rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A general-purpose comparator compares an external input pin to the onboard 1.2V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The device also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers a dual battery-backed event counter that tracks the number of rising or falling edges detected on dedicated input pins.

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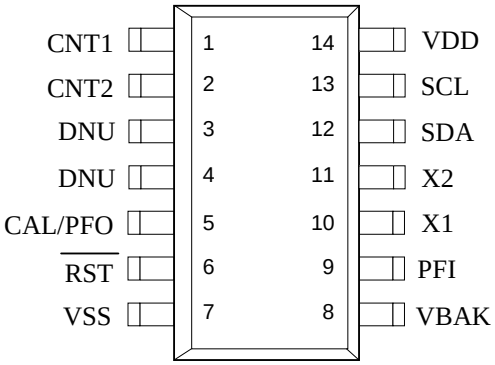
Pin Configuration



Pin Name	Function
CNT1, CNT2	Battery-backed Counter Inputs
CAL/PFO	Clock Calibration and Early Power-fail Output
/RST	Reset Input/Output
PFI	Early Power-fail Input
X1, X2	Crystal Connections
SDA	Serial Data
SCL	Serial Clock
DNU	Do Not Use
VBAK	Battery-Backup Supply
VDD	Supply Voltage
VSS	Ground

Ordering Information			
Base Configuration	Operating Voltage	Reset Threshold	Ordering Part Number
FM4005	2.7-5.5V	2.6V, 2.9, 3.9, 4.4V	FM4005-S
			FM4005-G

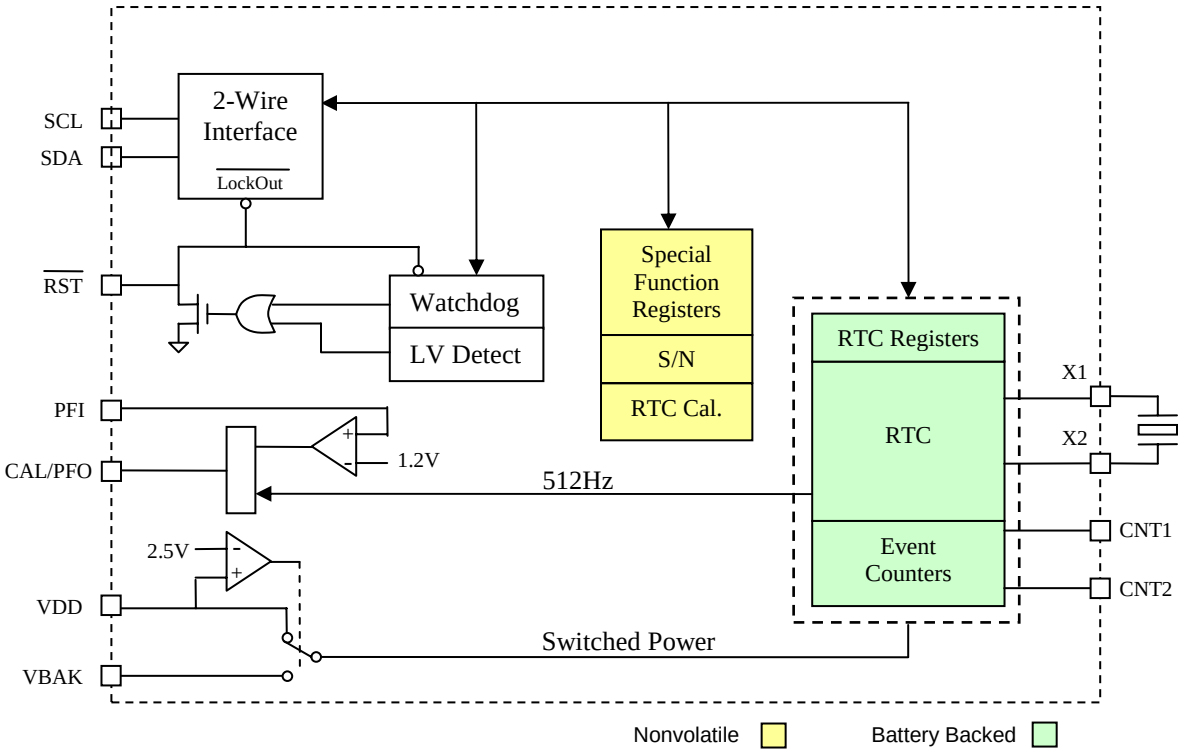


Figure 1. Block Diagram

Pin Descriptions

Pin Name	Type	Pin Description
CNT1, CNT2	Input	Event Counter Inputs: These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable.
CAL/PFO	Output	In calibration mode, this pin supplies a 512 Hz square-wave output for clock calibration. In normal operation, this is the early power-fail output.
X1, X2	I/O	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and leave X2 floating.
/RST	I/O	Active low reset output with weak pull-up. Also input for manual reset.
SDA	I/O	Serial Data & Address: This is a bi-directional line for the two-wire interface. It is open-drain and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. A pull-up resistor is required.
SCL	Input	Serial Clock: The serial clock line for the two-wire interface. Data is clocked out of the part on the falling edge, and in on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
PFI	Input	Early Power-fail Input: Typically connected to an unregulated power supply to detect an early power failure. This pin should not be left floating.
DNU	-	Do Not Use: This pin must be left floating.
VBAK	Supply	Backup supply voltage: A 3V battery or a large value capacitor. If V_{DD}<3.6V and no backup supply is used, this pin should be tied to V_{DD}. If V_{DD}>3.6V and no backup supply is used, this pin should be left floating and the VBC bit should be set.
VDD	Supply	Supply Voltage.
VSS	Supply	Ground

Overview

The FM4005 combines a real-time clock (RTC) and a processor companion. The companion is a highly integrated peripheral that includes a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM4005 integrates these functions that share a common interface in a single package.

The real-time clock and supervisor functions are accessed with a standard 2-wire device ID. The clock and supervisor functions are controlled by 25 special function registers. Some of these functions such as the RTC and event counter circuits are maintained by the power source on the VBAK pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below an internally set threshold. Each functional block is described below.

Processor Supervisor

Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM4005 has a reset pin (/RST) to drive the processor reset input during power faults (and power-up) and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the /RST pin. When V_{DD} is above the programmed trip point, /RST output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}) the /RST pin will be driven low. It will remain low until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, /RST will continue to drive low for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the /RST pin will return to the weak high state. While /RST is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. Any register read or write operation started while V_{DD} is above V_{TP} will be completed internally.

The bits VTP1 and VTP0 control the trip point of the low voltage detect circuit. They are located in register 0Bh, bits 1 and 0. Figure 2 illustrates the reset operation in response to the V_{DD} voltage.

VTP	VTP1	VTP0
2.6V	0	0
2.9V	0	1
3.9V	1	0
4.4V	1	1

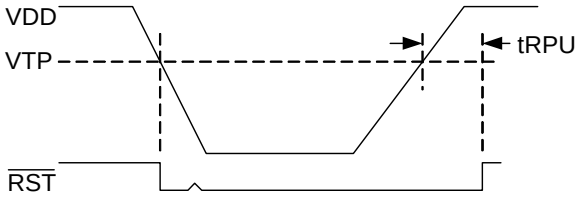


Figure 2. Low VDD Reset

The watchdog timer can also be used to assert the reset signal (/RST). The watchdog is a free running programmable timer. The period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must timeout in order to drive /RST active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If not enabled, the watchdog timer runs but has no effect on /RST. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4-0, the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when VDD is below VTP. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog timeout	WDT4.0	0Ah, D4-0
Watchdog enable	WDE	0Ah, D7
Watchdog restart	WR3-0	09h, D3-0

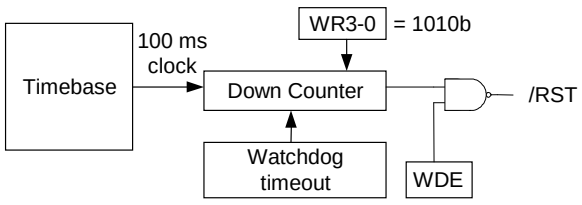


Figure 3. Watchdog Timer

Manual Reset

The /RST pin is bi-directional and allows the FM4005 to filter and de-bounce a manual reset switch. The /RST input detects an external low condition and responds by driving the /RST signal low for 100 ms. Note that an internal weak pull-up on /RST eliminates the need for additional external components.

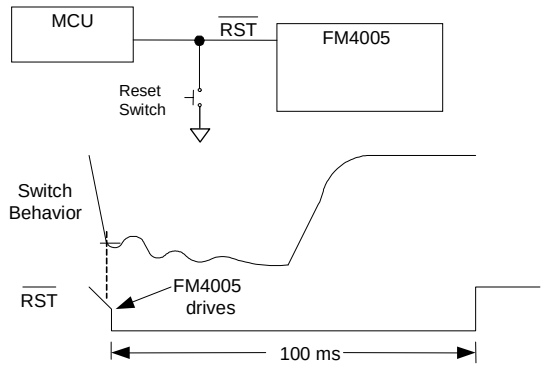


Figure 4. Manual Reset

Reset Flags

In case of a reset condition, a flag will be set to indicate the source of the reset. A low V_{DD} reset or manual reset is indicated by the POR flag, register 09h bit 6. A watchdog reset is indicated by the WTR flag, register 09h bit 7. Note that the bits are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below. The voltage on the PFI input pin is compared to an onboard 1.2V reference. When the PFI input voltage drops below this threshold, the comparator will drive the CAL/PFO pin to a low state. The comparator has 350 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

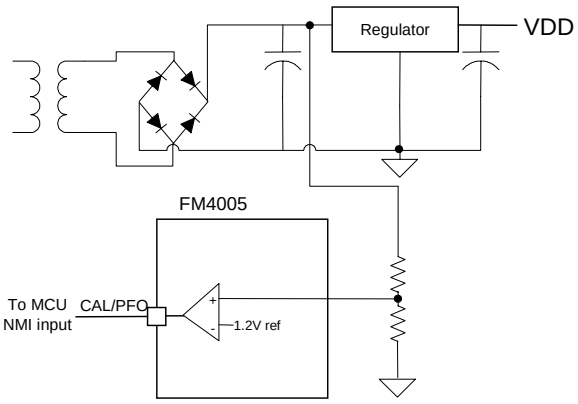


Figure 5. Comparator as a Power-fail Warning

The comparator is a general purpose device and its application is not limited to the NMI function.

The comparator is not integrated into the special function registers except as it shares its output pin with the CAL output. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the CAL/PFO output pin will be driven with a 512 Hz square wave and the comparator will be ignored. Since most users only invoke the calibration mode during production, this should have no impact on system operations using the comparator.

Note: The maximum voltage on the comparator input PFI is limited to 3.75V under normal operating conditions.

Event Counter

The FM4005 offers the user two battery-backed event counters. The input pins CNT1 and CNT2 are programmable edge detectors. Each controls a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1 is located in registers 0Dh and 0Eh. Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime VDD is above VTP, and they will be incremented as long as a valid VBAK power source is provided. To read, set the RC bit register 0Ch bit 3 to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode.

The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0;

Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC bit 3.

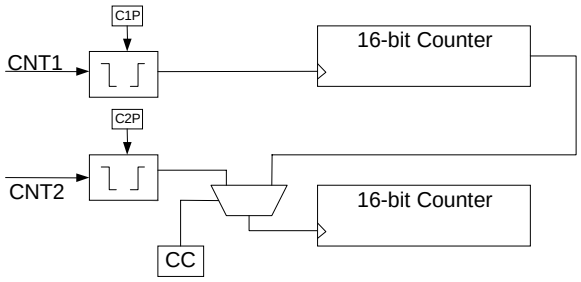


Figure 6. Event Counter

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile register that can be locked by the user once the serial number is set. The serial number registers can be written an unlimited number of times. *However once the lock bit is set the values cannot be altered and the lock cannot be removed.* Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL, register 0Bh, bit 7. Setting the SNL bit to a 1 disables writes to the serial number registers, and *the SNL bit cannot be cleared.*

Real-time Clock Operation

The real-time clock (RTC) is a timekeeping device that can be battery or capacitor backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram (Figure 7) illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h described below. Changing the R bit from 0 to 1 transfers timekeeping information from the core into holding registers that can be read by the user. If a timekeeper update is pending while R is set, then the core will be updated prior to loading the user registers. The registers are frozen and will not be updated again until the R bit is cleared to 0. R is used for reading the time.

Setting the W bit to 1 locks the user registers. Clearing it to 0 causes the values in the user registers to be loaded into the timekeeper core. W is used for writing new time values. Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the VDD pin will drop. When VDD drops below 2.5V, the RTC (and event counters) will switch to the backup power supply on VBAK. The clock uses very little current which maximizes battery or capacitor life.

When a battery is used as a backup source, V_{DD} must be applied prior to inserting the battery to prevent battery drain. Once V_{DD} is applied and a battery is inserted, the current drain on the battery is guaranteed to be less than I_{BAK}(max).

Trickle Charger

To facilitate capacitor backup the VBAK pin can optionally provide a trickle charge current. When the VBC bit, register 0Bh bit 2, is set to 1 the VBAK pin will source approximately 15 µA until VBAK reaches VDD or 3.75V whichever is less. In 3V systems, this charges the capacitor to VDD without an external diode and resistor charger. In 5V systems, it provides the same convenience and also prevents the user from exceeding the VBAK maximum voltage specification.

Note: systems using lithium batteries should clear the VBC bit to 0 to prevent battery charging. The VBAK circuitry includes an internal 1 KΩ series resistor as a safety element.

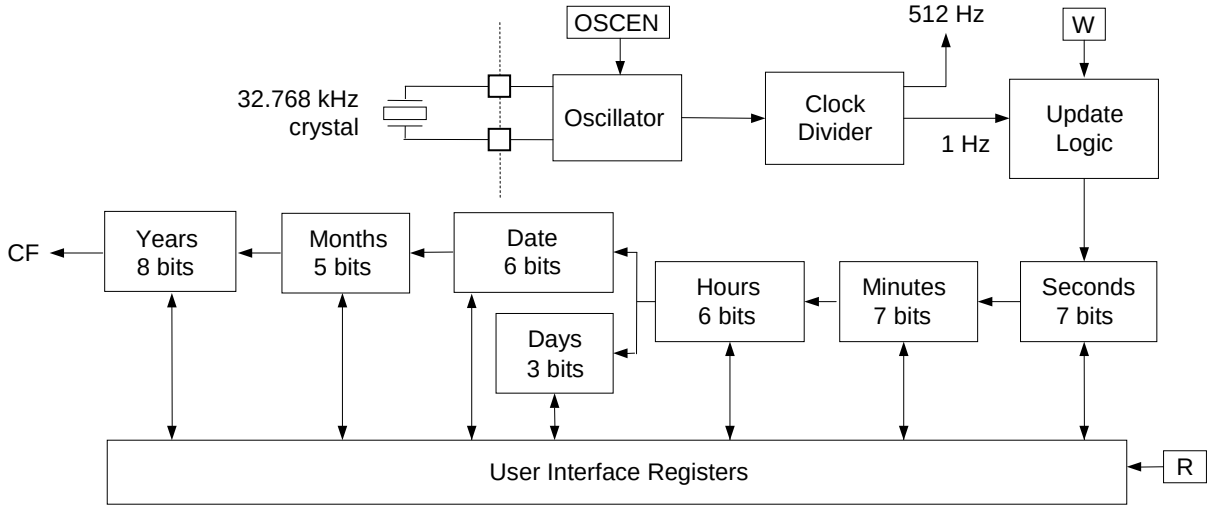


Figure 7. Real-Time Clock Core Block Diagram

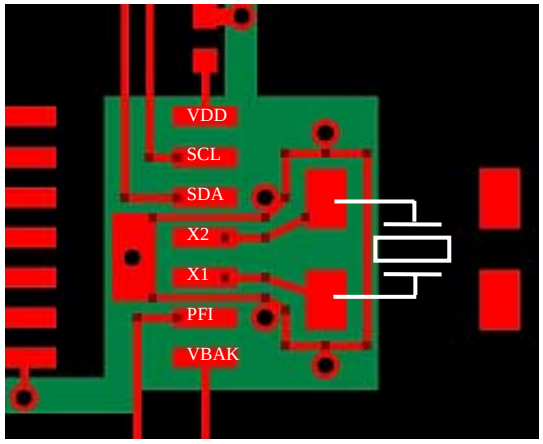
Calibration

When the CAL bit in register 00h is set to 1, the clock enters calibration mode. In calibration mode, the CAL/PFO output pin is dedicated to the calibration function and the comparator output is temporarily unavailable. Calibration operates by applying a digital correction to the counter based on the frequency error. In this mode, the CAL/PFO pin is driven with a 512 Hz (nominal) square wave. Any measured deviation from 512 Hz translates into a timekeeping error. The user converts the measured error in ppm and writes the appropriate correction value to the calibration register. The correction factors are listed in the table below. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to 1, where as negative ppm adjustments have CALS = 0. After calibration, the clock will have a maximum error of ± 2.17 ppm or ± 0.09 minutes per month at the calibrated temperature.

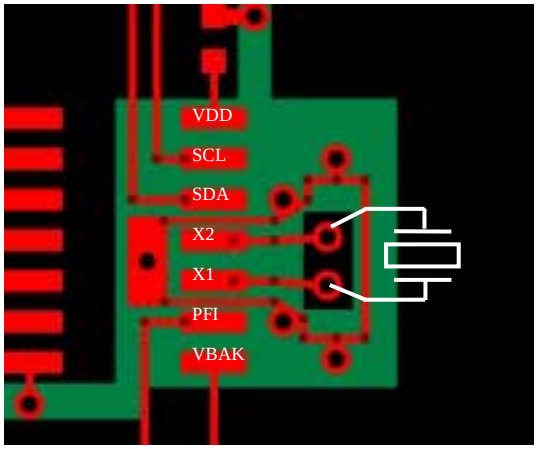
The calibration setting is stored in a nonvolatile register so is not lost should the backup source fail. It is accessed with bits CAL.4-0 in register 01h. This value only can be written when the CAL bit is set to a 1. To exit the calibration mode, the user must clear the CAL bit to a 0. When the CAL bit is 0, the CAL/PFO pin will revert to the comparator output function.

Layout Requirements

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring must be placed around these pads and the guard ring grounded. SDA and SCL traces should be routed away from the X1/X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve +/- 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Negative Calibration for fast clocks: Calibration will achieve +/- 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 25 special function registers. The interface protocol is described below. The registers contain timekeeping data, control bits, or information flags. A description of each register follows the summary table below.

Register Map Summary Table

Nonvolatile = ☐ Battery-backed = ☐

Address	Data D7	D6	D5	D4	D3	D2	D1	D0	Function	Range
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch					RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	-	-	WP1	WP0	VBC	VTP1	VTP0	Companion Control	
0Ah	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	-	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
08h	10 years				years				Years	00-99
07h	0	0	0	10 mo	months				Month	1-12
06h	0	0	10 date		date				Date	1-31
05h	0	0	0	0	0	day			Day	1-7
04h	0	0	10 hours		hours				Hours	0-23
03h	0	10 minutes			minutes				Minutes	0-59
02h	0	10 seconds			seconds				Seconds	0-59
01h	/OSCEN	reserved	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL/Control	
00h	reserved	CF	reserved	reserved	reserved	CAL	W	R	RTC Control	

Note: When the device is first powered up and programmed, all registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers. All other register values should be treated as unknown.

Default Register Values

Address	Hex Value
18h	0x00
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00
12h	0x00
11h	0x00
0Bh	0x00
0Ah	0x1F
01h	0x80

Register Description

Address Description

18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
	Byte 6 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
16h	**Serial Number Byte 5**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC=1. Battery-backed, read/write .							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1 MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							

0Ch	Event Counter Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to 1 takes a snapshot of the four counters bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
CC	Counter Cascade. When CC=0, the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC=1, the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P is not used when CC=1. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = 0, rising edges when C2P = 1. C2P has no effect on counter operation when CC=1. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = 0, rising edges when C1P = 1. Battery-backed, read/write.							

0Bh	Companion Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	SNL	-	-	-	-	VBC	VTP1	VTP0
SNL	Serial Number Lock. Setting to a 1 makes registers 11h to 18h and SNL permanently read-only. **SNL cannot be cleared once set to 1.** Nonvolatile, read/write.							
VBC	VBAK charger control. Setting VBC to 1 causes a 15 µA trickle charge current to be supplied on VBAK. Clearing VBC to 0 disables the charge current. Nonvolatile, read/write.							
VTP1-0	VTP select. These bits control the reset trip point for the low VDD reset function. Nonvolatile, read/write.							

VTP	VTP1	VTP0
2.6V	0	0
2.9V	0	1
3.9V	1	0
4.4V	1	1

0Ah	Watchdog Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0
WDE	Watchdog Enable. When WDE=1 the watchdog timer can cause the /RST signal to go active. When WDE = 0 the timer runs but has no effect on /RST. Note as the timer is free-running, users should restart the timer using WR3-0 prior to setting WDE=1. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.							
WDT4-0	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR3-0. Nonvolatile, read/write.							

Watchdog timeout	WDT4	WDT3	WDT2	WDT1	WDT0
Invalid – default 100 ms	0	0	0	0	0
100 ms	0	0	0	0	1
200 ms	0	0	0	1	0
300 ms	0	0	0	1	1
.					
.					
.					
2000 ms	1	0	1	0	0
2100 ms	1	0	1	0	1
2200 ms	1	0	1	1	0
.					
.					
.					
2900 ms	1	1	1	0	1
3000 ms	1	1	1	1	0
Disable count	1	1	1	1	1

09h	Watchdog Restart & Flags							
	D7	D6	D5	D4	D3	D2	D1	D0
	WTR	POR	LB	-	WR3	WR2	WR1	WR0
WTR	Watchdog Timer Reset Flag: When the /RST signal is activated by the watchdog the WTR bit will be set to 1. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).							
POR	Power-on Reset Flag: When the /RST pin is activated by either $V_{DD} < V_{TP}$ or a manual reset, the POR bit will be							

	set to 1. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
LB	Low Backup Flag: On power up, if the VBAK source is below the minimum voltage to operate the RTC and event counters, this bit will be set to 1. The user should clear it to 0 when initializing the system. Battery-backed. Read/Write (internally set, user can clear bit).
WR3-0	Watchdog Restart: Writing a pattern 1010b to WR3-0 restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR3-0 has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Write-only.

08h **Timekeeping – Years**

D7	D6	D5	D4	D3	D2	D1	D0
10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0

Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99. Battery-backed, read/write.

07h **Timekeeping – Months**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0

Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12. Battery-backed, read/write.

06h **Timekeeping – Date of the month**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0

Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Battery-backed, read/write.

05h **Timekeeping – Day of the week**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Day.2	Day.1	Day.0

Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.

04h **Timekeeping – Hours**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0

Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23. Battery-backed, read/write.

03h **Timekeeping – Minutes**

D7	D6	D5	D4	D3	D2	D1	D0
0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0

Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.

02h **Timekeeping – Seconds**

D7	D6	D5	D4	D3	D2	D1	D0
0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0

Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.

01h **CAL/Control**

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{OSCEN}}$	Reserved	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0

/OSCEN	/Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Disabling the oscillator can save battery power during storage. On a power-up without battery, this bit is set to 1. Battery-backed, read/write.

Reserved	Reserved bits. Do not use. Should remain set to 0.
CALS	Calibration sign. Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. Calibration is explained on page 7. Nonvolatile, read/write.
CAL.4-0	These five bits control the calibration of the clock. Nonvolatile, read/write.

00h	**Flags/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Reserved	CF	Reserved	Reserved	Reserved	CAL	W	R
CF	Century Overflow Flag. This bit is set to a 1 when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to 0 when the Flag register is read. It is read-only for the user. Battery-backed, read/write.							
CAL	Calibration Mode. When set to 1, the clock enters calibration mode. When CAL is set to 0, the clock operates normally, and the CAL/PFO pin is controlled by the comparator. Battery-backed, read/write.							
W	Write Time. Setting the W bit to 1 freezes the clock. The user can then write the timekeeping registers with updated values. Resetting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters and restarts the clock. Battery-backed, read/write.							
R	Read Time. Setting the R bit to 1 copies a static image of the timekeeping core and place it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to 0.							

Two-wire Interface

The FM4005 employs an industry standard two-wire bus that is familiar to many users. Since the FM4005 is a real-time clock and processor companion and not a memory device, it is accessed using a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM4005 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions: Start, Stop, Data bit, and Acknowledge. The figure below illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications.

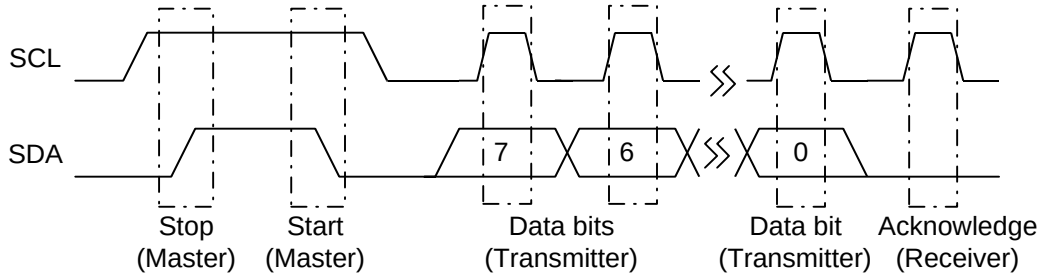


Figure 8. Data Transfer Protocol

Start Condition

A Start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All read and write transactions begin with a Start condition. An operation in progress can be aborted by asserting a Start condition at any time. Aborting an operation using the Start condition will ready the FM4005 for a new operation.

If the power supply drops below the specified VTP during operation, any 2-wire transaction in progress will be aborted and the system must issue a Start condition prior to performing another operation.

Stop Condition

A Stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations must end with a Stop condition.

If an operation is pending when a stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a Stop condition.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high.

Acknowledge

The Acknowledge (ACK) takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter must release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a No-Acknowledge (NACK) and the operation is aborted.

The receiver might NACK for two distinct reasons. First is that a byte transfer fails. In this case, the NACK ends the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not send an ACK to deliberately terminate an operation. For example, during a read operation, the FM4005 will continue to place data onto the bus as long as the receiver sends ACKs (and clocks). When a read operation is complete and no more data is needed, the receiver must NACK the last byte. If the receiver ACKs the last byte, this will cause the FM4005 to attempt to drive the bus on the next clock while the master is sending a new command such as a Stop.

Slave Address

The first byte that the FM4005 expects after a Start condition is the slave address. As shown in Figure 9 below, the slave address contains the Slave ID and a bit that specifies if the transaction is a read or a write.

The FM4005 Companion is accessed by setting bits 7-4 (Slave ID) of the slave address to 1101b.

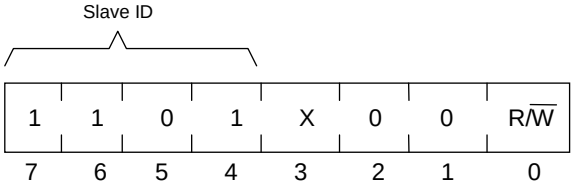


Figure 9. Slave Address

Addressing Overview

The RTC and Processor Companion registers use only one byte of address. Addresses 00h to 18h correspond to special function registers. Attempting to load an address above location 18h is an illegal condition; the FM4005 will return a NACK and abort the 2-wire transaction.

Data Transfer

After the address information has been transmitted, data transfer between the bus master and the FM4005 begins. For a read, the FM4005 will place 8 data bits on the bus then wait for an ACK from the master. If the ACK occurs, the FM4005 will transfer the next byte. If the ACK is not sent, the FM4005 will end the read operation. For a write operation, the FM4005 will accept 8 data bits from the master then send an Acknowledge. All data transfer occurs MSB (most significant bit) first.

Register Write Operation

All register writes begin with a Slave Address, then a register address. The bus master indicates a write operation by setting the slave address LSB to a 0. After addressing, the bus master sends each byte of data to the selected register and the device generates an Acknowledge condition. Any number of sequential bytes may be written. The device internally increments the address for each new data byte. If the end of the address range is reached, the address counter will wrap to 00h. Internally, the actual write operation occurs after the 8th data bit is transferred. It is completed before the Acknowledge is sent. Therefore, if the user desires to abort a write without altering the register contents, this should be done using a Start or Stop condition prior to the 8th data bit. The figures below illustrate a single- and multiple-writes to the RTC registers.

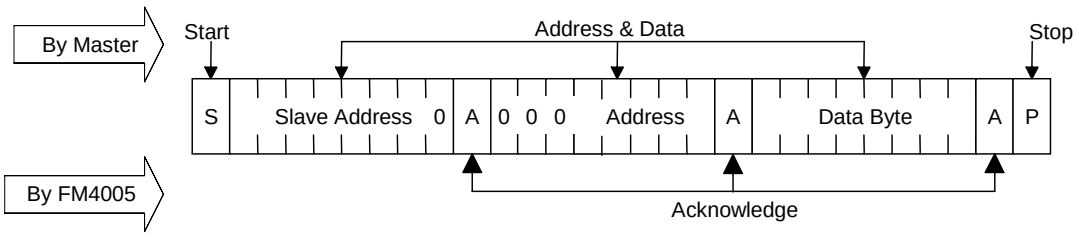


Figure 10. Single Register Write

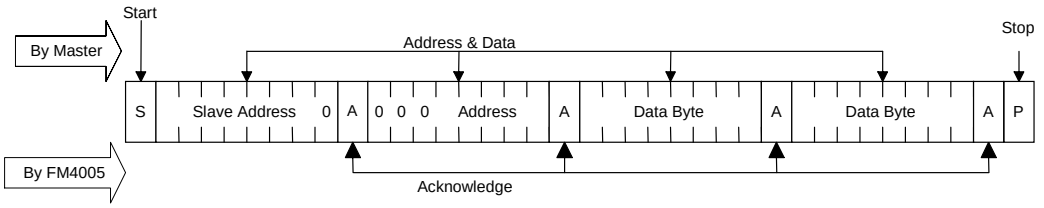


Figure 11. Multiple Register Writes

Register Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM4005 will begin shifting data out from the current register address on the next clock. The address auto-increment feature operates the same for reads as it does for writes.

There are two types of register read operations. They are current address read and selective address read. In a current address read, the FM4005 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to first set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM4005 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete device address, the FM4005 will begin shifting data out from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Each time the bus master acknowledges a byte, this indicates that the FM4005 should read out the next sequential byte.

There are four ways to terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM4005 attempts to read out additional data onto the bus. The four valid methods follow.

1. The bus master issues a NACK in the 9th clock cycle and a Stop in the 10th clock cycle. This is illustrated in the diagrams below and is preferred.
2. The bus master issues a NACK in the 9th clock cycle and a Start in the 10th.
3. The bus master issues a Stop in the 9th clock cycle.
4. The bus master issues a Start in the 9th clock cycle.

If the internal address reaches the top of the address space, it will wrap around to 00h on the next read cycle. The figures below show the proper operation for current address reads.

Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point

for a read operation. This involves using the first two bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address byte that is loaded into the internal address latch. After the FM4005 acknowledges the address, the bus master issues a Start condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a 1. The operation is now a read from the current address. Read operations are illustrated below.

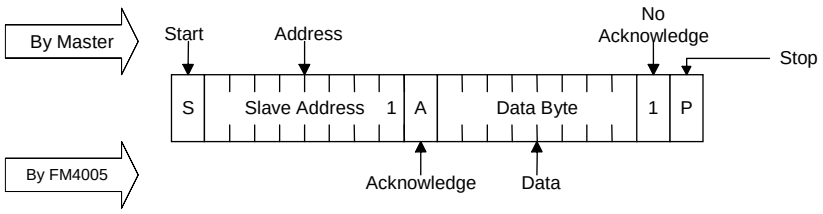


Figure 12. Current Address Register Read

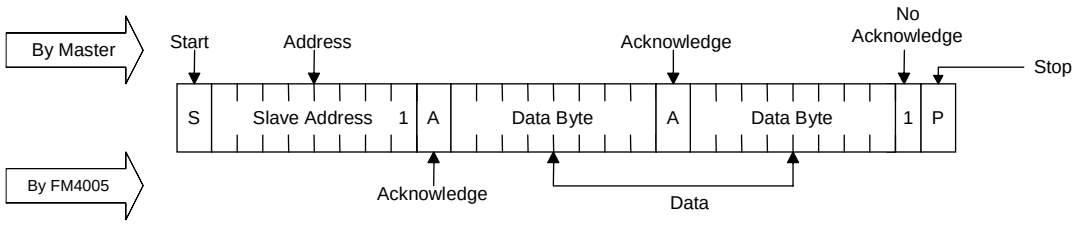


Figure 13. Multiple Register Read

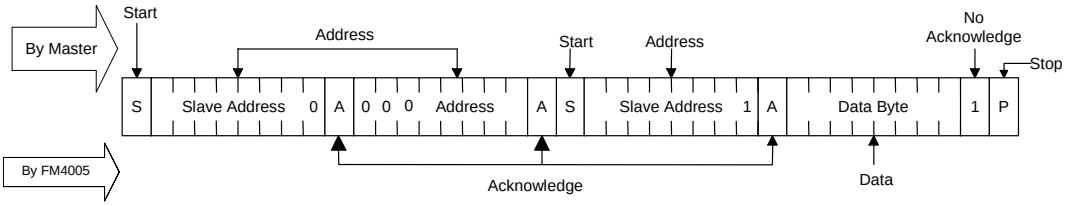


Figure 14. Single Selective Read

* Although not required, it is recommended that A5-A7 in the Address byte are zeros in order to preserve compatibility with future devices.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V * and $V_{IN} < V_{DD}$+1.0V **
V_{BAK}	Backup Supply Voltage	-1.0V to +4.5V
T_{STG}	Storage temperature	-55°C to + 125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C

* PFI input voltage must not exceed 4.5V.

** The "$V_{IN} < V_{DD}$+1.0V" restriction does not apply to the SCL and SDA inputs which do not employ a diode to V_{DD}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	2.7	-	5.5	V	7
I_{DD}	V_{DD} Supply Current					1
	@ SCL = 100 kHz			500	µA	
	@ SCL = 400 kHz			900	µA	
	@ SCL = 1 MHz			1500	µA	
I_{SB}	Standby Current					2
	For $V_{DD} < 5.5V$			150	µA	
	For $V_{DD} < 3.6V$			120	µA	
V_{BAK}	RTC Backup Voltage	2.0	3.0	3.75	V	9
I_{BAK}	RTC Backup Current			1	µA	4
I_{BAKTC}	Trickle Charge Current	5		25	µA	10
V_{TP0}	V_{DD} Trip Point Voltage, VTP(1:0) = 00b	2.55	2.6	2.70	V	5
V_{TP1}	V_{DD} Trip Point Voltage, VTP(1:0) = 01b	2.85	2.9	3.00	V	5
V_{TP2}	V_{DD} Trip Point Voltage, VTP(1:0) = 10b	3.80	3.9	4.00	V	5
V_{TP3}	V_{DD} Trip Point Voltage, VTP(1:0) = 11b	4.25	4.4	4.50	V	5
V_{RST}	V_{DD} for valid /RST @ I_{OL} = 80 µA at V_{OL}					6
	$V_{BAK} > V_{BAK}$ min	0			V	
	$V_{BAK} < V_{BAK}$ min	1.6			V	
I_{LI}	Input Leakage Current			1	µA	3
I_{LO}	Output Leakage Current			1	µA	3
V_{IL}	Input Low Voltage					
	All inputs except as listed	-0.3		0.3 V_{DD}	V	8
	CNT1-2 battery backed ($V_{DD} < 2.5V$)	-0.3		0.5	V	
	CNT1-2 ($V_{DD} > 2.5V$)	-0.3		0.8	V	
V_{IH}	Input High Voltage					
	All inputs except as listed	0.7 V_{DD}		V_{DD} + 0.3	V	
	PFI (comparator input)	-		3.75	V	
	CNT1-2 battery backed ($V_{DD} < 2.5V$)	V_{BAK} – 0.5		V_{BAK} + 0.3	V	
	CNT1-2 $V_{DD} > 2.5V$	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{OL}	Output Low Voltage			0.4	V	
	@ I_{OL} = 3 mA					
V_{OH}	Output High Voltage	2.4			V	
	(CAL/PFO) @ I_{OH} = -2 mA					
R_{RST}	Pull-up resistance for /RST inactive	50		400	KΩ	
V_{PFI}	Power Fail Input Reference Voltage	1.175	1.20	1.225	V	
V_{HYS}	Power Fail Input (PFI) Hysteresis (Rising)		-	100	mV	

Notes
1. SCL toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V.
2. All inputs at V_{SS} or $V_{DD,}$ static. Stop command issued.
3. V_{IN} or V_{OUT} = V_{SS} to V_{DD}. Does not apply to PFI, or /RST pins.
4. V_{BAK} = 3.0V, V_{DD} < 2.4V, oscillator running, CNT1-2 at VBAK.
5. /RST is asserted active when V_{DD} < V_{TP}.
6. The minimum V_{DD} to guarantee the level of /RST remains a valid V_{OL} level.
7. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
8. Includes /RST input detection of external reset condition to trigger driving of /RST signal by FM4005.
9. The VBAK trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
10. VBAK will source current when trickle charger is enabled (VBC bit=1), V_{DD} > V_{BAK}, and V_{BAK} < V_{BAK} max.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V, C_L = 100 pF unless otherwise specified)

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz	
t_{LOW}	Clock Low Period	4.7		1.3		0.6		µs	
t_{HIGH}	Clock High Period	4.0		0.6		0.4		µs	
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9		0.55	µs	
t_{BUF}	Bus Free Before New Transmission	4.7		1.3		0.5		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		0.25		µs	
$t_{SU:STA}$	Start Condition Setup for Repeated Start	4.7		0.6		0.25		µs	
$t_{HD:DAT}$	Data In Hold	0		0		0		ns	
$t_{SU:DAT}$	Data In Setup	250		100		100		ns	
t_R	Input Rise Time		1000		300		300	ns	1
t_F	Input Fall Time		300		300		100	ns	1
$t_{SU:STO}$	Stop Condition Setup	4.0		0.6		0.25		µs	
t_{DH}	Data Output Hold (from SCL @ VIL)	0		0		0		ns	
t_{SP}	Noise Suppression Time Constant on SCL, SDA		50		50		50	ns	

Notes: All SCL specifications as well as start and stop conditions apply to both read and write operations.
1. This parameter is characterized but not tested.

Supervisor Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Min	Max	Units	Notes
t_{RPU}	Reset inactive after V_{DD}>V_{TP}	100	200	ms	
t_{RNR}	V_{DD} < V_{TP} noise immunity	10	25	µs	1
t_{VF}	Fall time of VDD from V_{TP} to 0V	100	-	µs	1,2
t_{VR}	Rise time of VDD from 0V to VTP	100	-	µs	1,2
t_{WDP}	Pulse Width of /RST for Watchdog Reset	100	200	ms	
t_{WDOG}	Timeout of Watchdog	t_{DOG}	2*t_{DOG}	ms	3
f_{CNT}	Frequency of Event Counters	0	10	MHz	

Notes
1 This parameter is characterized but not tested.
2 Slew rate for proper transition between the battery-backed and normal operation.
3 t_{DOG} is the programmed time in register 0Ah, V_{DD} > V_{TP} and t_{RPU} satisfied.

Data Retention (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V)

Parameter	Min	Units	Notes
Data Retention (S/N and other NV bits)	10	Years	

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.0V)

Symbol	Parameter	Max	Units	Notes
C_{IO}	Input/output capacitance	8	pF	1
C_{XTAL}	X1, X2 Crystal pin capacitance	12	pF	1, 2

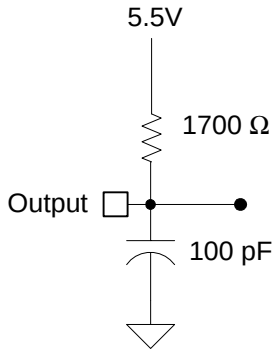
Notes
1 This parameter is characterized but not tested.
2 The crystal attached to the X1/X2 pins must be rated as 6pF.

AC Test Conditions

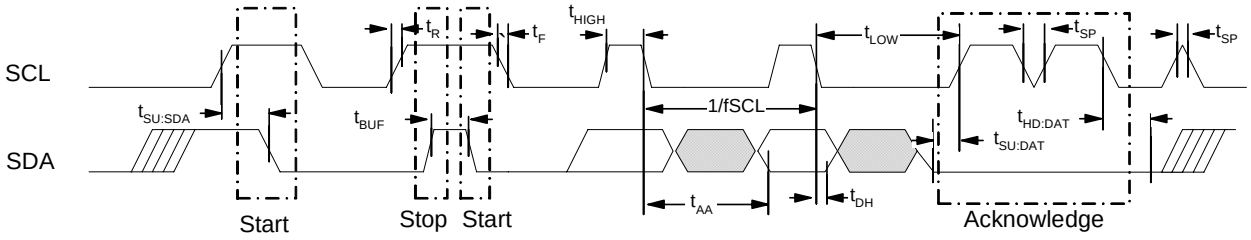
Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Diagram Notes
All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

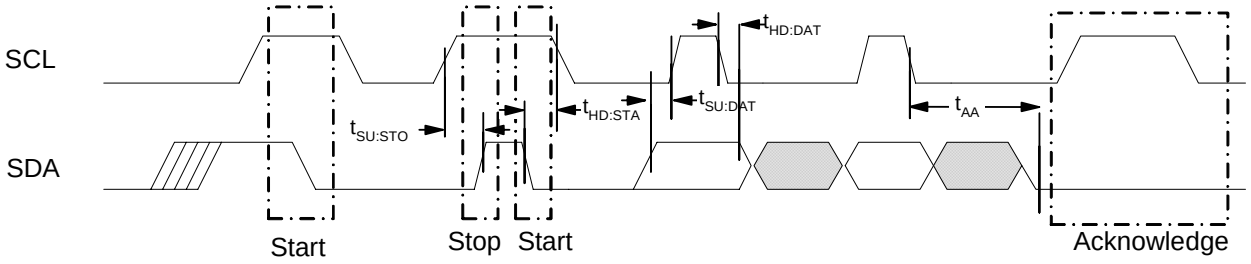
Equivalent AC Load Circuit



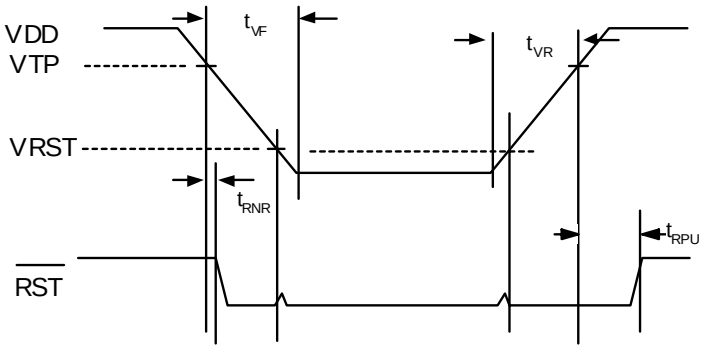
Read Bus Timing



Write Bus Timing

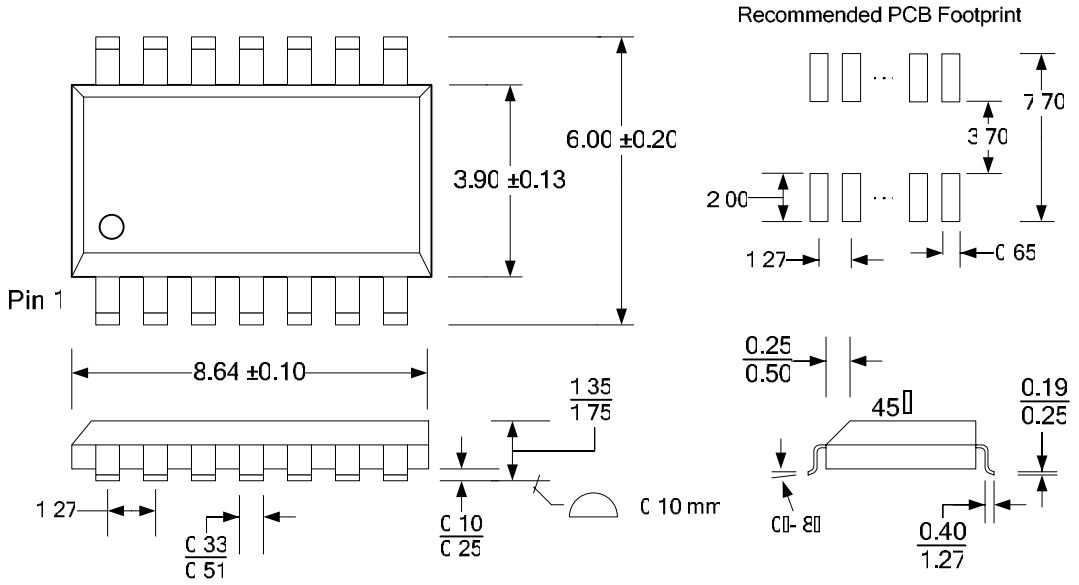


/RST Timing



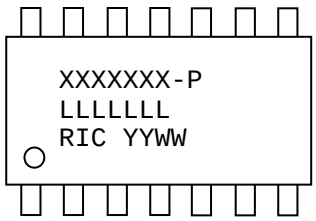
Mechanical Drawing

14-pin SOIC (JEDEC Standard MS-012 variation AB)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme



Legend:
XXXX= part number, P= package type (-S, -G)
LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM4005, Standard SOIC package, Year 2004, Work Week 40
FM4005-S
A40003S
RIC 0440

Revision History

Revision	Date	Summary
0.1	5/5/03	Initial release.
0.2	3/15/04	Added WP text to register 0Bh in Register Description table. Updated DC Operating Conditions table. Fixed package drawing dimensions.
1.0	3/30/04	Changed product status to Preliminary. Added V_{TP} and V_{PFI} parameters in DC Operating table. Changed V_{HYS} limits. Added "green" package.
1.1	4/5/04	Changed spec limits on V_{TP}, V_{PFI}, and V_{HYS} parameters in DC Operating table.
2.0	10/25/04	Changed to Pre-Production status. Added text to Trickle Charger section. Improved spec limits on V_{TP}, V_{PFI}, and V_{HYS} parameters and changed V_{IH} max limits in DC Operating table. Added companion register table with default values. Added Package Marking Scheme and board footprint. Devices marked with Date Codes 0440 and higher comply with the revision of the datasheet.
2.1	12/8/04	Changed description of POR flag and manual reset (pg. 5, 12). Added notes to Absolute Maximum Ratings.