

BCD-To-Seven Segment Latch/Decoder/Driver

CMOS MSI (Low-Power Complementary MOS)

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test (\overline{LT}), blanking (\overline{BI}), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	- 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	- 0.5 to $V_{DD} + 0.5$	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	- 55 to + 125	°C
Power Dissipation, per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	- 65 to + 150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

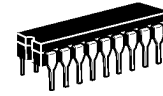
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

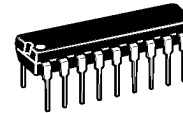
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MC14513B



L SUFFIX
CERAMIC
CASE 726



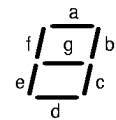
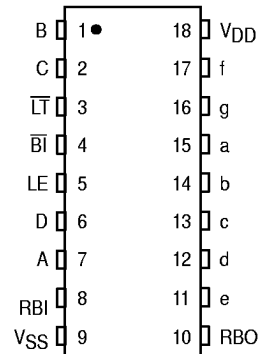
P SUFFIX
PLASTIC
CASE 707

ORDERING INFORMATION

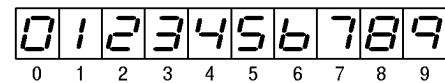
MC14XXXBCP Plastic
MC14XXXBCL Ceramic

$T_A = -55^\circ$ to 125° C for all packages.

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs				Outputs												
RBI	LE	\overline{BI}	\overline{LT}	D	C	B	A	RBO	a	b	c	d	e	f	g	Display
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	0	1	0	2
X	0	1	1	0	0	1	1	0	1	1	1	0	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	0	1	0	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†			*				*	

X = Don't Care

†RBO = RBI ($\overline{D} \overline{C} \overline{B} \overline{A}$), indicated by other rows of table

*Depends upon the BCD code previously applied when LE = 0



MOTOROLA

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage — Segment Outputs "0" Level V _{in} = V _{DD} or 0 "1" Level V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.1	—	4.1	5.0	—	4.1	—	Vdc
		10	9.1	—	9.1	10	—	9.1	—	
		15	14.1	—	14.1	15	—	14.1	—	
Output Voltage — RBO Output "0" Level V _{in} = V _{DD} or 0 "1" Level V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # "0" Level (V _O = 3.8 or 0.5 Vdc) (V _O = 8.8 or 1.0 Vdc) (V _O = 13.8 or 1.5 Vdc) "1" Level (V _O = 0.5 or 3.8 Vdc) (V _O = 1.0 or 8.8 Vdc) (V _O = 1.5 or 13.8 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Voltage — Segments Source (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA) (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA) (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA)	V _{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc
		—	—	—	—	4.24	—	—	—	
		3.9	—	3.9	4.12	—	3.5	—	—	
		—	—	—	3.94	—	—	—	—	
		3.4	—	3.4	3.70	—	3.0	—	—	
	10	9.1	—	9.1	9.58	—	9.1	—	—	Vdc
		—	—	—	9.26	—	—	—	—	
		9.0	—	9.0	9.17	—	8.6	—	—	
		—	—	—	9.04	—	—	—	—	
		8.6	—	8.6	8.90	—	8.2	—	—	
	15	14.1	—	14.1	14.59	—	14.1	—	—	Vdc
		—	—	—	14.27	—	—	—	—	
		14	—	14	14.18	—	13.6	—	—	
		—	—	—	14.07	—	—	—	—	
		13.6	—	13.6	13.95	—	13.2	—	—	
15	—	—	—	13.80	—	—	—	—	Vdc	
	—	—	—	—	—	—	—	—		
	—	—	—	—	—	—	—	—		
	—	—	—	—	—	—	—	—		
	—	—	—	—	—	—	—	—		

(continued)

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Drive Current — RBO Output (V _{OH} = 2.5 V) Source (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) (V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OH}	5.0	-0.40	—	-0.32	-0.64	—	-0.22	—	mAdc
		10	-0.21	—	-0.17	-0.34	—	-0.12	—	
		15	-0.81	—	-0.66	-1.30	—	-0.46	—	
	I _{OL}	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
		10	0.47	—	0.38	0.75	—	0.26	—	
		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments (V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current***† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.8 μA/kHz) f + I _{DD}							
		15	I _T = (5.7 μA/kHz) f + I _{DD}							

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =
 1.0 Vdc min @ V_{DD} = 5.0 Vdc
 2.0 Vdc min @ V_{DD} = 10 Vdc
 2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

Input LE and RBI low, and Inputs D, $\overline{B1}$ and $\overline{L1}$ high.
 f in respect to a system clock.
 All outputs connected to respective C_L loads.

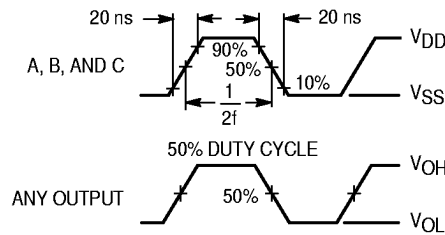
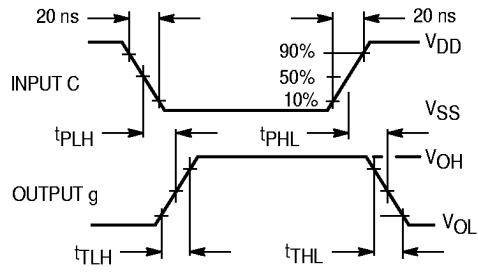


Figure 1. Dynamic Power Dissipation Signal Waveforms

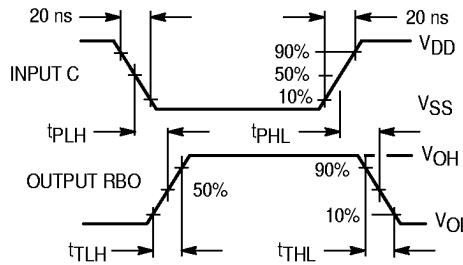
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time — Segment Outputs	t_{TLH}	5.0	—	40	80	ns
		10	—	30	60	
		15	—	25	50	
Output Rise Time — RBO Output	t_{TLH}	5.0	—	480	960	ns
		10	—	240	480	
		15	—	190	380	
Output Fall Time — Segment Outputs* $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	t_{THL}	5.0	—	125	250	ns
		10	—	75	150	
		15	—	65	130	
Output Fall Time — RBO Outputs $t_{THL} = (3.25 \text{ ns/pF}) C_L + 107.5 \text{ ns}$ $t_{THL} = (1.35 \text{ ns/pF}) C_L + 67.5 \text{ ns}$ $t_{THL} = (0.95 \text{ ns/pF}) C_L + 62.5 \text{ ns}$	t_{THL}	5.0	—	270	540	ns
		10	—	135	270	
		15	—	110	220	
Propagation Delay Time — A, B, C, D Inputs* $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	t_{PLH}	5.0	—	640	1280	ns
		10	—	250	500	
		15	—	175	350	
	t_{PHL}	5.0	—	720	1440	ns
		10	—	290	580	
		15	—	200	400	
Propagation Delay Time — RBI and BI Inputs* $t_{PLH} = (1.05 \text{ ns/pF}) C_L + 547.5 \text{ ns}$ $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	t_{PLH}	5.0	—	600	750	ns
		10	—	200	300	
		15	—	150	220	
	t_{PHL}	5.0	—	485	970	ns
		10	—	200	400	
		15	—	160	320	
Propagation Delay Time — \overline{LT} Input* $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	t_{PLH}	5.0	—	313	625	ns
		10	—	125	250	
		15	—	90	180	
	t_{PHL}	5.0	—	313	625	ns
		10	—	125	250	
		15	—	90	180	
Setup Time	t_{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t_h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

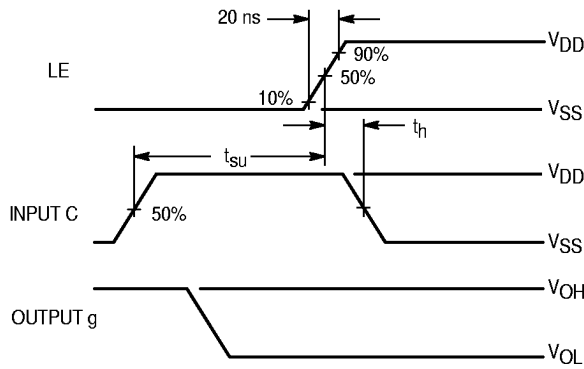
* The formulas given are for the typical characteristics only.



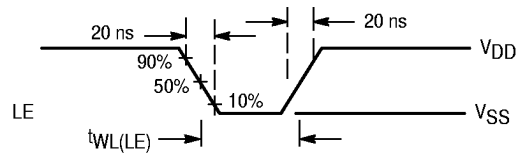
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, \overline{BI} and \overline{LT} high.



b. Inputs A, B, D and LE low, and Inputs RBI, \overline{BI} and \overline{LT} high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, \overline{BI} and \overline{LT} high.

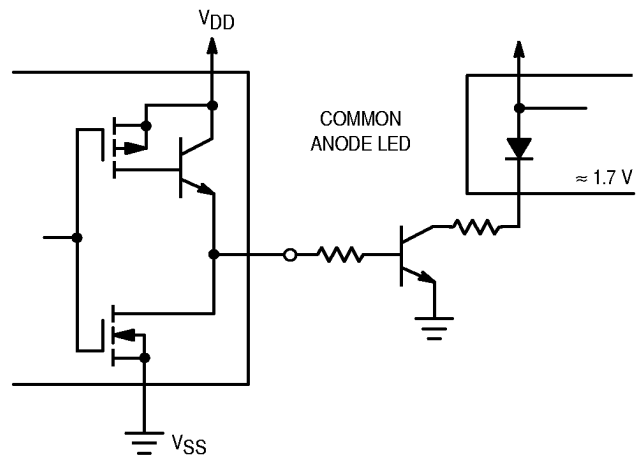
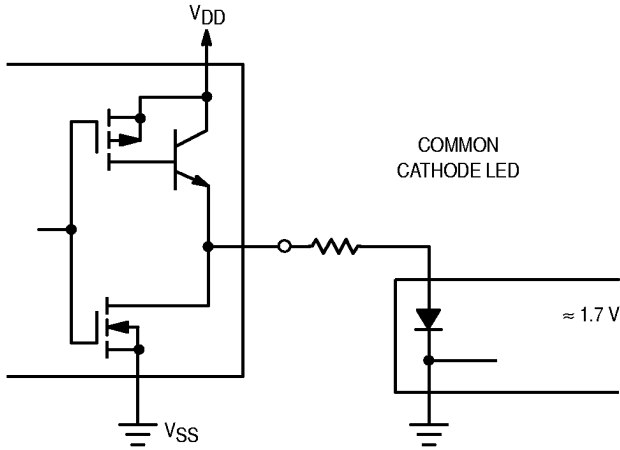


d. Pulse Width: Data DCBA strobed into latches.

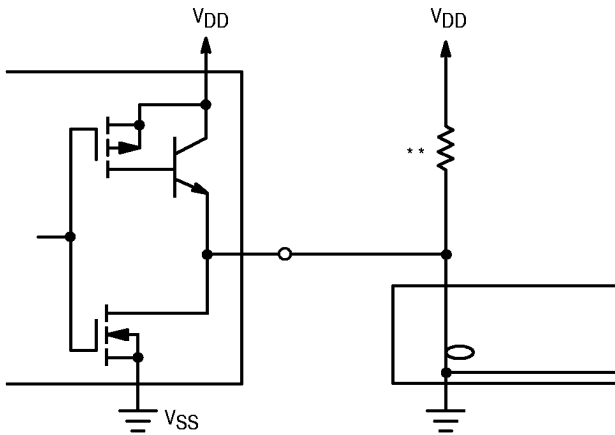
Figure 2. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

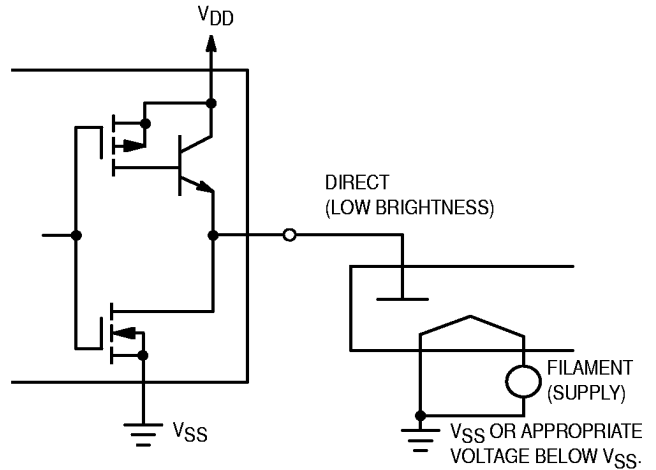
LIGHT EMITTING DIODE (LED) READOUT



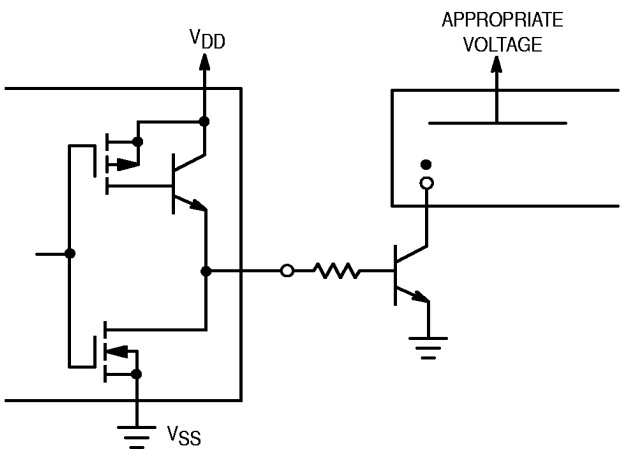
INCANDESCENT READOUT



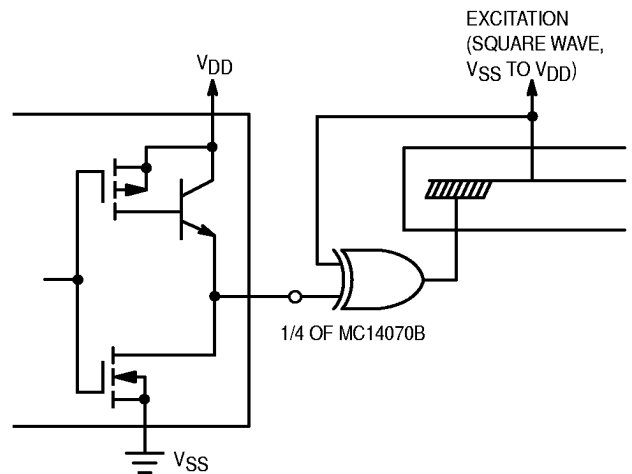
FLUORESCENT READOUT



GAS DISCHARGE READOUT



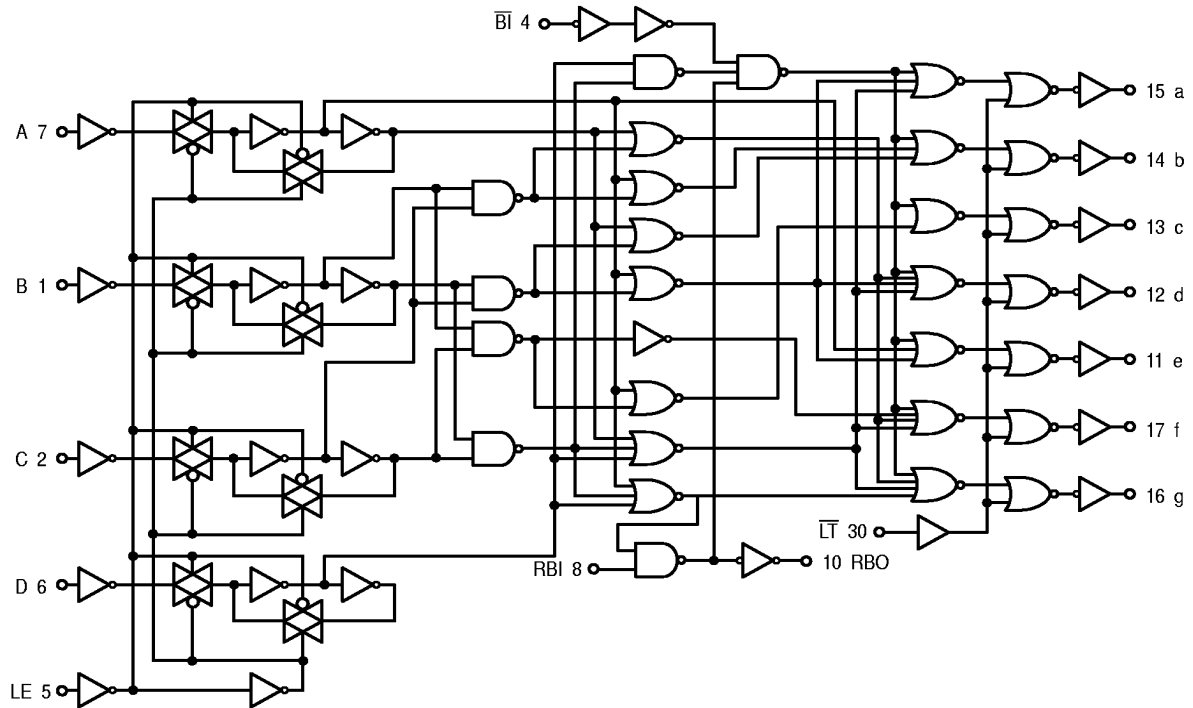
LIQUID CRYSTAL (LC) READOUT



** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC's not recommended for life of LC readouts.

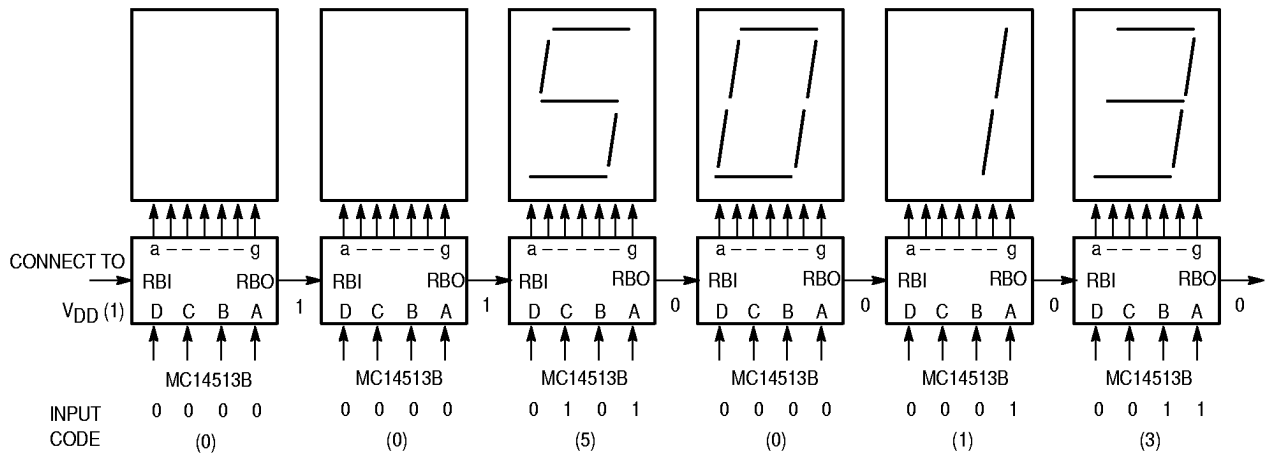
LOGIC DIAGRAM



TYPICAL APPLICATIONS FOR RIPPLE BLANKING

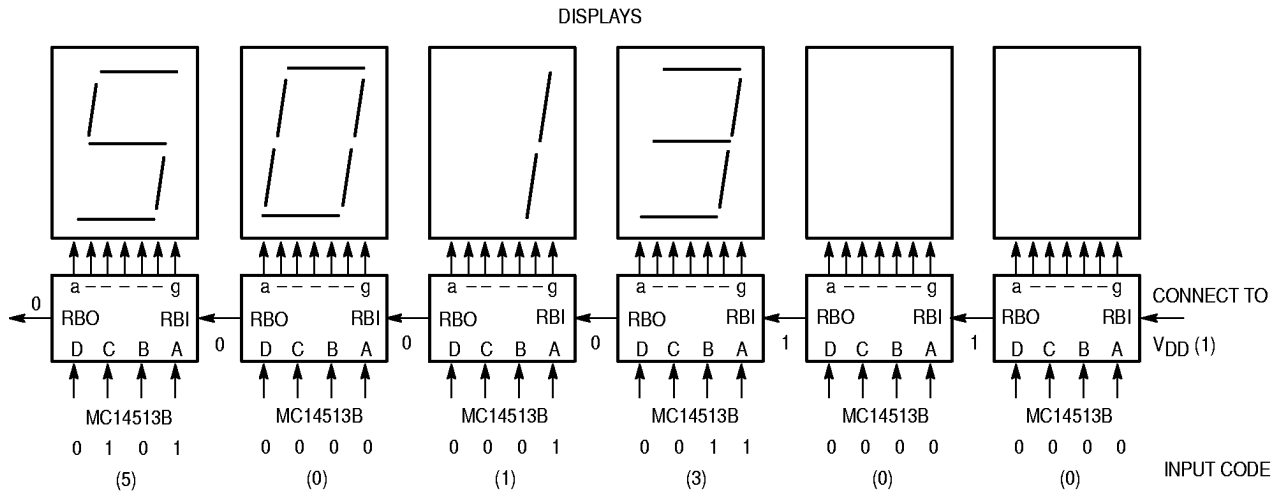
LEADING EDGE ZERO SUPPRESSION

DISPLAYS



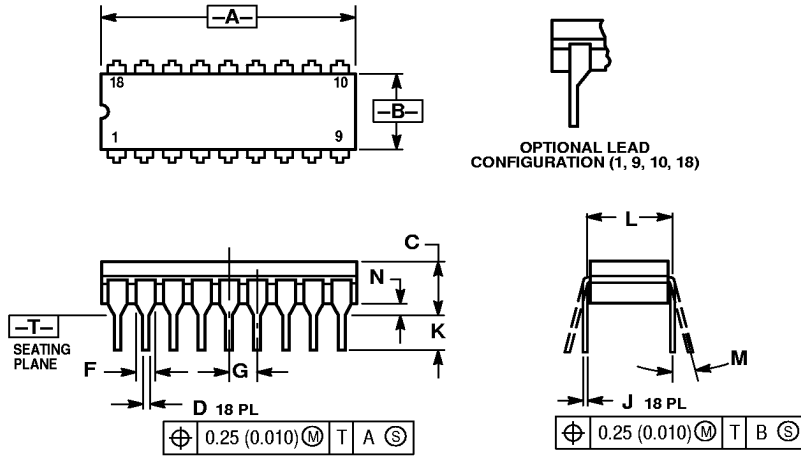
TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)

TRAILING EDGE ZERO SUPPRESSION



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 726-04 ISSUE G

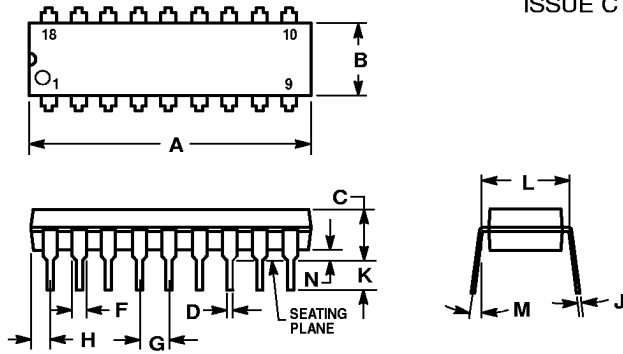


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P SUFFIX PLASTIC DIP PACKAGE CASE 707-02 ISSUE C



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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