ML4818*

Phase Modulation/Soft Switching Controller

GENERAL DESCRIPTION

The ML4818 is a complete phase modulation control IC suitable for full bridge soft switching converters. Unlike conventional PWM circuits, the phase modulation technique allows for zero-voltage switching transitions and square wave drive across the transformer. The IC modulates the phases of the two sides of the bridge to control output power.

The ML4818 can be operated in current mode. The delay times for the outputs are externally programmable to allow the zero-voltage switching transitions to take place.

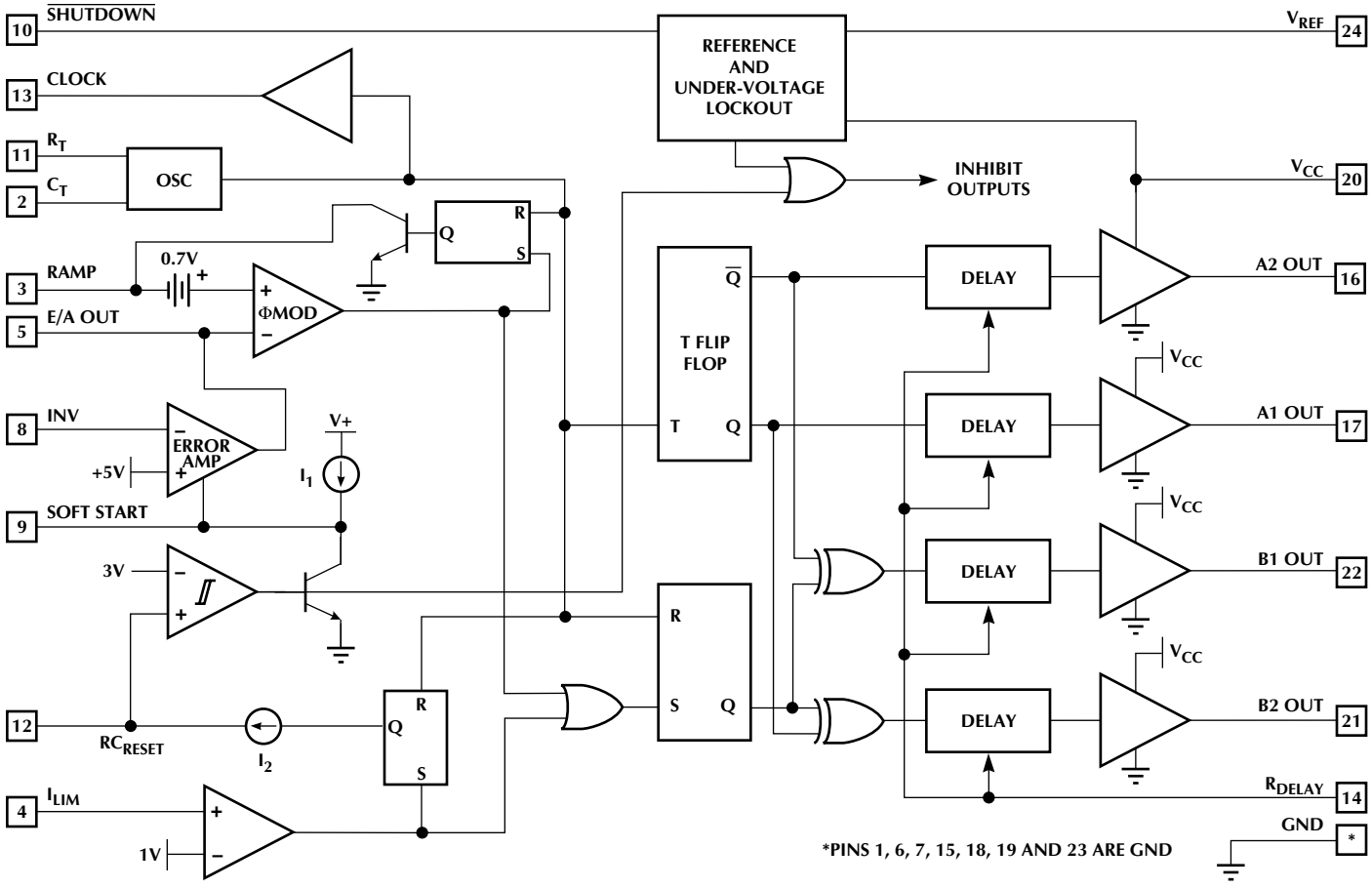
Pulse-by-pulse current limit, integrating fault detection, and soft start reset are provided. The under-voltage lockout circuit features a 6V hysteresis with a low starting current to allow off-line start up with a low power bleed resistor. A shutdown function powers down the IC, putting it into a low quiescent state.

FEATURES

- Full bridge phase modulation zero voltage switching circuit with programmable ZV transition times
- Constant frequency operation to 500kHz
- Current mode operation
- Cycle-by-cycle current limiting with integrating fault detection and restart delay
- Precision buffered 5V reference (+1%)
- Four 1.5A peak current totem-pole output drivers
- Under-voltage lockout circuit with 6V hysteresis
- Power DIP package allows higher dissipation

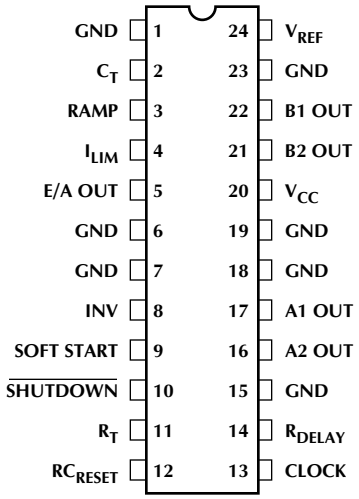
* Some Packages Are Obsolete)

BLOCK DIAGRAM



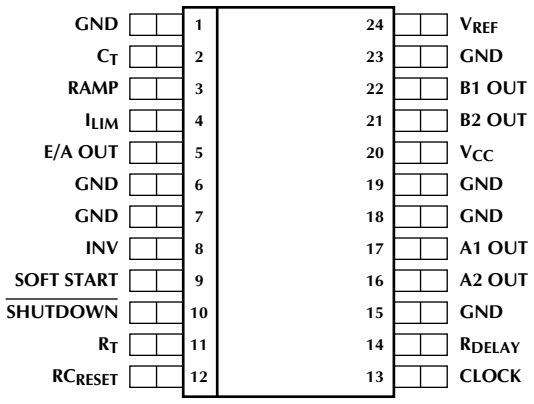
PIN CONNECTION

24-Pin Power DIP



TOP VIEW

24-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Ground
2	C_T	Timing capacitor for oscillator
3	RAMP	Non-inverting input to main comparator. Connected to current sense resistor for current mode
4	I_{LIM}	Current limit sense pin. Normally connected to current sense resistor
5	E/A OUT	Output of error amplifier and input to PWM comparator
6,7	GND	Ground and substrate
8	INV	Inverting input to error amp
9	SOFT START	Normally connected to soft start capacitor
10	$\overline{SHUTDOWN}$	Pulling this pin low puts the IC into a power down mode and turns off all outputs. This pin is internally pulled up to V_{REF}.
11	R_T	Resistor which sets discharge current for oscillator timing capacitor
12	RC_{RESET}	Timing elements for Integrating fault detection and reset delay circuits
13	CLOCK	Oscillator output
14	R_{DELAY}	Resistor to ground on this pin programs the amount of delay from the time an output turns off until its complementary output turns on
15	GND	Ground
16	A2 OUT	High current totem pole output A1
17	A1 OUT	High current totem pole output A2
18,19	GND	Ground and substrate
20	V_{CC}	Positive supply for the IC
21	B2 OUT	High current totem pole output B1
22	B1 OUT	High current totem pole output B2
23	GND	Ground
24	V_{REF}	Buffered output for the 5V voltage reference

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 30V
Output Driver Current, Source or Sink
  DC 0.5A
  Pulse (0.5 µs) 1.5A
Analog Inputs
  (C_T, RAMP, I_{LIM}, E/A OUT, INV,
  SOFT START, RC_{RESET}) ..... –0.3V to 6V
CLOCK Output Current (R_T) .....–5mA
Error Amplifier Output Current (E/A OUT) 5mA
SOFT START Sink Current ..... 50 mA
Oscillator Charging Current (C_T) .....–5mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 Sec)..... 260°C
Thermal Resistance (θ_{JA})
  Plastic Power DIP ..... 40°C/W
  Plastic SOIC ..... 80°C/W

OPERATING CONDITIONS

Operating Temperature Range ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 15V, R_T = 12.7kΩ, C_T = 250pF, R_{CLK} = 3kΩ, R_{DELAY} = 5kΩ, T_A = Operating Temperature Range (Note 1).

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
OSCILLATOR					
Initial Accuracy	T_A = 25°C	410	450	525	kHz
Voltage Stability	12V < V_{CC} < 25V		–0.3		%/V
Temperature Stability			0.2		%
Total Variation	line, temp.	375		525	kHz
C_T Discharge Current	V_{C_T} = 2V	4.7	5.5	6.3	mA
Clock Out High		2.4	3.1	6	V
Clock Out Low			0	0.4	V
Ramp Peak		0	4.1		V
Ramp Valley			1.5	5	V
Ramp Valley to Peak		0	2.6	5	V
REFERENCE					
Output Voltage	T_A = 25°C, I_O = 1mA	4.95	5.0	5.05	V
Line Regulation	12V < V_{CC} < 25V	–20	2	20	mV
Load Regulation	1mA < I_O < 10mA	–20	3	20	mV
Temperature Stability			.2		mV/°C
Total Variation		4.85		5.15	V
Output Noise Voltage	10Hz to 10kHz		50		mV
Long Term Stability	T_J = 125°C, 1000 hrs		5	25	mV
Short Circuit Current	V_{REF} = 0V	–20	–50		mA
ERROR AMPLIFIER					
Input Offset Voltage		–40		30	mV
Input Bias Current		–3	0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1 < V_O < 4V	70	75		dB
PSRR	12 < V_{CC} < 25V	65	80		dB

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
ERROR AMPLIFIER (Continued)					
Output Sink Current	$V_{EA\ OUT}$ = 1V	1	3.2		mA
Output Source Current	$V_{EA\ OUT}$ = 5.1V	–0.5	–2.2	–20	mA
Output High Voltage	$I_{EA\ OUT}$ = –0.5mA	5.0	5.5	6.0	V
Output Low Voltage	$I_{EA\ OUT}$ = 1mA			0.8	V
Unity Gain Bandwidth		2.0	2.8		MHz
Slew Rate		8.5		V/µs	
PHASE MODULATOR					
RAMP Bias Current	V_{RAMP} = 2.5V		–1	–10	µA
EA OUT Zero DC Threshold	V_{RAMP} = 0V	0.4	0.6	0.9	V
t_{PD}, RAMP to Output			50	80	ns
t_{DELAY}	C_L = 1nF	99	200	250	ns
R_{DELAY} Voltage		4	4.3	5	V
SOFT START					
Charge Current	$V_{SOFT\ START}$ = 4V	–15	–25	–30	µA
Discharge Current	$V_{SOFT\ START}$ = 1V	10	20	30	mA
CURRENT LIMIT/SHUTDOWN					
I_{LIM} Bias Current	0V < $V_{I_{LIM}}$ < 4V	–10	–1	10	µA
Current Limit Threshold	$V_{\overline{SHUTDOWN}}$ = 0V	0.92	1.02	1.12	V
t_{PD}, I_{LIM}		50		ns	
RC_{RESET} Shutdown Threshold		3.15	3.4	3.65	V
RC_{RESET} Restart Threshold		1.0	1.3	1.6	V
RC_{RESET} Charging Current	$V_{I_{LIM}}$ =2V, $V_{RC_{RESET}}$ = 1.5V	–400	–523	–1000	µA
$\overline{SHUTDOWN}$ Threshold		2.0	2.4	2.8	V
$\overline{SHUTDOWN}$ Input Bias Current	$V_{\overline{SHUTDOWN}}$ = 0	–100	–25	10	µA
OUTPUT					
Output Low Level	I_{OUT} = 20mA I_{OUT} = 200mA, T_A = 25°C		0.1 0.7	0.4 2.8	V V
Output High Level	I_{OUT} = –20mA I_{OUT} = –200mA, T_A = 25°C	12.0 11.0	13.5 13.0		V V
Rise/Fall Time	C_L = 1000pF		50	75	ns
UNDER-VOLTAGE LOCKOUT					
Start Threshold		15.5	16.5	17.2	V
Stop Threshold		9.25	10.2	10.7	V
SUPPLY					
Start Up Current	V_{CC} < 15.8V		3	4	mA
I_{CC}	V_{INV} = 4V, V_{RAMP} = $V_{I_{LIM}}$ = 0V, C_L = 1nF, T_A = 25°C (Note 2)		60	70	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: V_{CC} must be brought above the UVLO start voltage (17.2V) before dropping to V_{CC} = 15V to ensure start-up.

FUNCTIONAL DESCRIPTION

PHASE MODULATOR

Power is controlled by modulating the switching phase on sides A and B of the full H-bridge converter (Figure 1). Power is delivered to the output through the transformer secondary. The power conversion process is described by the following sequence and illustrated by the timing diagram of Figure 2:

1. A2 and B1 are high (Q1 and Q2 are on), beginning the power conversion cycle.

2. After the Φ MOD comparator trips, B1 goes low turning off Q2. The parasitic drain-to-source capacitances of Q2 and Q4 charge to +VIN. This forces the drain-to-source voltage across Q3 to 0V.

3. B2 now goes high after t_{DELAY} (set by R_{DELAY}). Since the voltage across Q3 is now 0V, B2 turns Q3 on at zero voltage.

4. The CLOCK now goes high turning A2 off. During this period, Q1 and Q2 and Q4 are off. The transformer leakage current discharges the drain-to-source capacitance on Q4 until there is 0V across it.

5. A1 will remain low for a period defined by t_{DELAY}, then it goes high. The voltage across Q4 is now 0V as A1 turns it on at zero voltage.

6. The previous sequence is now repeated with the opposite polarity on all outputs (see Figure 2).

The above sequence is then repeated but with the opposite polarity on all outputs.

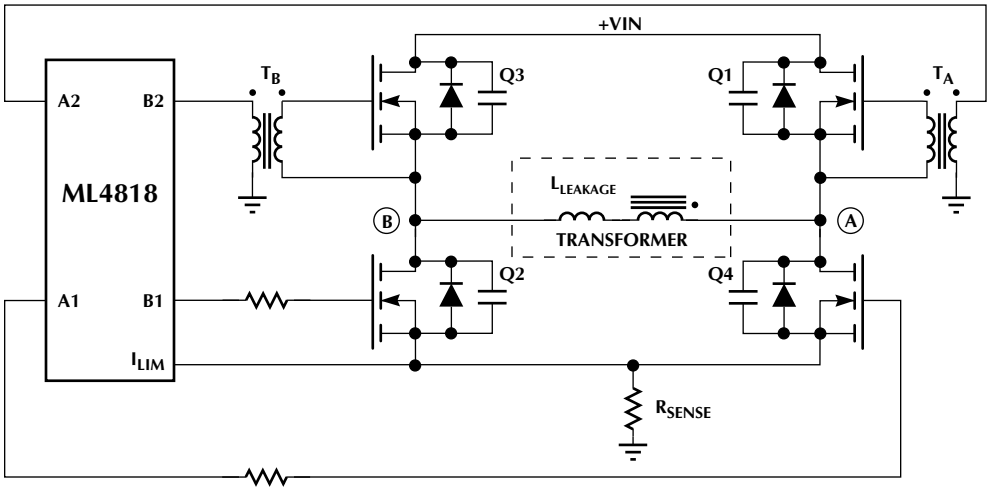


Figure 1. Simplified diagram of Phase Modulated power Outputs.

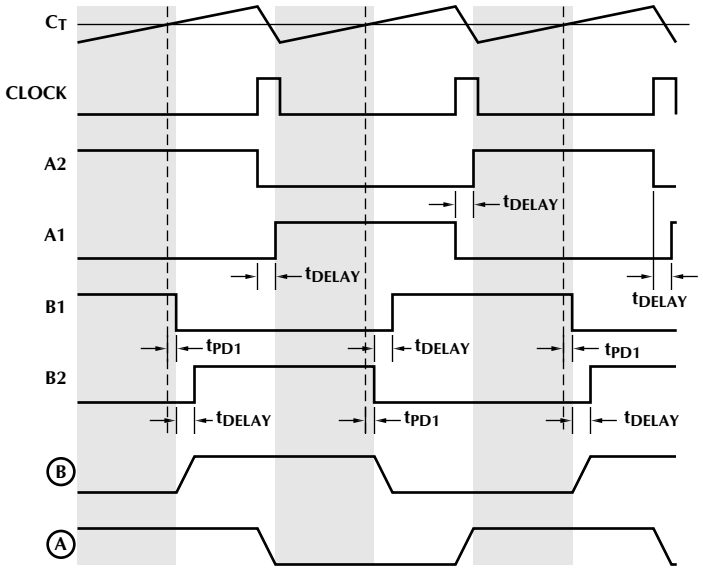


Figure 2. Phase Modulation control waveforms (Shaded areas indicate a power cycle).

The ML4818 can also be used in current mode by sensing load current on the RAMP input (pin 3).

The four output delay timers are programmed via an external R_{DELAY} resistor as shown below. This resistor value should be no less than 1kΩ. Expressing R_{DELAY} in kΩ the delay, in ns is:

$$T_{DELAY} = 33 \times R_{DELAY} + 45 \quad (1)$$

The ML4818 contains special logic circuits to provide for voltage mode feed-forward and lock out long pulses into the internal logic. This prevents instability from occuring when the Φ Comparator trips in voltage mode.

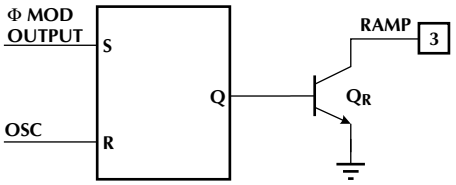


Figure 3. Voltage Feed-Forward Circuit.

The collector of Q_R in figure 3 is high only during a power cycle. When the power cycle terminates, RAMP is pulled low. In voltage mode operation, a capacitor is connected from RAMP to GND with a resistor from RAMP to V_{IN} to provide input voltage feed forward.

OSCILLATOR

The ML4818 oscillator charges the external capacitor, C_T, with a current (I_{SET}) equal to $5/R_T$. When the C_T voltage reaches the upper threshold (Ramp Peak), the comparator changes state, turning on the current sink which discharges C_T to the lower threshold (Ramp Valley). The C_T pin is clamped to Ramp Valley by Q1 (Figure 5) to prevent inaccuracy due to undershoot on C_T.

To use the CLOCK output for driving external synchronization circuitry, a pull-down resistor is required from CLOCK to GND.

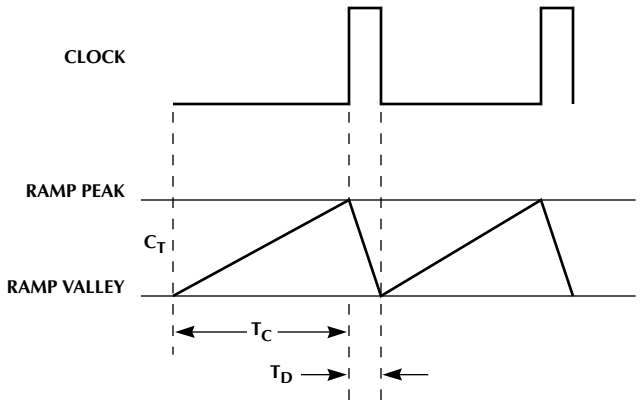


Figure 4. Ocillator Timing Diagram

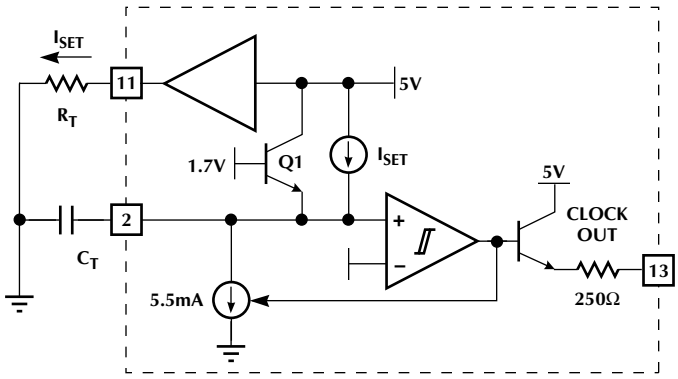


Figure 5. Ocillator Block Diagram

For frequencies of less than 500kHz, oscillator frequency can be set by using the following formulae:

$$f_{OSC} = \frac{1}{0.52 C_T R_T + 500 C_T} \quad (2)$$

ERROR AMPLIFIER

The ML4818 error amplifier is a 2.5MHz bandwidth, 8.5V/µs slew rate op-amp with provision for limiting the positive output voltage swing (output inhibit line) to implement the soft start function. The error amplifier output source current is limited to 4.5mA.

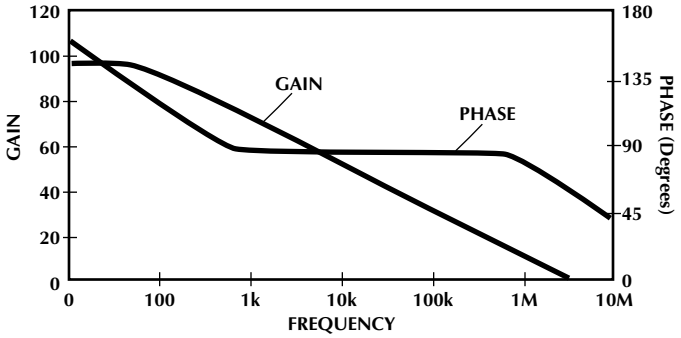


Figure 6. Error Amplifier Open-Loop Gain and Phase vs. Frequency.

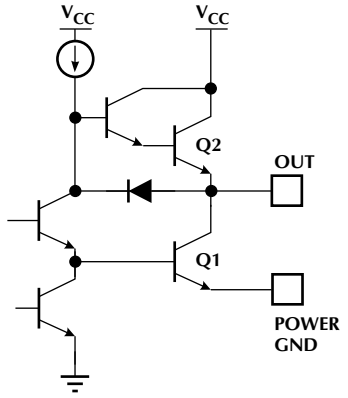


Figure 7. Power Driver Simplified Schematic.

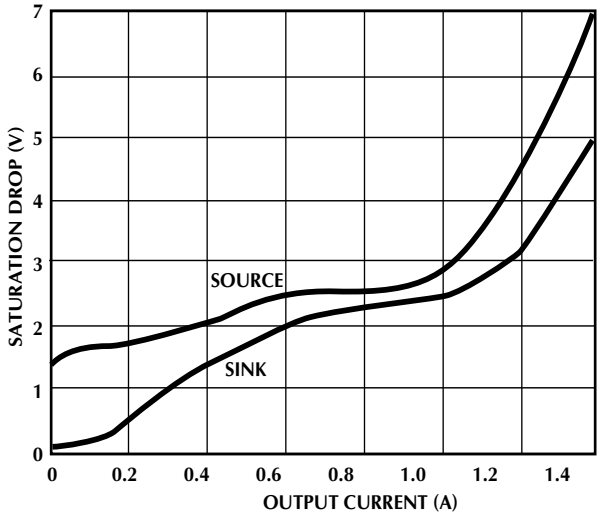


Figure 8. Output Drive Saturation Voltage vs. Output Current.

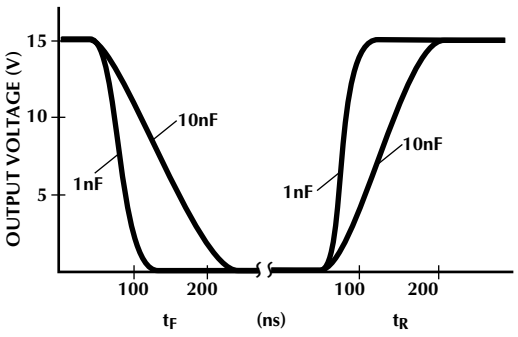


Figure 9. Output Rise/Fall Time.

OUTPUT DRIVER STAGE

The ML4818 has four high current high speed totem pole output drivers each capable of 1.5A peak output, designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors. Figure 8 illustrates the saturation characteristics of the ouput drive transistors shown in Figure 7. Typical rise and fall time characteristics of the output drivers are illustrated with capacitive loads of 1nF and 10nF in Figure 9.

CURRENT LIMIT, FAULT DETECTION AND SOFT START

Current limit is implemented when the current sensed on I_{LIM} reaches the 1V limit. At this point, the PWM cycle is terminated. The flip flop (Figure 10) turns on the current source to charge C_{RST} and remains on for the duration of the clock period. When C_{RST} has charged to 3.4V, a soft start reset occurs. The number of times the PWM cycle is terminated due to over-current is "remembered" on C_{RST}. Over time, C_{RST} is discharged by R_{RST} providing a measure of "forgetting" when the over-current condition no longer occurs. This integrating fault detection is useful in differentiation between short circuit and load surge conditions.

Since the per cycle charge on RC_{RESET} is proportional to how early in the power cycle the over-current occurs, a reset will occur more quickly under output short circuit conditions (Figures 11a and 11b) than during a load surge (Figures 11c and 11d).

When the soft start reset occurs, the output is inhibited and the soft start capacitor is discharged. The output will remain off until C_{RST} discharges to 1.3V through R_{RST}, providing a reset delay. When the IC restarts, the error amplifier output voltage is limited to the voltage at SOFT START, thus limiting the duty cycle.

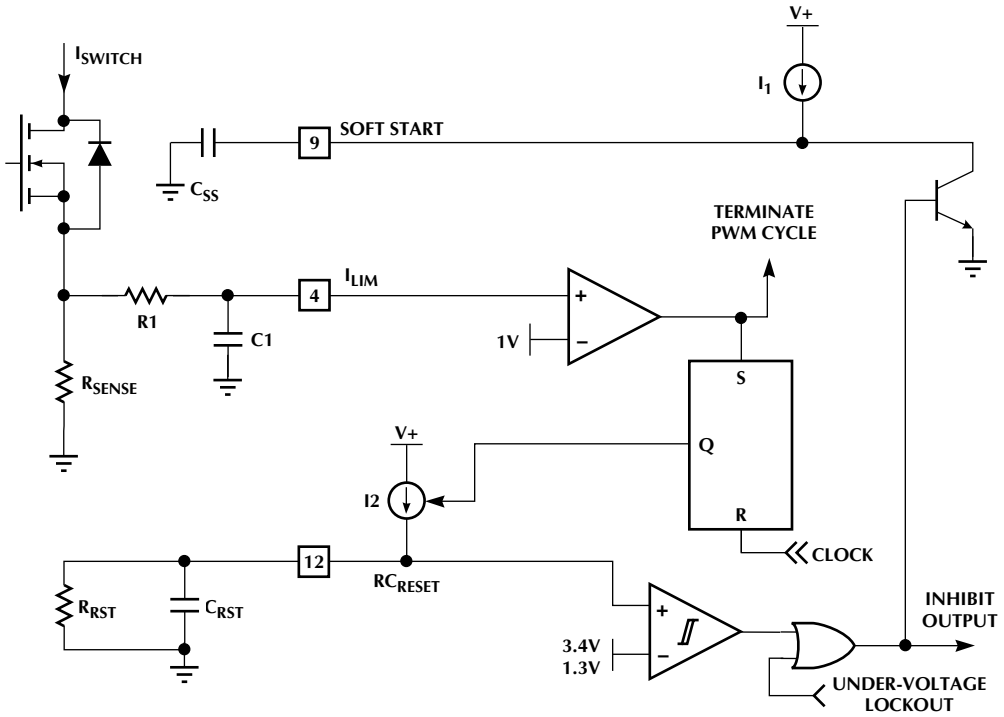


Figure 10. Over-Current, Soft-Start, and Integrating Fault Detect Circuits.

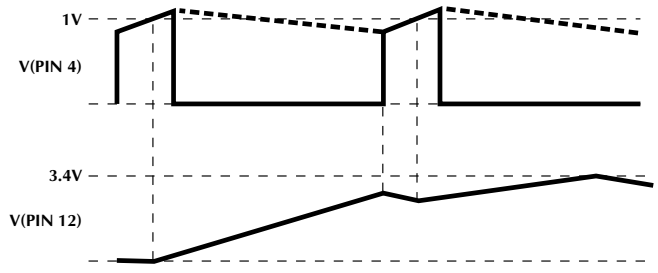


Figure 11a, 11b. I_{LIMIT} and Resulting RC_{RESET} Waveforms During Short Circuit.

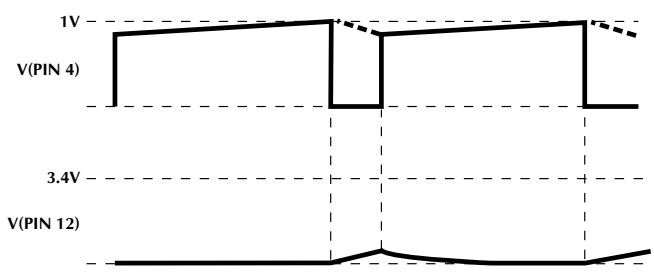


Figure 11c, 11d. I_{LIMIT} and Resulting RC_{RESET} Waveforms During Load Surge.

UNDER-VOLTAGE LOCKOUT

On power up, when V_{CC} is below 16V, the IC draws very little current (1.1mA typ.) and V_{REF} is disabled. When V_{CC} rises above 16V, the IC becomes active and V_{REF} is enabled and will stay in that condition until V_{CC} falls below 10.2V. (see Figure 12).

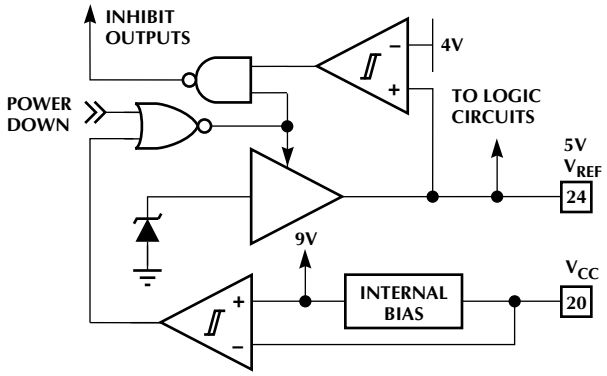


Figure 12. Under-Voltage Lockout and Reference Circuits.

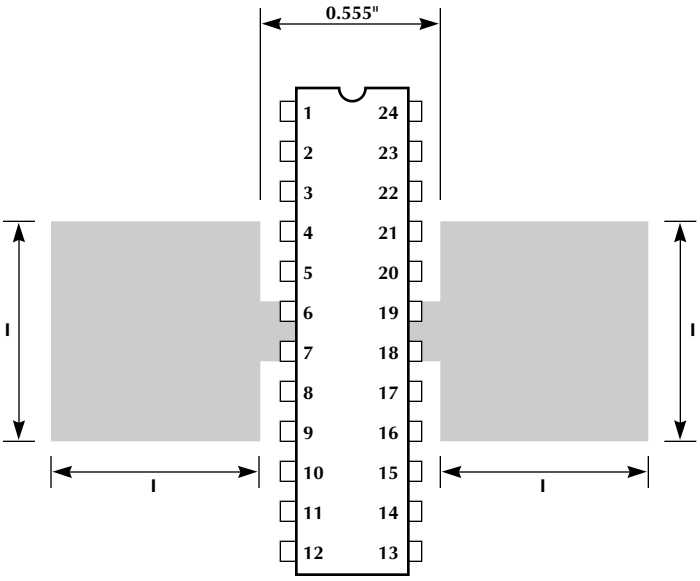


Figure 14. PC Board Copper Area Used as a Heat Sink.

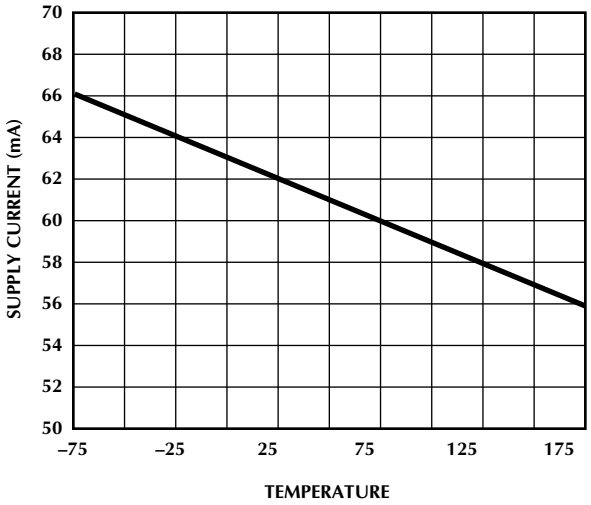


Figure 13. Supply Current vs. Temperature (°C).

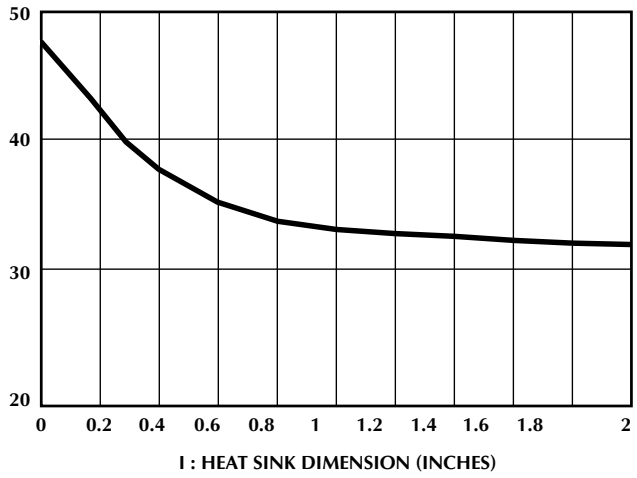


Figure 15. θ_{JA} as a Function of l (see figure 15).

THERMAL INFORMATION

The ML4818 is offered in a Power DIP package. This package features improved thermal conduction through the leadframe. Much of the heat is conducted through the center 4 grounded leads. Thermal dissipation can be improved with this package by using copper area on the board to function as a heat sink. Increasing this area can reduce the θ_{JA} (see figures 14 and 15), increasing the power handling capability of the package. Additional improvement may be obtained by using an external heat sink (available from Staver).

APPLICATIONS

The application circuit shown in Figure 16 features the ML4818 in a primary-side controlled voltage mode application with voltage feed-forward. Input voltage is rectified 120VAC (nominal). Feed-forward is provided by the RAMP pin via the resistor connected to the high voltage input. Current is sensed through sense transformer T4.

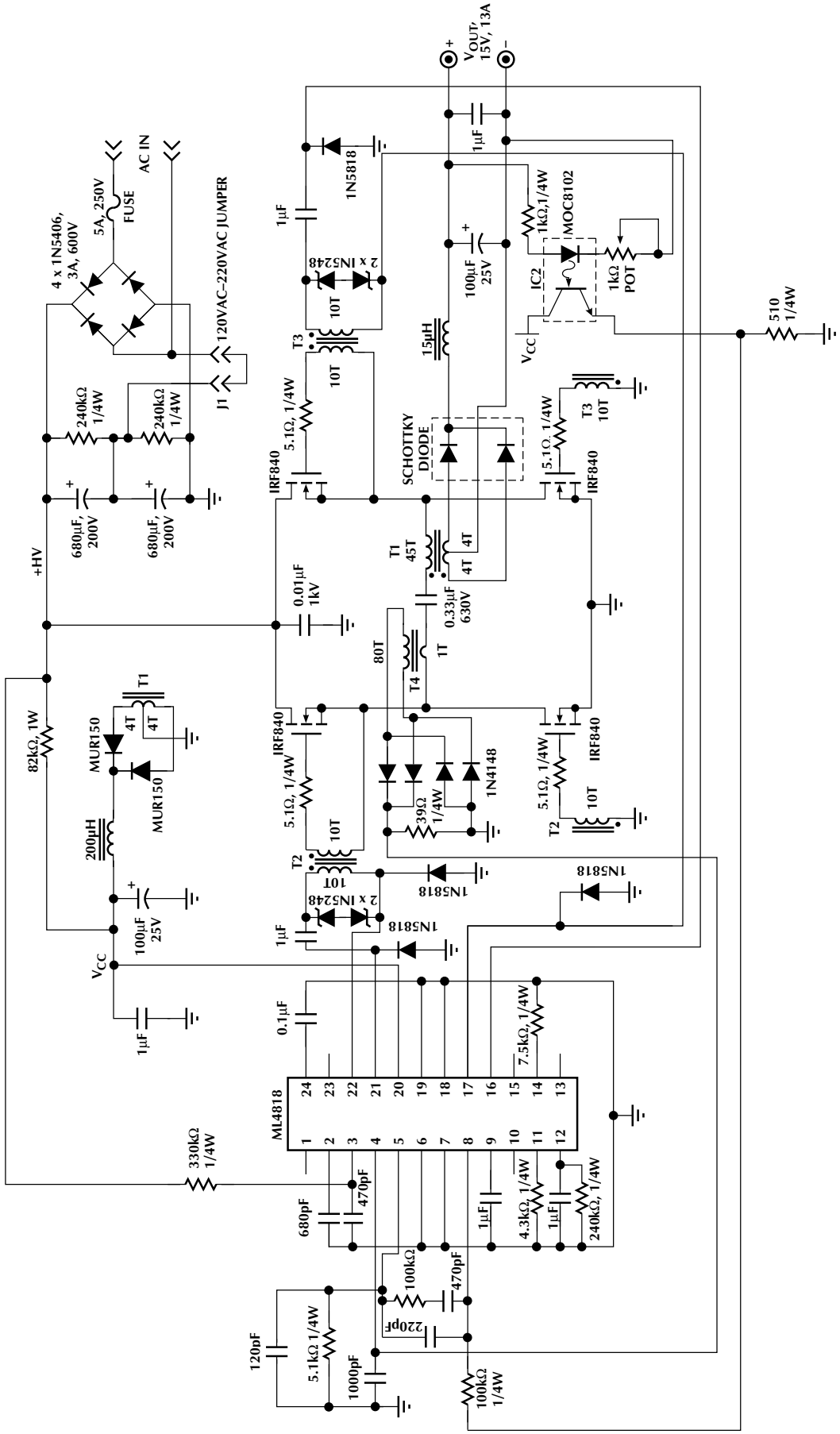
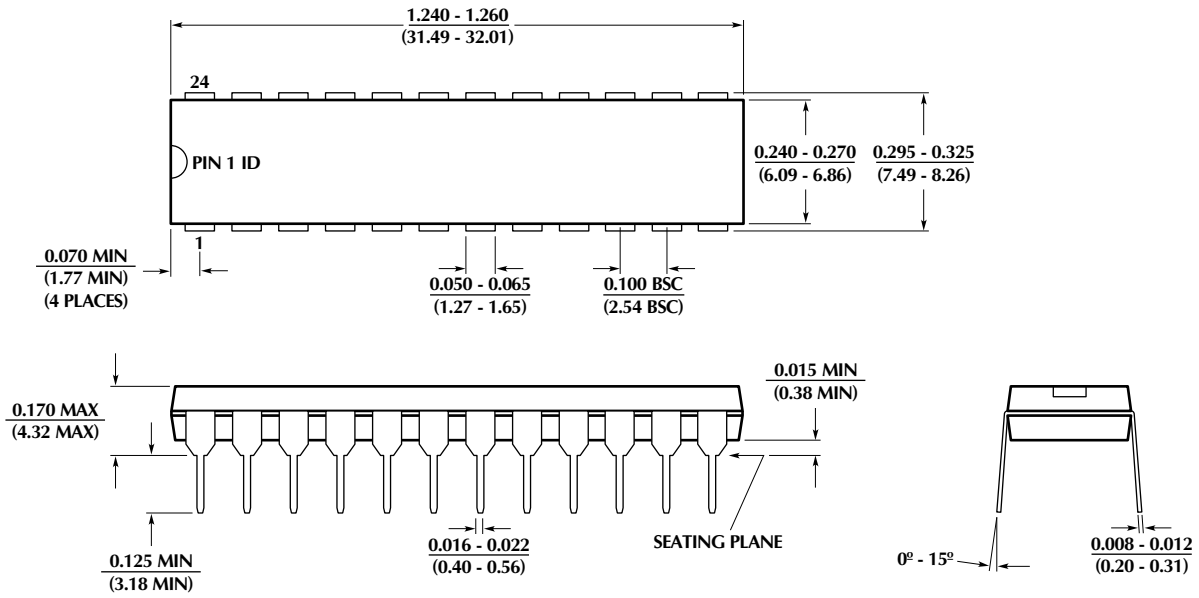


Figure 16. Offline Full Bridge Converter.

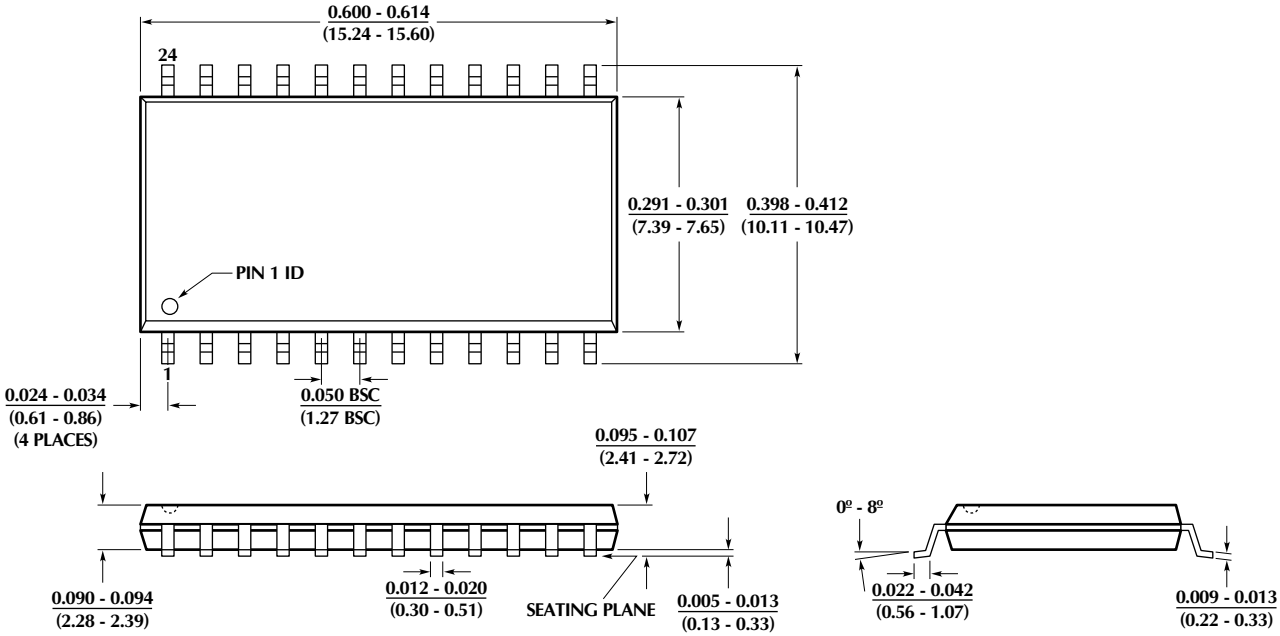
PHYSICAL DIMENSIONS inches (millimeters)

Package: P24N
24-Pin Narrow PDIP



PHYSICAL DIMENSIONS inches (millimeters)

Package: S24
24-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4818CP	0°C to 70°C	Power DIP (P24)
ML4818CS	0°C to 70°C	SOIC (S24W) (Obsolete)

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