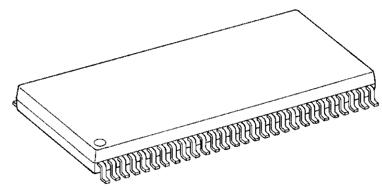
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16652FT

LOW VOLTAGE 16-BIT BUS TRANSCEIVER / REGISTER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16652FT is a high parformance CMOS 16-bit BUS TRANSCEIVER / REGISTER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.
This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25 g (Typ.)

FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6 V
- High Speed Operation : t_{pd} = 2.9 ns (max) at V_{CC} = 3.0~3.6 V
  : t_{pd} = 3.5 ns (max) at V_{CC} = 2.3~2.7 V
  : tpd = 7.0 ns (max) at V_{CC} = 1.8 V
- 3.6 V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±24 mA (min) at V_{CC} = 3.0 V
  : I_{OH} / I_{OL} = ±18 mA (min) at V_{CC} = 2.3 V
  : I_{OH} / I_{OL} = ±6 mA (min) at V_{CC} = 1.8 V
- Latch-up Performance : ±300 mA
- ESD Performance : Human Body Model > ±2000 V
  : Machine Model > ±200 V
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5 V and 3.3 V signals.
- Power Down Protection is provided on all inputs and outputs
- Supports live insertion / withdrawal (Note 3)

(Note 1) : Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
(Note 2) : All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.
(Note 3) : To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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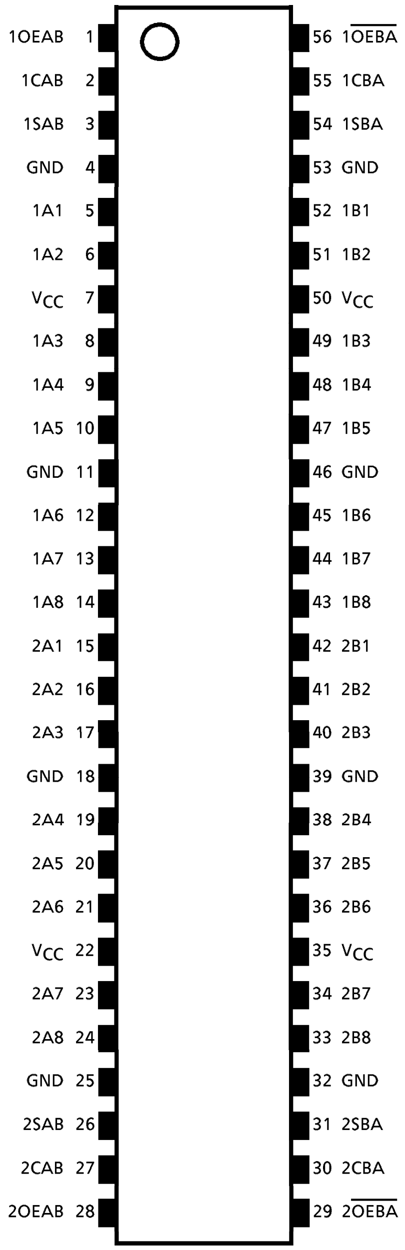
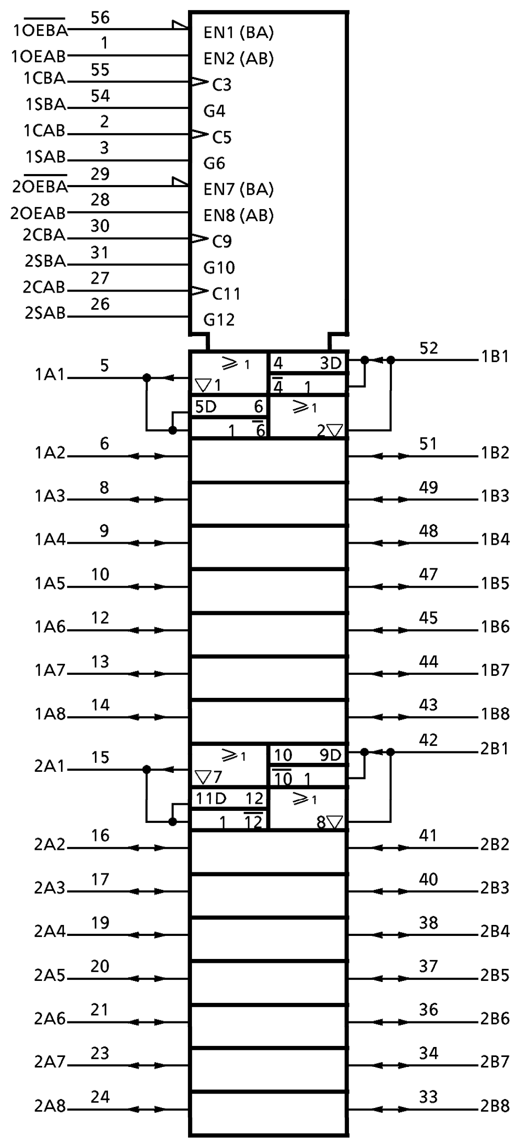
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



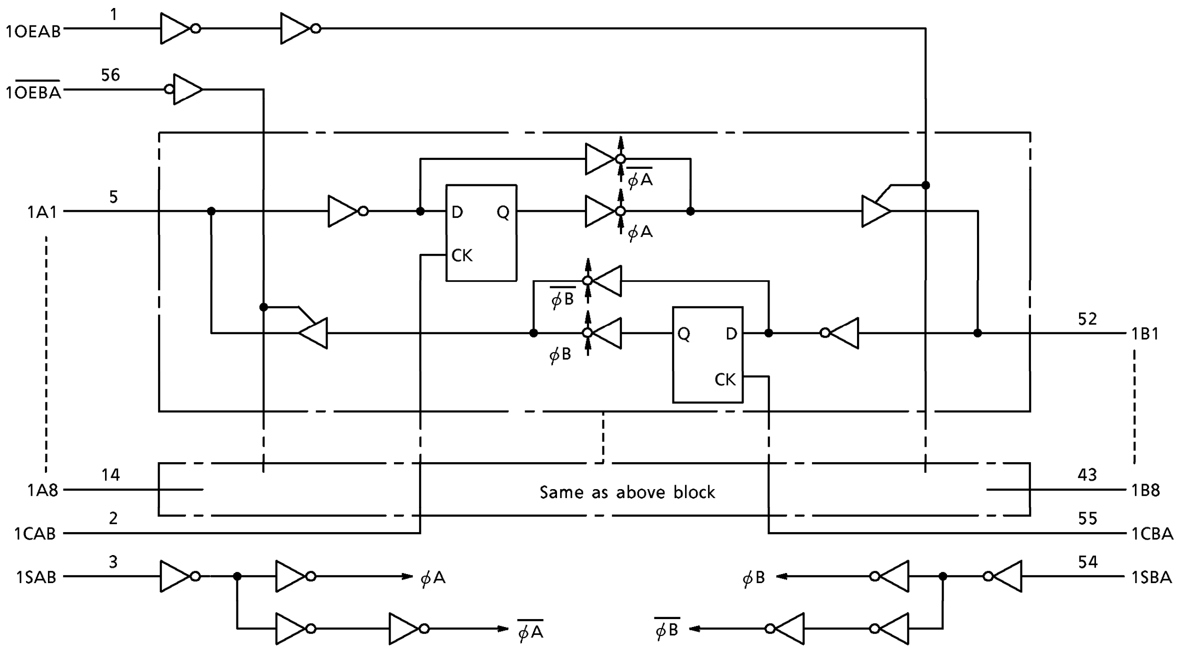
TRUTH TABLE

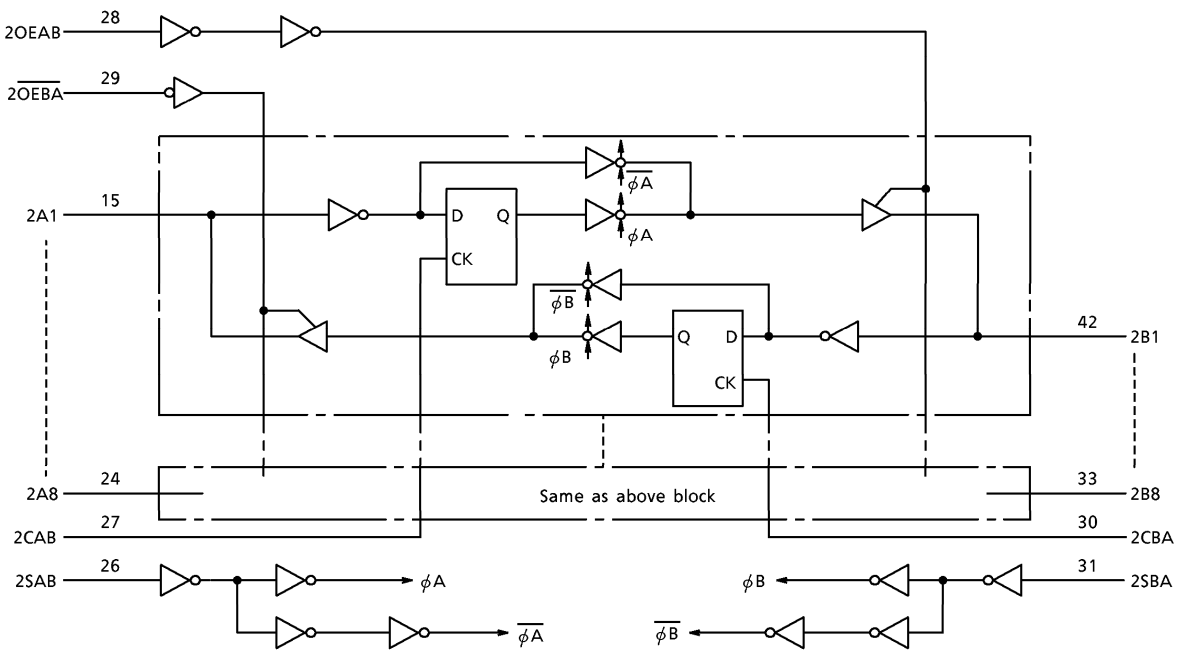
CONTROL INPUTS						BUS		FUNCTION
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A	B	
L	H	X*	X*	X	X	INPUT	INPUT	The output functions of A and B Busses are disabled.
						Z	Z	
		↑	↑	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUT	OUTPUT	The data on the A bus are displayed on the B bus.
						L	L	
						H	H	
		↑	X*	L	X	L	L	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
						H	H	
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		↑	X*	H	X	L	L	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
						H	H	
L	L	X*	X*	X	L	OUTPUT	INPUT	The data on the B Bus are displayed on the A bus.
						L	L	
						H	H	
		X*	↑	X	L	L	L	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
						H	H	
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↑	X	H	L	L	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
						H	H	
H	L	X*	X*	H	H	OUTPUT	OUTPUT	The data in the A storage flop-flops are displayed on the B Bus, and the data in the B storage flop-flops are displayed on the A.
						Qn	Qn	

X : Don’t care
Z : High Impedance
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

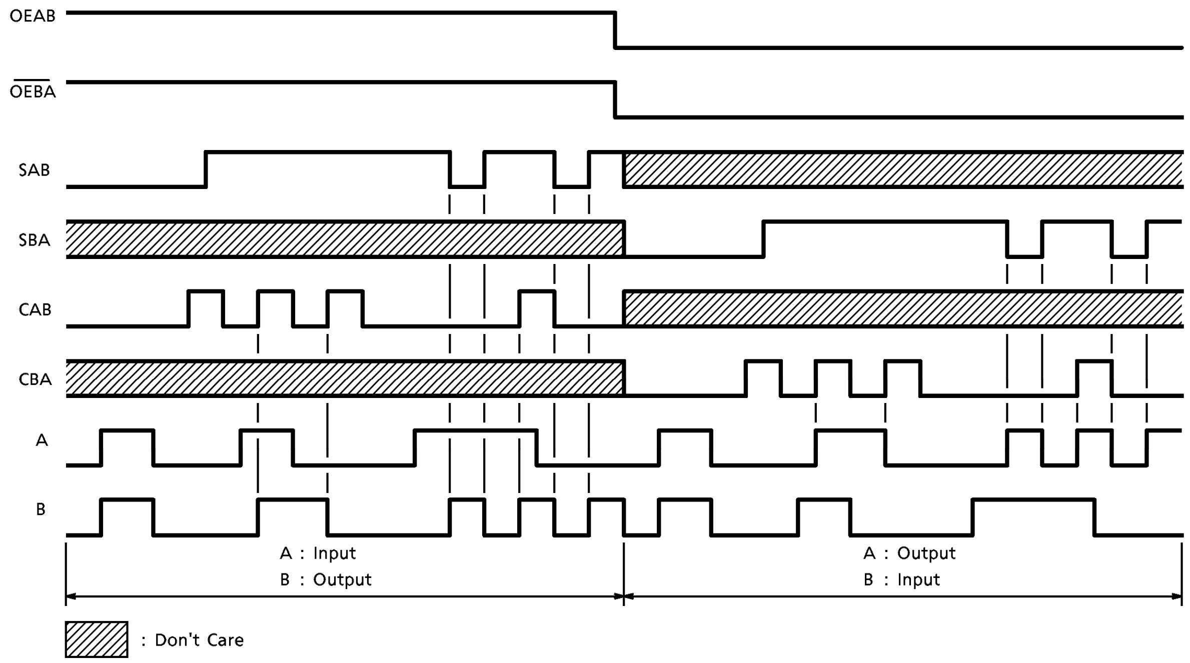
* The clocks are not internally gated with either OEAB or $\overline{OEBA}$. Therefore, data on the A and / or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM





TIMING CHART



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	−0.5~4.6	V
DC Input Voltage (OEAB, $\overline{OEBA}$, SAB, SBA, CAB, CBA)	V_{IN}	−0.5~4.6	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~4.6 (Note 1)	V
		−0.5~V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC}/Ground Current Per Supply Pin	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) : Off-State
(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (OEAB, $\overline{OEBA}$, SAB, SBA, CAB, CBA)	V_{IN}	−0.3~3.6	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	±24 (Note 7)	mA
		±18 (Note 8)	
		±6 (Note 9)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) : Data Retention Only
(Note 5) : Off-State
(Note 6) : High or Low State
(Note 7) : V_{CC} = 3.0~3.6 V
(Note 8) : V_{CC} = 2.3~2.7 V
(Note 9) : V_{CC} = 1.8 V
(Note 10) : V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 2.7 V < V_{CC} ≦ 3.6 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7~3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	V
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 18 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~3.6 V		2.7~3.6	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7~3.6	—	±20.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7~3.6	—	750	μA

ELECTRICAL CHARACTERISTICS
DC characteristics (Ta = −40~85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.3~2.7	1.6	—	V
	"L" Level	V_{IL}			2.3~2.7	—	0.7	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.3~2.7	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	2.3	2.0	—	
				I_{OH} = −12 mA	2.3	1.8	—	
				I_{OH} = −18 mA	2.3	1.7	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3~2.7	—	0.2	V
				I_{OL} = 12 mA	2.3	—	0.4	
				I_{OL} = 18 mA	2.3	—	0.6	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.3~2.7	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~3.6 V		2.3~2.7	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.3~2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3~2.7	—	±20.0	

ELECTRICAL CHARACTERISTICS
DC characteristics (Ta = −40~85°C, 1.8 V ≦ V_{CC} < 2.3 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	0.7 × V_{CC}	—	V
	"L" Level	V_{IL}			1.8~2.3	—	0.2 × V_{CC}	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	1.8	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	1.8	1.4	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	V
				I_{OL} = 6 mA	1.8	—	0.3	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		1.8	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0~3.6 V		1.8	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		1.8	—	±20.0	

AC characteristics (Ta = −40~85°C, Input t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	(Fig.1, 3)	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	7.0	ns
			2.5 ± 0.2	0.8	3.5	
			3.3 ± 0.3	0.6	2.9	
Propagation Delay Time (CAB, CBA-Bn, An)	t_{pLH} t_{pHL}	(Fig.1, 3)	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.4	
			3.3 ± 0.3	0.6	3.2	
Propagation Delay Time (SAB, SBA-Bn, An)	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.4	
			3.3 ± 0.3	0.6	3.5	
Output Enable Time (OEAB, $\overline{OEBA}$-An, Bn)	t_{pZL} t_{pZH}	(Fig.1, 4, 5)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
Output Disable Time (OEAB, $\overline{OEBA}$-An, Bn)	t_{pLZ} t_{pHZ}	(Fig.1, 4, 5)	1.8	1.5	8.1	ns
			2.5 ± 0.2	0.8	4.5	
			3.3 ± 0.3	0.6	3.9	
Minimum Pulse Width	$t_{w (H)}$ $t_{w (L)}$	(Fig.1, 3)	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time	t_s	(Fig.1, 3)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Hold Time	t_h	(Fig.1, 3)	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	0.25	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	0.6	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	−0.25	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	−0.6	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	−0.8	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	1.5	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	1.9	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	2.2	

(Note 12) : Parameter guaranteed by design.

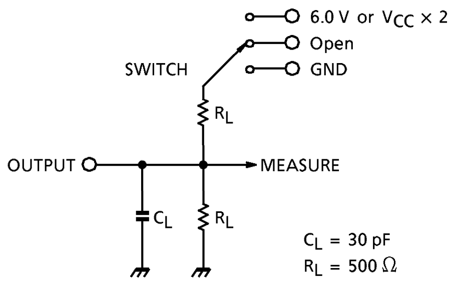
Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Input Capacitance	C_{IN}	OEAB, $\overline{OEBA}$, SAB, SBA, CAB, CBA	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	$C_{I/O}$	An, Bn	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10$ MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

TEST CIRCUIT

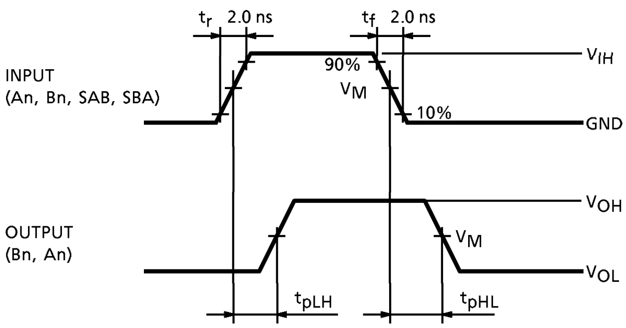
Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @V_{CC} = 3.3 ± 0.3 V V_{CC} × 2 @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}



SYMBOL	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Fig.3 t_{pLH}, t_{pHL}, t_w, t_s, t_h

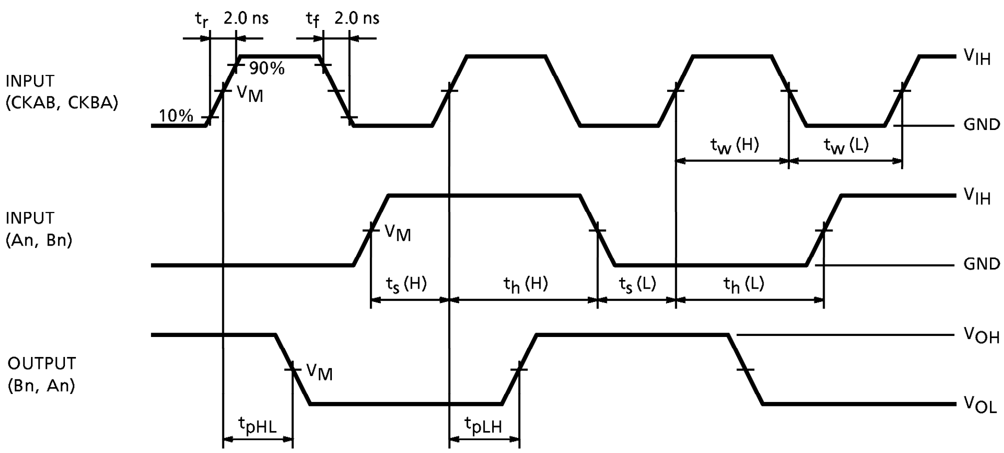


Fig.4 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

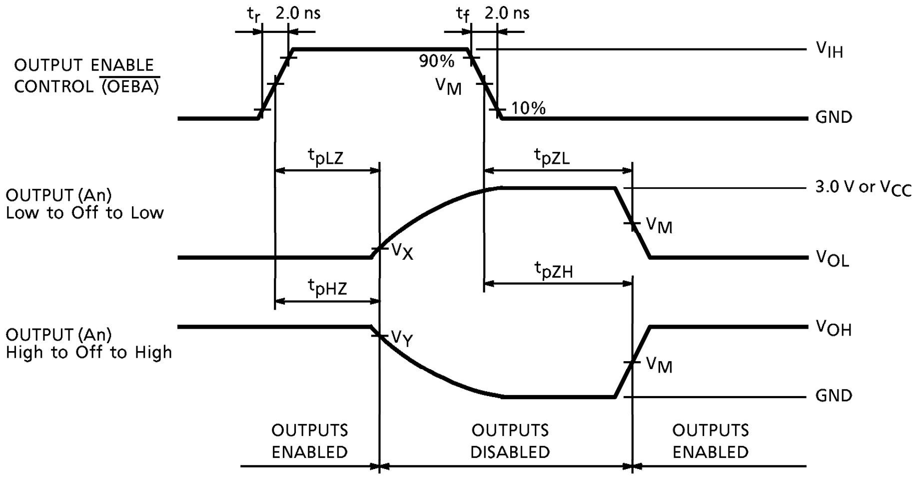
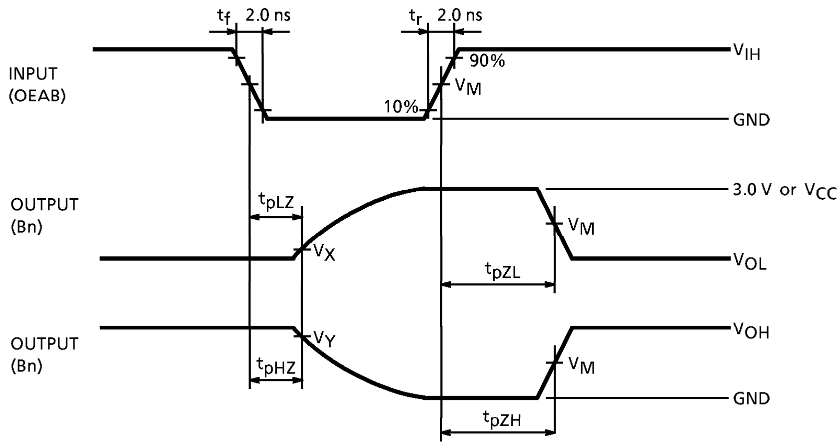
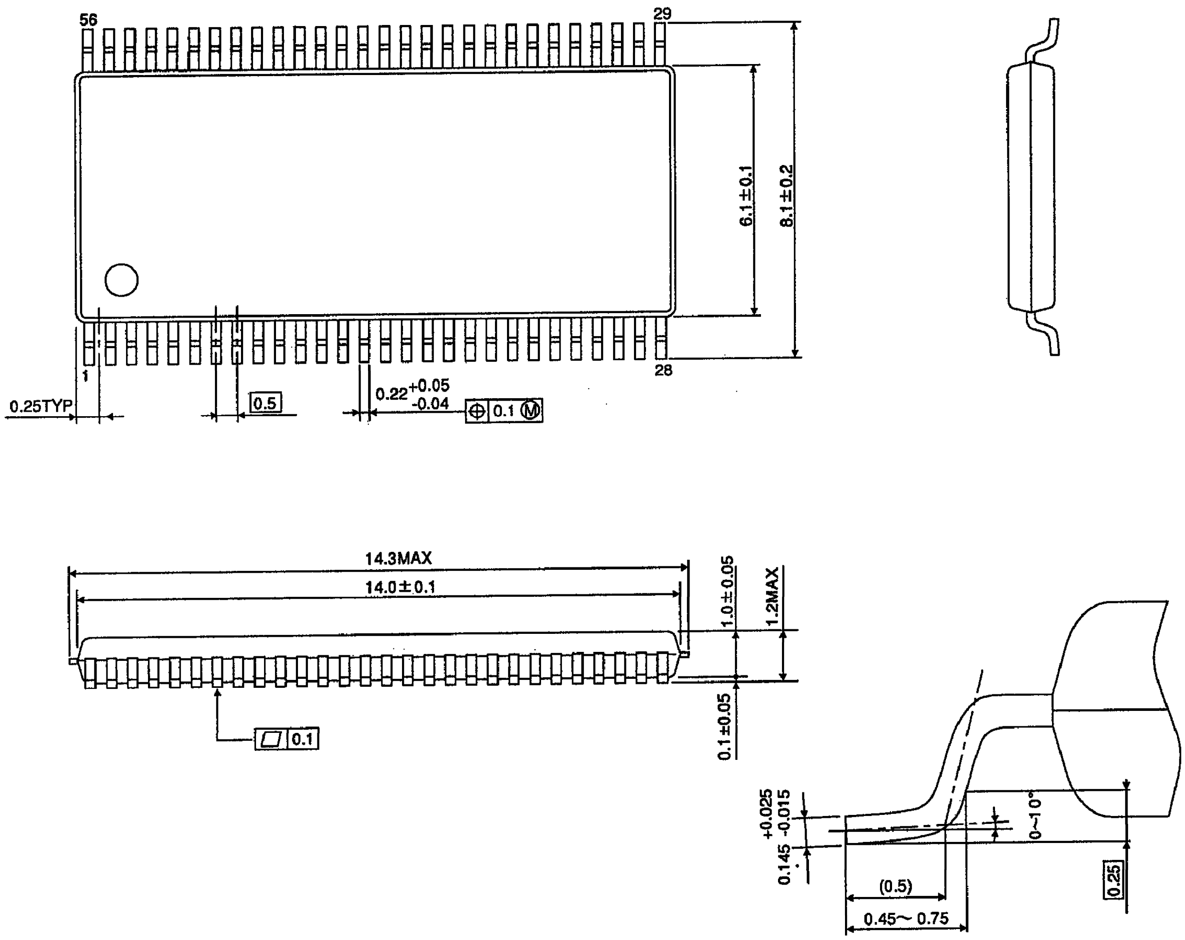


Fig.5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



PACKAGE DIMENSIONS
TSSOP56-P-0061-0.50 Unit : mm



Weight : 0.25 g (Typ.)