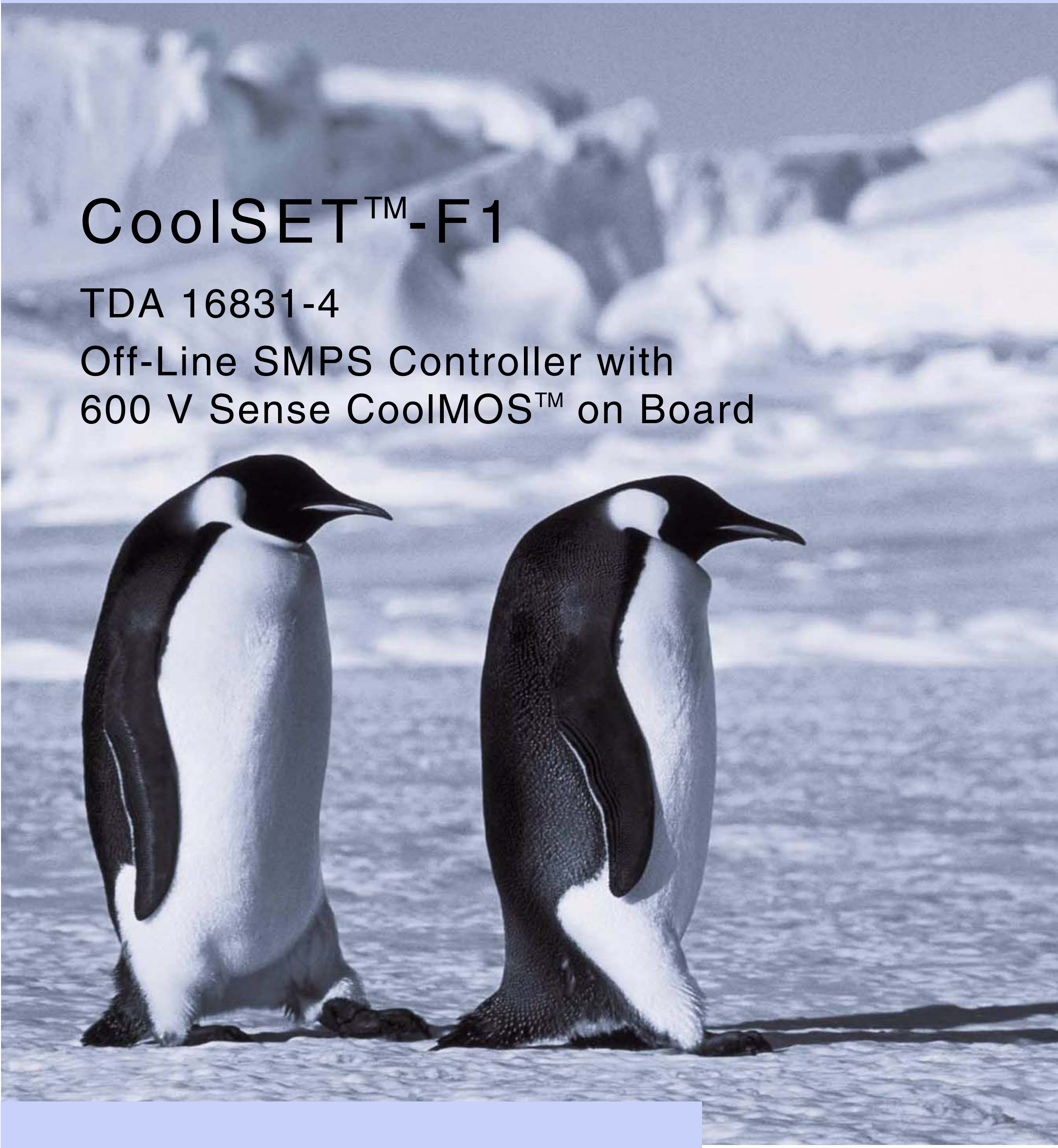
Data Sheet, Aug. 2002



CoolSET™-F1

TDA 16831-4

Off-Line SMPS Controller with 600 V Sense CoolMOS™ on Board

Power Management & Supply

Never stop thinking.

Revision History:	2002-08-08	DS0
Previous Version:	1999-12-10	

Page	Subjects (major changes since last revision)
4	Update of available types.

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Off-Line SMPS Controller with 600 V Sense CoolMOS™ on Board

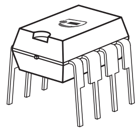
TDA 16831-4

CoolSET

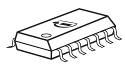
1 Overview

1.1 Features

- PWM controller + sense CoolMOS attached in one compact package
- 600 V avalanche rugged CoolMOS
- Typical R_{DSon} = 0.5 ... 3.5 Ω at T_j = 25°C
- Only 4 active Pins
- Standard DIP-8 Package for Output Power ≤40 W
- Only few external components required
- Low start up current
- Current mode control
- Input Undervoltage Lockout
- Max. Duty Cycle limitation
- Thermal Shutdown
- Modulated Gate Drive for low EMI



P-DIP-8-6



P-DSO-14-11

Type	Ordering Code	Package
TDA 16831	Q67000-A9420	P-DIP-8-6
TDA 16832	Discontiued[1)]	P-DIP-8-6
TDA 16833	Q67000-A9389	P-DIP-8-6
TDA 16834	Discontiued[1)]	P-DIP-8-6
TDA 16831G	Q67000-A9421	P-DSO-14-11
TDA 16832G	Discontiued[1)]	P-DSO-14-11
TDA 16833G	Q67000-A9419	P-DSO-14-11

1) Last ordering:28.02.2003
Last delivery:31.08.2003

Device	Output Power Range/Required Heatsink[1]	
	V_{in} = 85-270 VAC	V_{in} = 190-265 VAC
TDA 16831	10 W / no heatsink	10 W / no heatsink
TDA 16832	20 W / 6 cm^2	20 W / no heatsink
TDA 16833	30 W / 3 cm^2	40 W / no heatsink
TDA 16834	40 W / 3 cm^2	40 W / no heatsink
TDA 16831G	10 W / no heatsink	10 W / no heatsink
TDA 16832G	20 W / 8 cm^2	20 W / no heatsink
TDA 16833G	20 W / no heatsink	40 W / 3 cm^2

[1] T_A = 70°C

1.2 Pin Configurations

1.2.1 P-DIP-8-6 for Applications with $P_{OUT} \leq$ 40 W: TDA 16831/2/3/4

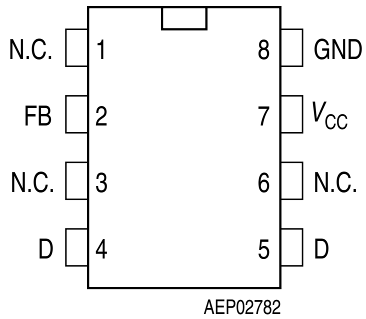


Figure 1 TDA 16831/2/3/4

Pin Definitions and Functions

Pin	Symbol	Function
1	N.C.	Not Connected
2	FB	PWM Feedback Input
3	N.C.	Not Connected
4	D	600 V Drain CoolMOS
5	D	600 V Drain CoolMOS
6	N.C.	Not Connected
7	V_{CC}	PWM Supply Voltage
8	GND	PWM GND and Source of CoolMOS

1.2.2 P-DSO-14-11 for Applications with $P_{OUT} \leq 20$ W: TDA 16831G/2G/3G

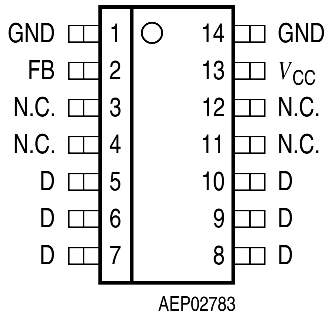


Figure 2 TDA 16831G/2G/3G

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	PWM GND and CoolMOS Source
2	FB	PWM Feedback Input
3	N.C.	Not Connected
4	N.C.	Not Connected
5, 6, 7	D	600 V Drain CoolMOS
8, 9, 10	D	600 V Drain CoolMOS
11	N.C.	Not Connected
12	N.C.	Not Connected
13	V_{CC}	PWM Supply Voltage
14	GND	PWM GND and Source of CoolMOS

1.3 Block Diagram

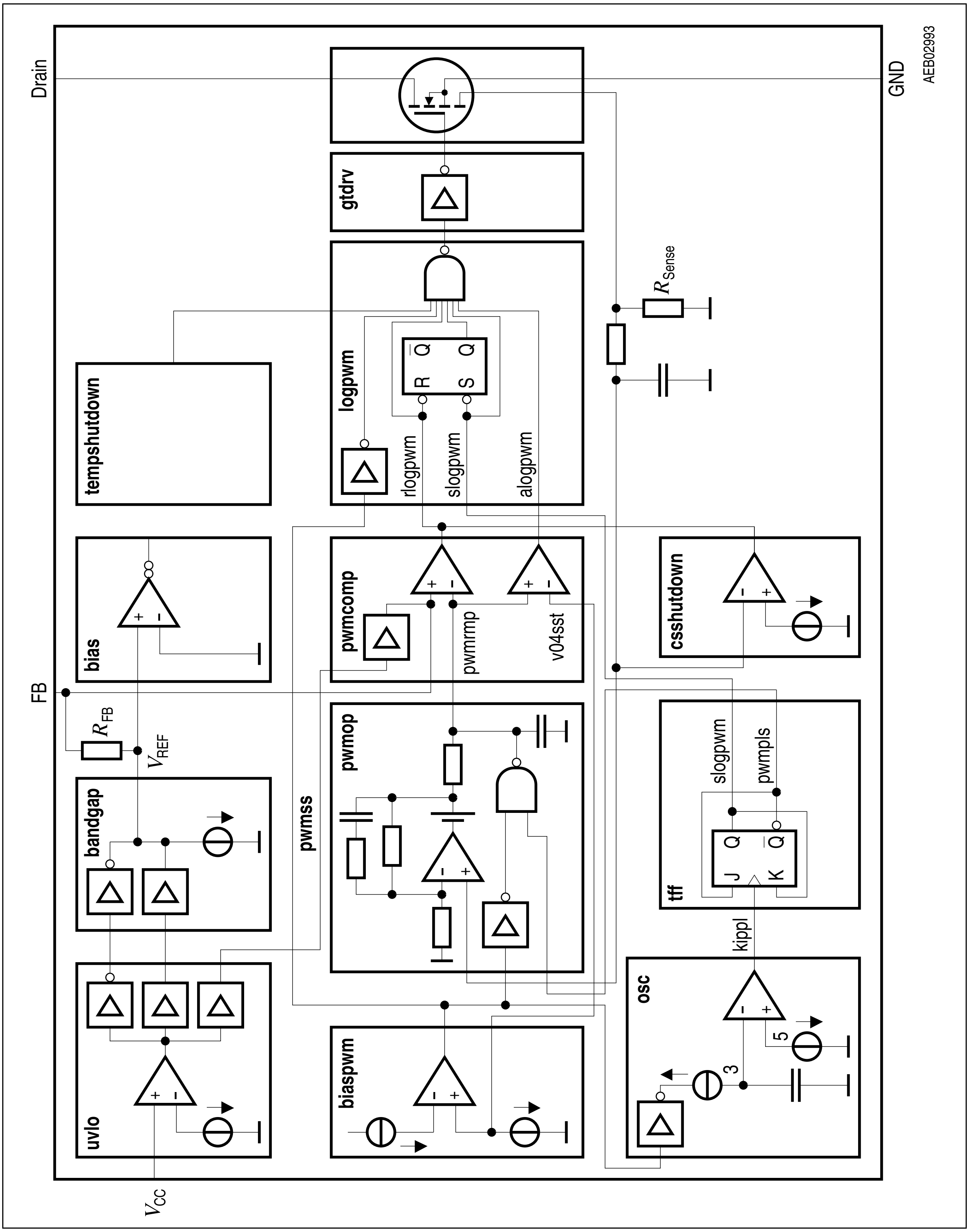


Figure 3 Block Diagram

2 Circuit Description

The TDA 16831-4 is a current mode pulse width modulator with integrated sense CoolMOS transistor. It fulfills the requirements of minimum external control circuitry for a flyback application.

Current mode control means that the current through the MOS transistor is compared with a reference signal derived from the output voltage of the flyback application. The result of that comparison determines the on time of the MOS transistor.

To minimize external circuitry the sense resistor which gives information about MOS current is integrated. The oscillator resistor and capacitor which determine the switching frequency are integrated, too. Special efforts have been made to compensate temperature dependency and to minimize tolerances of this resistor.

The circuit in detail: (see **Figure 3**)

Start Up Circuit (uvlo)

Uvlo is monitoring the external supply voltage V_{CC}. When V_{CC} is exceeding the on threshold V_{CCH} = 12 V, the bandgap, the bias circuit and the soft start circuit are switched on. When V_{CC} is falling below the off-threshold V_{CCL} = 9 V the circuit is switched off. During start up the current consumption is about 30 µA.

Bandgap (bg)

The bandgap generates an internal very accurate reference voltage of 5.5 V to supply the internal circuits.

Current Source (bias)

The bias circuit provides the internal circuits with constant current.

Oscillator (osc)

The oscillator is generating a frequency twice the switching frequency f_{switch} = 100 kHz. Resistor, capacitor and current source which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor is internally trimmed, in order to achieve a very accurate switching frequency. Temperature coefficient of switching frequency is very low (see **Page 18**).

Divider Flip Flop (tff)

Tff is a flip flop which divides the oscillator frequency by one half to create the switching frequency. The maximum duty cycle is set to Dmax = 0.5.

Current Sense Amplifier (pwmop)

The positive input of the pwmop is applied to the internal sense resistor. With the internal sense resistor (R_{sense}) the sensed current coming from the CoolMOS is converted into a sense voltage. The sense voltage is amplified with a gain of 32 dB. The amplified sense voltage is connected to the negative input of the pwm comparator. Each time when the CoolMOS transistor is switched on, a current spike is superposed to the true current information. To eliminate this current spike the sense voltage is smoothed via an internal resistor capacitor network with a time constant of T_{d1} = 100 ns. This is the first leading edge blanking and only a small spike is left. To reduce this small spike the current sense amplifier is creating a virtual ramp at the output. This is done by a second resistor capacitor network with T_{d2} = 100 ns and an op-offset of 0.8 V which is seen at the output of the amplifier. When gate drive is switched off the output capacitor is discharged via pulse signal pwmpls. The oscillator signal slogpwm sets the RS-flip-flop. The gate drive circuit is switched on, when capacitor voltage exceeds the internal threshold of 0.4 V. This leads to a linear ramp, which is created by the output of the amplifier. Therefore duty cycle of 0% is possible. The amplifier is compensated through an internal compensation network.

The transfer function of the amplifier can be described as

$$\frac{V_o}{V_i} = \frac{K_i}{p \times (1 + T \times p)};\ p = j\omega$$

the step response is described with

$$V_o = V_i \times K_i \times \left(t_{on} - T + T \times e^{\frac{-t_{on}}{T}} \right)$$

$$K_i = \frac{40}{t_{on}}$$

$$T = 850\ \text{ns}$$

Comparator (pwmcomp)

The comparator pwmcomp compares the amplified current signal pwmrmp of the CoolMOS with the reference signal pwmin. Pwmin is created by an external optocoupler or external transistor and gives the information of the feedback circuitry. When the pwmrmp exceeds the reference signal pwmin the comparator switches the CoolMOS off.

Logic (logpwm)

The logic logpwm comprises a RS-flip-flop and a NAND-gate. The NAND-gate insures that CoolMOS transistor is only switched on when sosta is on and pwmin has exceeded minimum threshold and pwmin is below pwmrmp and currentshutdown is off and tempshutdown is off and tff sets the starting impulse. CoolMOS transistor is switched off when pwmrmp exceeds pwmin or duty cycle exceeds 0.5 or pwmcs exceeds I_{max} or silicon temperature exceeds T_{max} or uvlo is going below threshold. The RS-flip-flop ensures that with every frequency period only one switch on can occur (double pulse suppression).

Gate Drive (gtdrv)

Gtdrv is the driver circuit for the CoolMOS and is optimized to minimize EMI influences and to provide high circuit efficiency. This is done by smoothing the switch on slope when reaching the CoolMOS threshold. Leading switch on spike is minimized then. When CoolMOS is witched off, the falling slope of the gate driver is slowed down when reaching 2 V. So an overshoot below ground can't occur. Also gate drive circuit is designed to eliminate cross conduction of the output stage.

Current Shut Down (cssd)

Current shut down circuit switches the CoolMOS immediately off when the sense current is exceeding an internal threshold of 100 mV at R_{sense}.

Tempshutdown (tsd)

Tempshutdown switches the CoolMOS off when junction temperature of the PWM controller is exceeding an internal threshold.

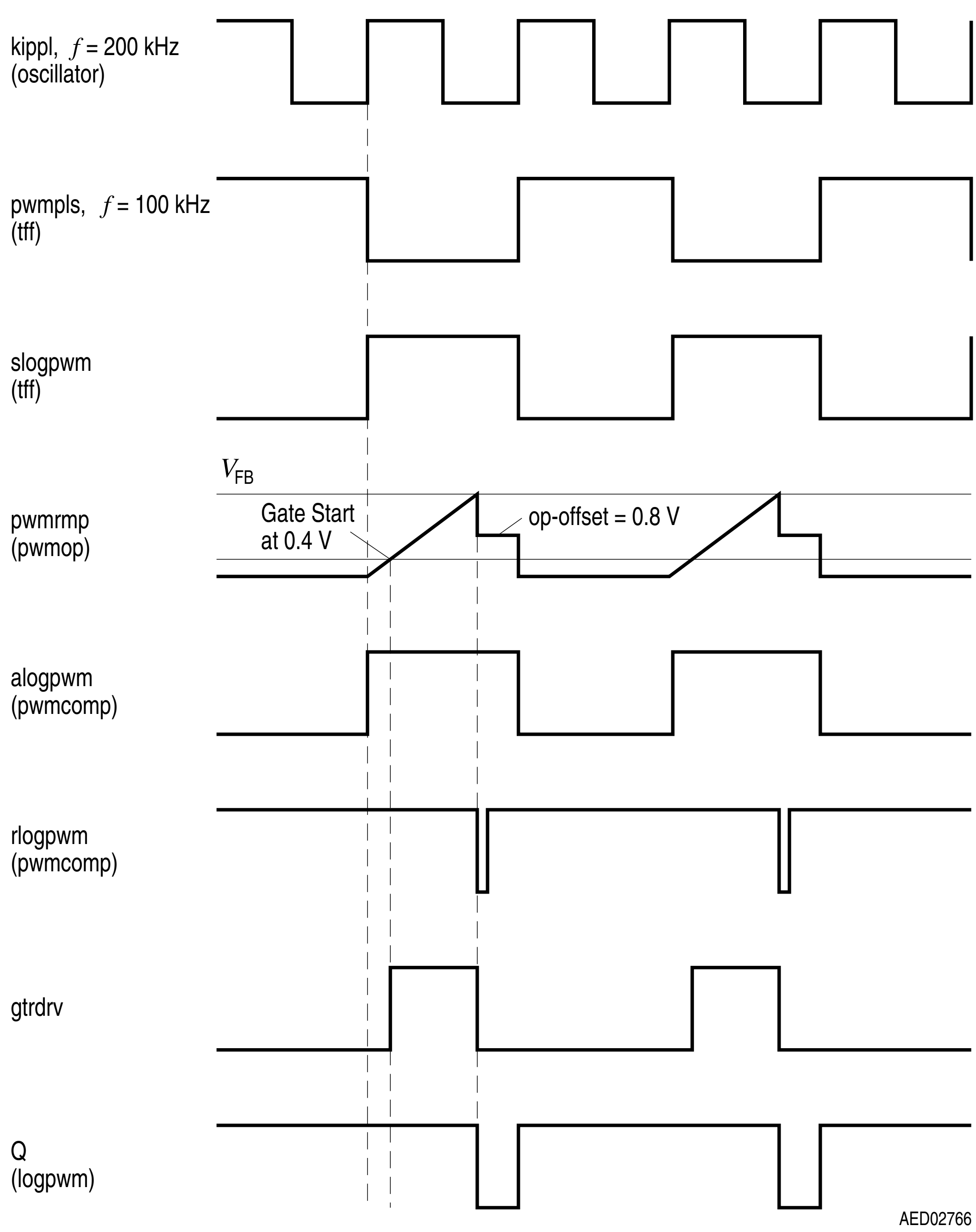


Figure 4 Signal Diagram

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply Voltage	V_{CC}	-0.3	V_Z	V	Zener Voltage[1]
Supply + Zener Current	I_{CCZ}	0	20	mA	**Page 14** Beware of P_{max}[2]
Drain Source Voltage	V_{DS}		600	V	
Avalanche Current	I_{AC}		$I_{csthmax}$	A	t = 100 ns
Voltage at FB	V_{FB}	-0.3	5.5	V	
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_{stg}	-50	150		
Thermal Resistance System-Air	R_{thSA}		90	K/W	P-DIP-8-6
			125		P-DSO-14-11

[1] Be aware that V_{CC} capacitor is discharged before IC is plugged into the application board.

[2] Power dissipation should be observed.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply Voltage	V_{CC}	V_{CCH}	V_Z	V	
Junction Temperature	T_j	-25	120	°C	

3.3 Supply Section

-25°C < T_j < 120°C, V_{CC} = 15 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Quiescent Current	I_{CCL}		25	80	µA	
Supply Current Active	I_{CCHA}		4.5	6	mA	TDA 16831/2/G
			6	7.5		TDA 16833/G
			7	8.5		TDA 16834
V_{CC} Turn-On Threshold	V_{CCH}		12	12.5	V	
V_{CC} Turn-Off Threshold	V_{CCL}	8.5	9			
V_{CC} Turn-On/Off Hysteresis	V_{CCHY}		3			
V_{CC} Zener Clamp	V_Z	16	17.5	19		
Controller Thermal Shutdown	T_{jSD}	120	135	150	°C	TDA 16831/2/3/G/4
Thermal Hysteresis	T_{jHy}		2			

3.4 Oscillator Section

-25°C < T_j < 120°C, V_{CC} = 15 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Accuracy	f	90	100	110	kHz	
Temperature Coefficient	TK f		1000		ppm/°C	

3.5 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Duty Cycle	D	0		0.5		
Transimpedance ΔV_{FB} / ΔI_{Drain} [1]	Z_{PWM}		4		V/A	TDA 16831/G
			2			TDA 16832/G
			1.3			TDA 16833/G/4
OP Gain Bandwidth[2]	Bw		2		MHz	
OP Phase Margin[2]	Phi_m		70		Degree	
V_{FB} Operating Range min. Level	V_{FBmin}	0.45		0.85	V	for D = 0 $I_{cs} = 0.95\ I_{csth}$
V_{FB} Operating Range max. Level	V_{FBmax}	3.5		4.8		
Feedback Resistance	R_{FB}	3.0	3.7	4.9	KΩ	
Temperature Coefficient R_{FB}	R_{FBTK}		600		ppm/°C	
Internal Reference Voltage	V_{refint}	5.3	5.5	5.7	V	
Temperature Coefficient V_{refint}	V_{reftk}		0.2		mV/°C	

[1] For discontinuous mode the V_{FB} is described by:

$$V_{FB} = Z_{PWM} \times \frac{I_{PK}}{t_{on}} \times \left(t_{on} - T_1 + T_1 \times e^{\frac{-t_{on}}{T_1}} \right) + 0.6 \times \left(1 - e^{\frac{-t_{on}}{T_2}} \right)$$

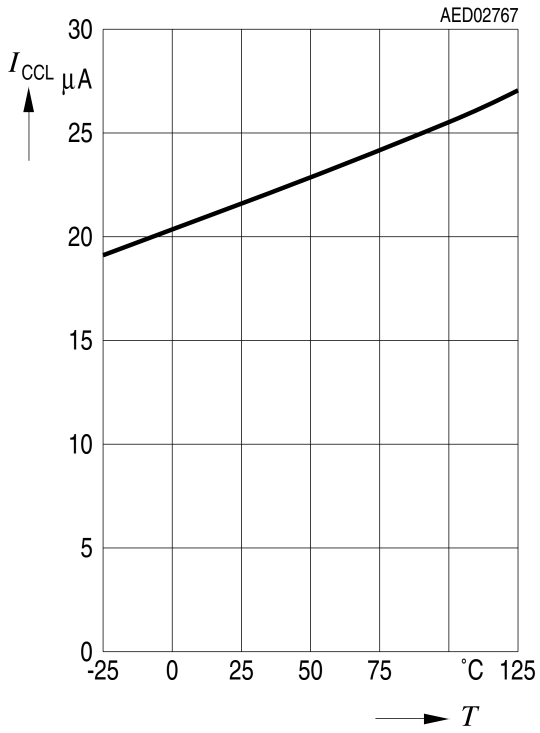
T_1 = 850 ns; T_2 = 200 ns

[2] Guaranteed by design

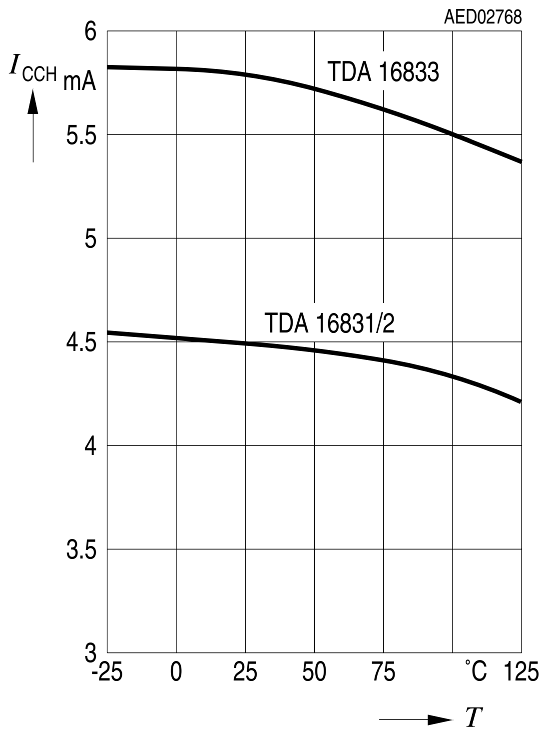
3.6 Output Section

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Drain Source Breakdown Voltage T_A = 25°C	$V_{(BR)DSS}$	600			V	
Drain Source On-Resistance T_A = 25°C	R_{DSon}		3.5		Ω	TDA 16831/2/G
			1			TDA 16833/G
			0.5			TDA 16834
Drain Source On-Resistance -25 < T_A < 120°C	R_{DSon}			9	Ω	TDA 16831/2/G
				2.7		TDA 16833/G
				1.6		TDA 16834
Zero Gate Voltage Drain Current	I_{DSS}		0.5	50	µA	V_{GS} = 0 TDA16833 t_{DR} = 100 ns
Output Capacitance	C_{OSS}		25		pF	
Avalanche Current	I_{AR}		$I_{csthmax}$		A	
I_{source} Current Limit Threshold	I_{csth}	0.6	0.9	1.4	A	TDA 16831/G
		1.2	1.8	2.7		TDA 16832/G
		2.2	2.9	4.8		TDA 16833/G
		2.2	2.9	4.8		TDA 16834
Time Constant I_{csth}	t_{csth}		300		ns	
Rise Time	t_{rise}		70			
Fall Time	t_{fall}		50			

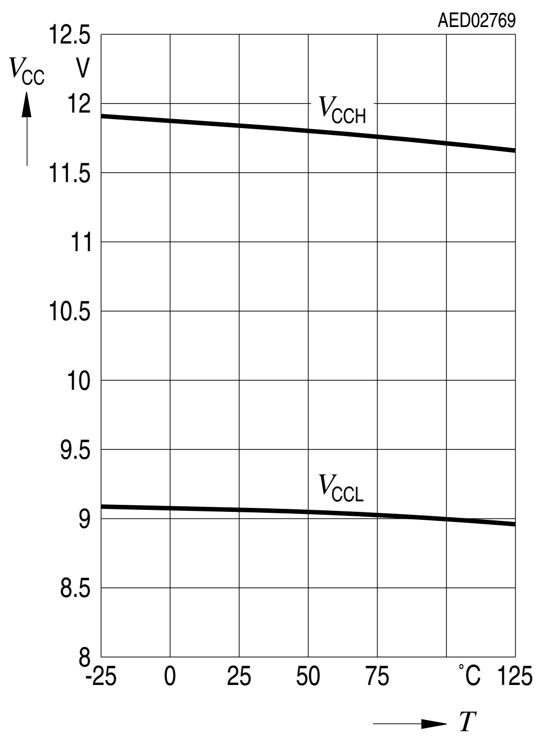
Quiescent Current versus Temperature



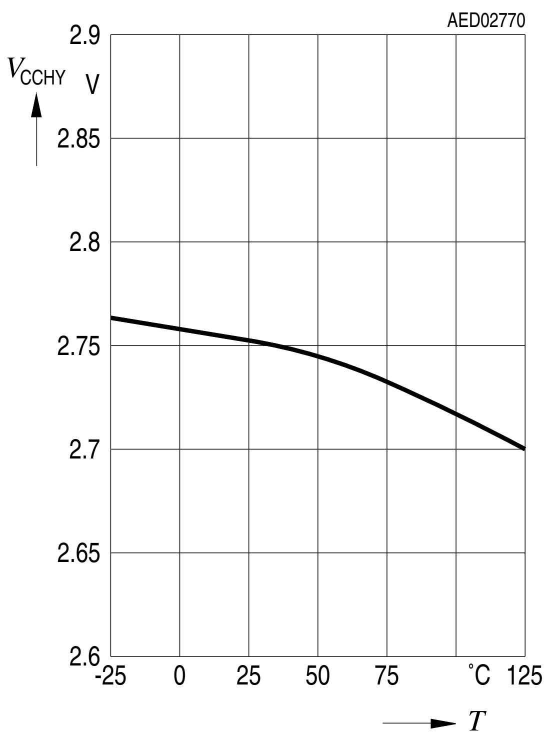
Supply Current Active versus Temperature



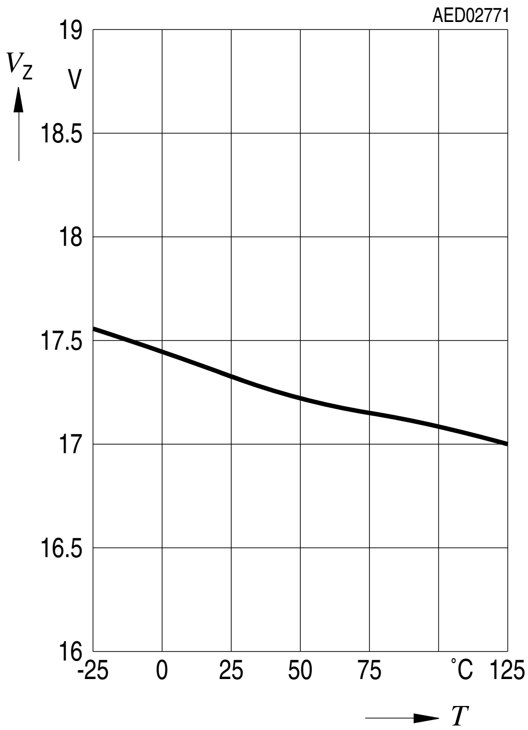
Turn On/Off Supply Voltage versus Temperature



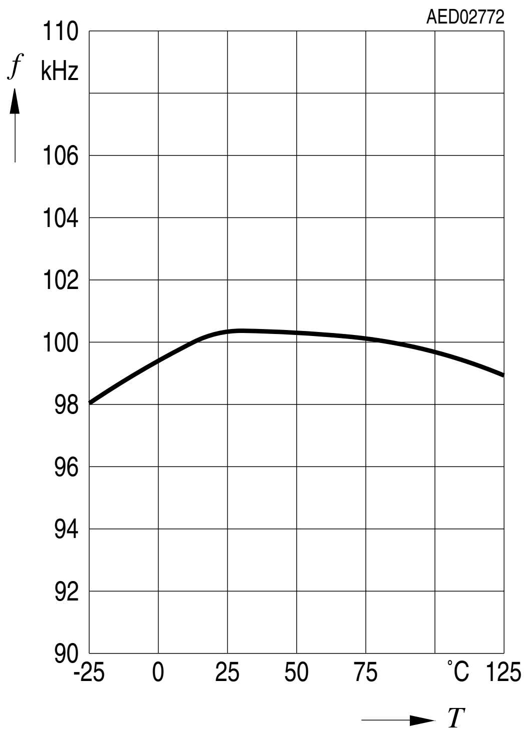
Turn On/Off Hysteresis



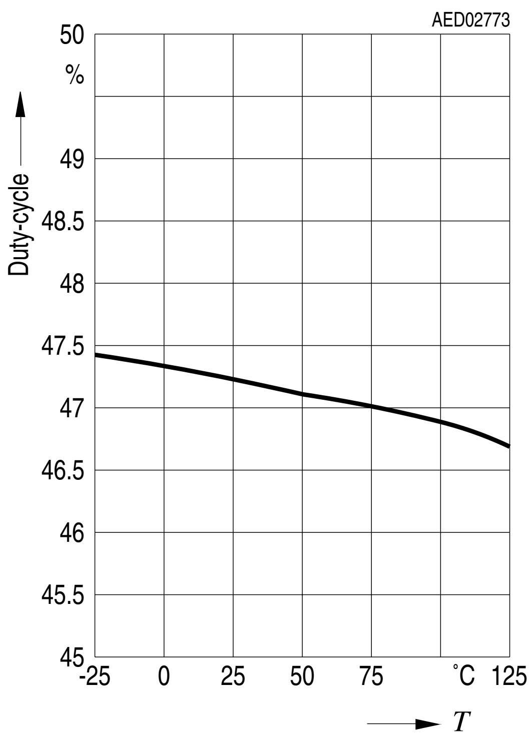
V_{CC} Zener Clamp



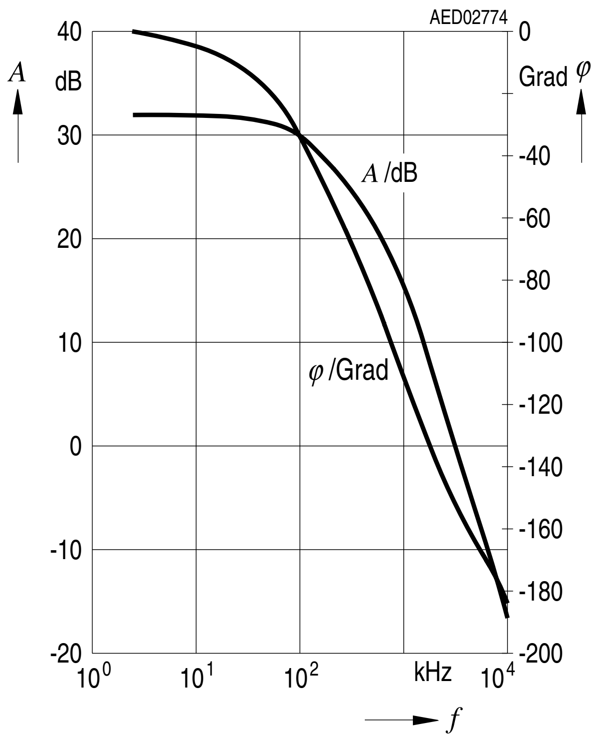
Switching Frequency versus Temperature



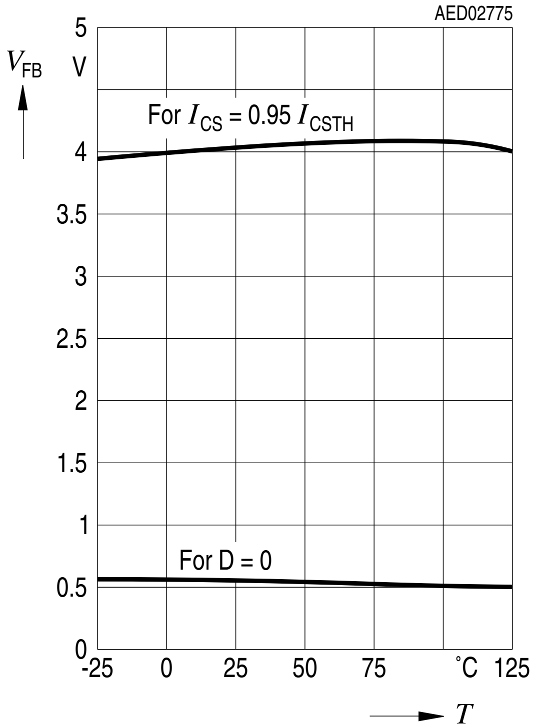
Maximum Duty Cycle versus Temperature TDA 16831/2/3/G/4



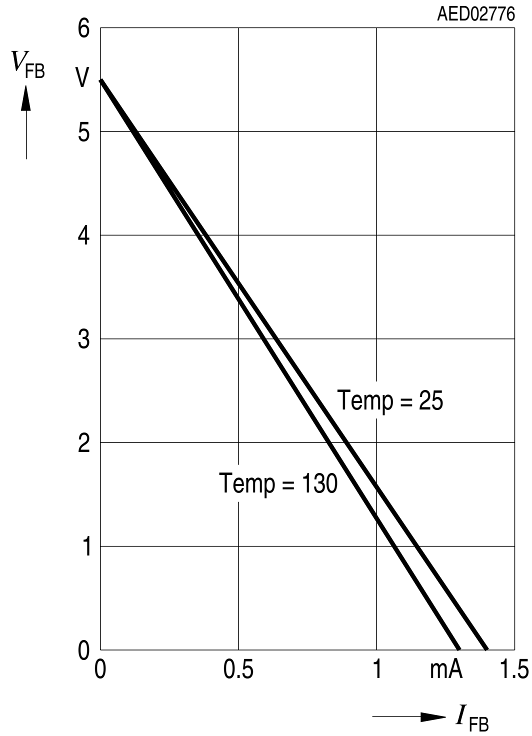
Operational Amplifier Phase and Amplitude versus Frequency



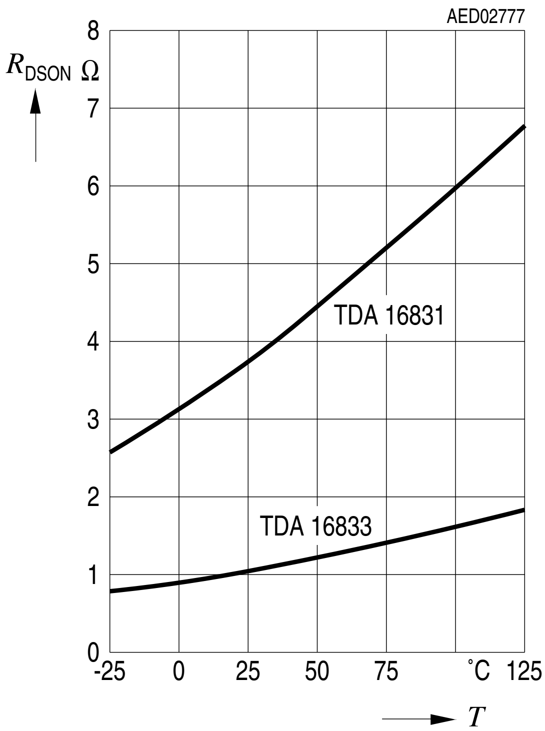
Feedback Voltage Operating Range versus Temperature



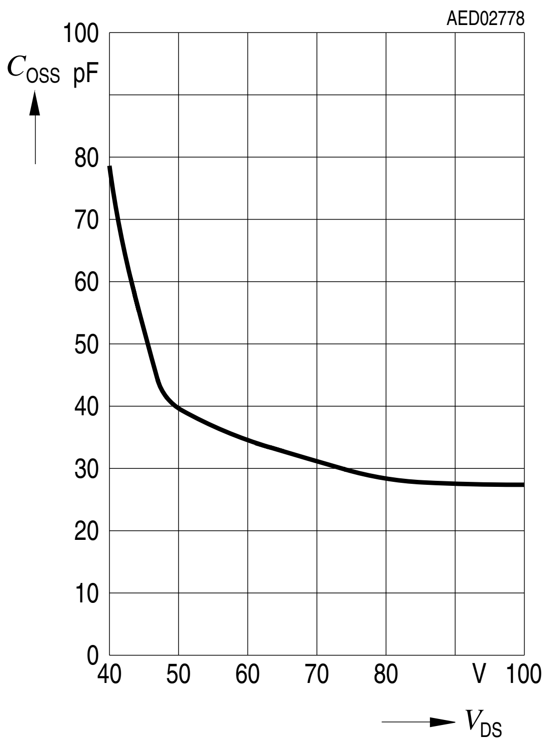
Feedback Voltage versus Feedback Current



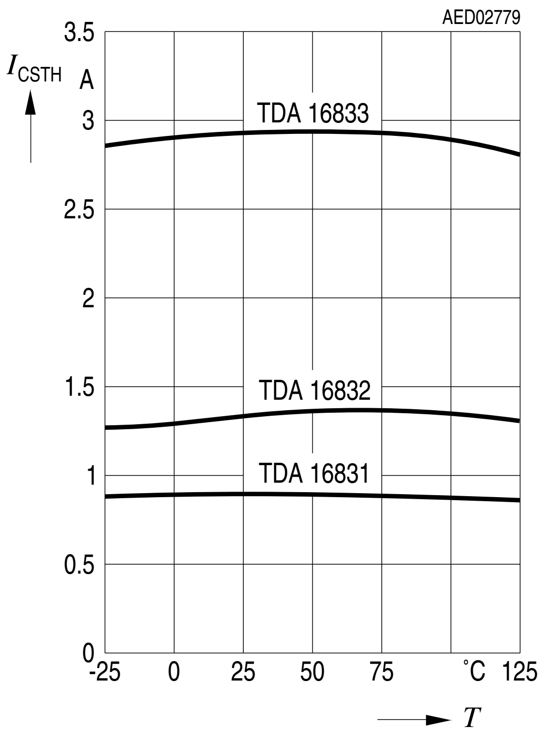
R_{DSon} versus Temperature



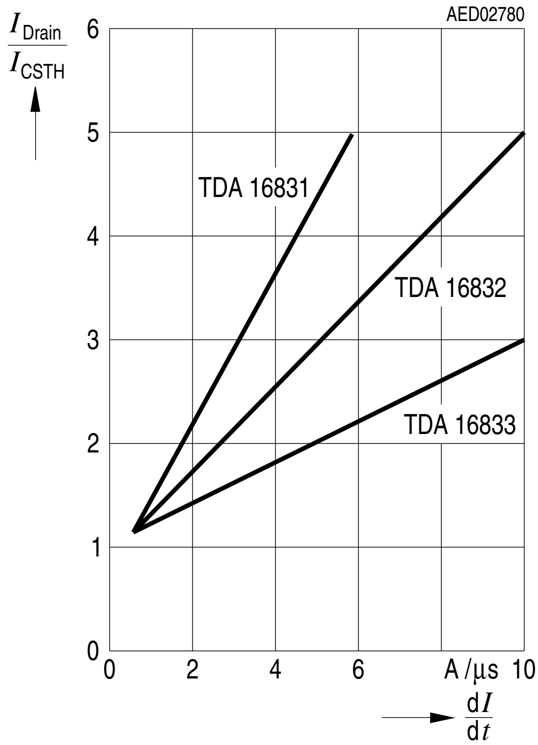
TDA 16833 Output Capacitance C_{OSS} versus V_{DS}



I_{source} Current Limit Threshold I_{csth} versus Temperature



Normalized Overcurrent Shutdown versus Drain Current Slope



4 Application Circuit

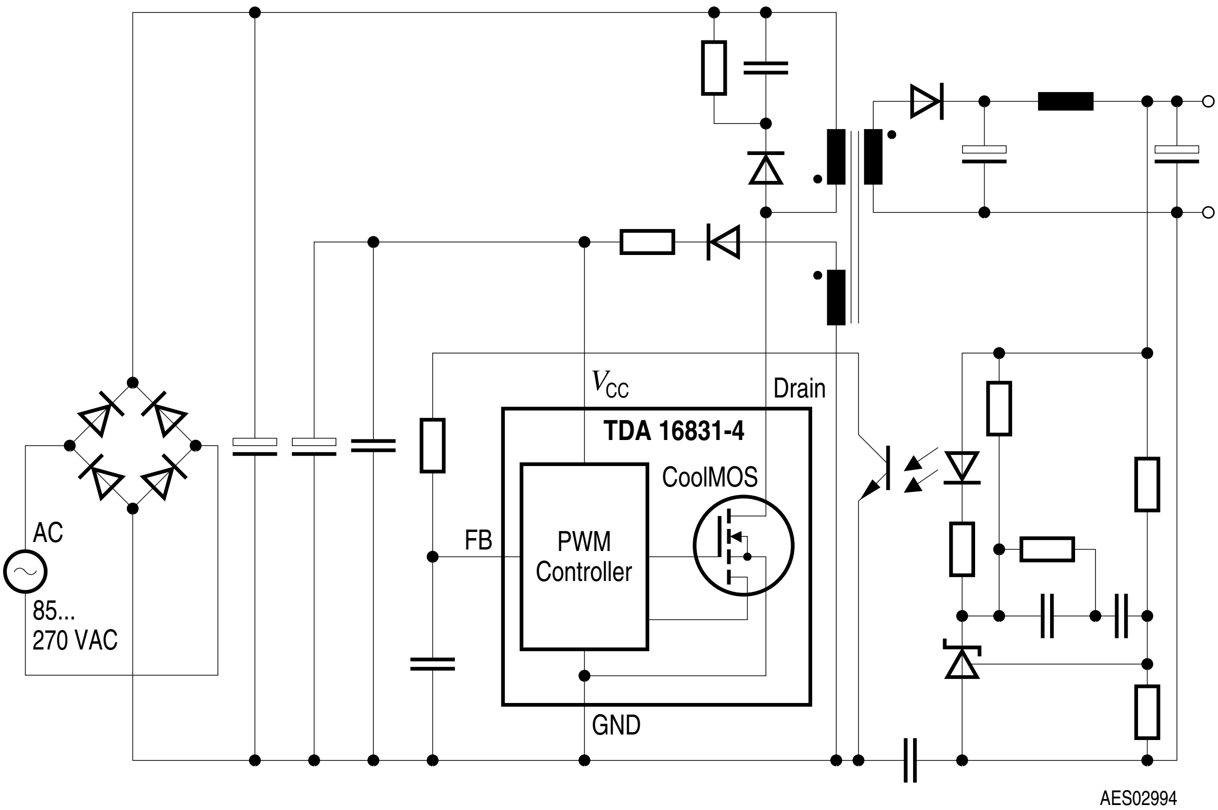
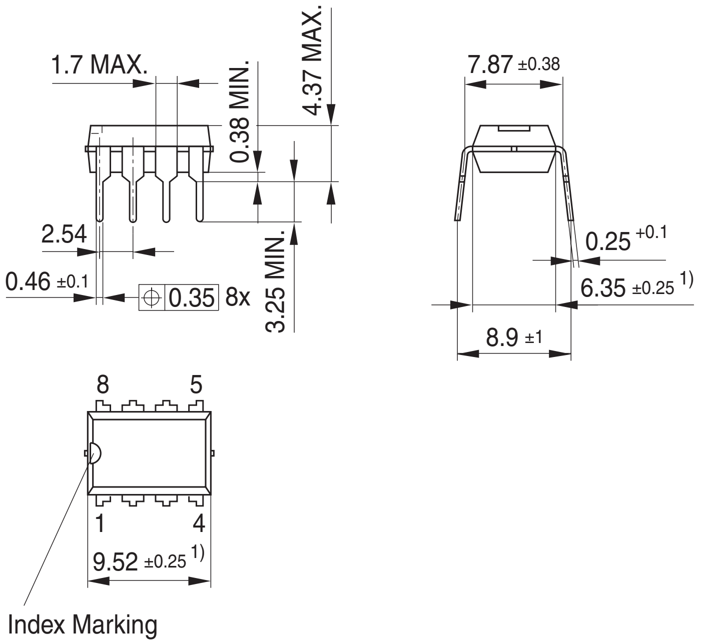


Figure 5 TDA 16832/2G/3G: 4 Active Pins, Version without Soft Start

5 Package Outlines

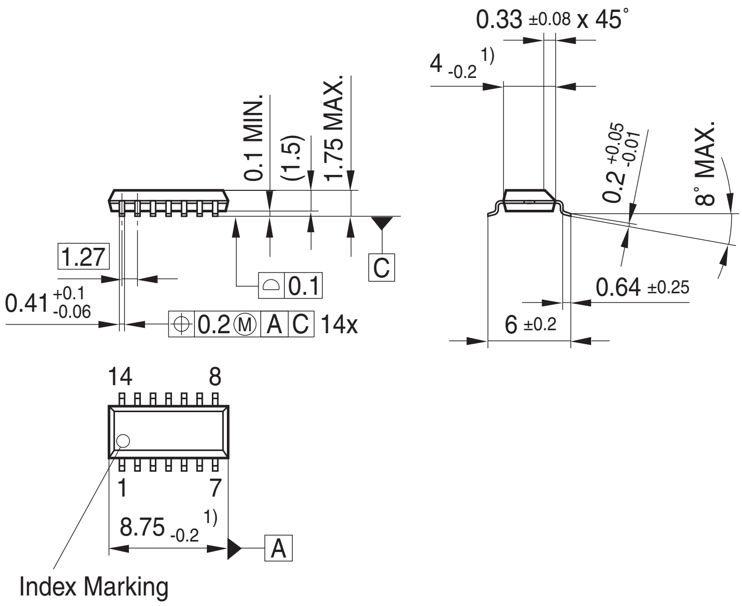
P-DIP-8-6
(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05583

P-DSO-14-11
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09033

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Dimensions in mm

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