Specification Update

1. Revision History

Date of revision	Version	Description
September 21, 1998	A	Creation for new part number TSC87251G1A

World Wide Web: http://www.temic–semi.de/
Product Hotline: C251@temic.fr

2. Preface

This document is an update to the specifications contained in Table 1.

TSC80251G1 products implement a C251 architecture compliant to INTEL's MCS®251. Hence some of INTEL's specification update apply to TEMIC products. This includes INTEL's core stepping as outlined in Table 2.

Note:
This document only applies to TEMIC's products and does not imply any product from INTEL has the same behavior. INTEL's Errata references are provided for information only when they are documented by Intel Corporation. Please refer to INTEL's documents if you intend to use INTEL's products in your system. Please refer to TEMIC's documents if you intend to use TEMIC's products in your systems.

Table 1. Affected Documents/Related Documents

Title	Reference
TSC80251G1A Datasheet	Rev. A – September 21, 1998
TSC80251G1 Design Guide 1996	Rev. A – December 18, 1996
TSC80251 Programmer's Guide 1996	Rev. B – October 23, 1996

Table 2. TEMIC Products to INTEL's Core Version Reference

TEMIC Products	INTEL's Core Version			
	A	B	C	D
TSC87251G1A–xyyyy	X			

Notes:
x provides factory programmed configuration option when needed.
yyyy provides speed, temperature range, packaging and conditioning options.
zzzz provides the customer code for MaskROM.
Please refer to Ordering Information in the Design Guide for full information on the options.

3. Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specifications (See Table 1).

Note:
Errata removed from the specification update are archived and available upon request.

Table 3. Codes Used in Summary Table

Page	
(Page)	Page location of item in this document.
Status	
Doc	Document change or update will be implemented.
Fix	This erratum is intended to be fixed in a future version of the component.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

4. Summary Tables of Changes

The following tables indicate the errata or documentation changes which apply to TSC80251G1 derivatives. TEMIC may fix some of the errata in a future version of the component, and account for the other outstanding issues through documentation or specification changes as noted.

Table 4. Errata

TEMIC Reference	INTEL Reference	Page	Status	Errata
80251G1A–01	9600001	4	Fix	Negative flag
80251G1A–02	9600002	4	Fix	WSB – wait state for memory region 01:
80251G1A–03	9600003	5	Fix	EJMP at upper boundary of any 64–Kbyte region of memory
80251G1A–04	9600004	6	Fix	Short jumps from memory region FF: to FE:
80251G1A–05	9600005	7	Fix	Interrupt when CPU is executing user code not in FF: region
80251G1A–06	N.A.	8	Fix	Timers 0 and 1 autoreload
80251G1A–07	(1)	8	Fix	JBC Instruction
80251G1A–08	N.A.	9	Eval	Timer 1 Counter with Timer 0 in Mode 3

Note:
1. Not reported when releasing this specification update.

Table 5. Specification Changes

TEMIC Reference	INTEL Reference	Page	Status	Specification Changes
				None

Table 6. Specification Clarifications

TEMIC Reference	INTEL Reference	Page	Status	Specification Clarifications
				None

Table 7. Documentation Changes

TEMIC Reference	INTEL Reference	Page	Status	Documentation Changes
DOC–01	–	10	Doc	Electrical and Mechanical Information
DOC–02	–	10	Doc	Ordering Information

5. Errata

Reference	Erratum
80251G1A–01	**Negative flag**

Problem

The Negative (N) Flag of PSW1 should be set or cleared corresponding to bit 15 of the result. Instead, it corresponds to bit 7 of the result.

Implication

The following instructions are affected: SRL WRj – SRA WRj – SLL WRj – INC WRj, #short – DEC WRj, #short.

Workaround

There are two ways to work around this erratum:

- Follow the affected instructions listed above with an operation that will rectify the Negative (N) flag correctly.

```
srl WRj
anl WRj,#0FFFFh
sll WRj
anl WRj,WRj
```

- Check bit 15 of the result vs. relying on the N flag for sign.

Affected Products

All TSC80251G1 Step A derivatives are affected.

Reference	Erratum
80251G1A–02	**WSB – Wait state for memory region 01:**

Problem

The WSB bit of configuration byte CONFIG1 is intended to configure 0 or 1 wait states for all MOVX (including MOVX @DPTR and MOVX @Ri) instructions for the region 01:0000h–01:FFFFh. However, in Step A devices, the MOVX @Ri uses WSA of the configuration byte CONFIG0 instead of WSB.

Implication

The error affects the generating wait state by using WSB bit of configuration byte CONFIG0 during MOVX instruction at region 01:0000h to 01:FFFFh.

Workaround

There are two ways to work around this erratum:

- Configure both WSA and WSB bits with the same wait state if both MOVX @DPTR and MOVX @Ri instructions are used and require the same wait state.
- If it is required that WSB be configured different from WSA, then limit usage of the MOVX instruction to the MOVX @DPTR format rather than the MOVX @Ri format.

Affected Products

All TSC80251G1 Step A derivatives are affected.

Reference	Erratum
80251G1A–03	**EJMP at upper boundary of any 64-Kbyte region of memory**

Problem

The EJMP instruction is intended for extended jumps from one 64-Kbyte region of memory to another 64-Kbyte region of memory. However, when EJMP occurs at the upper boundary of any 64-Kbyte region of memory, the Program Counter (PC) will land in the wrong 64K–byte region of memory.

Example

The code: “FEFFFD 8A00XXXX EJMP #00XXXXh” should branch to address 00:XXXXh, but it branches to address region 01:XXXXh instead.

The operation of this instruction is shown below:

```
(PC)        <--  (PC) + 2          PC= FEFFFFh
(PC.23:16)  <--  (Addr.23:16)      PC= 00FFFFh
(PC)        <--  (PC) + 2          PC= 010001h(1)
(PC.15:0)   <--  (Addr.15:0)       PC= 01XXXXh
```

Note:

1. *Overflow occurs when incrementing the PC for the lower two bytes of destination address. The overflow has incremented the PC.23:16 and caused a deviation from the destination Addr.23:16.*

Implication

The erratum affects the function of EJMP instruction at the upper boundary region.

Workaround

Avoid this instruction being used at the upper boundary of any 64-Kbyte memory region.

Affected Products

All TSC80251G1 Step A derivatives are affected.

Reference	Erratum
80251G1A–04	**Short jumps from memory region FF: to FE:**

Problem

The short jump instruction is intended for a +127 or –128 byte jump relative to the current instruction. However, a short jump from the address in the lower boundary of region FF: will not branch to the address in upper boundary of region FE: even though the destination address is within this –128 byte range. Instead of landing at address in region FE:, it will remain at address in region FF:.

Example

```
FEFFF0                          ORG FEFFF0h
FEFFF0 00          REL_ADR:     nop
FF0002                          ORG FF0002h
FF0002 80EC                     sjmp REL_ADR
```

This code should branch to address FEFFF0h, but it branches to address FFFFF0h in the same region FF: instead.

Implication

The following instructions are affected: SJMP – CJNE – DJNZ – JB – JBC – JC – JE – JG – JLE – JNB – JNC – JNE – JNZ – JSG – JSGE – JSL – JSLE – JZ.

Please note that there is no errata for short jumps from upper boundary of region FE: to lower boundary of region FF: and no errata for short jumps from upper boundary of region 00: to lower boundary of region 01: and vice–versa.

Workaround

Avoid these instructions being used for a short jump from the lower boundary of region FF: to the upper boundary of region FE:.

Affected Products

All TSC80251G1 Step A derivatives are affected.

Reference	Erratum
80251G1A–05	**Interrupt when CPU is executing User Code not in FF: region**

Problem

The reset vector and interrupt vectors are defined at the FF: region. If an interrupt occurs, the CPU is not able to jump to the interrupt vector when the CPU is executing the user code at regions other than FF:.

Example

If the user code size is 128–Kbyte, the first 64–Kbyte of the user code is located at FF: region and the other 64–Kbyte of the user code is located at FE: region. The reset vector and the interrupt vector for the external interrupt 0 (INT0#) are defined at the FF: region as shown below.

```
                                ORG FF:0000h
FF0000 02 0100                  ljmp MAIN
                                ORG FF:0003h
FF0003 02 0300                  ljmp EXT_INT0
                                ORG FF:0100h
FF0100 12 0200   MAIN:          lcall INITIALIZE_INT0
                                ORG FF:0300h
FF0000 02 0100   EXT_INT0:      push PSW
                                ...
                                reti
```

When the CPU is executing the user code from the FE: region, if an external interrupt (INT0#) occurs, the CPU is not able to jump to interrupt vector (EXT_INT0) as defined at FF: region. It is jumping to the FE: region instead.

Implication

This error affects additional interrupt vectors to be initialized at other memory regions.

Workaround

Bit 4 (INTR bit) of configuration byte (CONFIG1) must be set to 1. All needed interrupt vectors must be defined at other regions (other than FF: region) as well. For an example, if the user code size is 128-Kbyte and the first 64-Kbyte of the user code and the interrupt vector for external interrupt 0 is defined at FF: region.

```
ORG FF:0003h
ljmp EXT_INT0
```

Then there are two possible ways of locating the other 64-Kbyte user code and the workaround:

- If the other 64-Kbyte user code is located at FE: region, the following instructions must be added to the user code at FE: region:.

```
ORG FE:0003h
ejmp EXT_INT0
```

- If the other 64-Kbyte user code is located at 00: region, the following instructions must be added to the user code at 00: region.

```
ORG 00:0003h
ejmp EXT_INT0
```

Affected Products

All TSC80251G1A derivatives are affected.

Reference	Erratum
80251G1A–06	**Timers 0 and 1 Autoreload**

Problem

The overflow flags TF0 and TF1 are not set when timer 0 and timer 1 are in Autoreload mode (mode 2) with reload value FFh or when a software reload is done with value FFFFh.

Implication

Only the flag is affected, the count and reload operations will run normally.

Workaround

Do not use autoreload mode with TH0 or TH1 set to FFh. Do not reload timer 0 or timer 1 with FFFFh value.

Affected Products

All TSC80251G1A derivatives are affected.

Reference	Erratum
80251G1A–07	**JBC instruction**

Problem

The JBC instruction uses a Read Read Modify Write instruction. The write back is performed in any case, regardless of the value of the bit. In such case a bit set between the first and second read will be overwritten and information is lost.

Implication

This error affects only the following bits: external interrupts flag (IE0 and IE1) and keyboard interrupt flags (P1F.x).

Workaround

The workaround for this erratum is to not use the JBC instruction for the flags IE0, IE1 and P1F.x.

Affected Products

All TSC80251G1A derivatives are affected.

Reference	Erratum
80251G1A–08	**Timer 1 Counter with Timer 0 in Mode 3**

Problem

When timer 0 is programmed in mode 3 TR1 bit is used to control TH0 timer and should not control timer 1. In this configuration, when timer 1 is used in counter mode (C_T1#= 1) TR1 also controls counting.

Implication

This errata leads to bad event counting on timer 1. This errata does not affect timer 1 when configured as timer (C_T1#= 0) i.e. when used as baud rate generator.

Workaround

There is no generic workaround for this erratum. Please contact C251 hotline for a case by case workaround.

Affected Products

All TSC80251G1A derivatives are affected.

6. Specification Changes

None for this revision of this specification update.

7. Specification Clarifications

None for this revision of this specification update.

8. Documentation Changes

Reference	Changes
DOC–01	**Electrical and Mechanical Information**

All chapters in Section III of the TSC80251G1 Design Guide (see Table 1) are replaced by the corresponding chapters of the new TSC80251G1A datasheet (see Table 1).

Reference	Changes
DOC–02	**Ordering Information**

Section V of the TSC80251G1 Design Guide (see Table 1) is replaced by the corresponding chapter of the new TSC80251G1A datasheet (see Table 1).