General Description

The AAT3232 Low Dropout Linear Regulator is ideal for portable applications where longer battery life is critical. It features low quiescent current (30µA typical) and low dropout voltage (300mV max) at full output current. The device is able to protect itself from short circuit conditions with fold back current limiting. Thermal shutdown is activated to prevent damage under extreme conditions.

The AAT3232 also features a low-power shutdown mode for longer battery life. A pin is provided to improve PSRR performance, by connecting an external capacitor from the AAT3232's reference output to ground.

The AAT3232 is available in a space saving 5-pin SOT-23 in 7 factory programmed voltages of 2.5V, 2.7V, 2.8V, 3.0V, 3.3V, 3.5V and 3.8V.

Features

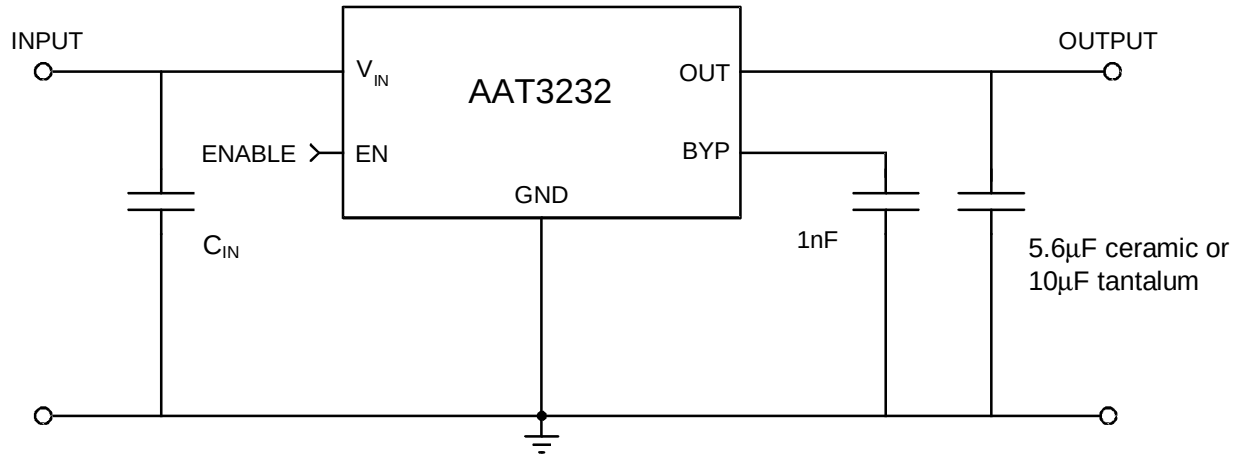
- Low Dropout - 300mV (max) at 300mA
- Guaranteed 300mA Output
- High accuracy
- 30µA Quiescent Current
- Current limit protection
- Short circuit current fold back
- Over-Temperature protection
- Noise reduction bypass capacitor
- Shutdown mode for longer battery life
- Low Temperature coefficient
- 7 Factory programmed output voltages
- SOT-23 5-pin package

Applications

- Cellular Phones
- Notebook Computers
- Portable Communication Devices
- Handheld Electronics

Preliminary Information

Typical Application



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description	Max	Units
V_{IN}	Input Voltage	8	V
I_{OUT}	DC Output Current	$P_D/(V_{IN}-V_O)$	mA
T_J	Operating Junction Temperature Range	150	°C
Θ_{JA}	Thermal Resistance (SOT-23-5)	260	°C/W
P_D	Maximum Power Dissipation (SOT-23-5)	380	mW
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Recommended Operating Conditions

Symbol	Description	Rating	Units
V_{IN}	Input Voltage	(V_{OUT}+0.3) to 7	V
T	Ambient Temperature Range	-40 to +85	°C

Electrical Characteristics (T_J=25°C unless otherwise noted)

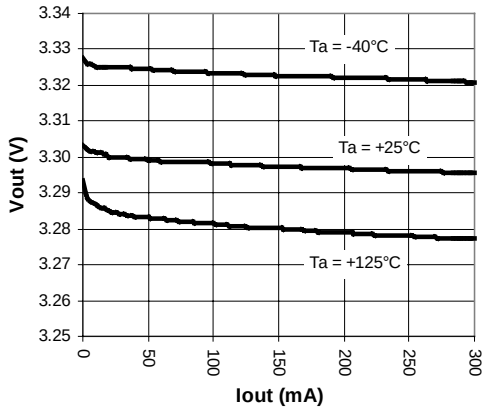
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage		-1.5		1.5	%
I_{OUT}	Output Current	V_{OUT} > 1.2V	300			mA
I_{SC}	Short Circuit Current	V_{OUT} < 0.4V			300	mA
I_Q	Ground Current	V_{IN} = 5V, no load		30	50	µA
I_{SD}	Shutdown Current	V_{IN} = 5V, EN = low			1	µA
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	I_{OUT} = 5mA, V_{IN} = V_{OUT} + 1 to V_{OUT} + 2		0.02	0.1	%
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{OUT} = 1mA to 300mA		0.2	1	%
V_{DO}	Dropout Voltage[1]	I_{OUT} = 300mA		200	300	mV
V_{ENL}	Enable Threshold Low		0.5			V
V_{ENH}	Enable Threshold High				V_{IN}-0.5	V
PSRR	Power Supply Rejection Ratio	1 kHz		55		dB
T_{SD}	Over Temp Shutdown Threshold			150		°C
T_{HYS}	Over Temp Shutdown Hysteresis			30		°C
e_N	Output Noise			20		μV_{RMS}
TC	Ouput Voltage Temp. Coeff.			40		ppm/°C

Note 1: V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.

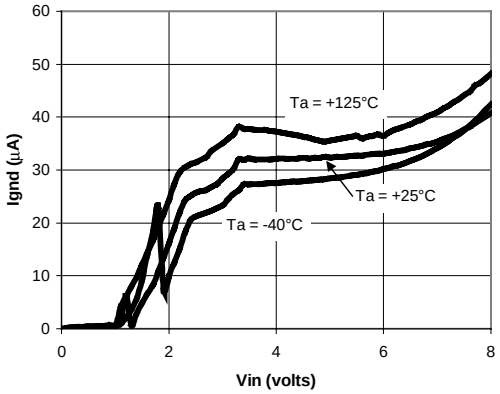
Typical Characteristics

(Unless otherwise noted, $V_{IN} = V_{OUT} + 1V$, $T_A = 25°C$, $C_{NOISE} = 10nF$, $C_{IN} = 2.0\mu F$, $C_{OUT} = 5.6\mu F$ ceramic, $I_{OUT} = 100mA$)

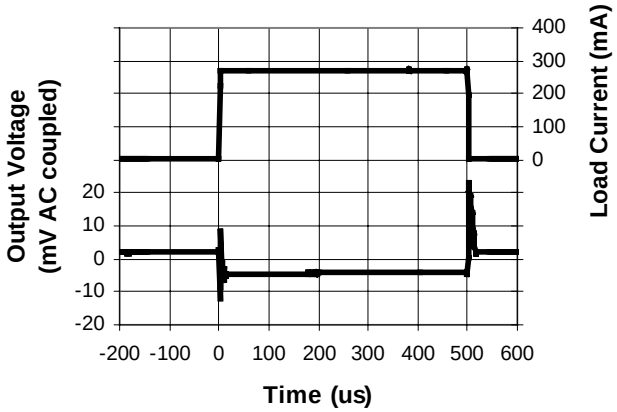
Output Voltage vs. Load Current



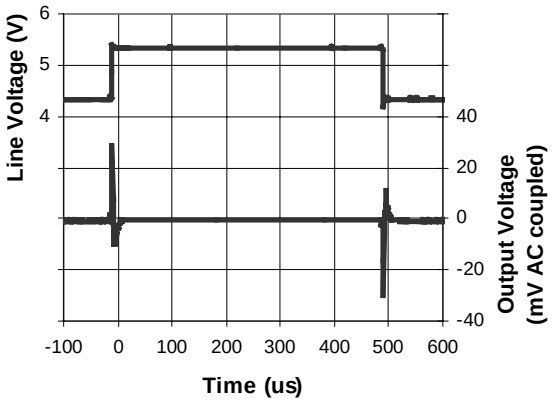
Ground Current vs. Input Voltage



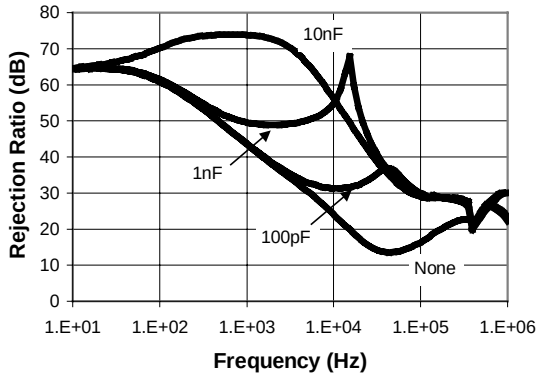
Step Load Transient Response



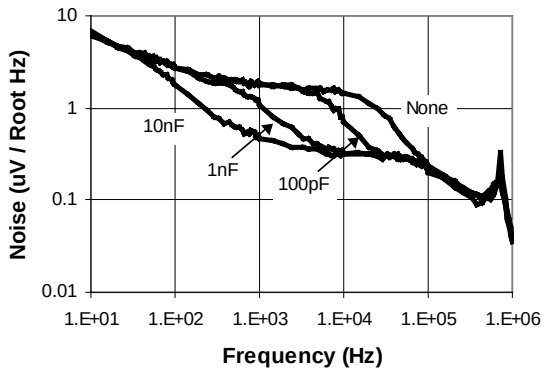
Line Transient Response



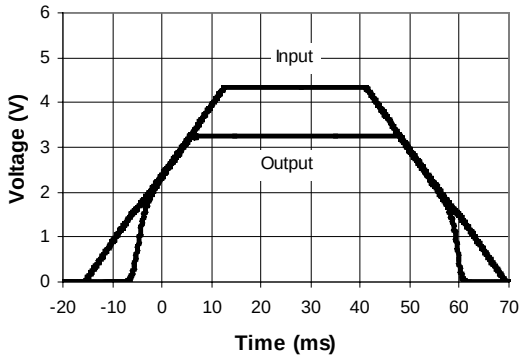
Power Supply Rejection Ratio



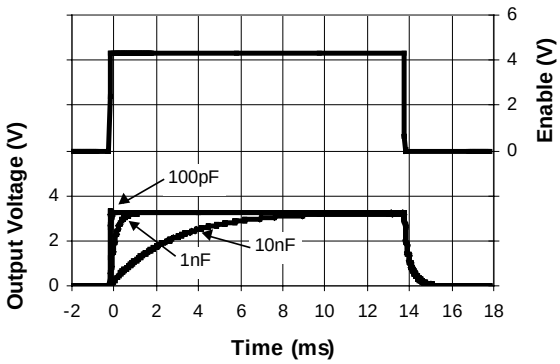
Output Noise



Power-Up, Power-Down Response



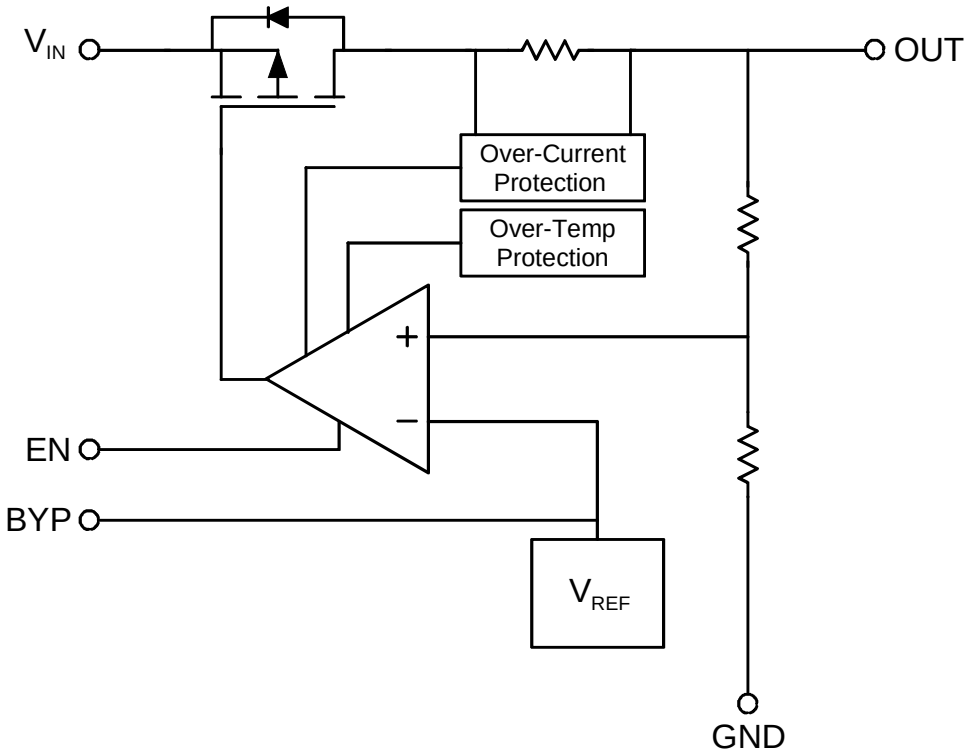
Turn On / Turn Off



Pin Descriptions

Pin #	Symbol	Function
1	V_{IN}	Input voltage pin – should be decoupled with 1µF or greater capacitor.
2	GND	Ground connection pin
3	EN	Enable pin – pin is internally pulled high. When pulled low the PMOS pass transistor turns off and the device enters low-power mode, consuming less than 1µA.
4	BYP	Bypass capacitor connection -- to improve AC ripple rejection, connect a 1nF capacitor to GND. This will also provide a soft start function.
5	OUT	Output pin – should be decoupled with 2.2µF or greater output capacitor. See Detailed Description section for further information.

Functional Block Diagram



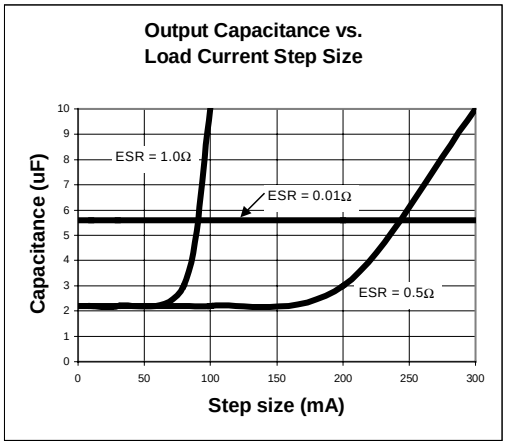
Detailed Description

The AAT3232 is intended for use in systems where minimal current consumption is desired. During steady state operation, ground current is 30 µA typical. All remaining current is available to run the load. This part can also be run with drop out voltages as small as 300 mV allowing very efficient systems to be designed. Several compromises have been made for this device to operate with both low steady state current consumption and very low drop out voltage. The primary compromise is the requirement of larger capacitors over those required by other power hungry high performance LDO's. Since the AAT3232 has considerably faster response than some ultra low current consumption LDOs available, it should not be considered a low performance LDO. The second compromise is the inability to sink current. If current is sourced by the load rather than sunk by the load, the AAT3232 will simply stop supplying current rather than actively reducing the output voltage. As long as the output voltage does not exceed the absolute maximum specification, the AAT3232 will not be damaged.

Output Capacitor

Output capacitor size is dependent upon the magnitude and the rate of change of the load variation. 10 µF tantalum or 5.6 µF ceramic is needed only if the load will change by 270 mA (90% of Imax) in less than a couple of microseconds. Smaller capacitors can be used if the output current step size, or rate of change, is less. (See graph titled Output Capacitance vs. Load Current Step Size.) In addition, if adequate bypassing is used at the load, the output capacitor near the LDO can be reduced.

The AAT3232 has been optimized for operation with capacitors that are not of the low series resistance type. There are two benefits of using an LDO designed to work with series resistance. First, capacitors sized 10 µF or greater with low ESR are generally more expensive than the higher ESR types such as tantalum and electrolytic. Secondly, output capacitors need not be placed next to the regulator. Most applications use a large higher-ESR capacitor placed near the



regulator and low ESR decoupling capacitors placed near the load. In cases where very compact design is desirable, a small 1206 case size ceramic capacitor and the load are placed and connected immediately adjacent to the LDO and the trace from the output pin to the output capacitor should have at least 5 milliohms of resistance. For example at least ten squares should be used on a one ounce copper layer. Also see Layout Tips, below.

Enable

The enable pin is the on/off switch for the LDO. When it is a logic high, the LDO is functioning normally. When it is a logic low, the LDO is in a low power, shut down mode. It has standard CMOS voltage levels set by the AAT3232 input voltage. Voltages at this terminal should be within the absolute maximum rating (-0.5V, to Vin + 0.5V). The enable pin is internally pulled up so that it may be left floating for normal operation. However, since the pull up current is only 500 nA, if open drain logic is used to drive the enable pin, several hundred microseconds may be required for the enable voltage to reach a logic high level.

Cnoise

The LDO's internal reference can be bypassed by connecting a capacitor from BYP to GND, reducing most of the internally generated noise seen at the output. (See graph titled Output Noise in the previous section.) A large capacitor on Cnoise also improves the PSRR of the AAT3232. (See graph titled Power Supply Rejection Ratio) In addition, a large capacitor

slows down the rate at which the reference turns on. The result is that output voltage climbs slowly when the LDO is turned on either by applying power to the input terminal or by activating Enable. (See graph titled Turn On / Turn Off.) As a result, Cnoise can also be used as a soft start adjustment.

Input Capacitor

The input capacitor has two purposes: The first is to prevent load current surges from injecting noise onto the line. The second is to prevent line noise from affecting the operation of the regulator. In most circuits, the same value capacitor is used for input and output capacitors. If cost and space are an issue, a ceramic capacitor of a few microfarads works well.

Additional PSRR

In cases where greater PSRR than normally provided by the AAT3232 is required, additional filtering may be placed on the input line. This allows the filter to drop voltage without affecting the load voltage. For example, if the maximum load required is 100mA, and a drop out voltage of 1.5 volts is available, then a 10 ohm resistor and a 6.8uF capacitor can be used as an input filter. For optimal results, the input filter should be designed to reject signals above one kilohertz, which is where the AAT3232's PSRR rolls off.

Layout

Since the AAT3232 is designed to operate with series resistance, it is not necessary to have the regulator close to the output capacitor. However, if a ceramic output capacitor is used, a small amount of ESR should be placed between the output capacitor and the regulator; 10 squares of trace on 1 oz. copper (about 5 mΩ) is enough, but 10 mΩ gives better results. The load should be connected to the output capacitor's side of the resistive trace rather than the regulator's side of the resistive trace.

PC board layout guidelines (in order of importance):

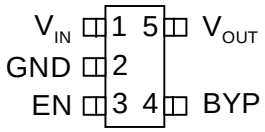
1. Cnoise capacitor to BYP and GND: Traces should be kept short.
2. Input capacitor to Vin and GND: Traces should be wide and short.
3. Filter resistor to Input capacitor (for the case of additional PSRR filtering): Connection need not be short but other loads should not be connected to the LDO side of the resistor.
4. Enable is not sensitive to position.

Ordering Information

Output Voltage	Package	Marking	Part Number	
			Bulk	Tape and Reel
2.5V	SOT-23-5		N/A	AAT3232IGV-2.5-T1
2.7V	SOT-23-5		N/A	AAT3232IGV-2.7-T1
2.8V	SOT-23-5		N/A	AAT3232IGV-2.8-T1
3.0V	SOT-23-5		N/A	AAT3232IGV-3.0-T1
3.3V	SOT-23-5		N/A	AAT3232IGV-3.3-T1
3.5V	SOT-23-5		N/A	AAT3232IGV-3.5-T1
3.8V	SOT-23-5		N/A	AAT3232IGV-3.8-T1

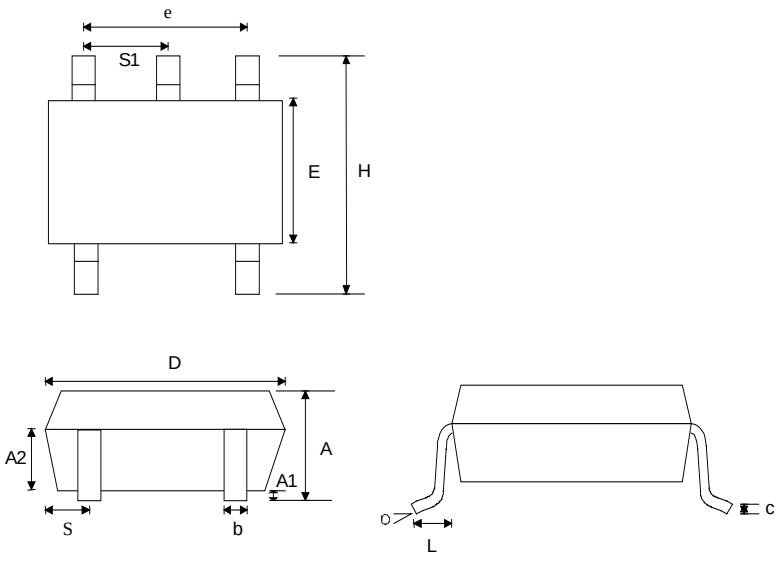
Pin Configuration

5-lead SOT-23
(Top View)



Package Information

SOT-23-5



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.00	1.30	0.039	0.051
A1	0.00	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.35	0.50	0.014	0.020
c	0.10	0.25	0.004	0.010
D	2.70	3.10	0.106	0.122
E	1.40	1.80	0.055	0.071
e	1.90		0.075	
H	2.60	3.00	0.102	0.118
L	0.37		0.015	
S	0.45	0.55	0.018	0.022
S1	0.85	1.05	0.033	0.041
Θ	1°	9°	1°	9°

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