CYM1851

1,024K x 32 Static RAM Module

Features

- **High-density 32-megabit SRAM module**
- **32-bit Standard Footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed SRAMs**
  - **— Access time of 12 ns**
- **Low active power**
  - **— 8.36W (max.) at 12 ns**
- **72 pins**
- **Available in ZIP, SIMM, or angled SIMM format**

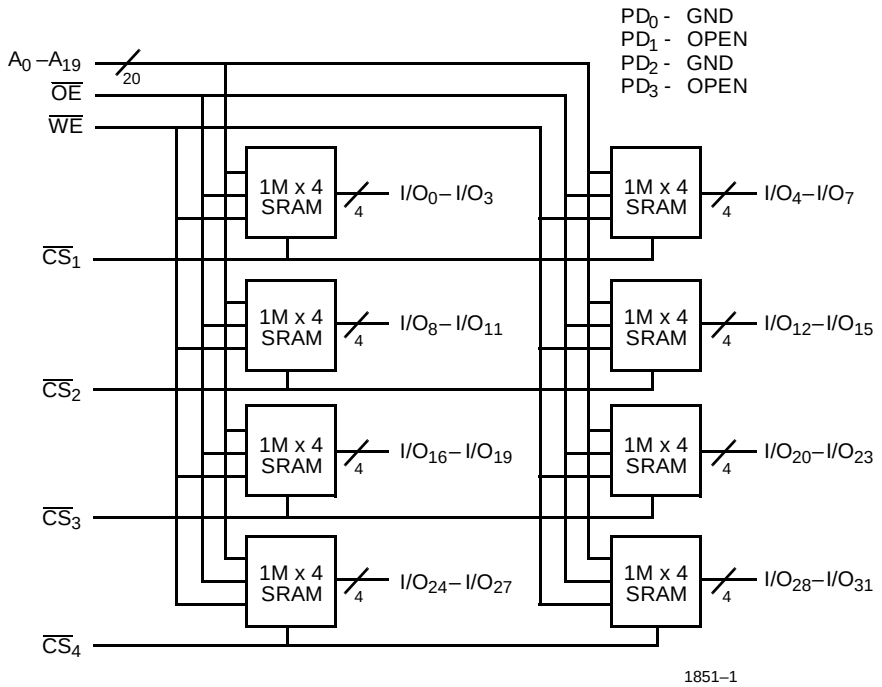
Functional Description

The CYM1851 is a high-performance 32-megabit static RAM module organized as 1,024K words by 32 bits. This module is constructed from eight 1,024K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1851 is designed for use with standard 72-pin SIMM sockets. The pinout is downward compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1,024K words (CYM1851). The CYM1851 is offered in vertical and angled SIMM configurations and both are available with either tin-lead or 10 micro-inches of gold flash on the edge contacts.

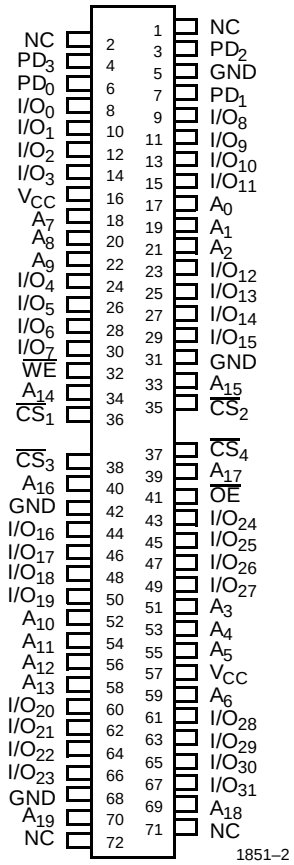
Presence detect pins (PD_0–PD_3) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.

Logic Block Diagram



Pin Configuration

ZIP/SIMM Top View



Selection Guide

	1851-12	1851-15	1851-20	1851-25	1851-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	1520	1520	1200	1200	960
Maximum Standby Current (mA)	480	480	480	480	480

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –10°C to +85°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +V_{CC}

DC Input Voltage .....–0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–16	+16	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_N$ ≤ V_{IL}	-20, -25, -35		1200	mA
			-12, -15		1520	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V	-20, -25, -35		80	mA
			-12, -15		240	mA

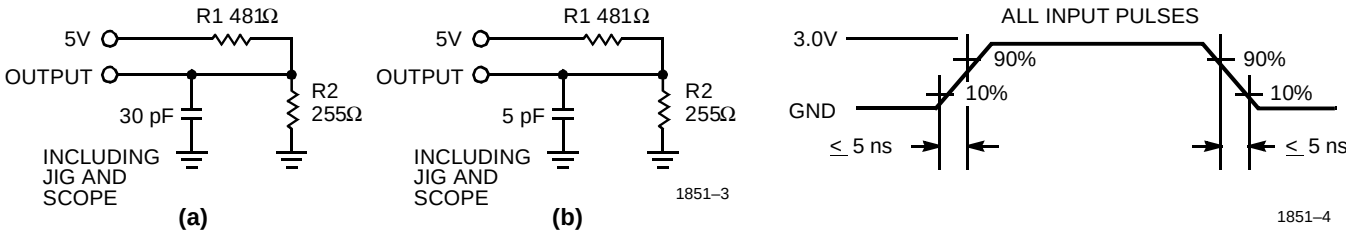
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance ($\overline{WE}$, $\overline{OE}$, $A_{0–19}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		20	pF
C_{OUT}	Output Capacitance		20	pF

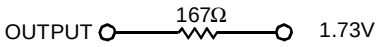
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1851-12		1851-15		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		7		8	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15	ns
WRITE CYCLE[6]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	9		10		ns
t_{AW}	Address Set-Up to Write End	9		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	1		1		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		ns
t_{SD}	Data Set-Up to Write End	7		8		ns
t_{HD}	Data Hold from Write End	1		1		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	7	0	8	ns

Notes:

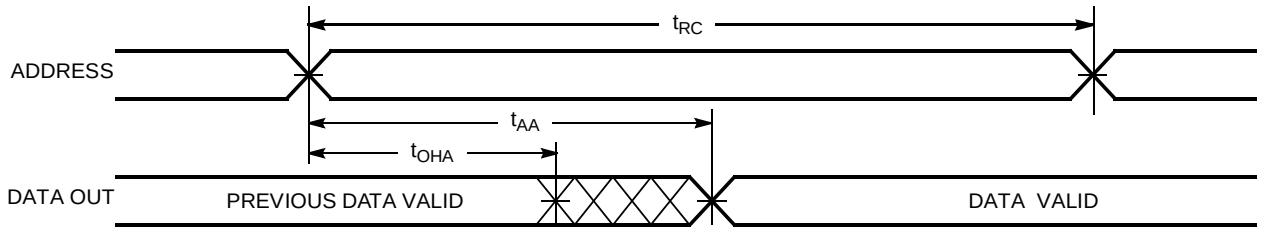
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3](continued)

Parameter	Description	1851-20		1851-25		1851-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		35		ns
t_{AA}	Address to Data Valid		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		18	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		12		15	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		35	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	17		20		30		ns
t_{AW}	Address Set-Up to Write End	17		20		30		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		30		ns
t_{SD}	Data Set-Up to Write End	12		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	12	0	12	0	15	ns

Switching Waveforms

Read Cycle No. 1 [7,8]

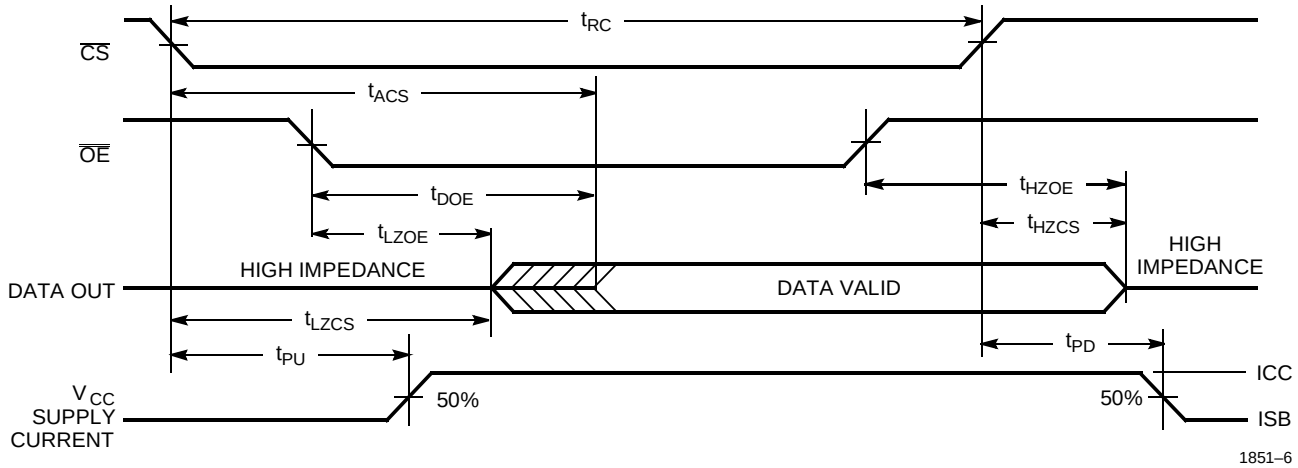


1851–5

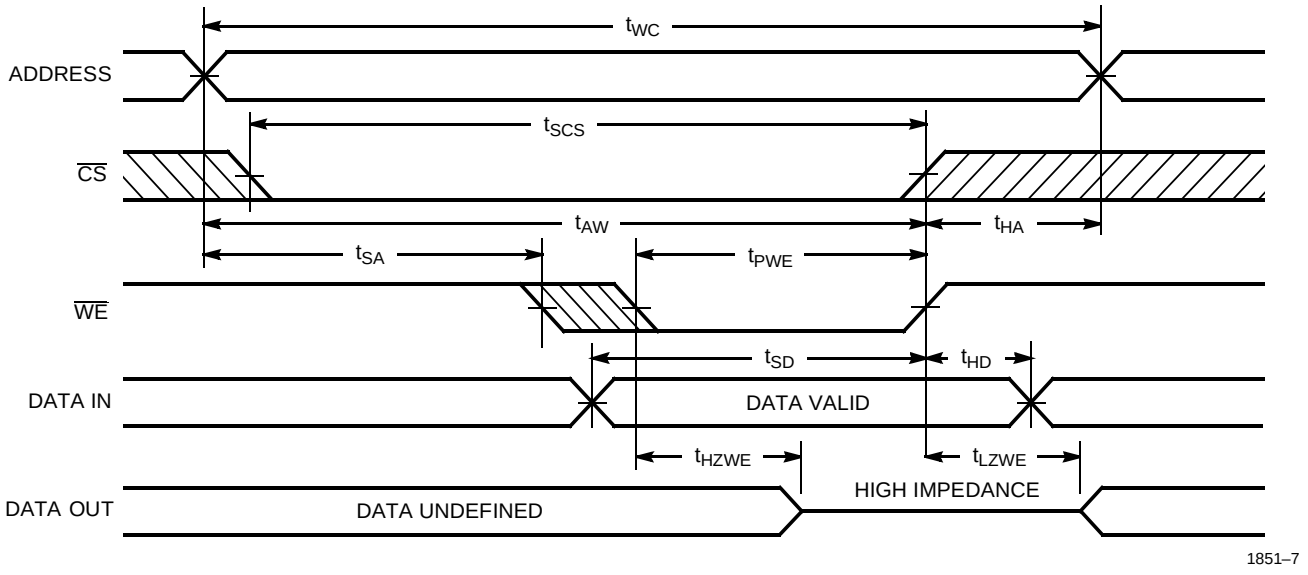
Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL}, and $\overline{OE}$= V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2 [7,9]



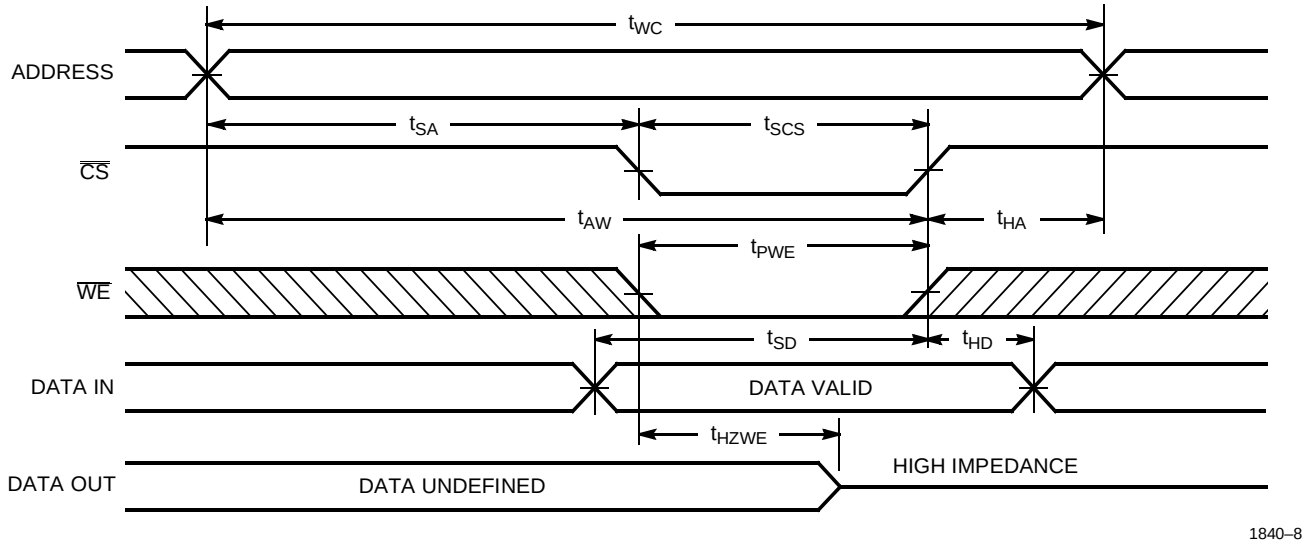
Write Cycle No. 1 (WE Controlled) [6]



Note:
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled) [6,10]



Note:
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

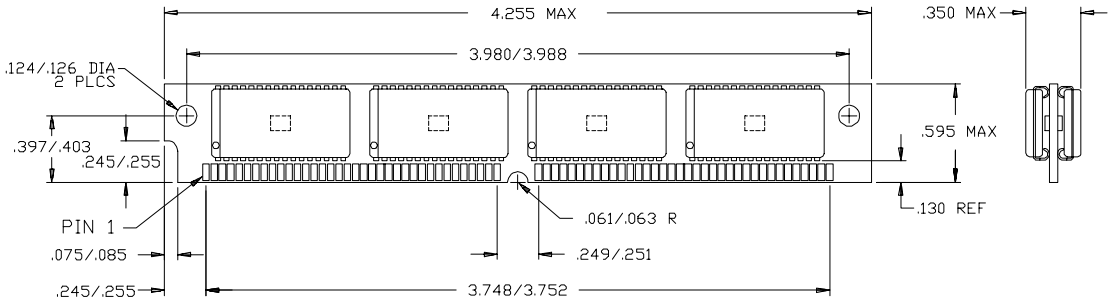
Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
12	CYM1851PM-12C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851P8-12C	PM04	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1851PN-12C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851P6-12C	PN04	72-Pin Plastic Angled SIMM Module (gold contacts)	
	CYM1851PZ-12C	PZ09	72-Pin Plastic ZIP Module	
15	CYM1851PM-15C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851P8-15C	PM04	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1851PN-15C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851P6-15C	PN04	72-Pin Plastic Angled SIMM Module (gold contacts)	
	CYM1851PZ-15C	PZ09	72-Pin Plastic ZIP Module	
20	CYM1851PM-20C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851P8-20C	PM04	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1851PN-20C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851P6-20C	PN04	72-Pin Plastic Angled SIMM Module (gold contacts)	
	CYM1851PZ-20C	PZ09	72-Pin Plastic ZIP Module	
25	CYM1851PM-25C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851P8-25C	PM04	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1851PN-25C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851P6-25C	PN04	72-Pin Plastic Angled SIMM Module (gold contacts)	
	CYM1851PZ-25C	PZ09	72-Pin Plastic ZIP Module	
35	CYM1851PM-35C	PM04	72-Pin Plastic SIMM Module	Commercial
	CYM1851P8-35C	PM04	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1851PN-35C	PN04	72-Pin Plastic Angled SIMM Module	
	CYM1851P6-35C	PN04	72-Pin Plastic Angled SIMM Module (gold contacts)	
	CYM1851PZ-35C	PZ09	72-Pin Plastic ZIP Module	

Document #: 38-M-00052-D

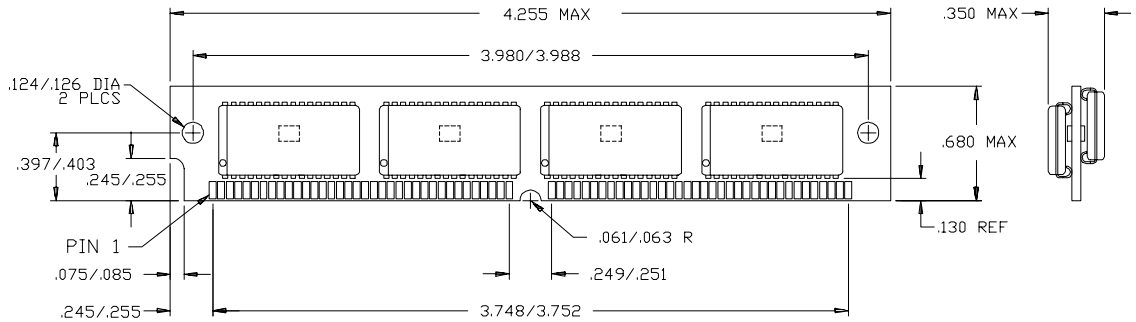
Package Diagrams

72-Pin Plastic SIMM Module PM04



Package Diagrams (continued)

72-Pin Plastic Angled SIMM Module PN04



72-Pin Plastic ZIP Module PZ09