Ordering number: EN 5599

CMOS LSI

LC864332A/28A/24A/20A/16A/12A

8-bit Single Chip Microcontroller

Overview

The LC864332A/28A/24A/20A/16A/12A microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks:

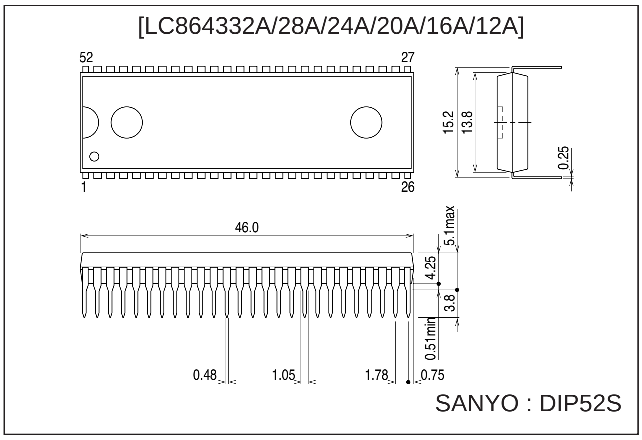
- CPU : Operable at a minimum bus cycle time of 0.5 µs
- On-chip ROM maximum capacity : 32K bytes
- On-chip RAM capacity : 384 bytes
- CRT display RAM : 640 × 9 bits
- Closed-caption TV controller and the on-screen display controller
- 16-bit timer/counter
- 4-channel × 5-bit A/D converter
- 8-bit synchronous serial-interface circuit
- Closed-caption data slicer
- 12-source 10-vectored interrupt system

All of the functions above are fabricated on a single chip.

Package Dimensions

unit : mm

3128-DIP52S



Feature

(1) Read-only memory (ROM) :	LC864332A	32768 × 8 bits
	LC864328A	28672 × 8 bits
	LC864324A	24576 × 8 bits
	LC864320A	20480 × 8 bits
	LC864316A	16384 × 8 bits
	LC864312A	12288 × 8 bits

(2) Random access memory (RAM) : 384 × 8 bits
640 × 9 bits (for CRT display)

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(3) OSD functions

- Screen for display : 34 columns × 16 rows (at standard character size)
- Display for RAM : 640 × 9 bits (6 columns for control + 34 columns for display) × 16 rows × 9 bits
- 380 kinds of user specified characters
  - Caption/Text mode : (9 × 9 dots) × 126 kinds
  - OSD mode : (12 × 18 dots) × 254 characters (127 characters can also be used for Caption/Text mode)
- Various character attributes
  - Character colors : 16 colors
  - Character background colors : 16 colors
  - Fringe / shadow colors : 16 colors
  - Full screen colors : 16 colors
  - Fringe / shadow
  - Rounding
  - Underline
  - Italic character (slanting)
- Close-character attribute data changing available
- Vertical display start line setting in row unit available (Row overlapping available)
- Horizontal display start position setting available
- Display mode specification by row (Display mode mixable)
  caption mode / text mode / OSD mode
- Eight kinds of character size
  Horiz. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4)
  (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4)
- Shuttering and scrolling in row unit available
- Horizontal pitch of character selectable : 9 to 16 dots
- Polarity of R, G, B, I, BL output programmable
- Polarity of $\overline{HS}$, $\overline{VS}$ input programmable

(4) Data slicer clock switching function
Clock source can be selected from LC oscillation or CF (or Crystal) oscillation.

(5) Bus cycle time / Instruction cycle time
The LC864332A/28A/24A/20A/16A/12A microcontrollers are designed to read the ROM twice within one instruction cycle.
It has about 1.7 times performance capability within the same instruction-cycle compared to our 4-bit microcontrollers (LC66000 series).
The bus cycle time indicates the speed to read ROM.

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Supply voltage
0.49 µs	0.99 µs	Ceramic or Crystal	12.08 MHz	4.5 V to 5.5 V
7.5 µs	15.0 µs	Internal RC	800 kHz	4.5 V to 5.5 V

(6) Ports

- Input/output port : 2 ports (16 lines)
  Input/output port programmable in nibble units : 1 port (8 lines)
  (When the N-ch open drain output is selected, bit-unit input is possible.)
  Input/output port programmable in a bit : 1 ports (8 lines)
- Input ports : 2 ports (8 lines)

(7) A/D converter

- 4-channel × 5-bit A/D converter (Converted with program)

(8) PWM output

- 10-channel × 7-bit PWM

(9) Timer

- Timer 0 : 16-bit timer / counter
  2-bit prescaler + 8-bit built-in programmable prescaler
  Mode 0 : Two 8-bit timers with a programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is fixed to 1 tCYC.
- Timer 1 : 16-bit timer / PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9 to 16 bits)
  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM can be selected with program : tCYC or 1/2tCYC.

(10) Remote-controlled receiver circuit (shares with the P73/INT3/T0IN terminal)

- Noise rejection function
- Polarity switching

(11) Watchdog timer

External RC circuit is required
Interrupt or system reset is selectable

(12) Interrupt system

- 12-source 10-vectored interrupts:
  1. External interrupt INT0
  2. External interrupt INT1
  3. External interrupt INT2, Timer/counter T0L (lower 8 bits)
  4. External interrupt INT3
  5. Timer/counter T0H (upper 8 bits)
  6. Timer T1H, T1L
  7. Serial interface 0 (SIO0)
  8. Data slicer
  9. Vertical synchronous signal interrupt ($\overline{\text{VS}}$)
  10. Port 0

- Interrupt priority control available
  Three interrupt priorities are supported (low, high and the highest) and multilevel nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 10 listed above. To the external interrupt INT0 and INT1, high or the highest priority can be given.

(13) Subroutine stack levels

- A maximum of 128 levels (Set the stack inside a RAM)

(14) Multiplication/division instruction

- 16 bits × 8 bits (7-instruction cycle times)
- 16 bits / 8 bits (7-instruction cycle times)

(15) 3 oscillation circuits
- On-chip RC ocscillation circuit for the system clock
- On-chip CF oscillation circuit for the system clock
- On-chip LC oscillation circuit for the CRT synchronization

(16) Standby function
- HALT mode function

  The HALT mode is used to reduce the power dissipation. In this mode, the program execution is stopped.
  This mode can be released by the interrupt request signal or the system reset.
- HOLD Mode

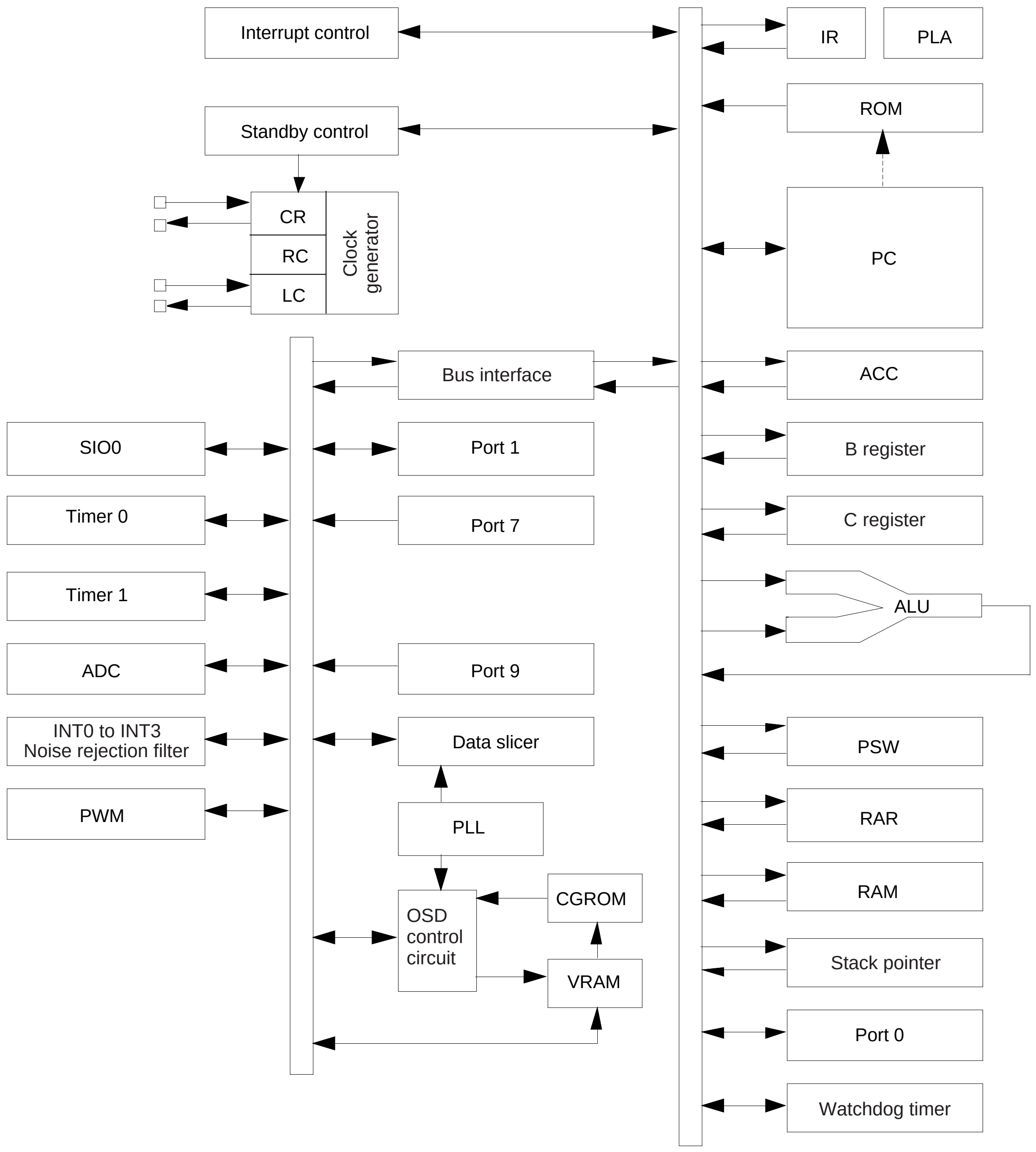
  The HOLD mode is used to stop oscillations ; the RC (internal) and the ceramic oscillations.
  This mode can be released by the following operations.
  - Set the reset terminal ($\overline{\text{RES}}$) to low level.
  - Feed the selected level to either P70/INT0 or P71/INT1.
  - Feed the Port 0 interrupt condition.

(17) Factory shipment

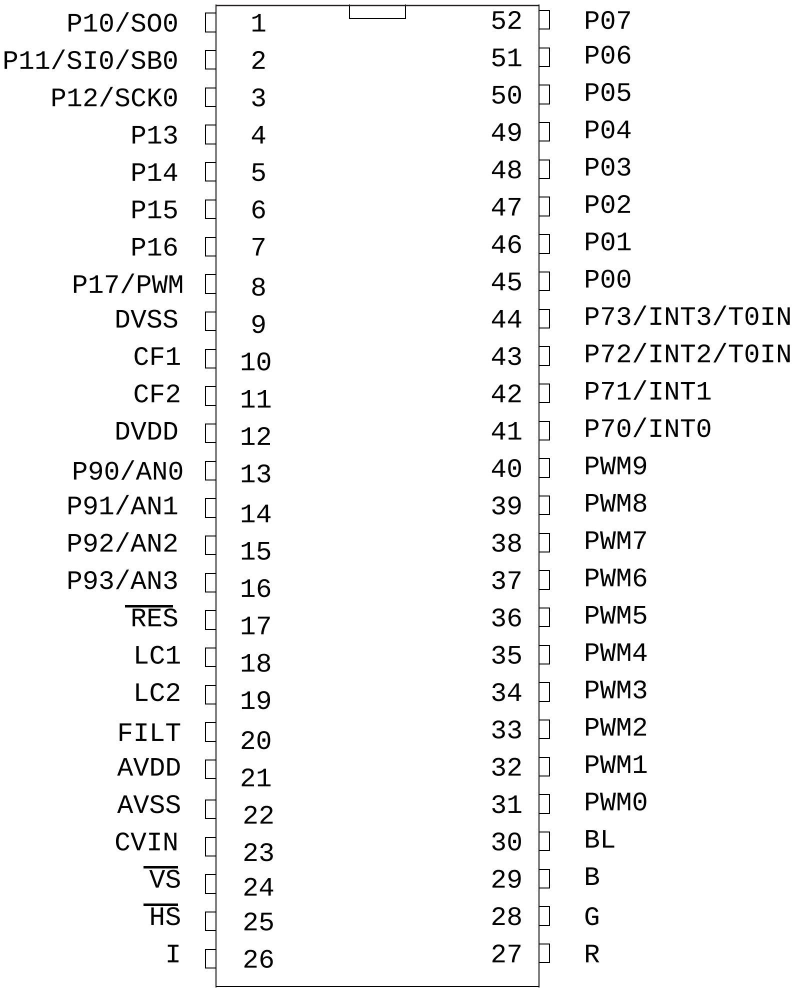
DIP52S

(18) Development Tool
- Evaluation chip : LC866098
- EPROM with a Window : LC86E4332
- One time ROM version : LC86P4332
- Emulator : EVA86000 (Main) + ECB864300 (Evaluation board) + POD864100 (Pod)

System Block Diagram


Interrupt control
Standby control
CR
RC
LC
Clock generator
IR
PLA
ROM
PC
Bus interface
ACC
SIO0
Port 1
B register
Timer 0
Port 7
C register
Timer 1
ALU
ADC
Port 9
INT0 to INT3
Noise rejection filter
Data slicer
PSW
PWM
PLL
RAR
CGROM
RAM
OSD
control
circuit
VRAM
Stack pointer
Port 0
Watchdog timer

Pin Assignment


P10/SO0 1
P11/SI0/SB0 2
P12/SCK0 3
P13 4
P14 5
P15 6
P16 7
P17/PWM 8
DVSS 9
CF1 10
CF2 11
DVDD 12
P90/AN0 13
P91/AN1 14
P92/AN2 15
P93/AN3 16
$\overline{\text{RES}}$ 17
LC1 18
LC2 19
FILT 20
AVDD 21
AVSS 22
CVIN 23
$\overline{\text{VS}}$ 24
$\overline{\text{HS}}$ 25
I 26
52 P07
51 P06
50 P05
49 P04
48 P03
47 P02
46 P01
45 P00
44 P73/INT3/T0IN
43 P72/INT2/T0IN
42 P71/INT1
41 P70/INT0
40 PWM9
39 PWM8
38 PWM7
37 PWM6
36 PWM5
35 PWM4
34 PWM3
33 PWM2
32 PWM1
31 PWM0
30 BL
29 B
28 G
27 R

Top view

Pin Description

- Port option can be specified in bit units except the pull-up resistor selection of port 0.

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option
DVSS	9	—	Negative power supply for digital circuit	
CF1	10	Input	Input terminal for ceramic resonator	
CF2	11	Output	Output terminal for ceramic resonator	
DVDD	12	—	Positive power supply for digital circuit	
$\overline{\text{RES}}$	17	Input	Reset terminal	
LC1	18	Input	LC oscillation circuit input terminal	
LC2	19	Output	LC oscillation circuit output terminal	
FILT	20	Output	Filter terminal for PLL	
AVDD	21	—	Positive power supply for analog circuit	
AVSS	22	—	Negative power supply for analog circuit	
CVIN	23	Input	Video signal input terminal	
$\overline{\text{VS}}$	24	Input	Vertical synchronization signal input terminal	
$\overline{\text{HS}}$	25	Input	Horizontal synchronization signal input terminal	
I	26	Output	Image intensity output	
R	27	Output	Red (R) output terminal of RGB image output	
G	28	Output	Green (G) output terminal of RGB image output	
B	29	Output	Blue (B) output terminal of RGB image output	
BL	30	Ouptut	Fast blanking control signal Switch TV image signal and caption / OSD image signal	
PWM0 to PWM9	31 to 40	Output	PWM0 to 9 output terminal 15 V withstand	
Port 0 P00 to P07	45 to 52	I/O	8-bit Input/output port Input/output can be specified in nibble units HOLD release input Interrupt input	Pull-up resistor Provided/not provided (in bit units) Output Format CMOS/Nch-OD (in bit units)
Port 1 P10 to P17	1 to 8	I/O	8-bit Input/output port Input/output can be specified in bit units. Other function P10 SIO0 data output P11 SIO0 data input / bus input / output P12 SIO0 clock input / output P17 Timrt 1 (PWM) output	Output Format CMOS/Nch-OD (in bit units)
Port 7 P70 P71 to P73	41 42 to 44	I/O Input	4-bit input port Other function P70 INT0 input / HOLD release input / Nch-transistor output for watchdog timer P71 INT1 input / HOLD release input P72 INT2 input / timer 0 event input P73 INT3 input (noise rejection filter attached input) / timer 0 event input Interrupt receiver format vector address	Pull-up resistor provided/ not provided (in bit units)

	Rising	Falling	Rising/falling	H level	L level	Vector
INT0	enable	enable	disable	enable	enable	03H
INT1	enable	enable	disable	enable	enable	0BH
INT2	enable	enable	enable	disable	disable	13H
INT3	enable	enable	enable	disable	disable	1BH

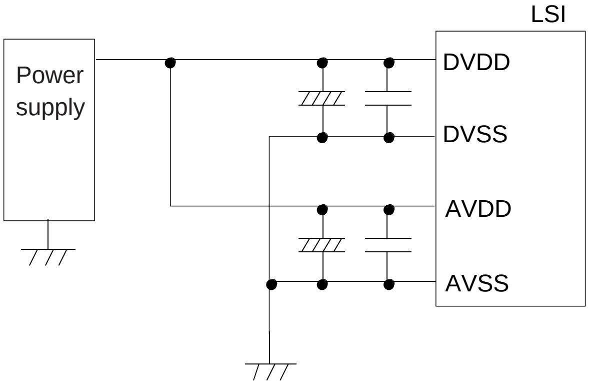
Pin name	Pin No.	I/O	Function Description	Option
Port 9 P90 to P93	13 to 16	Input	4-bit input port Other function AD converter input port (4 lines)	

- Any port option can be selected in bit units.
- Port 0 portion : Pull-up resistor is provided when CMOS output is selected.
  The pull-up resister is not provided when N-ch Open Drain is selected.
- Port 1 option : Programmable pull-up resister is provided when any output form is selected.

- Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

- AVDD and AVSS are the power supply terminals for built-in analog circuit. DVDD and DVSS are the power supply terminals for built-in digital circuit. Connect them like the following figure to reduce the mutual noise-influence.



Specifications

1. Absolute Maximum Ratings at Ta=25°C , V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD} [V]	min	typ	max	
Supply voltage		V_{DD} max	DVDD, AVDD	DVDD = AVDD		–0.3		+7.0	V
Input voltage		V_I(1)	• P71, 72, 73 • Port 9 • $\overline{\text{RES}}$, $\overline{\text{HS}}$, $\overline{\text{VS}}$, CVIN			–0.3		V_{DD}+0.3	
Output voltage		V_O(1)	R, G, B, BL, I, FILT			–0.3		V_{DD}+0.3	
		V_O(2)	PWM0 to PWM9			–0.3		+15	
Input/output voltage		V_{IO}	Ports 0, 1, P70			–0.3		V_{DD}+0.3	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1	• Pull-up MOS transistor output • At each pin		–2			mA
		I_{OPH}(2)	Ports 0, 1	• CMOS output • At each pin		–4			
		I_{OPH}(3)	R, G, B, BL, I	• CMOS output • At each pin		–5			
	Total output current	ΣI_{OAH}(1)	Port 1	The total of all pins		–10			
		ΣI_{OAH}(2)	Port 0	The total of all pins		–10			
		ΣI_{OAH}(3)	R, G, B, BL, I	The total of all pins		–15			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1	At each pin				20	
		I_{OPL}(2)	P70	At each pin				30	
		I_{OPL}(3)	• R, G, B, BL, I • PWM0 to PWM9	At each pin				5	
	Total output current	ΣI_{OAL}(1)	Port 0	The total of all pins				40	
		ΣI_{OAL}(2)	Port 1, P70	The total of all pins				40	
		ΣI_{OAL}(3)	R, G, B, BL, I	The total of all pins				15	
		ΣI_{OAL}(4)	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIP52S	Ta = –30 to +70°C				430	mW
Operating temperature range		Topr				–30		+70	°C
Storage temperature range		Tstg				–55		+150	

* DVSS and AVSS must be supplied the same voltage, V_{SS}. V_{SS} = DVSS = AVSS
DVDD and AVDD must be supplied the same voltage, V_{DD}. V_{DD} = DVDD = AVDD

2. Recommended Operating Range at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage range	V_{DD}	DVDD, AVDD	0.97 µs ≤ tCYC tCYC ≤ 1.02 µs		4.5		5.5	V
Hold voltage	V_{HD}	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high-level voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V_{DD}		V_{DD}	
	V_{IH}(2)	• Port 1 (Schmitt) • P72, 73 • $\overline{HS}$, $\overline{VS}$	Output disable	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V_{DD}-0.5		V_{DD}	
	V_{IH}(5)	Port 9 port input		4.5 to 5.5	0.7V_{DD}		V_{DD}	
Input low-level voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Port 1 (Schmitt) • P72, 73 • $\overline{HS}$, $\overline{VS}$ • Port 9	Output disable	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.6V_{DD}	
	V_{IL}(5)	Port 9 port input		4.5 to 5.5	V_{SS}		0.3V_{DD}	
CVIN input amplitude	V_{CVIN}	CVIN		5.0	1Vp-p –3dB	1Vp-p	1Vp-p +3dB	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.97	1	1.02	µs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.97		40	

* Vp-p : Peak-to-peak voltage

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmCF(2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 1.		11.84	12.08	12.32	
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.3	0.8	2.0	
Oscillation stable time period (Note 2)	tmsCF(1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms
	tmsCF(2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 3.			0.02	0.2	

(Note 1) Refer to Table 1 and 2 for the oscillation constant.

(Note 2) The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released the main-clock oscillation stop instruction released.
Refer to the Figure 3 for details.

3. Electrical Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Input high-level current	I_{IH}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V_{IN} = V_{DD} (including the off-leak current of the output transistor)	4.5 to 5.5			1	µA
	I_{IH}(2)	• Port 7 without pull-up MOS transistor • Port 9 • $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	V_{IN} = V_{DD}	4.5 to 5.5			1	
Input low-level current	I_{IL}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • V_{IN} = V_{SS} (including the off-leak current of the output transistor)	4.5 to 5.5	–1			
	I_{IL}(2)	• Port 7 without pull-up MOS transistor • Port 9	V_{IN} = V_{SS}	4.5 to 5.5	–1			
	I_{IL}(3)	• $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	V_{IN} = V_{SS}	4.5 to 5.5	–1			
Output high-level voltage	V_{OH}(1)	CMOS output of ports 0, 1	I_{OH} = –1.0 mA	4.5 to 5.5	V_{DD}–1			V
	V_{OH}(2)	R, G, B, BL, I	I_{OH} = –0.1 mA	4.5 to 5.5	V_{DD}–0.5			
Output low-level voltage	V_{OL}(1)	Ports 0, 1	I_{OL} = 10 mA	4.5 to 5.5			1.5	
	V_{OL}(2)	Ports 0, 1	• I_{OL} = 1.6 mA • The total current of the ports 0, 1 is 40 mA or less.	4.5 to 5.5			0.4	
	V_{OL}(3)	• R, G, B, BL, I • PWM0 to PWM9	• I_{OL} = 3.0 mA • The current of any unmesured pin is 3 mA or less.	4.5 to 5.5			0.4	
	V_{OL}(4)	P70	I_{OL} = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports 0, 1 • Port 7	V_{OH} = 0.9 V_{DD}	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I_{OFF}	PWM0 to PWM9	V_{OUT} = 13.5 V	4.5 to 5.5			5	µA
Hysteresis voltage	V_{HIS}	• Ports 0, 1 • Port 7 • $\overline{RES}$ • $\overline{HS}$, $\overline{VS}$	Output disable	4.5 to 5.5		0.1V_{DD}		V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Input clamp voltage	V_{CLMP}	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	• f = 1MHz • Unmeasured terminals for the input are set to V_{SS} level. • Ta = 25°C	4.5 to 5.5		10		pF

4. Serial Input/Output Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions		Ratings			Unit
						V_{DD} [V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0 • SCLK0	Refer to Figure 5.	4.5 to 5.5	2			tCYC
		Low level pulse width	tCKL(1)				1			
		High level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	• SCK0 • SCLK0	• Use an external pull-up resistor (1 kΩ) when an open drain output • Refer to Figure 5.	4.5 to 5.5	2			
		Low level pulse width	tCKL(2)					1/2tCKCY		
		High level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	• SI0	• Set to the rise of SCK0 • Refer to Figure 5.	4.5 to 5.5	0.1			µs
	Data hold time		tCKI			4.5 to 5.5	0.1			
Serial output	Output delay time (External serial clock)		tCKO(1)	• SO0	• Use an external pull-up resistor (1 kΩ) when an open drain output. • Set to the fall of SCK0 • Refer to Figure 5.	4.5 to 5.5			7/12tCYC +0.2	µs
	Output delay time (Internal serial clock)		tCKO(2)			4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is set to 1/1)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is set to 1/16)	• Interrupt acceptable • Timer0-countable	4.5 to 5.5	32			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 5.5	200			µs
	tPIH(5) tPIL(5)	$\overline{\text{HS}}$, $\overline{\text{VS}}$	Display position controllable Each active edge of $\overline{\text{HS}}$, $\overline{\text{VS}}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10			tCYC
Rising/falling time	tTHL tTLH	$\overline{\text{HS}}$	Refer to Figure 7.	4.5 to 5.5			500	ns
Horizontal pull-in range	FH	$\overline{\text{HS}}$	The monitor point in Figure 10 is 1/2 V_{DD}.	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Resolution	N			4.5 to 5.5		5		bit
Absolute precision	ET	(Note 3)		4.5 to 5.5		±1/4	±3/4	LSB
Conversion time	tCAD	From Vref selection to when the result is output	1 bit conversion time = 2tCYC	4.5 to 5.5		2		µs
Reference current	I_{REF}		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V_{AIN}	AN0 to AN3		4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		$V_{AIN} = V_{DD}$	4.5 to 5.5			1	µA
	I_{AINL}		$V_{AIN} = V_{SS}$	4.5 to 5.5	–1			

(Note 3) Absolute precision excepts quantizing error (±1/2 LSB).

7. Current Drain Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Current drain during basic operation (Note 4)	$I_{DDOP}(1)$	DVDD, AVDD	• FmCF = 12 MHz or FmCF = 12.08 MHz When ceramic resonator oscillation • FmLC = 14.11 MHz When LC oscillation • System clock : CF oscillation • Internal RC oscillation stops	4.5 to 5.5		16	28	mA
Current drain in HALT mode (Note 4)	$I_{DDHALT}(1)$	DVDD, AVDD	• HALT mode • FmCF = 12 MHz or FmCF = 12.08 MHz When ceramic resonator oscillation • FmLC = 0 Hz (When oscillation stops) • System clock : CF oscillation • Internal RC oscillation stops.	4.5 to 5.5		5	10	mA
	$I_{DDHALT}(2)$	DVDD, AVDD	• HALT mode • FmCF = 0 MHz (When oscillation stops) • FmLC = 0 Hz (When oscillation stops) • System clock : Internal RC	4.5 to 5.5		600	1200	µA
Current drain in HOLD mode (Note 4)	I_{DDHOLD}	DVDD, AVDD	• HOLD mode • All oscillation stops.	4.5 to 5.5		0.05	20	µA

Note 4 : The currents to the output transistors and the pull-up MOS transistors are ignored.

Oscillation types	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
12.08 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ021	33 pF	33 pF
	Kyocera	KBR-12.08M	33 pF	33 pF

* Both C1 and C2 must use a K rank (±10%) and SL characteristics.

Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)

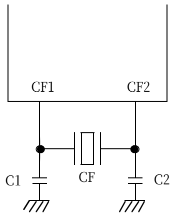
Oscillation type	L	C3	C4
14.11 MHz LC oscillation	4.7 µH	33 pF	45 pF (Trimmer)
	4.7 µH ±10% (Variable)	33 pF	33 pF

* See Figures 11 and 12.

Table 2. LC oscillation Guaranteed Constant (OSD clock)

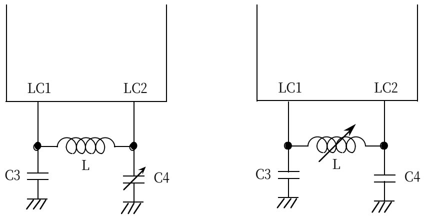
(Notes)

- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
- If you use other oscillators than those shown above, we provide no guarantee for the characteristics.
- Adjust the voltage of monitor point in figure 10 to 1/2 V_{DD} ±10% by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



Main clock

Figure 1 Ceramic Resonator Oscillation



OSD clock

Figure 2 LC Resonator Oscillation

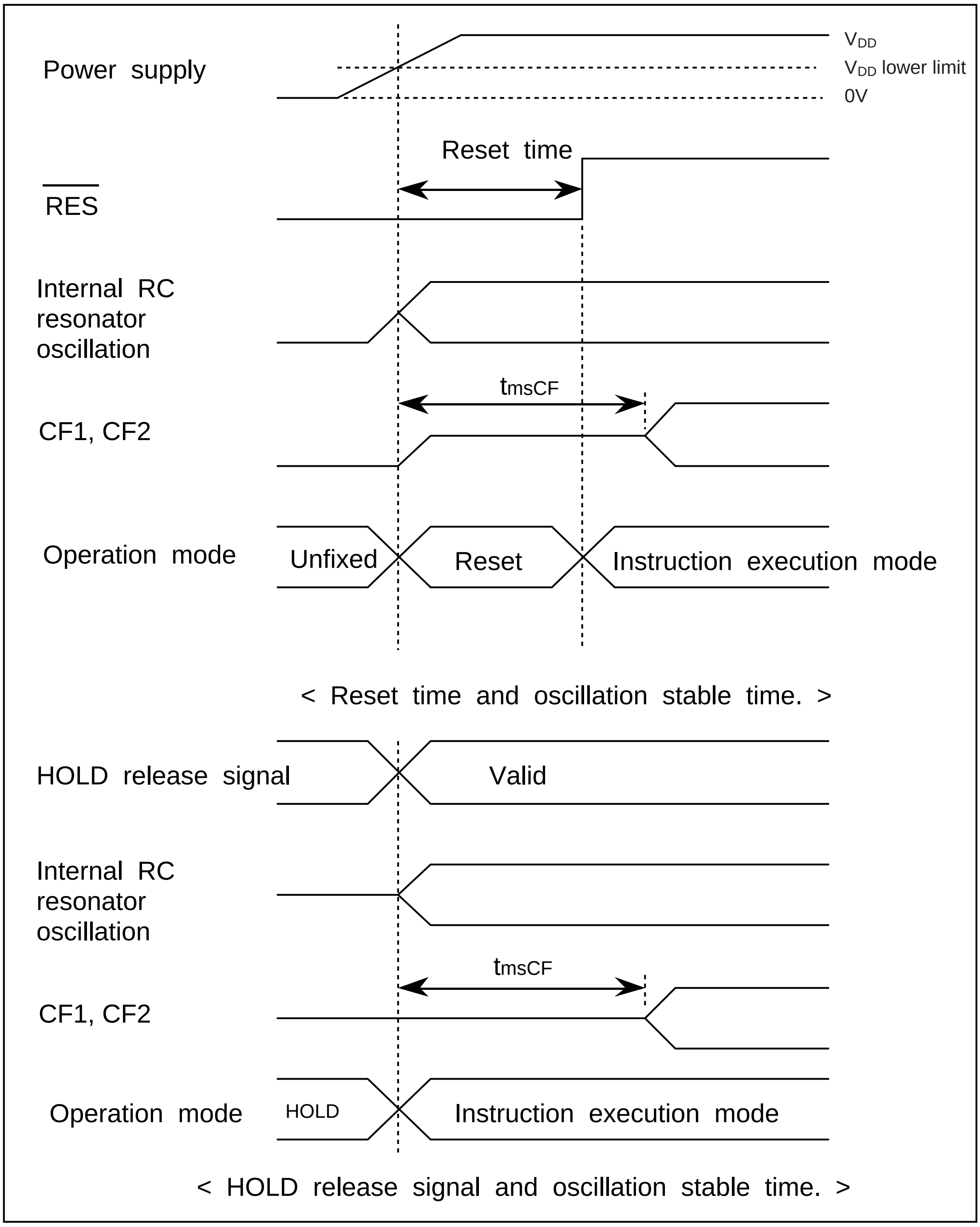
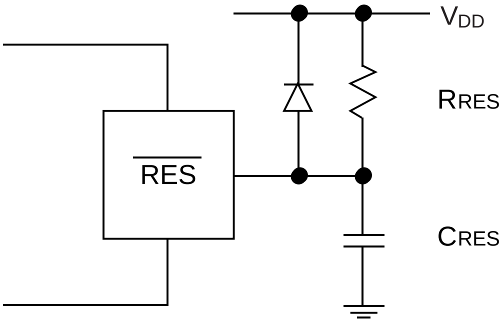
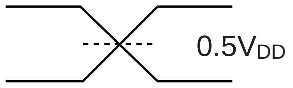

Power supply
VDD
VDD lower limit
0V
Reset time
RES
Internal RC resonator oscillation
tmsCF
CF1, CF2
Operation mode
Unfixed
Reset
Instruction execution mode
< Reset time and oscillation stable time. >
HOLD release signal
Valid
Internal RC resonator oscillation
tmsCF
CF1, CF2
Operation mode
HOLD
Instruction execution mode
< HOLD release signal and oscillation stable time. >

Figure 3 Oscillation Stable Time

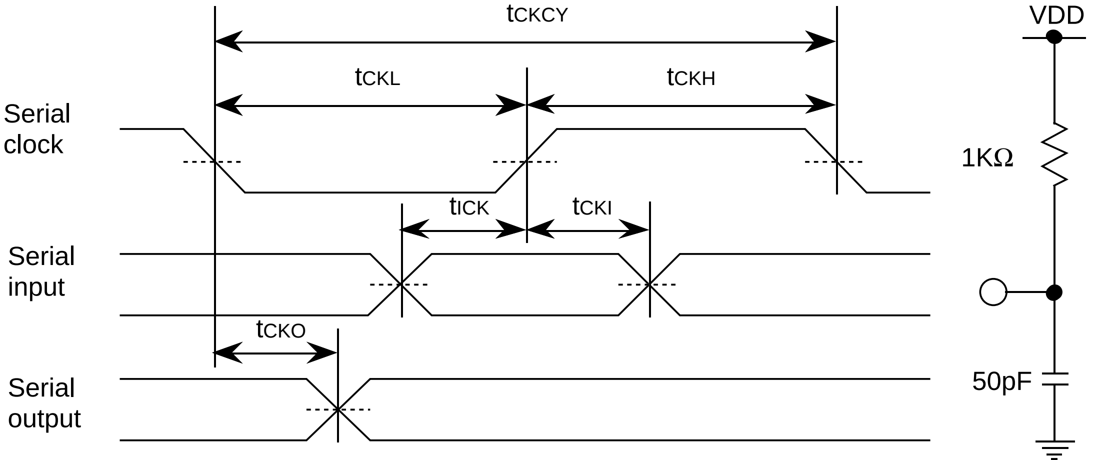

VDD
RRES
RES
CRES

(Note) Set the values of C_{RES}, R_{RES} so that the reset time is 200 µs or longer.

Figure 4 Reset Circuit



< AC timing point >


tCKCY
tCKL
tCKH
Serial clock
tICK
tCKI
Serial input
tCKO
Serial output
VDD
1KΩ
50pF

< Timing >

< Test load >

Figure 5 Serial Input/output Test Condition

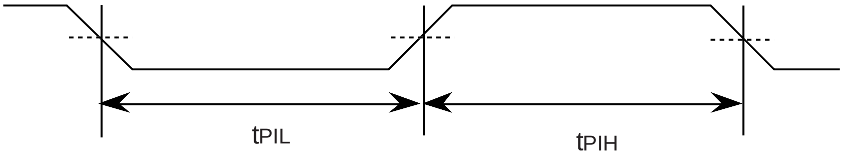
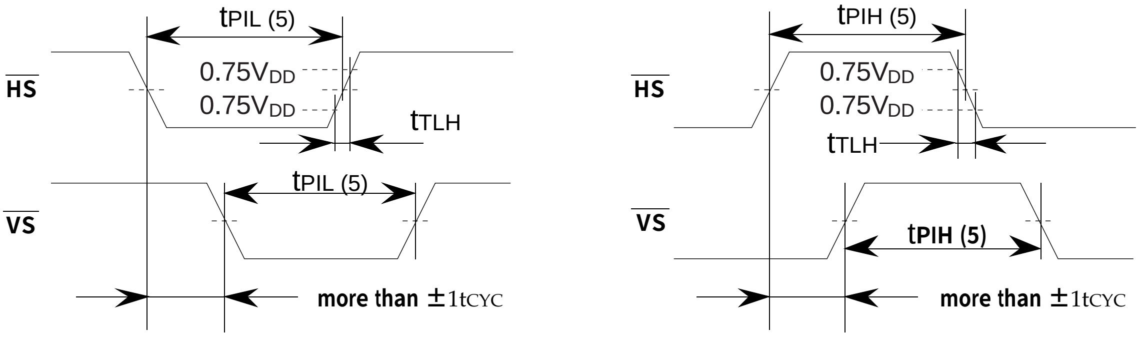


Figure 6 Pulse Input Timing Condition - 1


tPIL (5)
HS
0.75VDD
0.75VDD
tTLH
tPIL (5)
VS
more than ±1tCYC
tPIH (5)
HS
0.75VDD
0.75VDD
tTLH
VS
tPIH (5)
more than ±1tCYC

(a) In case of active low

(b) In case of active high

Figure 7 Pulse Input Timing Condition - 2

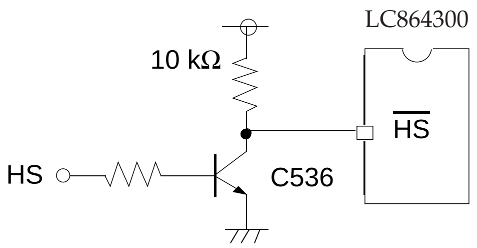

LC864300
10 kΩ
HS
HS
C536

Figure 8 Recommended Interface Circuit

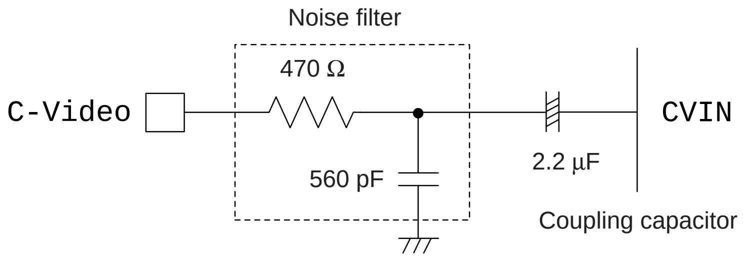

Noise filter
470 Ω
C-Video
560 pF
2.2 µF
CVIN
Coupling capacitor

Figure 9 CVIN Recommended Circuit

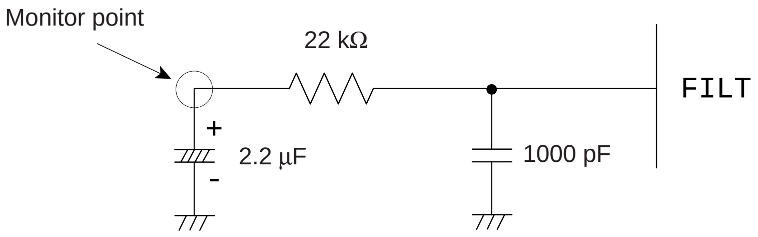

Monitor point
22 kΩ
FILT
+
2.2 µF
-
1000 pF

Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the pattern length on the board.

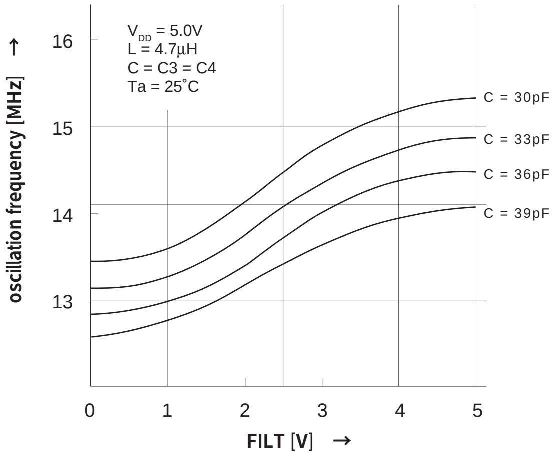


Figure 11 FILT-LC Oscillation Frequency(1)

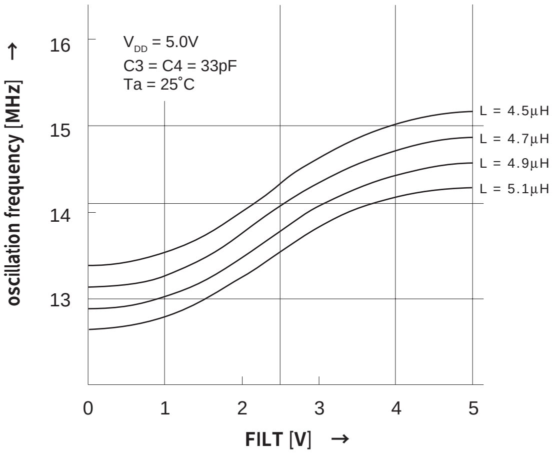


Figure 12 FILT-LC Oscillation Frequency(2)

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use
  ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1998. Specifications and information herein are subject to change without notice.