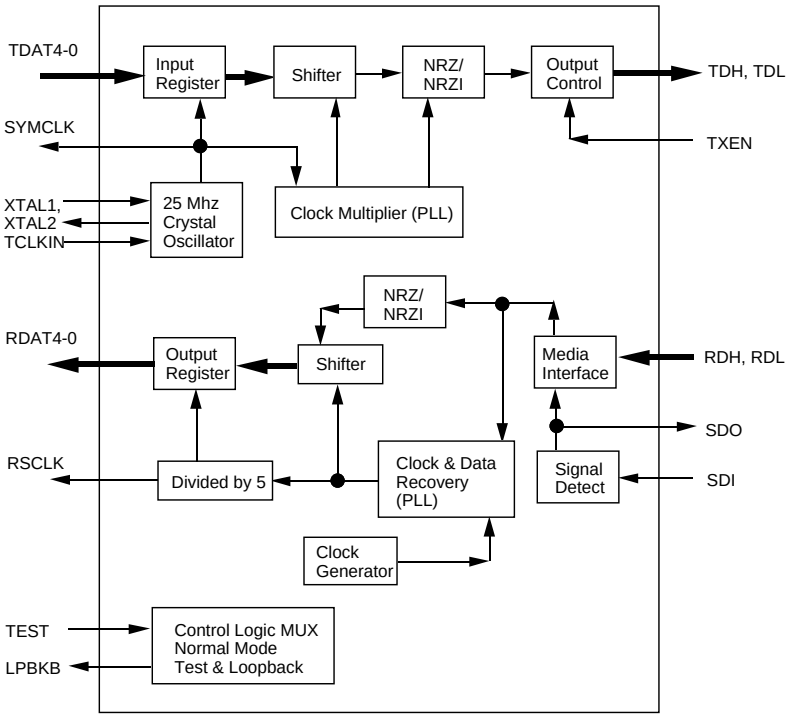
1.0 FEATURES

- Full-Duplex Operation
- Generates 125-Mhz Transmit Clock and 25-Mhz SYMCLK
- Converts 5-Bit Parallel Transmit Data to 1-Bit Serial Data
- Converts Transmit NRZ Data to NRZI Data
- Loopback and Transmitter-Off Modes
- Recovers 125-MHz Clock from Incoming serial NRZI Data Stream
- Reclocks Incoming Serial NRZI Data Stream Using Recovered Clock
- Converts Received Serial Bit Stream to 5-Bit Paralled Form
- Converts NRZI data to NRZ
- Generates 25-MHz Receive Clock
- Package type
  - -52 PLCC
  - -52 PQFP

2.0 GENERAL DESCRIPTION

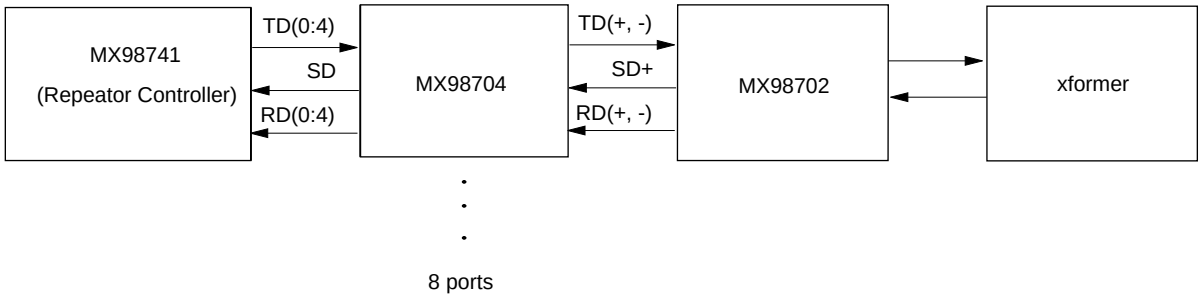
The 100Base-Tx Physical Data Transceiver (PDTR) includes the Physical Data Transmitter (PDT) and the Physical Data Receiver (PDR). The PDT converts encoded symbols into a serial NRZI data stream. The on-chip PLL generates a bit rate clock from the TCLKIN or crystal reference. The PDR uses a built-in clock recovery PLL to extract clock information from the received data stream. The recovered clock is used for serial-to-parallel data conversion.

2.1 FUNCTIONAL BLOCK DIAGRAM



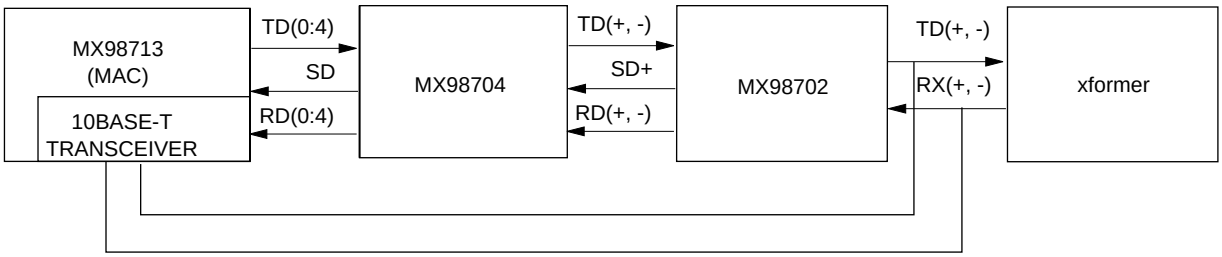
Data Transceiver Functions Block Diagram

2.1.1 100 BASE-TX HUB APPLICATION



100 BASE-TX HUB SYSTEM DIAGRAM

2.1.2 10/100-TX NIC APPLICATION



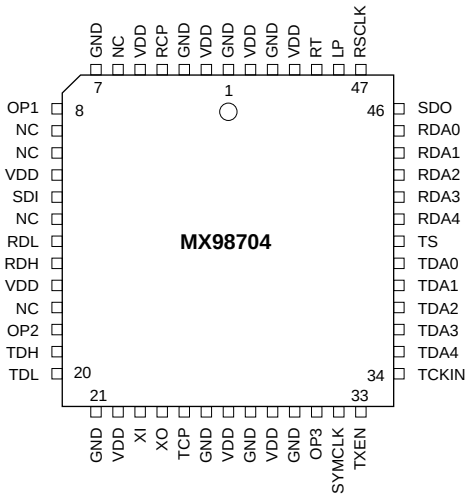
10/100-TX NIC Application

2.2 SYSTEM APPLICATION

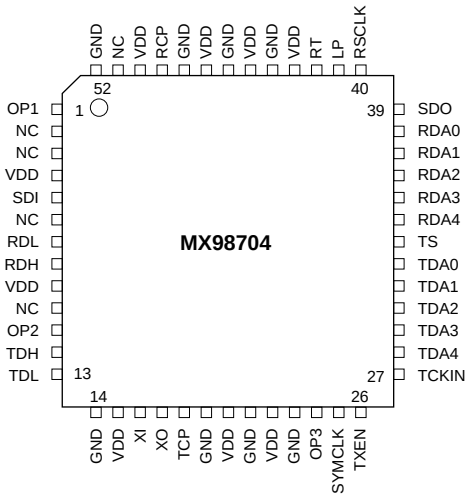
The MX98704 can be used in 100 BASE-TX HUB application, and 10/100-TX NIC application.

3.0 PIN ASSIGMENT

3.1 PIN ASSIGNMENT-52 LEAD PLASTIC LEADED CHIP CARRIER



3.2 PIN ASSIGNMENT-52 PQFP



4.0 PIN DESCRIPTIONS

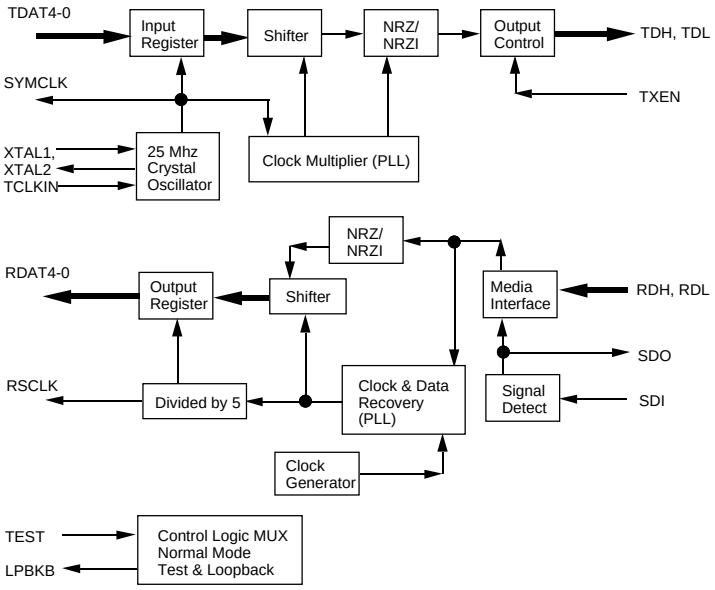
MX Physicial Data Transceiver (PDTR) Function Pin

PIN (PLCC)	PIN (PQFP)	PIN NAME	TYPE	DESCRIPTION
1	46	GND	I	Ground.
2	47	VDD	I	Power Supply. 5V
3	48	GND	I	Ground.
4	49	Test	O	Receiver Filter.
5	50	VDD	I	Power Supply. 5V
6	51	N/C		
7	52	GND	I	Ground.
8	1	OP1	I	Parameter Option (GND is recommended)
9	2	N/C		
10	3	N/C		
11	4	VDD	I	power Supply. 5V
12	5	SDI	I	Signal Detect Input. This signal indicates that the received signal is above the detection threshold.
13	6	N/C		
14	7	RDL	I	Received Data. (Differential Line Receiver Inputs). These pins receive NRZI data.
15	8	RDH	I	Received Data. (Differential Line Receiver Inputs). These pins receive NRZI data.
16	9	VDD	I	Power Supply. 5V
17	10	NC	O	
18	11	OP2	I	Parameter Option (GND is recommended)
19	12	TDH	O	Transmit Data. These transmit output carrier differential NRZ data. They can be forced to logical 0 (TDH Low, TDL high) by asserting the TXEN input.
20	13	TDL	O	Transmit Data. These transmit output carrier differential NRZ data. They can be forced to logical 0 (TDH Low, TDL high) by asserting the TXEN input.
21	14	GND	I	Ground.
22	15	VDD	I	Power Supply. 5V
23	16	XTALI	I	25MHz Transmit clock. These pins are 25MHz crystal connection for transmit clock.
24	17	XTALO	O	25MHz Transmit colck. These pins are 25MHz crystal connection for transmit clock.

PIN (PLCC)	PIN (PQFP)	PIN NAME	TYPE	DESCRIPTION
25	18	Test	O	Transmit Filter.
26	19	GND	I	Ground.
27	20	VDD	I	Power Supply. 5V
28	21	GND	I	Ground.
29	22	VDD	I	Power Supply. 5V
30	23	GND	I	Ground.
31	24	OP3	O	Parameter Option (GND is recommended)
32	25	SYMCLK	O	Local Symbol Clock. This pin supplies the frequency reference to the transmit logic. It is the buffered 25MHz oscillator output.
33	26	TXEN	I	Transmit Enable. When held LOW, the TDH output is forced LOW, and TDL output is forced HIGH so that the transmitter will output logical 0. This TTL-level signal has an internal pullup resistor.
34	27	TCLKIN	I	Transmit Clock In. This pin is a 25Mhz optional clock input.
35-39	28-32	TDAT4-0	I	Transmit Data. These five inputs are 4B/5B encoded transmit data symbols, latched by the rising edge of SYMCLK. TDAT4 is the Most Significant Bit.
40	33	TSB	I	Three-State. While this pin input is low, the interface output pins are forced into the high-impedance state. Pins controlled by this signal are PDAT4-0, SDO, BYTCLK, SYMCLK and RSCLK. This TTL-level signal has an internal pullup resistor.
41-45	34-38	RDAT4-0	O	Receive Data. These 5-bit parallel data symbols from transceiver are clocked by the falling edge of RSCLK and carry the NRZ data symbols to the controller. RDAT4 is the Most Significant Bit.
46	39	SDO	O	Signal Detect Output. SDO is the SDI input Asynchronized by RSCLK. It has the same logical sense as SDI.
47	40	RSCLK	O	Recovered Symbol Clock. This is a 25MHz clock, which is derived from the receive clock synchronization PLL circuit. It is synchronous to the received serial data, and is the recovered bit clock divided-by-five.
48	41	LPBKB	I	Loopback. (Active LOW) The function is used during system loopback test to bypass the transmission medium. This TTL-level signal has an internal pullup resistor.
49	42	TEST	I	Test Mode Enable. When asserted, the PDTR is in Test mode. For normal operation, TEST pin must be tied High. This TTL-level signal has an internal pullup resistor.
50	43	VDD	I	Power Supply. 5V
51	44	GND	I	Ground.
52	45	VDD	I	Power Supply. 5V

5.0 FUNCTIONAL DESCRIPTION

Functional block diagram of the complete chip.



Data Transceiver Functions Block Diagram

5.1 NORMAL OPERATION MODE

The 5-bit data symbols to be transmitted are input from the PDTR chip on TDAT4-TDAT0.. The 5-bit symbol is latched into the PDT by the rising edge of SYMCLK, serialized and shifted to the output (TDAT4 bit is the first bit transmitted, and TDAT0 is the last bit transmitted). The TDH/TDL pair is connected to the serial link.

To generate the serial link data rate, the PDT uses SYMCLK as the frequency reference. All of the internal logic of PDT runs on an internal clock that is PLL-multiplied from the external reference source. The PDT's internal PLL is referenced to the falling edge of SYMCLK only.

The input clock frequency required to achieve 125 Mbaud on serial link is 25MHz at SYMCLK. The external TCLKIN or external Crystal reference clock (XTAL1, XTAL2) must meet I.E.E.E. frequency and stability requirements. The PDT serial output typically contains less than 0.4ns peak-to-peak jitters at 125 Mbaud. The latency from the SYMCLK to the serial output is typical 4 to 6 bits (8 ns/bit).

The PDR accepts encoded NRZI serial data on the RDH/ RDL inputs. It latches the unframed symbol (5 bits) to the RDAT4-0 outputs on the falling edge of RSCLK. Five new bits are valid on each rising edge of RSCLK. RDAT4 is the first bit received and RDAT0 is the last bit received from the serial interface.

The heart of PDR is its clock-recovery PLL, which extracts encoded clock information from the serial NRZ data stream and recovers the data. The PLL examines every data transition in the received serial stream and aligns its internal bit clock with these data transitions. In order to guarntee the correct operaion of PLL, the encoding scheme (4B/5B) must ensure adequate transition density of the encoded data stream.

The SDI input qualifies the data at RDH/ RDL. When SDI is LOW, the PDR uses SYMCLK as the PLL input reference. The LPBKB input selects the data source between RDH/ RDL and internal. When LPBKB is LOW, the SDI input is ignored.

5.2 TRANSMIT FUNCTIONS BLOCK

The transmitter consists of several blocks:

5.2.1 CLOCK MULTIPLIER

TCLKIN or Crystal Oscillator supplies the reference frequency which is multiplied by five using an on-chip PLL. The transmission rate and all serialization logic are controlled by the internally generated bit clock.

5.2.2 INPUT REGISTER

TDAT4-0 are clocked into the input Resister by the rising edge of SYMCLK.

5.2.3 SHIFT

Parallel data are loaded from the input Resistor into the Shifter at the internally generated symbol boundary, and serially shifted at the bit clock rate.

5.2.4 NRZ TO NRZI CONVERTER

The NRZ output of the Shifter is converted into NRZI data patterns for transmission.

5.2.5 OUTPUT CONTROL

The differential outputs carry the encoded serial NRZI bit stream. The TDH/ TDL pair can be forced to logical 0 (TDH LOW, TDL HIGH) by asserting TXEN input.

5.3 RECEIVER FUNCTIONS BLOCK

The receiver consists of several blocks:

5.3.1 CLOCK AND DATA RECOVERY PLL

The clock-recovery PLL separates the input data stream into clock and data patterns. The RSCLK is the recovered bit clock divided by five. This is a 25MHz clock.

5.3.2 MEDIA INTERFACE

The RDH/ RDL inputs are typically driven by differential PECL voltages, referenced to +5V. These inputs accept the encoded NRZI serial data.

5.3.3 SIGNAL DETECT (SD)

SDO is a level translation of SDI and indicates whether the receiver on SDI is receiving enough energy to produce a correct output. When SDO is not asserted low, RDAT4-RDAT0 are forced low. The system is in quite condition. SDO is an asynchronous signal that changes whenever the SDI change states.

5.3.4 NRZI TO NRZ CONVERTER

Serial data are retimed and associated jitter is removed. Retimed data are converted into NRZ format prior to the Shifter input.

5.3.5 SHIFT

The Shifter is serially loaded to parallel convert, using the recovered bit clock.

5.3.6 OUTPUT REGISTER

The Output Register is clocked by RSCLK falling edges. RSCLK is the recovered bit clock divided by five and is synchronous to the received serial data.

6.0 ABSOLUTE MAXIMUM RATINGS

Logic Power Referenced to GND	-0.5V to +7.0V
Received Power Referenced to RGND	-0.5V to +7.0V
Transmit Power Referenced to TGND	-0.5V to +7.0V
ECL output Power Referenced to GND	-0.5V to +0.7V
DC output current (High)	-50mA
ESD	2000V
Storage Temperature	-6.5°C to +150°C

7.0 ELECTRICAL CHARACTERISTICS

7.1 MAXIMUM RATINGS

RATING	SYMBOL	MIN	MAX	UNIT
Supply Voltage	Vcc	-0.3	+7.0	Vdc
Input Voltage	Vin	-0.3	Vcc	Vdc
Operating Temperature Range	Ta	0	70	C
Storage Temperature Range	Tstg	-56	+150	C
Junction Temperature	Tj	-40	+130	C

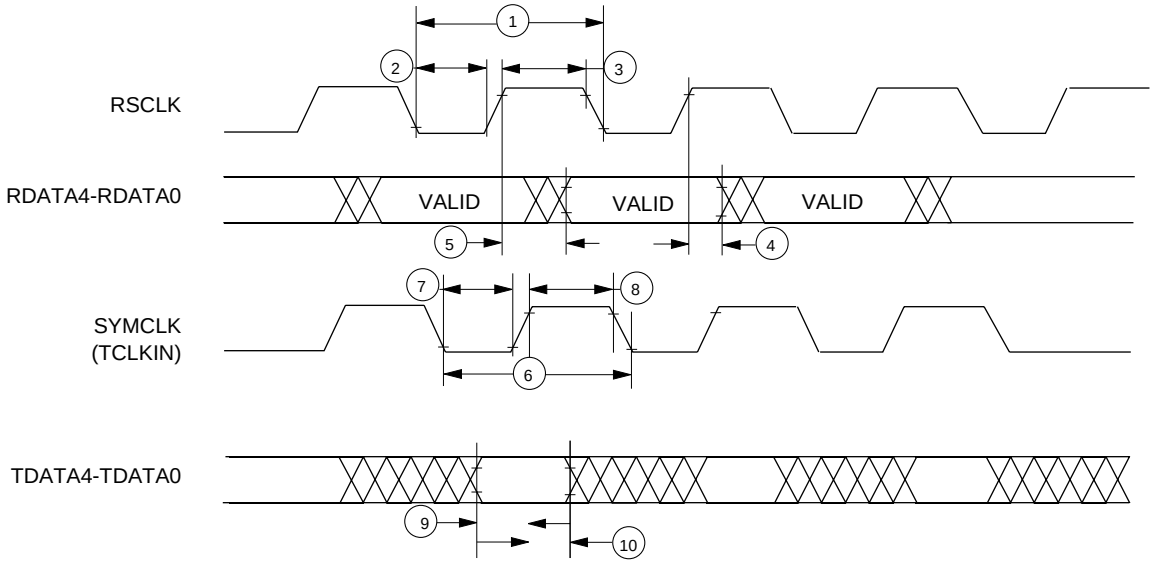
7.2 DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Supply Voltage	Vcc	-0.3	+7.0	Vdc
Input Voltage Low	Vil	-0.3	0.8	Vdc
Input Voltage High	Vih	2.0	VCC+0.3	Vdc
Output Voltage Low	Vol	0.4		Vdc
Output Voltage High	Voh	2.4		Vdc
ECL Output Voltage High	Voh	Vcc-1.1	Vcc-0.8	Vdc
ECL Output Voltage Low	Vol	Vcc-1.9	Vcc-1.6	Vdc
Power Supply Current	Idd		75	ma
Supply Voltage Purity	Vcc	50	mVP-P	

7.3 PARALLEL INTERFACE PARAMETERS

NUM	PARAMETER	MIN	MAX	UNIT
1	RSCLK Period	33	50	ns
2	RSCLK Time Low	20	20	ns
3	RSCLK Time Low	14	26	ns
4	Time to RDATA invalid	8	20	ns
5	Time to RDATA valid	20	32	ns
6	SYMCLK Period	33	50	ns
7	SYMCLK Time Low	20	26	ns
8	SYMCLK Time High	14	20	ns
9	TDATA Setup Time	12	40	ns
10	TDATA Hold Time	0	28	ns

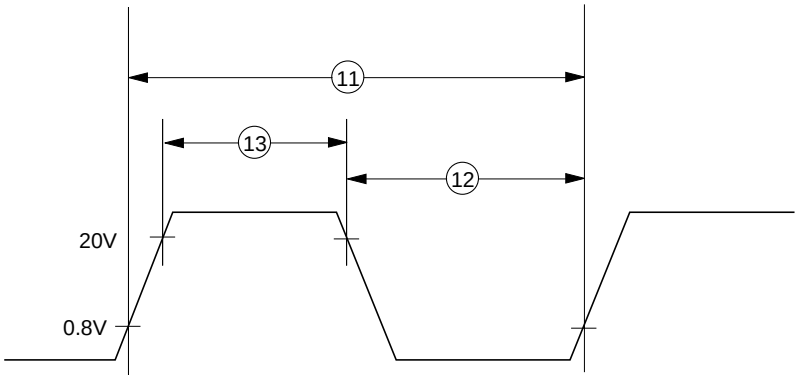
7.3.1 PARALLEL INTERFACE TIMING DIAGRAM



7.4 TCLKIN TIMING PARAMETERS

NUM	PARAMETER	MIN	MAX	UNIT
11	TCLKIN Period	33	50	ns
12	TCLKIN Time Low	8		ns
13	TCLKIN Time High	8		ns

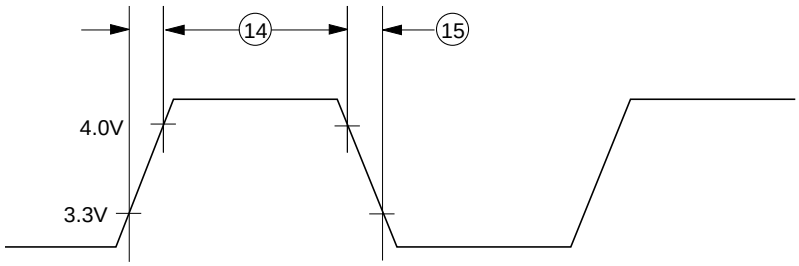
7.4.1 TCLKIN TIMING



7.5 ECL TIMING PARAMETERS

NUM	PARAMETER	MIN	MAX	UNIT
14	ECL Rise Time	0.9	3.0	ns
15	ECL Fall Time	0.9	3.0	ns

7.5.1 ECL TIMING



8.0 ORDER INFORMATION

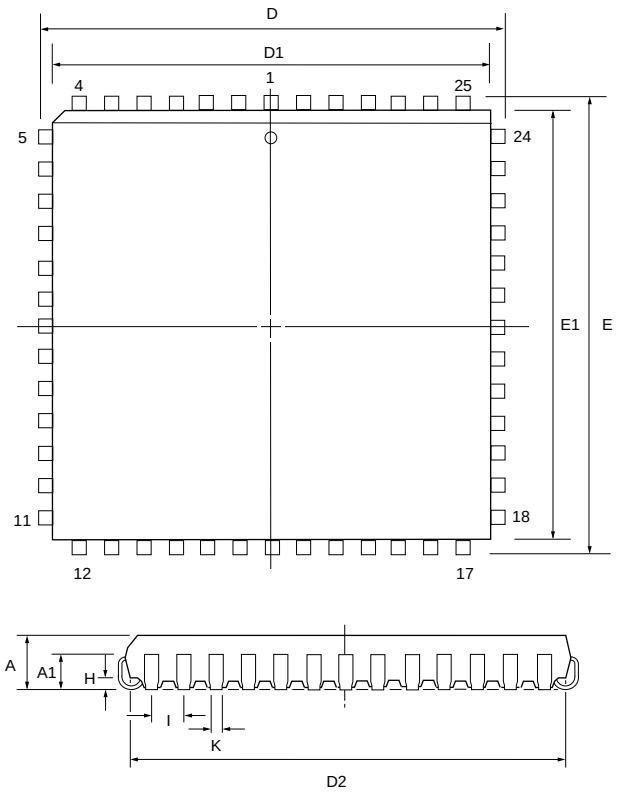
PARTS NO.	PACKAGE
MX98704QC	52-PIN PLCC
MX98704EC	52-PIN PQFP

9.0 PACKAGE INFORMATION

9.1 52-PIN PLCC

ITEM	MILLIMETERS	INCHES
D	20.066	.790
D1	19.126	.753
E	20.066	.790
E1	19.126	.753
D2	18.034	.710
A	4.572	.180
A1	2.667	.105
H	.762	.03
I	1.27	.05
K	0.457	.018

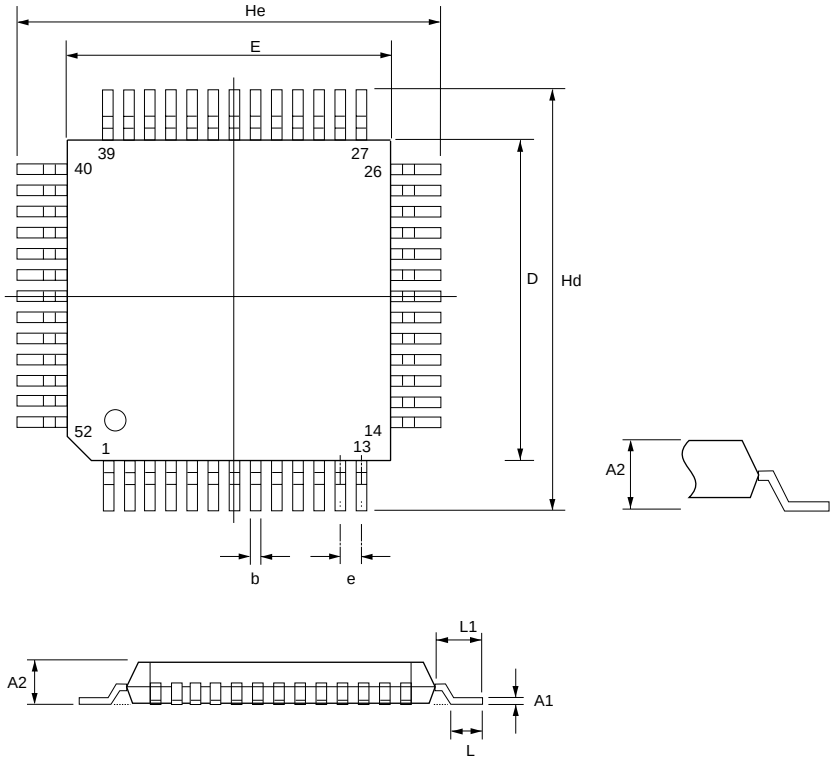
NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.



9.2 52-PIN PQFP

ITEM	MILLIMETERS	INCHES
A1	0.25	0.01
A2	2.05	0.81
b	0.3	0.012
D	10	0.394
E	10	0.394
e	0.65	0.026
Hd	13.2	0.52
He	13.2	0.52
L	0.8	0.031
L1	1.6	0.063

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.



MACRONIX INTERNATIONAL CO., LTD

HEADQUARTERS :
TEL : +886-3-578-8888
FAX : +886-3-578-8887

EUROPE OFFICE :
TEL : +32-2-456-8020
FAX : +32-2-456-8021

JAPAN OFFICE :
TEL : +81-44-246-9100
FAX : +81-44-246-9105

SINGAPORE OFFICE :
TEL : +65-747-2309
FAX : +65-748-4090

TAIPEI OFFICE :
TEL : +886-2-2509-3300
FAX : +886-2-2509-2200

MACRONIX AMERICA INC.
TEL : +1-408-453-8088
FAX : +1-408-453-8488

CHICAGO OFFICE :
TEL : +1-847-963-1900
FAX : +1-847-963-1909

http : //www.macronix.com

ITEM	MILLIMETERS	INCHES
D	12.535	.492
D1	12.015	.452
E	12.535	.492
E1	12.015	.452
D2	10.7	.420
A	4.38	.172
H	.510	.020
I	1.27	.050
K	0.455	.018

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.