Winbond Electronics Corp.

STEREO AUDIO DAC

1. GENERAL DESCRIPTION

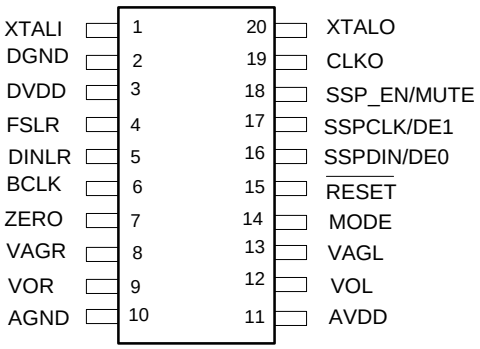
The Winbond W6630 is a stereo audio DAC chip incorporating 8X digital interpolatioin filters, 64X multi-level oversampling delta-sigma modulators, analog low-pass filter and output amplifiers. The operation voltage for this chip can be from 2.7 volt to 5.25 volt. Moreover, the 16 or 18 Bit linear input data for DAC consists of two formats, normal format and I^2S format. In addition, the device includes two control modes. One is hardware mode which can control mute and digital de-emphasis. The other one is software mode, where 4 x 9 bits internal control registers can be controlled by the serial setup port (SSP). Many functions such as 256 step attenuation, DAC mute, digital de-emphasis and format conversions can be setup through these registers.

Because the device can reach into the high performance and low-cost design , the main application for this device is used as some consumers system such as the VCD system, CD player system, and MPEG audio system .

2. FEATURES

- Power Supply from +2.7 to +5.25 Volt, typically +5 Volt, for Analog and Digital Power
- Sampling Clock Rate: 32 K, 44.1 K, and 48 KHz
- Master Clock Rate: 384 or 256 times of Sampling Clock Rate
- Stereo 16 or 18 Bits Linear PCM Data Input
- Two Types Linear PCM Data Input Format: Normal and I^2S Format
- Delta-Sigma DAC built-in digital De-emphasis filter, 8X Interpolator, 64X Oversampling Multi-Bit Modulator
- Stereo DAC Output built-in Analog Low Pass Filter and Ouput Amplifier with 5K Ω Load
- High Performance Audio Output: 100 dB SNR, 96 dB Dynamic Range and -90 dB THD+N
- Two Control Function Modes: Hardware Mode and Software Mode Selected by Mode Pin
- Software Mode Controlled by 4x9 bits Registers via Serial Setup Port (SSP)
- Main Control Functions: De-emphasis, Mute, 256 Step Attenuation, Channel Output Combination,
- Input Format Select such as 16 or 18 Bit, I^2S or Normal.
- Packaged in 20 pin SSOP

3. PIN CONFIGURATION



SSOP-20
(TOP VIEW)

Figure 3-1 Audio DAC Pin Configuration

4. PIN DESCRIPTIONS

4.1. Power Control Interface

PIN NAME	PIN NO.	I/O	FUNCTION
DVDD	3	I	This pin is the digital power supply from 2.7 volt to 5.25 volt, and +5 Volt typically.This pin should be decoupled to DGND with a 0.1 µF capacitor.
DGND	2	I	This pin is the digital ground and typically connected to 0 volt.
AVDD	11	I	This pin is the analog power supply from 2.7 volt to 5.25 volt, and +5 Volt typically.This pin should be decoupled to AGND with a 0.1 µF capacitor.
AGND	10	I	This pin is the analog ground and typically connected to 0 volt.

4.2. Analog Interface

PIN NAME	PIN NO.	I/O	FUNCTION
VOL	12	O	This pin is the analog left channel DAC output from output amplifier.The maximum output voltage for this pin is 0 dB, about 0.62 times AVDD Vpp.
VAGL	13	O	This is the analog signal ground output pin which supplies a 2.5 volt reference voltage for the left channel DAC output if AVDD is +5 volt typically. This pin should be decoupled to AGND with 10 µF capacitor.

4.2. Analog Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
VOR	9	O	This pin is the analog right channel DAC output from output amplifier.The maximum output voltage for this pin is 0 dB, about 0.62 times AVDD Vpp.
VAGR	8	O	This is the analog signal ground output pin which supplies a 2.5 volt reference voltage for the right channel DAC output if AVDD is +5 volt typically. This pin should be decoupled to AGND with 10 µF capacitor.

4.3. Digital Interface

PIN NAME	PIN NO.	I/O	FUNCTION
$\overline{\text{RESET}}$	15	I	This pin the device reset input pin. When it is logic -0, the chip is in reset status.
XTALI	1	I	This pin is the oscillator input and the system master clock input pin. It is 384 or 256 times sampling clock rate from FSLR pin(pin 4). It must be synchronized with FSLR pin. For the crystal input, the XTALO pin(pin 20) must be tied to the other side. For the oscillator input, the pin is clock input source.
XTALO	20	O	This pin is the oscillator output. For the crystal input, the XTALI pin(pin 1) must be tied to the other side. For the oscillator input, the pin is floating and become the inverting XTALI clock.
CLKO	19	O	The pin is the buffered and inverting clock output from XTALI (pin 1).
FSLR	4	I	This pin is an frame sync pulse for the left and right channel. It enables the 16 or 18 Bit linear DINLR(pin 5) input by BCLK pin(pin 6). It is the sampling clcok, and its valus is 32K, 44.1K, or 48KHz, typically 44.1 KHz.
BCLK	6	I	This pin is the input bit clock. It shifts data on the DINLR pin into the chip on the rising edge.
DINLR	5	I	This pin is the 16 or 18 bit linear PCM input data for the left and right channel controlled by the FSLR and BCLK pins. There are two formats, normal input and I^2S input, in the device.
ZERO	7	O	This pin is the zero detection output pin. It is the open drain pin. When the zero input data is detected, the pin output logic zero; otherwise, it becomes the high impedance output pin.

4.3. Digital Interface, continued

PIN NAME	PIN NO.	I/O	FUNCTION
MODE	14	I	This pin is the mode selection input pin for the hardware and software mode. For the hardware mode, this pin must be logic zero input and the SSP_EN pin become the mute input; the SSPCLK pin and SSPDIN pin become the digital de-emphasis control input pin. For the software mode, this pin must be logic one input, and the SSP_EN, SSPCLK, SSPDIN become the serial setup control input pin to select 4 x 9 bit registers.
SSP_EN/MUTE	18	I	This pin is the enable signal for serial setup port(SSP) in the software mode. If the hardware mode is selected, the pin becomes the DAC mute input pin when it is the logic zero, the device is in the mute state; otherwise, it is in the normal operation.
SSPCLK/DE1	17	I	This pin is the clock input for serial setup port (SSP) in the software mode. If the hardware mode is selected, this pin and SSPDIN/DE0 (pin 16) control the selection from the different digital de-emphasis filter.
SSPDIN/DE0	16	I/O	This pin is the serial data input for serial setup port(SSP) in the software mode. If the hardware mode is selected, this pin and SSPCLK/DE1(pin 17) control the selection from the different digital de-emphasis filter. It is reserved for the output pin when it enters the test mode.

5. BLOCK DIAGRAM

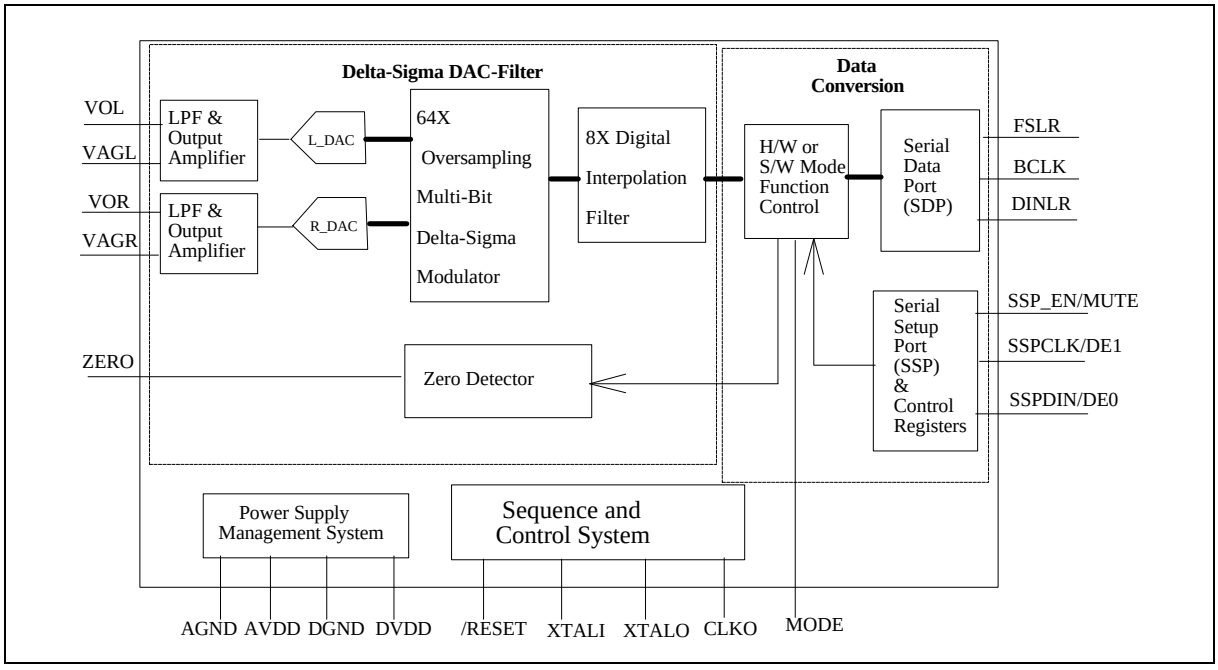


Figure 5. Winbond Stereo 16 or 18 Bit Audio DAC Block Diagram

6. FUNCTIONAL DESCRIPTIONS

Figure 5 illustrates the functional blocks of the Winbond's stereo 16 or 18 bit audio DAC .

6.1. Power Supply Management System

6.1.1. Power Supply for All Analog Signals Processing

All analog circuits are supplied with AVDD from +2.7 volt to 5.25 volt, typically +5 volt. In addition, the AVDD pin should be decoupled to AGND pin with a 0.1 μF capacitor.

6.1.2. Power Supply for All Digital Signals Processing

All digital circuits are supplied with DVDD from +2.7 volt to 5.25 volt, typically +5 volt. In addition, the DVDD pin should be decoupled to DGND pin with a 0.1 uF capacitor.

6.1.3. Analog Signal Ground Voltage Control System

The analog ground output for the left channel refers to VAGL pin, typically half of AVDD. Moreover the analog ground output for the right channel refers to VAGR pin, typically half of AVDD. These two pin should be connected to AGND pin with a 10 μF capacitor.

6.2. Delta-Sigma DAC-Filter

This device has built in stereo linear 16 or 18-bit D/A converter (DAC)- filter based on the delta-sigma technology. The linear input data from DINLR pin including the left and right channel are fed into the 8-times interpolation filter with -40 dB stop band attenuation and +- 0.15 dB ripple in the pass band, shown in Figure 6-1. Then the filtered data is quantized by 64-time oversampling multi-bit delta-sigma modulator whether the sampling rate is 256-times or 384-times sampling clock rate. The modulator is a 3rd-order noise shaper with multi-level amplitude quantizer. The structure is shown in Figure 6-2. And the quantization noise performance of the multi-level modulator is shown in Figure 6-3.The the quantized values are passed into the analog DAC for the left and right channel separtedly. Finally, the data are sented the analog low pass filter and output amplifer to generate the analog signal output at the VOL pin for the left channel , and at the VOR pin for the right channel.

6.3. Data Conversion

This block is the digital data conversion circuit. It consists of serial data port (SDP), serial setup port (SSP) with 4 x 9 registers, and mode function control block.

6.3.1. Serial Data Port (SDP)

This SDP block will convert the data input from DINLR pin into parallel data, separated into the left and right channel, depended on I^2S or normal data input format and 384-times or 256-times sampling clock rate. The timing diagram are shown in Figure 6-5 and 6-6. In the I^2S format, the data is compatible with Philips serial data protocol, the MSB bit is shifted into SDP block at the rising edge of second BCLK, and the following data bit are shifted into the SDP port at the following rising edge of sequence BCLK. Moreover when the FSLR is in low, the input data is corresponding to the left channel; and when the FSR is logic-1, the input data is corresponding to the right channel. For the normal format, the LSB bit is justified to the transition of FSLR pin, and the MSB bit is the first bit presented on the input data sequence. The data are latched into the SDP port same as the I^2S format at the rising edge of BCLK. But the left or right channel input location is reversed with I^2S format. In other word, the logic-one in the FSLR is the left channel data; and the logic-zero in the FSLR pin is the right channel data for the Normal data format. The FSLR pin is the sampling clcok rate. For this device, it should be 32K, 44.1K or 48 KHz input. All input data, whether is 16 or 18 bit, are 2's complement.

6.3.2. Serial Setup Port (SSP)

As for the SSP block, it is used to configure the 4 x 9 bits control registers in the software mode, or is used to setup some functions such as mute and de-emphasis in the hardware mode. The performance of digital de-emphasis filter is shown in Figure 6-4. It illustrates the de-emphasis frequence response and corresponding to the de-emphasis error for 32K, 44.1K, and 48 KHz. In this device, user can make advtantage of the MODE pin to select the software mode or the hardware mode. When the hardware mode is selected, the DINLR input data format is only choosed by the 16-bit normal data format. If more functions than one in the hardware mode must be generated by this chip, it must be setup control registers via SSP port whose timing shown in Figure 6-7. In the Figure 6-4, the first 5 bit are reserved bits (res) and must be logic-zero. Next 2 bits are address bits, A1 and A0 bit, to select the 4 control registers. For example, if A1 = 0 and A0 = 1, the second register will be configured. The final 9 bits, B8--B0, are data configuration bits. The setup of control registers refers to section 7, Control Registers. Many functions such as the 256 setp attenuation for the left and right channel, digital de-emphasis filter, zero detection, soft mute, input format selection, channel control, can be programmed by 4 x 9 registers in the software mode.

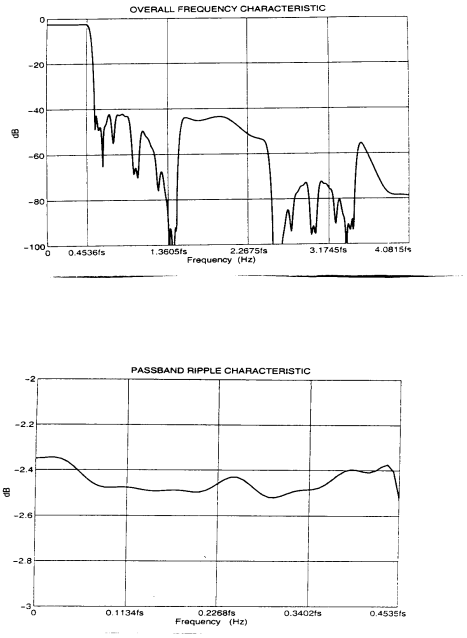


Figure 6-1 The Performance of Digital Filter

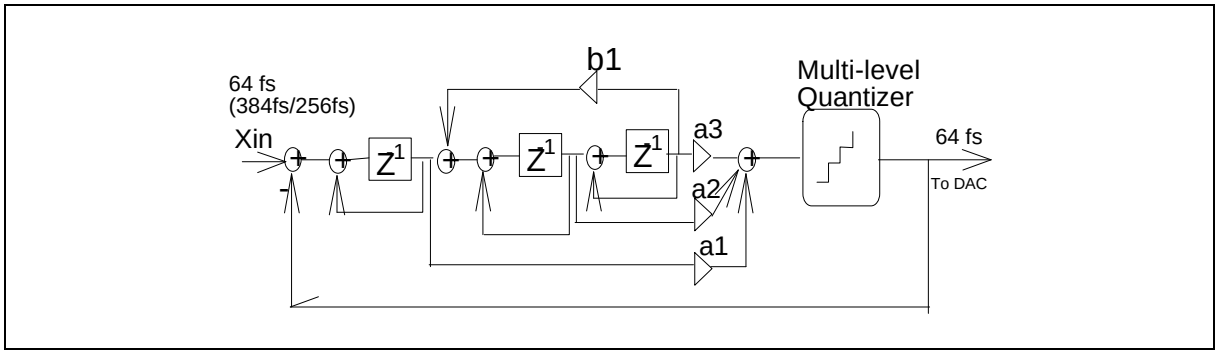


Figure 6-2 Function Block of 3rd-order Delta-Sigma DA Modulator

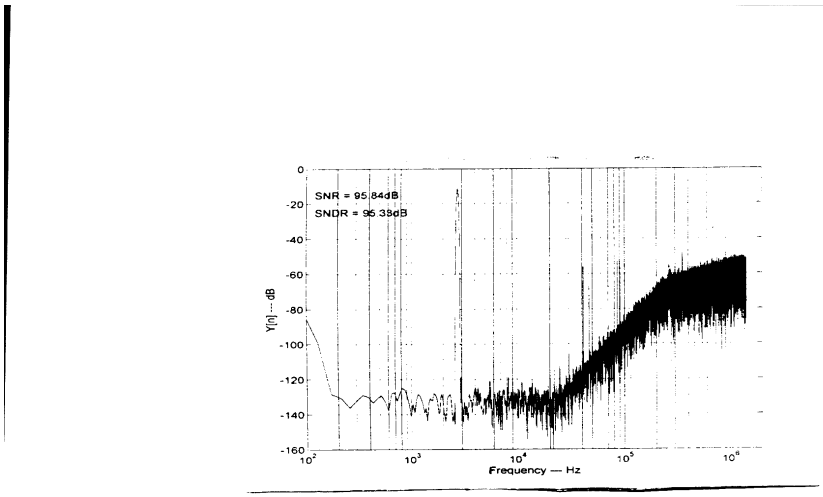


Figure 6-3 The Performance of 3rd Order Delta-Sigma DA Modulator

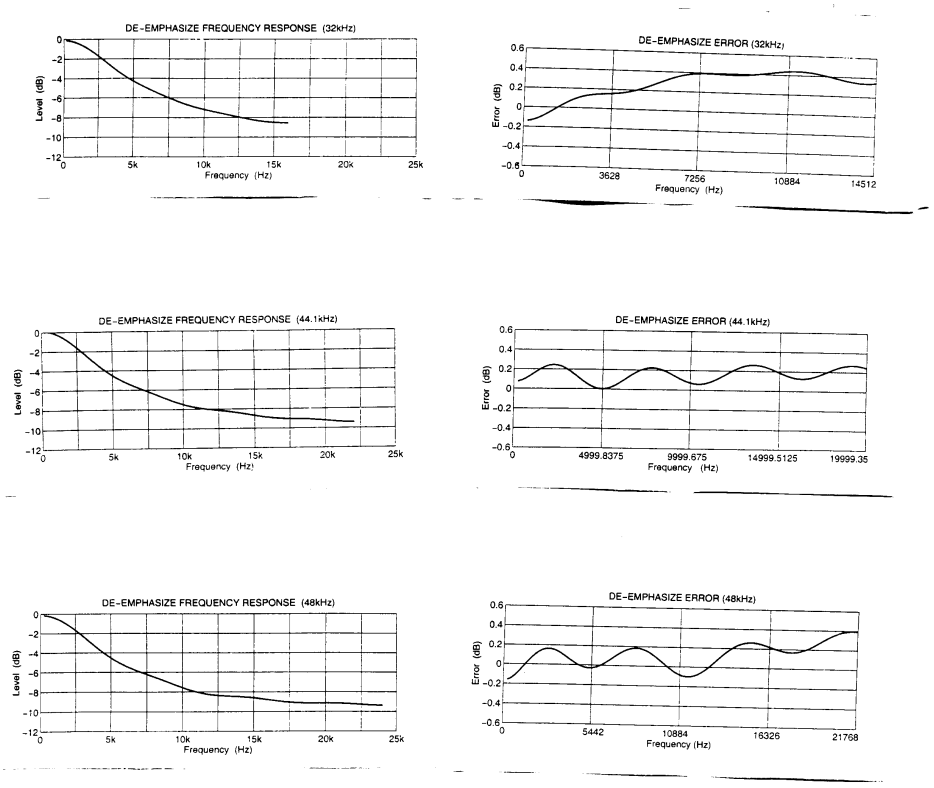


Figure 6-4 The Performance of Digital De-emphasis Filter

6.3.3. Mode Function Control

In the Mode Function Control block, the user can use MODE pin to select either hardware mode or software mode. If the MODE pin is logic-zero, the device enters the hardware mode. Meanwhile, the Pin 18 becomes mute pin; the pin 17 becomes DE1 pin for digital de-emphasis and the pin 16 becomes DE0 pin also for de-emphasis configuration. If the MODE pin actives logic-1, the device is in the software mode. Meanwhile, the pin 18 becomes SSP_EN pin as SSP enable signal; the pin 17 becomes the SSPCLK pin as SSP clcok ; and the pin 16 becomes the SSPDIN pin as SSP data input. These three pins in the software mode can configure the 4 x 9-bits control registers to obtain many differnt functions. Regarding to the configuration between the hardware and software mode, please refer to the section 7, Control and Status registers.

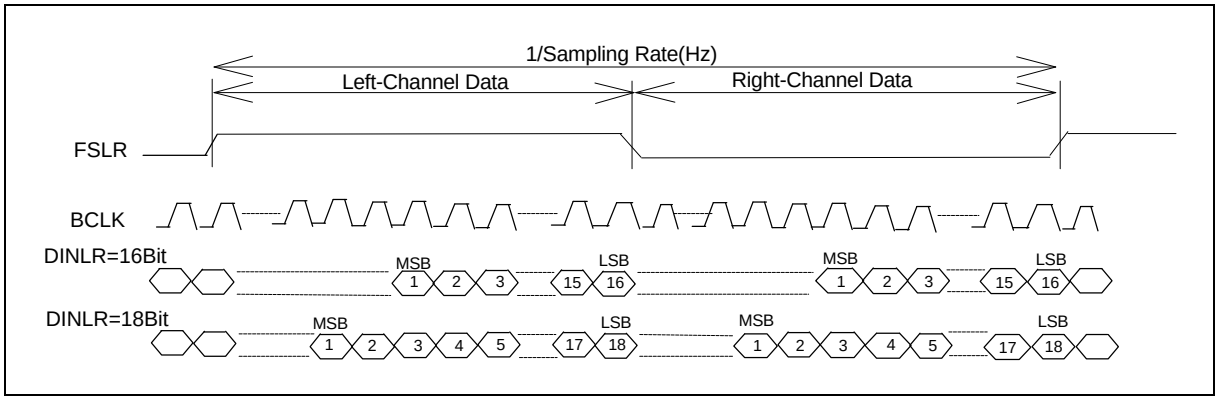


Figure 6-5 Normal Data Format Timing

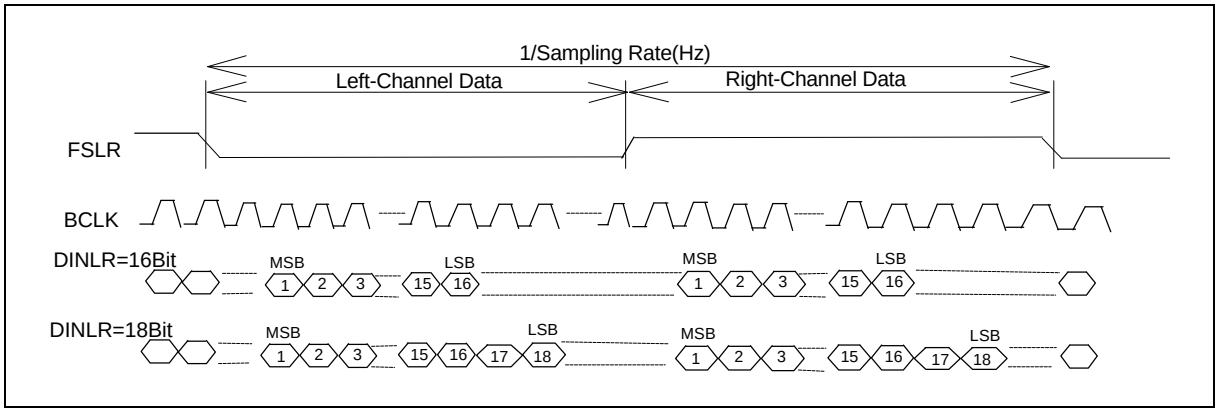


Figure 6-6. I^{2}S Data Format Timing

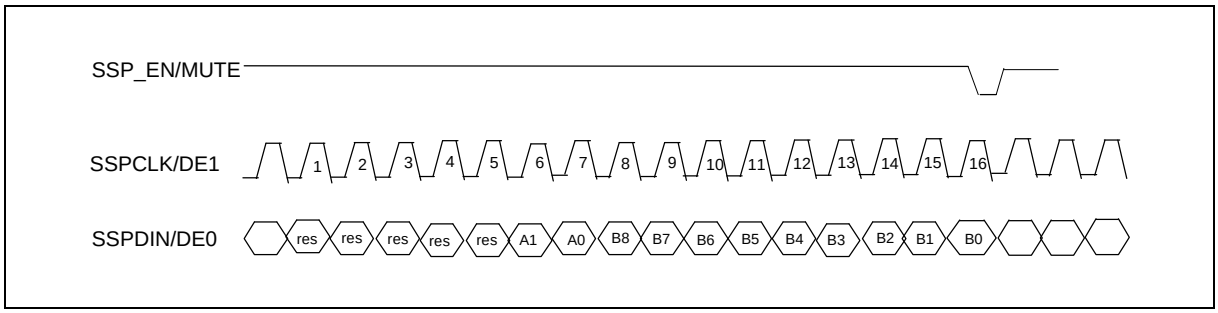


Figure 6-7 Serial Setup Port(SSP) Timing

6.4. Sequence and Control System

This block generates some internal clocks, providing clocks for interpolation filter and modulator operation. The master clock input pin XTALI(pin 1), which supports the clock of the digital circuit, may be asynchronous to all other blocks but synchronous to frame sync pulse FSLR (pin4), 32K, 44.1K or 48KHz. Its frequency should be either 256-times or 384-times sampling rate in FSLR pin.

The master clock can be either from the ocsillator input or crystal input. If the master clock is from the oscillator, the external clock must be inputted by XTALI pin and let XTALO pin open. If the master clock is from the crystal, both side of crystal must be tied between XTALI and XTALO pin and add two 10--20 pF capacitor to DGND at these pins. The XTALO output is inverting with XTALI clock. In addition, the CLKO pin is buffered and inverting with XTALI input clock.

This device can automatically detect the master clock input frequency by a prescaler circuit to decide the actual operation clock from 256-times or 384-times sampling clock. When the DAC is start-up initially such as power-on reset or power-up after hard reset, the steady DAC output will be delay by about 16 frame sync pulses when the attenuation will be recovered.

When the /RESET pin is held to logic 0, the device will go to initial state. Meanwhile, the DAC outputs, VOL and VOR, will enter half of AVDD level. Moreover the device is built-in power-on reset circuit in default. After the reset, the device will work well until the FSLR, sampling clock, is ready. But this cannot affect the configuration of control registers in the software mode.

7. CONTROL REGISTERS

7.1. Introduction

This device can be controlled either hardware mode or sofware mode by the MODE pin(pin 14). The differenent functions between the hardware and software mode are listed in Table 7-1, where CR is control register of the software mode. For example, CR3[0] is the bit 0 of control register 3.

If the pin 14, MODE pin, is low active, the device is selected by the hardware mode. It provides less functions than ones in the software mode. For hardware mode, only two functions are supported. One function is the soft mute for DAC output; the other one is the enable or disable the digital de-emphasis filter. In the hardware mode, the logic-0 presents at the pin18, SSP_EN/MUTE pin, will force both of DAC into the mute status, and both of DAC will output half of AVDD volts. As for the pin 17 (SSPCLK/DE1 pin) and pin16 (SSPDIN/DE0 pin), these two pins can configure the digital de-emphasis functions, shown in Table 7-2.

If the pin 14, MODE pin , is hold to logic-1, the device is in the software mode. In the meantime, the pin18, 17, and 16 become the SSP (Serial Setup Port) control signal. In other word, pin 18 become the enable signal of SSP; pin 17 becomes the serial latch clock of SSP; and pin 16 becomes the serial configuration data input of SSP. The control timing is illustrated in Figure 6-3. There are 4 available 16-Bit setup registers can be configured by the SSP port in the software mode. The functional description of each bit are illustrated in the sections that follow. All 4 registers must be in write status, not in read status.

FUNCTION	S/W SELECTION	S/W DEFAULT	H/W SELECTION	H/W DEFAULT
Din Input Format	I^2S, Normal (CR3[0])	Normal	Normal Only	Normal
Din Input Resolution	16, 18 Bits (CR3[2])	16 Bits	16 Bits Only	16 Bits
Frame Pulse (FSLR) Polarity	L/R = H/L, L/R = L/H (CR3[1])	L/R = H/L	L/R = H/L Only	L/R = H/L

Continued

FUNCTION	S/W SELECTION	S/W DEFAULT	H/W SELECTION	H/W DEFAULT
De-emphasis Control	32K, 44.1K, 48K, and Off (CR2[2:1])	Off	32K, 44.1K, 48K, and Off (Pin17, Pin 16)	Off
L/R Attenuation Control	8 Bits attenuation for L/R Channel (L:CR0[7:0]) (R:CR1[7:0])	0 dB	Not Support	0 dB
Mute Control	Yes (CR2[0])	Off	Yes	Off
Zero Detection	Yes (CR2[4])	Off	Not Support	Off
Channel Ouput Type Control	Yes (CR3[7:4])	L_chan = L R_chan = R	Not Support	L_chan = L R_chan = R

Table 7-1. The Comparison between the Software Mode and Hardware Mode

PIN 17(DE1)	PIN 16(DE0)	FUNCTION
0	0	Disable the digital de-emphasis filter
0	1	Enable the digital de-emphasis filter at 48 KHz
1	0	Enable the digital de-emphasis filter at 44.1 KHz
1	1	Enable the digital de-emphasis filter at 32 KHz

Table 7-2 Digital De-emphasis Filter Configuration in Hardware Mode

7.2. Control Registers in Software Mode

There are 4x9-bit registers for controlling the chip in the software mode. These registers are labeled CR0 to CR3. The descriptions are as follows. Note that "setting" is corresponding to logic "1" and "clearing" is corresponding to logic "0". In addition, the res bit indicates the reserved bit and must be logic-0. Because the first 5 bits are res bit and the data must be logic-0; the next 2 bits are address bits, A1 and A0 to select control register shown in Table 7-3; the final 9 bits are the actual configured data input bits. The following control register only show how to control the configured data bits. In other word, the control register only show Bit[9:0]. The detail timing is shown in the Figure 6-3.

A1	A0	CONTROL REGISTER SELECTION
0	0	Select Control register 0 (CR0)
0	1	Select Control register 1 (CR1)
1	0	Select Control register 2 (CR2)
1	1	Select Control register 3 (CR3)

Table 7-3 Control Register Selection

The map of control registers for the software mode is shown in Table 7-4.

CONTROL REGISTER	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR0	Latch L-channel Attenuation	AttL[7]	AttL[6]	AttL[5]	AttL[4]	AttL[3]	AttL[2]	AttL[1]	AttL[0]
CR1	Latch R-channel Attenuation	AttR[7]	AttR[6]	AttR[5]	AttR[4]	AttR[3]	AttR[2]	AttR[1]	AttR[0]
CR2	Reserved	Reserved	Reserved	Reserved	ZD (Zero Detection)	AG (Analog Ground Control)	DE[1] (De-emphasis)	DE[0] (De-emphasis)	Mute
CR3	Reserved	OTY[3] (DAC Output Type)	OTY[2] (DAC Output Type)	OTY[1] (DAC Output Type)	OTY[0] (DAC Output Type)	AttC (Atten. Control)	WS (Word Length Select)	LRP (L_chan & R_chan Polarity)	DinF (Din Input Format)

Table 7-4 4 x 9-bit Control Registers Map in Software Mode

7.2.1. Control Register 0 (CR0)

This is a 256-step attenuation control register for the left channel. The CR0 register is configured as 0FF in hexdecimal format when the /RESET pin is set to logic zero or power-on reset in default.

	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR0	LatchL	AttL[7]	AttL[6]	AttL[5]	AttL[4]	AttL[3]	AttL[2]	AttL[1]	AttL[0]

LatchL (B8):

This bit controls the attenuation latch for the left channel. If this bit set to logic 1, the device will load the attenuation value in AttL[7:0] to the device. Otherwise, if this bit is cleared, the AttL[7:0] value will not affect the attenuation for the left channel.

AttL[7:0] (B[7:0]):

These 8 bits are used to configure the attenuation value for the left channel. The formula of attenuation level is as follows.

$$AttL = 20 * \log (x/256)\ dB \text{ where } x = AttL[7:0], \text{ when } 0 \le AttL[7:0] \le 254$$

$$x = 256, \text{ when } AttL[7:0] = 255 .$$

When the bit 8, LatchL, is logic-1, the AttL[7:0] value will be loaded into this device and result in the attenuation in the left channel.

7.2.2. Control Register 1 (CR1)

This is a 256-step attenuation control register for the right channel. The CR1 register is configured as 0FF in hexdecimal format when the $\overline{\text{RESET}}$ pin is set to logic zero or power-on reset in default.

	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR1	LatchR	AttR[7]	AttR[6]	AttR[5]	AttR[4]	AttR[3]	AttR[2]	AttR[1]	AttR[0]

LatchR (B8):

This bit controls the attenuation latch for the right channel. If this bit set to logic 1, the device will load the attenuation value in AttR[7:0] to the device. Otherwise, if this bit is cleared, the AttR[7:0] value will not affect the attenuation for the right channel.

AttR[7:0] (B[7:0]):

These 8 bits are used to configure the attenuation value for the right channel. The formula of attenuation level is as follows.

$$AttR = 20 * \log (x/256)\ dB \text{ where } x = AttR[7:0], \text{ when } 0 \le AttR[7:0] \le 254$$
$$x = 256, \text{ when } AttR[7:0] = 255 .$$

When the bit 8, LatchR, is logic-1, the AttR[7:0] value will be loaded into this device and result in the attenuation in the right channel.

7.2.3. Control Register 2 (CR2)

This register controls the zero detection, soft mute and de-emphasis filter. The CR2 register becomes the 000 in hexdecimal format when the $\overline{\text{RESET}}$ pin is set to logic zero or power-on reset in default.

	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR2	Res	Res	Res	Res	ZD	AG	DE[1]	DE[0]	MUTE

Res[8:5] (B[8:5]):

These 4 bits are reserved bits. They should be logic-zero in the setup.

ZD (B4):

This bit control the zero detection status. When this bit is set to logic-1, if the linear data input from DINLR pin are zero code, this device will force both of DAC to half of AVDD level, i.e., delta-sigma is disconnected from output amplifier. When this bit is cleared, if the linear data input from DINLR pin are zero code, this device is general zero output from both of DAC, i.e., delta-sigma is connected to output amplifier. As for the other input data except for zero code, whether ZD is logic-0 or not, the DAC output will become normal output.

AG(B3):

This bit controls the level of analog ground for DAC. When this bit is set to logic-1, no matter what the linear data input from DINLR pin are, this device will force both of DAC to half of AVDD level, I. e., delta-sigma is disconnected from output amplifier. When this bit is cleared, if the linear data input from DINLR pin are zero code, this device is controlled by ZD bit (Bit 4).

DE[1:0](B[2:1]):

These two bits can be used to configure the digital de-emphasis filter as shown in Table 7-5.

DE[1]	DE[0]	FUNCTION
0	0	Disable the digital de-emphasis filter
0	1	Enable the digital de-emphasis filter at 48 KHz
1	0	Enable the digital de-emphasis filter at 44.1 KHz
1	1	Enable the digital de-emphasis filter at 32 KHz

Table 7-5 Digital De-emphasis Filter Configuration in Software Mode

Mute(B0):

This bit is used to control both of DAC to be soft muted. When this bit is set to logic-1, the both of DAC will be muted.

7.2.4. Control Register 3 (CR3)

This register is used to control the input data format or output type in both of DAC. The CR3 register becomes the 090 in hexdecimal format when the /RESET pin is set to logic zero or power-on reset in default.

	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Res	OTY[3]	OTY[2]	OTY[1]	OTY[0]	AttC	WS	LRP	DinF

Res (B8):

This bit is reserved bit. It should be logic-zero in the setup.

OTY[3:0](B[7:4]):

These four bits can be used to decide the output type in both of channel as shown in Table 7-6 in the following.

OTY[3]	OTY[2]	OTY[1]	OTY[0]	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
0	0	0	0	Mute	Mute
0	0	0	1	L_chan output	Mute
0	0	1	0	R_chan output	Mute
0	0	1	1	(L_chan + R_chan)/2 output	Mute
0	1	0	0	Mute	L_chan output
0	1	0	1	L_chan output	L_chan output
0	1	1	0	R_chan output	L_chan output
0	1	1	1	(L_chan + R_chan)/2 output	L_chan output
1	0	0	0	Mute	R_chan output
1	0	0	1	L_chan output	R_chan output
1	0	1	0	R_chan output	R_chan output
1	0	1	1	(L_chan + R_chan)/2 output	R_chan output
1	1	0	0	Mute	(L_chan + R_chan)/2 output
1	1	0	1	L_chan output	(L_chan + R_chan)/2 output
1	1	1	0	R_chan output	(L_chan + R_chan)/2 output
1	1	1	1	(L_chan + R_chan)/2 output	(L_chan + R_chan)/2 output

Table 7-6 The Output Type Selection by OTY[3:0] in Control Register CR3

AttC(B3):

This bit is used as the attenuation control bit. When this bit is set to logic-1, the attenuation for both of channel will be controlled by control register 0(CR0) and ignore the value in control register 1(CR1). If this bit is cleared, the attenuation is in normal operation. In other word, the control register 0(CR0) controls the attenuation in left channel; and the control register 1(CR1) controls the attenuation in the right channel.

WS(B2):

This bit is the input word length selection. When this bit is set to logic-1, the linear input data from DINLR(pin5) selects 18 Bit format. If the bit is cleared, the one will selects the 16-bit data format

LRP(B1):

This bit is used to control the polarity of sampling clock(FSLR pin). Note this bit only affects the normal data format and is ignored by I^2S data format. When this bit is set to logic-1, the left channel corresponds to the low state in FSLR pin and the right channel is located at the high state in FSLR pin. When the bit is cleared, the polarity of FSLR pin is reversed.

DinF(B0):

This bit is used to control the input data format from the normal or I^2S format. When this bit is set to logic-1, the input data format is the I^2S format. Otherwise it will become the normal data input.

8. ELECTRICAL CHARACTERISTICS

8.1. Absolute Maximum Ratings

(Voltage Referenced to DGND and AGND pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	AVDD, DVDD	-0.3 to +6.5	V
Analog V_{DD} to Digital V_{DD} Difference	AVDD–DVDD	±0.1	V
Analog Output Voltage	---	-0.3 to AVDD +0.3	V
Digital Input/Output Voltage	---	-0.3 to DVDD +0.3	V
Operating Temperature	T_{OP}	-25 to +85	°C
Storage Temperature	T_{STG}	-85 to +85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2. DC Characteristics

(AGND = DGND = 0 volt; TOP = -25 to +85° C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	AVDD, DVDD	----	2.7	5.0	5.25	V
Operating Current	Iop	AVDD = DVDD = +5 V, XTALI = 16.934 MHz	---	--	50	mA
Input High Voltage	V_{IH1}	All digital input pins except for ssp_en, sspclk, mode, reset	2.0	---	-----	V

8.2. DC Characteristics, continued

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL1}	All digital input pins except for ssp_en, sspclk, mode, reset	---	----	0.8	V
Input High Voltage	V_{IH2}	ssp_en, sspclk, mode, reset pin	2.6	---	-----	V
Input Low Voltage	V_{IL2}	ssp_en, sspclk, mode, reset pin	---	----	1.3	V
Output High Voltage	V_{OH}	CLKO	2.4	----	---	V
Output Low Voltage	V_{OL}	CLKO	---	---	0.4	V
Input High Current	I_{IL}	DGND≤ Vin ≤ DVDD	---	---	+40	µA
Input Low Current	I_{IH}	DGND≤ Vin ≤ DVDD	---	---	- 40	µA

8.3. Stereo Channel Output Performance

(AVDD = DVDD = +5V, AGND = DGND = 0 volt , Top = 25° C; FSLR = 44.1 KHz; XTALI = 384 x FSLR = 16.9344 MHz synchronous with FSLR; Linear 16 bit input data in DINLR; Measurement bandwidth is 20 KHz, Unless otherwise noted)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Signal to Noise Ratio at 5 Volt	SNR5	Fin = 1031Hz, A-weighted, AVDD = DVDD =+5 V	92	100	---	dB
Signal to Noise Ratio at 3 Volt	SNR3	Fin = 1031Hz, A-weighted, AVDD = DVDD =+3 V	---	91	---	dB
Dynamic Range at 5 Volt	DR5	Fin = 1031 Hz, A-weighted, AVDD = DVDD =+5 V	90	96	---	dB
Dynamic Range at 3 Volt	DR3	Fin = 1031 Hz, A-weighted, AVDD = DVDD = +3 V	---	91	---	dB
THD+N at 5 Volt @ 0 dB	THDN50	Fin = 1031 Hz @ 0dB; AVDD = DVDD=+5 V	---	-90	-80	dB
THD+N at 3 Volt @ 0 dB	THDN30	Fin = 1031 Hz @ 0dB; AVDD = DVDD =+3 V	---	-86	---	dB
THD+N at 5 Volt @ -60 dB	THDN56	Fin = 1031 Hz @ -60 dB; AVDD = DVDD =+5 V	---	-34	---	dB
Cross Talk	CTX	Fin = 1031 Hz @ 0dB; AVDD = DVDD =+5 V; L --> R & R --> L	---	-97	-90	dB
Level Non-linearity Error @ 0 dB, -60 dB	GNLE	Fin = 1031 Hz; AVDD = DVDD = +5 V	---	±0.5	---	dB
Digital De-emphasis Error	DEE	FSLR = 32K, 44.1K, 48 KHz	-0.2	---	+0.55	dB

8.4. Analog Electrical Characteristics

(AVDD = DVDD = +5V, AGND = DGND = 0 volt , Top = 25° C; Unless otherwise noted)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Load Resistance for VOL, VOR	RLDS	VOL, VOR	5	---	--	KW
Analog Output Range for VOL, VOR	AORS	VOL, VOR @ 0 dB	---	0.62 x AVDD	---	Vpp
Stereo Analog Ground Output Voltage for VAGL, VAGR	VAGS	to AGND	--	0.5 x AVDD	--	V
Gain Error	GES	VOL, VOR	--	±1	±5	%FSR
Bipolar Zero Error	ZDE	---	---	±30	---	mV

8.5. Digital Switching Characteristics

8.5.1 Stereo Input Data Timing

(DVDD = AVDD = 5 ±5%V; AGND = DGNDD = 0V; all digital circuits referenced to DGND; Top = +25° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset Pulse Width	TRPW	$\overline{\text{RESET}}$	20	---	---	nS
Master Clock Frequency at 384 x FSLR	TMC3	XTALI, XTALO	12.288	16.9344	18.432	MHz
Master Clock Frequency at 256 x FSLR	TMC2	XTALI, XTALO	8.192	11.2896	12.288	MHz
Frame Sync. Frequency for Stereo	TFS	FSLR	32	44.1	48	KHz
Clock Duty Cycle	TDC	XTALI, XTALO	30	50	70	%
Bit Clock Frequency	TBC	BCLK	---	---	10	MHz
Bit Clock Pulse Width at LOW or HIGH	TBCW	BCLK	50	---	--	nS
Receive Sync. Timing	TRE TER	BCLK Rising --> FSLR Edge FSLR Edge --> BCLK Rising	30 30	--- ---	--- ---	nS
Setup Time for DINLR Valid	TSTD	Refer to BCLK rising	30	---	---	nS
Hold Time for DINLR Valid	THTD	Refer to BCLK rising	30	---	---	nS

Note: these parameters are shown in Figure 8-1, 8-2 and 8-3

Figure 8-1 Reset Timing

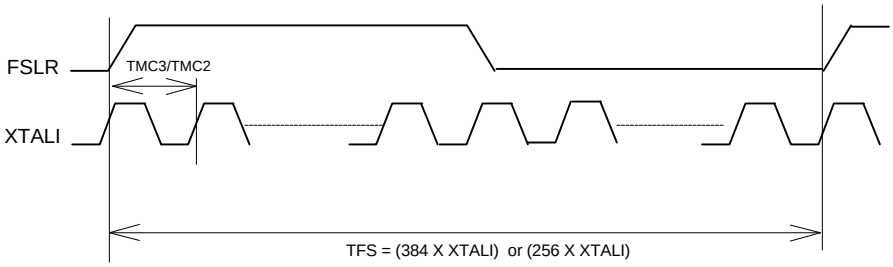


Figure 8-2 The Timing Between Sampling Clock (FSLR) and Master Clock (XTALI)

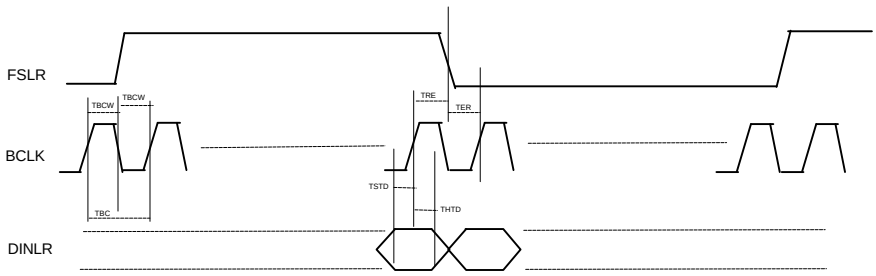


Figure 8-3 Data Input Timing

7.5.2. Serial Setup Port (SSP) Timing

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SSP Clock Frequency	T_{SPC}	SSPCLK	---	--	10	MHz
SSP Clock Pulse Width at High or LOW	T_{SPCW}	SSPCLK	50	---	---	nS

7.5.2. Serial Setup Port (SSP) Timing, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SSP Latch Timing	TSPRF	SSPCLK Rising --> SSP_EN Falling Edge	30	---	---	nS
	TSPFR	SSP_EN Falling --> SSPCLK Rsiing	30	---	---	
SSP Latch Pulse Width	TLPW	SSP_EN	30	--	---	nS
SSP Hold High after Latch	TLPH	SSP_EN	30	---	---	nS
SSPDIN Setup Time	TSST	Refer to SSPCLK rising	30	---	---	nS
SSPDIN Hold Time	TSHT	Refer to SSPCLK rising	30	---	---	nS

(DVDD = AVDD = 5 ±5% V; AGND = DGNDD = 0V; all digital circuits referenced to DGND; Top = +25° C)

Note: these parameters are shown in Figure 8-4

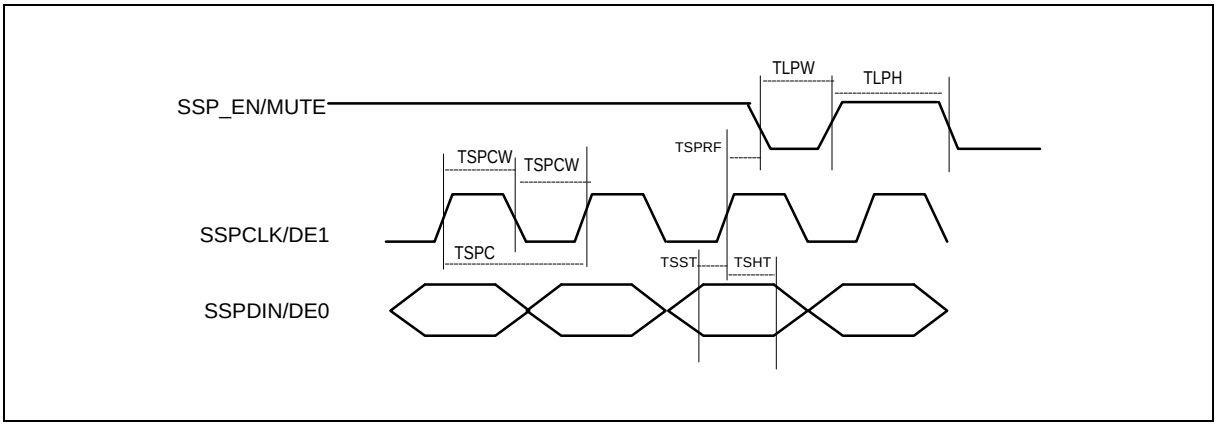


Figure 8-4 Serial Setup Port (SSP) Timing

9. APPLICATION INFORMATION

This device has two power supply. One is the digital power (DVDD); the other is the analog power (AVDD). The positive value is supplied from 2.7 to 5.25 volt. If this device is used as two power supply, the user had better add two diodes between the AVDD and DVDD pin as shown in Figure 9-1 in order to avoid occurring the latch-up condition. The latch-up circuit can be ignored if the two power supply are connected in common area.

The application circuit is referred to Figure 9-1 as follows. It uses the crystral as the master clock input. Therfore, the XTALO pin must be tied. If the oscillator input is used, the XTALO pin is opened, and is inputted to XTALI pin. The audio data input source can be either from digital output of CD player via digital audio interface or user design system. If user selects the software mode, the configuration value may be from the micro-processor via the serial setup port (SSP). As for the ZERO pin, it is the open-drain output pin. User must add a pull-up resistor about 1KΩ to ZERO pin .

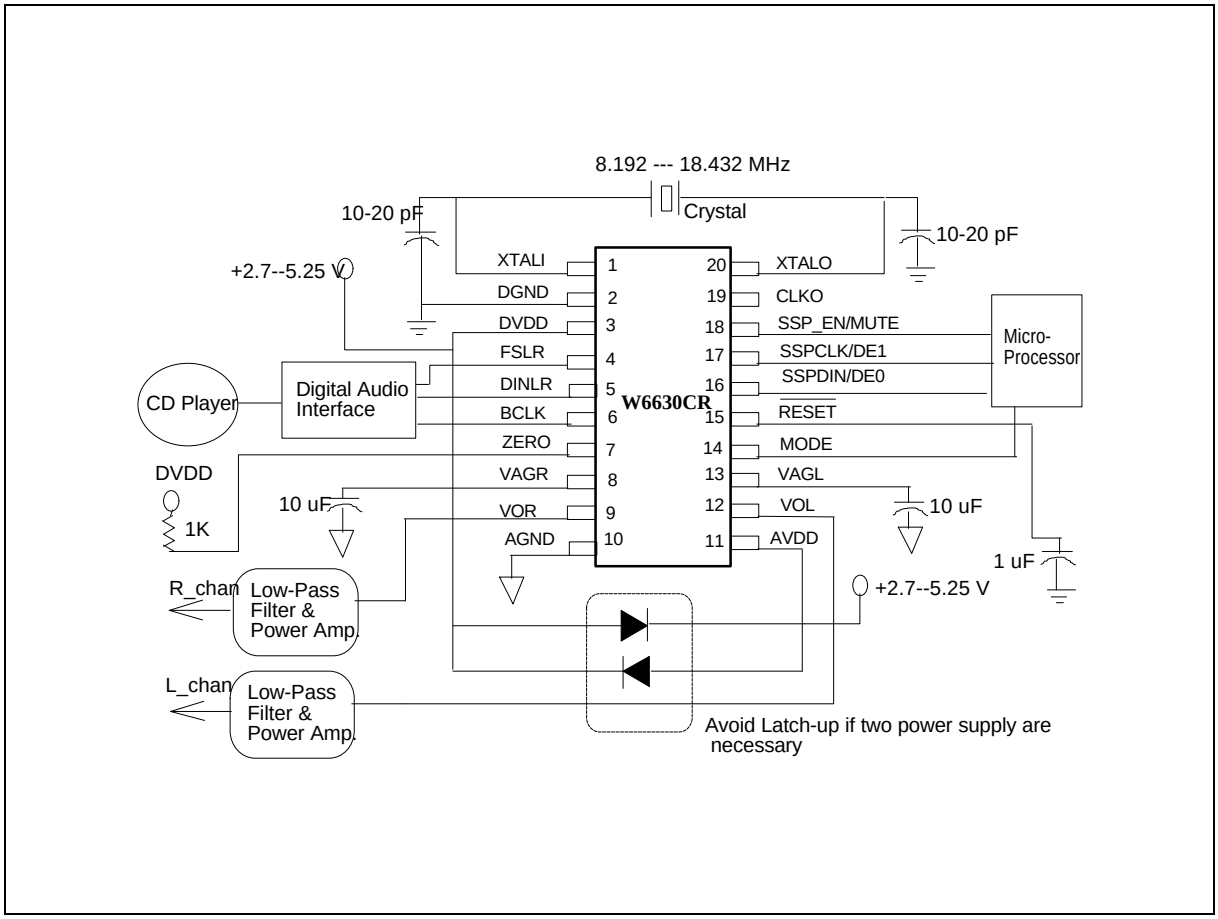
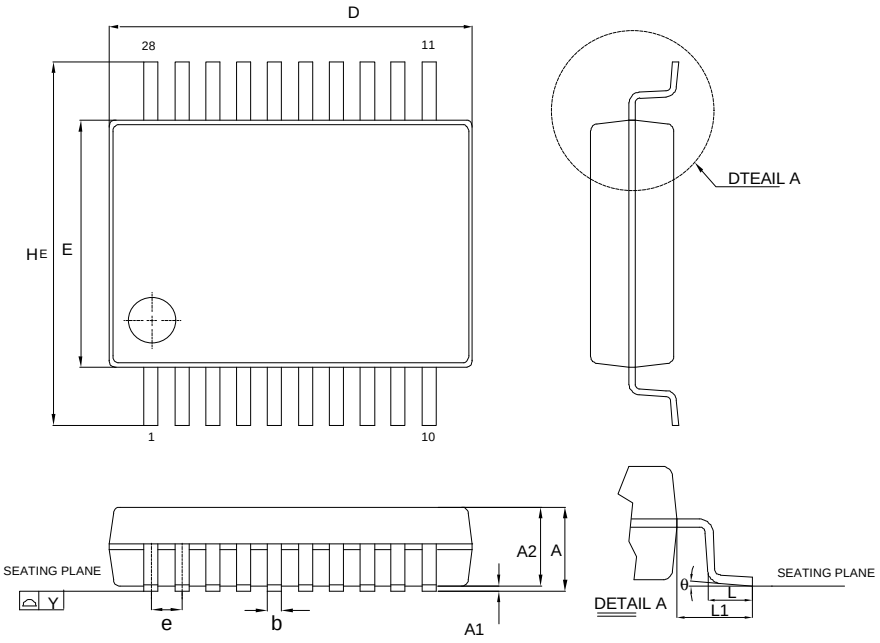


Figure 9-1 Application Circuit for Digital Input Data from the CD-Play

In addition, the stereo channel outputs optionally select low-pass filter and power amplifier to achieve the self-design requirement.

10. PACKAGE DIMENSIONS

(20-pin SSOP)



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.271	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
HE	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792646
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-27197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798