

**TOSHIBA**

TOSHIBA Original CMOS 16-Bit Microcontroller

**TLCS-900** Series

TMP96CM40

**TOSHIBA CORPORATION**

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs.  
Before use this LSI, refer the section, "Points of Note and Restrictions".  
Especially, take care below cautions.

## **\*\*CAUTION\*\***

### How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ( $\overline{\text{NMI}}$ , INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

## CMOS 16-bit Microcontrollers

## TMP96CM40F

## 1. Outline and Device Characteristics

TMP96CM40F is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C141BF does not have a ROM, the TMP96CM40F has a built-in ROM of 32K-byte, and the TMP96PM40 has a built-in OTP of 32K-byte.

TMP96CM40F is housed in an 80-pin flat package.

Device characteristics are as follows:

- (1) Original 16-bit CPU
  - TLCS-90 instruction mnemonic upward compatible.
  - 16M-byte linear address space
  - General-purpose registers and register bank system
  - 16-bit multiplication / division and bit transfer/arithmetic instructions
  - High-speed micro DMA : 4 channels (1.6  $\mu$ s/2 bytes @ 20 MHz)
- (2) Minimum instruction execution time : 200 ns @ 20 MHz
- (3) Internal RAM : 1 Kbyte  
Internal ROM : 32 Kbyte
- (4) External memory expansion
  - Can be expanded up to 16 Mbytes (for both programs and data).
  - Can mix 8- and 16-bit external data buses.
- (5) 8-bit timers : 2 channels
- (6) 8-bit PWM timers : 2 channels
- (7) 16-bit timers : 2 channels
- (8) Pattern generators : 4 bits, 2 channels
- (9) Serial interface : 2 channels
- (10) 10-bit A/D converter : 4 channels
- (11) Watchdog timer
- (12) Chip select/wait controller : 3 blocks
- (13) Interrupt functions
  - 3 CPU interrupts ... SWI instruction, privileged violation, and Illegal instruction
  - 14 internal interrupts
  - 6 external interrupts  7-level priority can be set.
- (14) I/O ports : 65 pins
- (15) Standby function : 3 halt modes (RUN, IDLE, STOP)

000707EBP1

- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.  
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

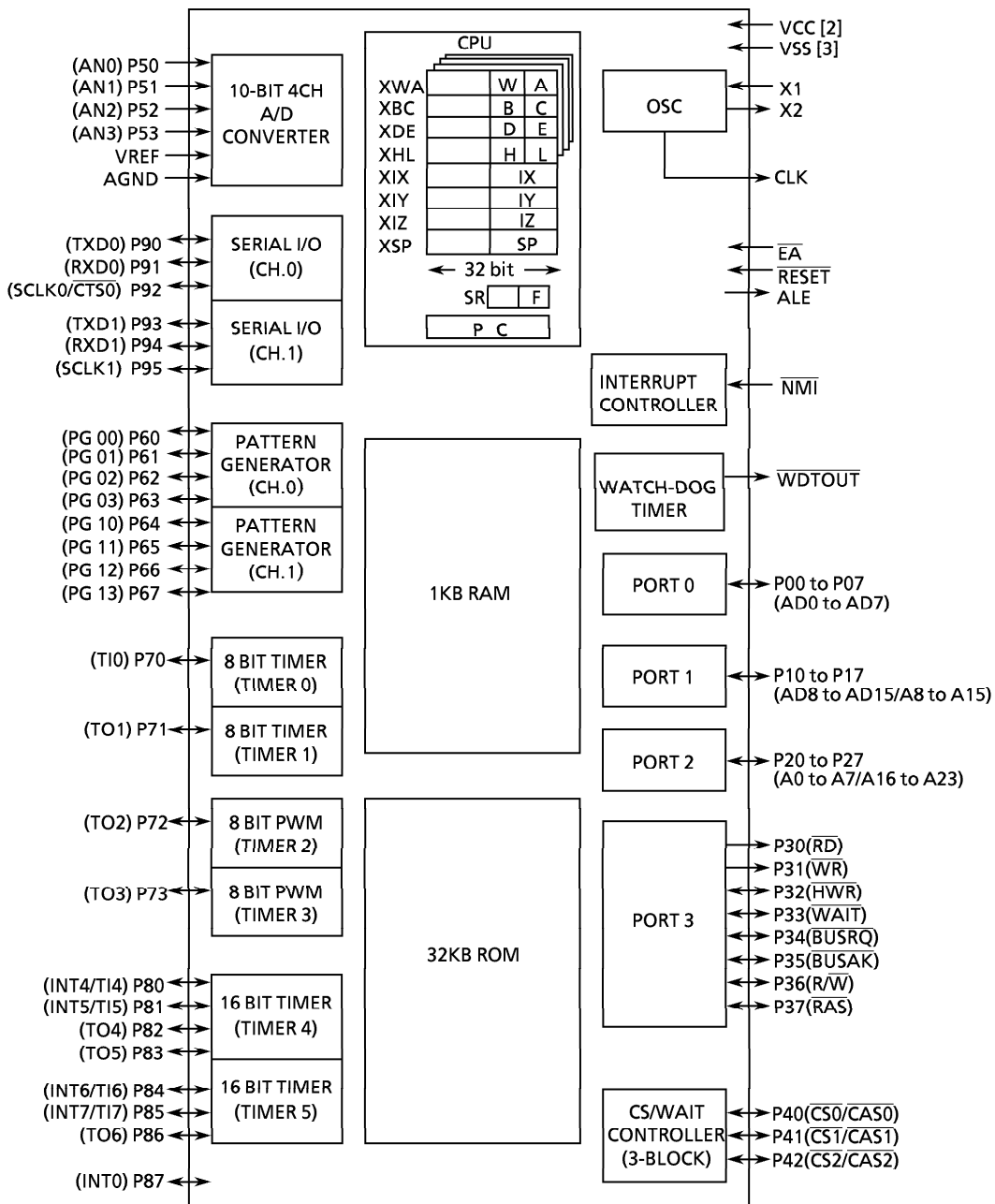


Figure1 TMP96CM40 Block Diagram

## 2. Pin Assignment and Functions

The assignment of input / output pins for TMP96CM40, their name and outline functions are described below.

### 2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96CM40F.

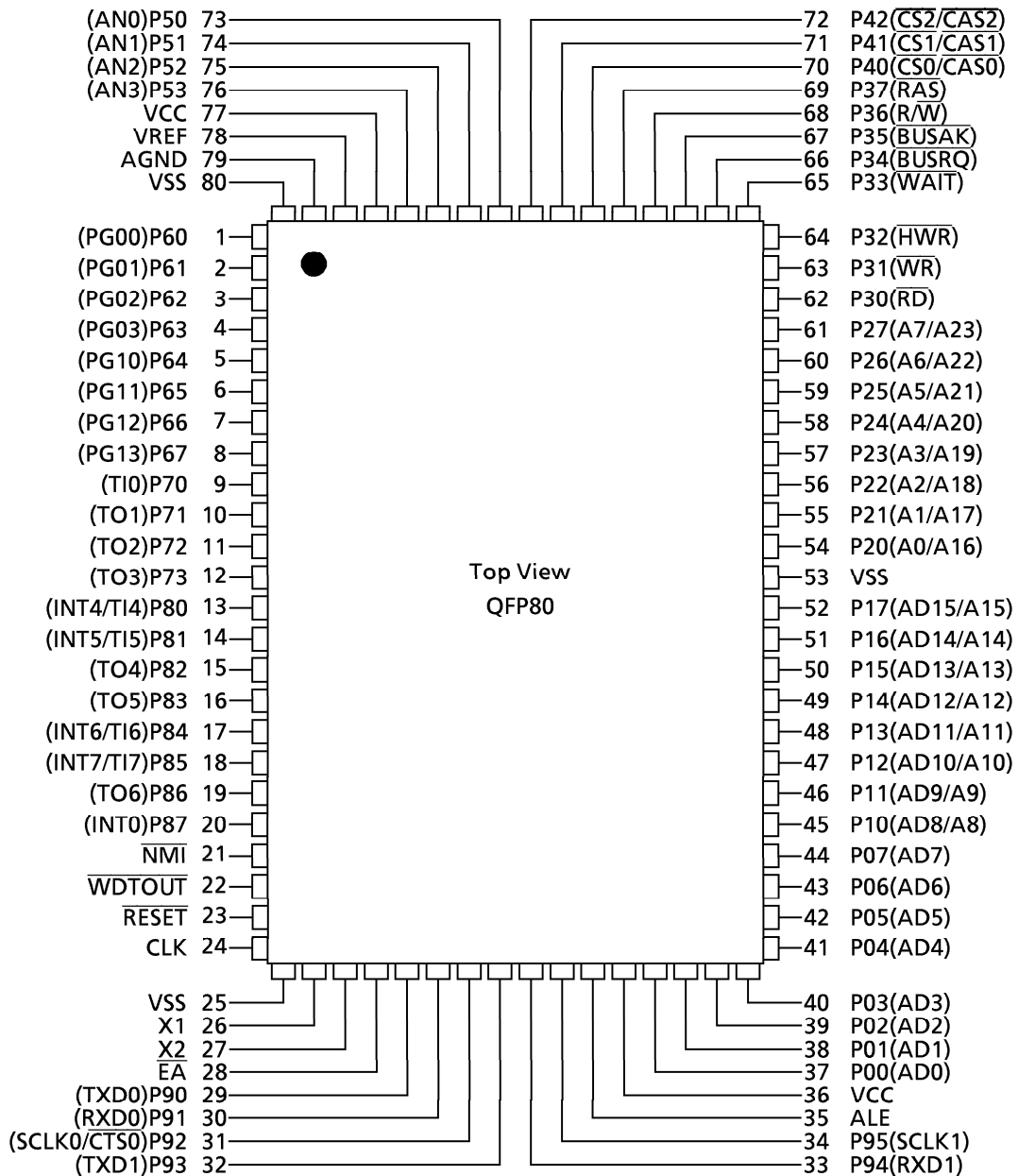


Figure 2.1 Pin Assignment (80-pin QFP)

## 2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address/data (lower): 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins are at high impedance after receiving $\overline{BUSRQ}$ . (For external DMAC)
P36 $\overline{R/W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the  $\overline{BUSRQ}$  and  $\overline{BUSAK}$  pins.

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) (Note) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P53 AN0 to AN3	4	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREF	1	Input	Pin for reference voltage input to A/D converter
AGND	1	Input	Ground pin for A/D converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Note : Case of the settable  $\overline{CS2}$  or  $\overline{CAS2}$  ; when TMP96CM40F is bus release, this pin is not added the internal pull-down resistor but is added the internal pull-up resistor.

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{\text{CTS0}}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
$\overline{\text{WDTOU}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs $\lceil X1 \div 4 \rceil$ clock. Pulled-up during reset.
$\overline{\text{EA}}$	1	Input	External access: 0 should be inputted with TMP96C141B. 1, with TMP96CM40 / TMP96PM40.
ALE	1	Output	Address latch enable
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	Oscillator connecting pin
VCC	2		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up/pull-down resistor can be released from the pin by software (except the  $\overline{\text{RESET}}$  pin).



### 3. Operation

This section describes the functions and basic operations of TMP96M40 device. The function of CPU and internal I/O devices are the same function as TMP96C141B.

Check the 「7. Care Points and Restriction of TMP96C141B」 because of the Care described. Regarding the function of TMP96CM40 (not described), see the part of TMP96C141B.

TMP96C141B/TMP96CM40/TMP96PM40 have much the same function but they are different from following points.

Parameter	TMP96C141B	TMP96CM40	TMP96PM40
Internal ROM	Not exist	Mask ROM32 Kbyte	PROM32 Kbyte
P00 to P07, AD0 to AD7	Only AD0 to AD7	After reset P00 to P07	
P10 to P17, AD8 to AD15, A8 to A15	Only AD8 to AD15	After reset P10 to P17	
P30, $\overline{RD}$	Only $\overline{RD}$	After reset P30	
P31, $\overline{WR}$	Only $\overline{WR}$	After reset P31	
Pin state at the bus release	TMP96C141B see Table 3.5 (1)	TMP96CM40 see Table 3.3 (1)	

#### 3.1 CPU

TMP96CM40 device has a built-in high-performance 16-bit CPU (900-CPU). (For CPU operation, see TLCS-900 CPU in the previous section.)

#### 3.2 Memory Map

TMP96CM40 has two register modes. One is a minimum mode; in this mode, the area of program memory is 64 Kbytes maximum. The other is a maximum mode; in this mode, The area of program memory is 16 Mbytes maximum.

Both minimum and maximum modes are the data memory area of 16 Mbytes maximum.

That is, the program memory can locate 0H to FFFFH in minimum mode and can locate 0H to FFFFFFFH in maximum mode.

##### (1) Internal ROM

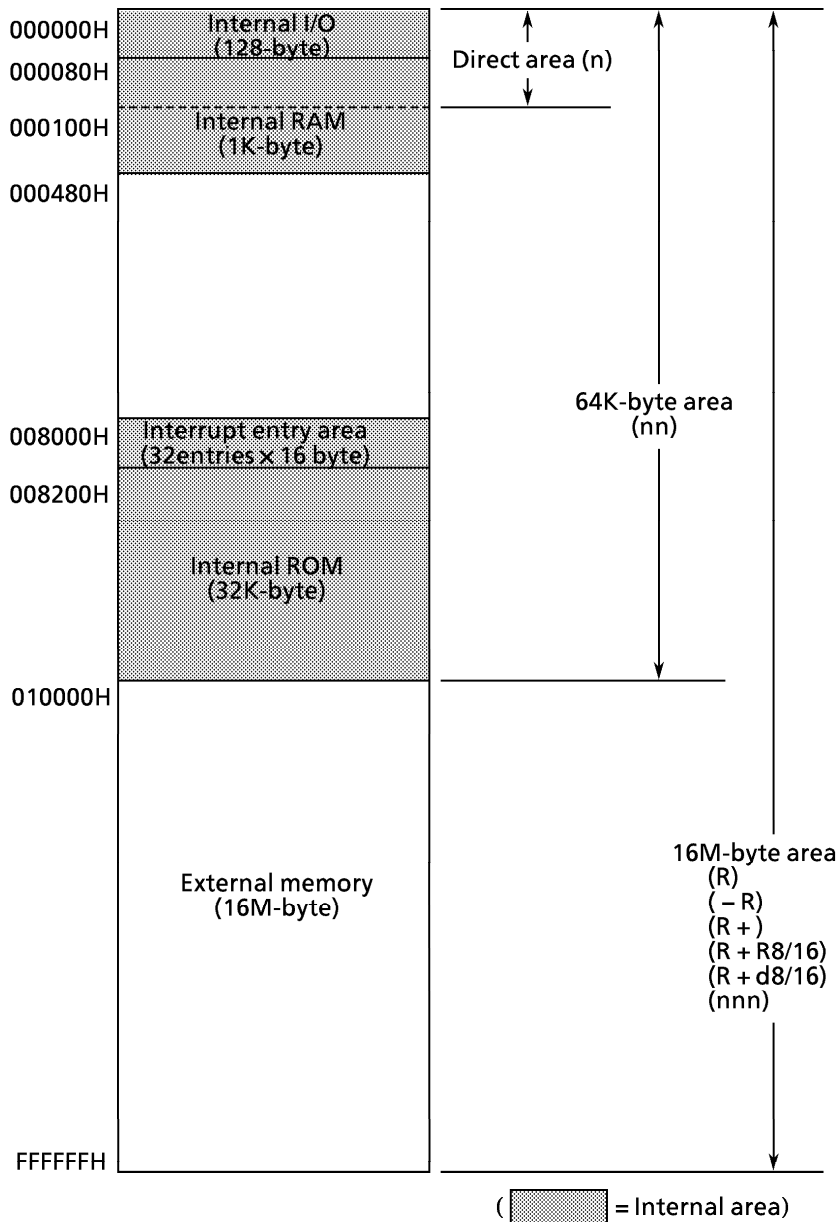
TMP96CM40 has the ROM of 32 Kbytes. This ROM is located to 8000H to FFFFH. After the RESET operation, instruction execution starts from address 8000H. A part of the internal ROM area (8000H to 81FFH) is interrupt entry area.

(2) Internal RAM

TMP96CM40 has the RAM of 1 Kbytes. This RAM is located to 80H to 47FH. The CPU can access the part of RAM (80H to FFH, 128 bytes) with using the short instruction code of direct addressing mode.

Memory Map

Figure 3.1 is a memory map of the TMP96CM40.



Note: The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.1 Memory map

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings (TMP96CM40)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>CC</sub>	- 0.5 to 6.5	V
Input Voltage	V <sub>IN</sub>	- 0.5 to V <sub>CC</sub> + 0.5	V
Output Current (total)	∑ I <sub>OL</sub>	100	mA
Output Current (total)	∑ I <sub>OH</sub>	- 100	mA
Power Dissipation (T <sub>a</sub> = 85°C)	P <sub>D</sub>	500	mW
Soldering Temperature (10 s)	T <sub>SOLDER</sub>	260	°C
Storage Temperature	T <sub>STG</sub>	- 65 to 150	°C
Operating Temperature	T <sub>OPR</sub>	- 40 to 85	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (TMP96CM40)

 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20\text{ to }70^\circ\text{C}$  (4 to 20 MHz)
(Typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$ )

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15)	V <sub>IL</sub>		-0.3	0.8	V
P2, P3, P4, P5, P6, P7, P8, P9	V <sub>IL1</sub>		-0.3	0.3 V <sub>CC</sub>	V
RESET, NMI, INT0 (P87)	V <sub>IL2</sub>		-0.3	0.25 V <sub>CC</sub>	V
EA	V <sub>IL3</sub>		-0.3	0.3	V
X1	V <sub>IL4</sub>		-0.3	0.2 V <sub>CC</sub>	V
Input High Voltage (AD0 - 15)	V <sub>IH</sub>		2.2	V <sub>CC</sub> + 0.3	V
P2, P3, P4, P5, P6, P7, P8, P9	V <sub>IH1</sub>		0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
RESET, NMI, INT0 (P87)	V <sub>IH2</sub>		0.75 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
EA	V <sub>IH3</sub>		V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V
X1	V <sub>IH4</sub>		0.8 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 $\mu$ A	2.4		V
	V <sub>OH1</sub>	I <sub>OH</sub> = -100 $\mu$ A	0.75 V <sub>CC</sub>		V
	V <sub>OH2</sub>	I <sub>OH</sub> = -20 $\mu$ A	0.9 V <sub>CC</sub>		V
Darlington Drive Current (8 Output Pins max.)	I <sub>DAR</sub>	V <sub>EXT</sub> = 1.5 V R <sub>EXT</sub> = 1.1 k $\Omega$	-1.0	-3.5	mA
Input Leakage Current	I <sub>LI</sub>	0.0 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub>	0.02 (Typ)	$\pm$ 5	$\mu$ A
Output Leakage Current	I <sub>LO</sub>	0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.05 (Typ)	$\pm$ 10	$\mu$ A
Operating Current (RUN)	I <sub>CC</sub>	f <sub>c</sub> = 20 MHz	30 (Typ)	TBD	mA
IDLE			2.0 (Typ)	10	mA
STOP (T <sub>a</sub> = -40 to 85 $^\circ$ C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.2 (Typ)	50	$\mu$ A
STOP (T <sub>a</sub> = 0 to 50 $^\circ$ C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2		10	$\mu$ A
Power Down Voltage (@ STOP, RAM Back up)	V <sub>STOP</sub>	V <sub>IL2</sub> = 0.2 V <sub>CC</sub> , V <sub>IH2</sub> = 0.8 V <sub>CC</sub>	2.0	6.0	V
RESET Pull Up Resistor	R <sub>RST</sub>		50	150	k $\Omega$
Pin Capacitance	C <sub>IO</sub>	f <sub>c</sub> = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P87)	V <sub>TH</sub>		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R <sub>KL</sub>		10	80	k $\Omega$
Programmable Pull Up Resistor	R <sub>KH</sub>		50	150	k $\Omega$

Note : I-DAR is guaranteed for a total of up to 8 ports.

## 4.3 AC Electrical Characteristics (TMP96CM40)

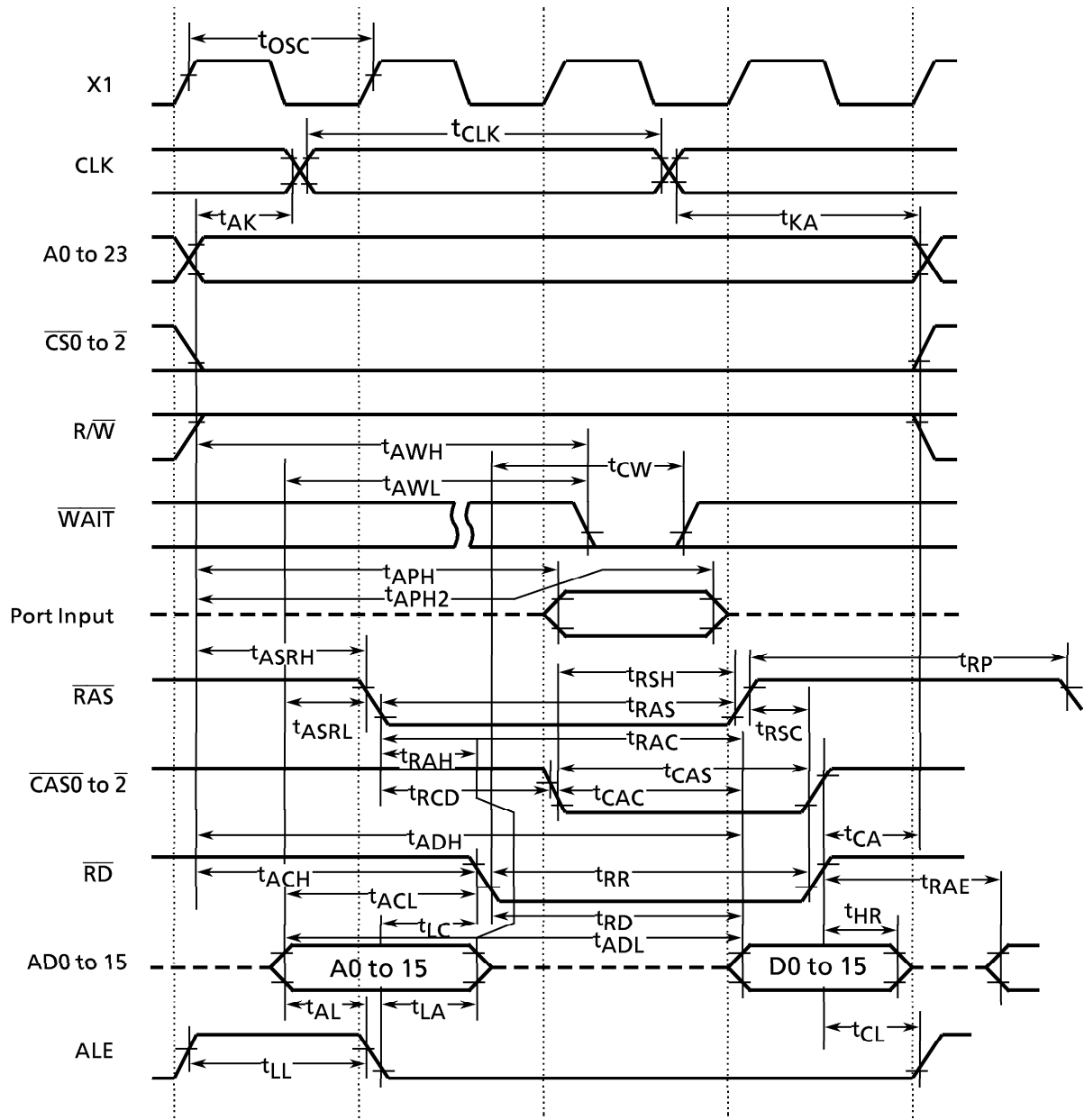
 $V_{cc} = 5\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20\text{ to }70^\circ\text{C}$  (4 to 20 MHz)

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	$t_{OSC}$	50	250	62.5		50		ns
2	CLK width	$t_{CLK}$	$2x - 40$		85		60		ns
3	A0 to 23 Valid $\rightarrow$ CLK Hold	$t_{AK}$	$0.5x - 20$		11		5		ns
4	CLK Valid $\rightarrow$ A0 to 23 Hold	$t_{KA}$	$1.5x - 70$		24		5		ns
5	A0 to 15 Valid $\rightarrow$ ALE fall	$t_{AL}$	$0.5x - 15$		16		10		ns
6	ALE fall $\rightarrow$ A0 to 15 Hold	$t_{LA}$	$0.5x - 15$		16		10		ns
7	ALE High width	$t_{LL}$	$x - 40$		23		10		ns
8	ALE fall $\rightarrow$ RD/WR fall	$t_{LC}$	$0.5x - 30$		1		-5		ns
9	RD/WR rise $\rightarrow$ ALE rise	$t_{CL}$	$0.5x - 20$		11		5		ns
10	A0 to 15 Valid $\rightarrow$ RD/WR fall	$t_{ACL}$	$x - 25$		38		25		ns
11	A0 to 23 Valid $\rightarrow$ RD/WR fall	$t_{ACH}$	$1.5x - 50$		44		25		ns
12	RD/WR rise $\rightarrow$ A0 to 23 Hold	$t_{CA}$	$0.5x - 20$		11		5		ns
13	A0 to 15 Valid $\rightarrow$ D0 to 15 input	$t_{ADL}$		$3.0x - 45$		143		105	ns
14	A0 to 23 Valid $\rightarrow$ D0 to 15 input	$t_{ADH}$		$3.5x - 65$		154		110	ns
15	RDfall $\rightarrow$ D0 to 15 input	$t_{RD}$		$2.0x - 50$		75		50	ns
16	RD Low width	$t_{RR}$	$2.0x - 40$		85		60		ns
17	RDrise $\rightarrow$ D0 to 15 Hold	$t_{HR}$	0		0		0		ns
18	RDrise $\rightarrow$ A0 to 15output	$t_{RAE}$	$x - 15$		48		35		ns
19	WR Low width	$t_{WW}$	$2.0x - 40$		85		60		ns
20	D0 to 15 Valid $\rightarrow$ WR rise	$t_{DW}$	$2.0x - 50$		75		50		ns
21	WR rise $\rightarrow$ D0 to 15 Hold	$t_{WD}$	$0.5x - 10$		21		15		ns
22	A0 to 23 Valid $\rightarrow$ WAIT input <sup>(1WAIT + n mode)</sup>	$t_{AEH}$		$3.5x - 90$		129		85	ns
23	A0 to 15 Valid $\rightarrow$ WAIT input <sup>(1WAIT + n mode)</sup>	$t_{AWL}$		$3.0x - 80$		108		70	ns
24	RD/WR fall $\rightarrow$ WAIT Hold <sup>(1WAIT + n mode)</sup>	$t_{CW}$	$2.0x + 0$		125		100		ns
25	A0 to 23 Valid $\rightarrow$ PORT input	$t_{APH}$		$2.5x - 120$		36		5	ns
26	A0 to 23 Valid $\rightarrow$ PORT Hold	$t_{APH2}$	$2.5x + 50$		206		175		ns
27	WR rise $\rightarrow$ PORT Valid	$t_{CP}$		200		200		200	ns
28	A0 to 23 Valid $\rightarrow$ RAS fall	$t_{ASRH}$	$1.0x - 40$		23		10		ns
29	A0 to 15 Valid $\rightarrow$ RAS fall	$t_{ASRL}$	$0.5x - 15$		16		10		ns
30	RAS fall $\rightarrow$ D0 to 15 input	$t_{RAC}$		$2.5x - 70$		86		55	ns
31	RAS fall $\rightarrow$ A0 to 15 Hold	$t_{RAH}$	$0.5x - 15$		16		10		ns
32	RAS Low width	$t_{RAS}$	$2.0x - 40$		85		60		ns
33	RAS High width	$t_{RP}$	$2.0x - 40$		85		60		ns
34	CAS fall $\rightarrow$ RAS rise	$t_{RSH}$	$1.0x - 35$		28		15		ns
35	RAS rise $\rightarrow$ CAS rise	$t_{RSC}$	$0.5x - 25$		6		0		ns
36	RAS fall $\rightarrow$ CAS fall	$t_{RCD}$	$1.0x - 40$		23		10		ns
37	CAS fall $\rightarrow$ D0 to 15 input	$t_{CAC}$		$1.5x - 65$		29		10	ns
38	CAS Low width	$t_{CAS}$	$1.5x - 30$		64		40		ns

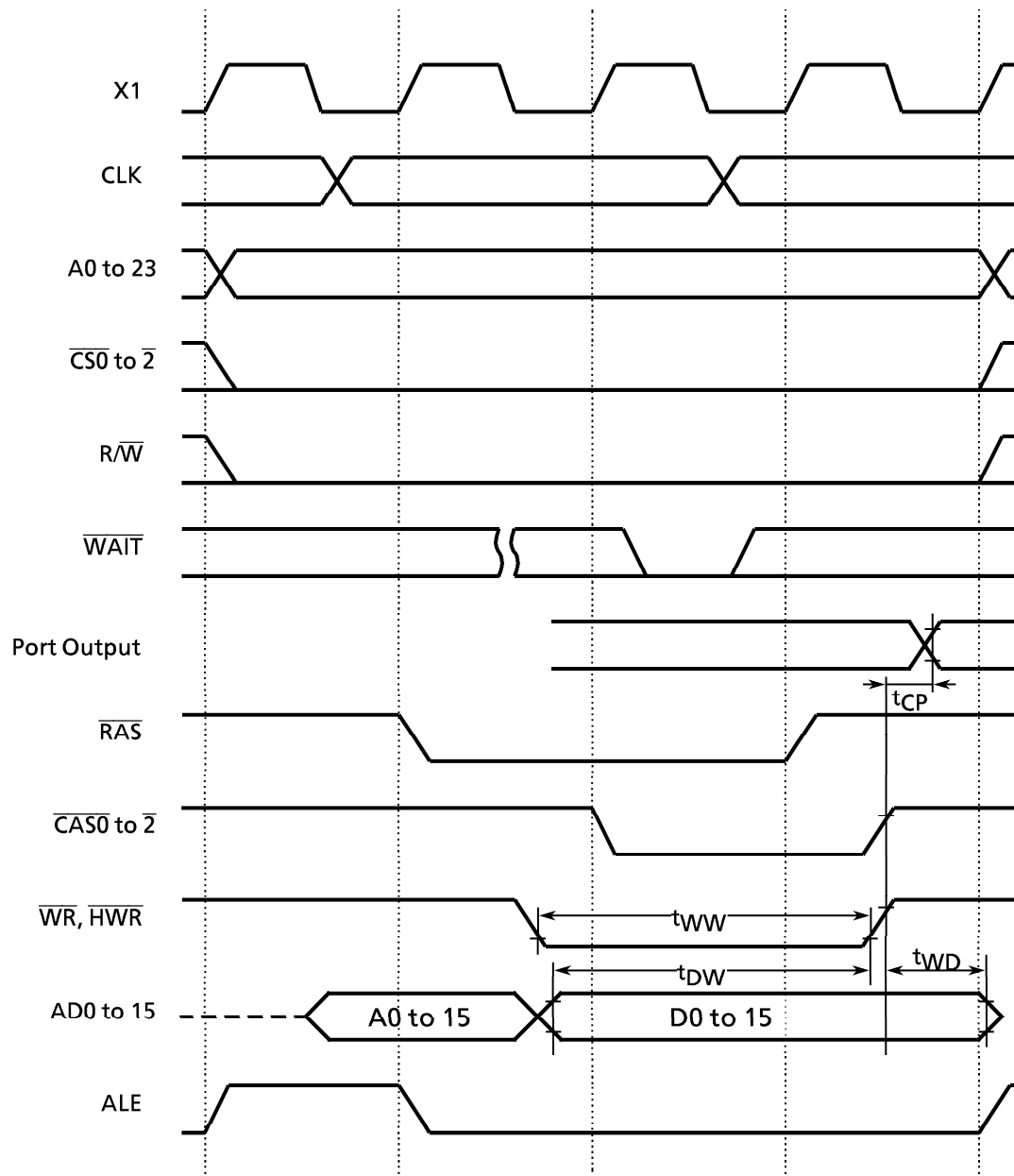
## AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL50 pF  
(However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, R/W, CLK, RAS, CAS0 to CAS2)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)  
High 0.8 Vcc / Low 0.2 Vcc (Except for AD0 to AD15)

(1) Read Cycle



(2) Write Cycle



## 4.4 A/D Conversion Characteristics (TMP96CM40)

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage		$V_{REF}$	$V_{CC} - 1.5$		$V_{CC}$	V
Analog reference voltage		$A_{GND}$	$V_{SS}$		$V_{SS}$	
Analog input voltage range		$V_{AIN}$	$V_{SS}$		$V_{CC}$	
Analog current for analog reference voltage		$I_{REF}$		0.5	1.5	mA
$4 \leq f_c \leq 16$ MHz	Low change mode	Total error (Quantize error of $\pm 0.5$ LSB not included)		$\pm 1.5$	$\pm 4.0$	LSB
	High change mode			$\pm 3.0$	$\pm 6.0$	
$16 < f_c \leq 20$ MHz	Low change mode			$\pm 1.5$	$\pm 4.0$	
	High change mode			$\pm 4.0$	$\pm 8.0$	

## 4.5 Serial Channel Timing – I/O Interface Mode

## (1) SCLK Input Mode

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	$t_{SCY}$	16X		1		0.8		$\mu\text{s}$
Output Data → Rising edge of SCLK	$t_{OSS}$	$t_{SCY}/2 - 5X - 50$		137		100		ns
SCLK rising edge → Output Data hold	$t_{OHS}$	$5X - 100$		212		150		ns
SCLK rising edge → Input Data hold	$t_{HSR}$	0		0		0		ns
SCLK rising edge → effective data input	$t_{SRD}$		$t_{SCY} - 5X - 100$		587		450	ns

## (2) SCLK Output Mode

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	$t_{SCY}$	16X	8192X	1	512	0.8	409.6	$\mu\text{s}$
Output Data → SCLK rising edge	$t_{OSS}$	$t_{SCY} - 2X - 150$		725		550		ns
SCLK rising edge → Output Data hold	$t_{OHS}$	$2X - 80$		45		20		ns
SCLK rising edge → Input Data hold	$t_{HSR}$	0		0		0		ns
SCLK rising edge → effective data input	$t_{SRD}$		$t_{SCY} - 2X - 150$		725		550	ns

## 4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	$t_{VCK}$	$8X + 100$		600		500		ns
Low level clock Pulse width	$t_{VCKL}$	$4X + 40$		290		240		ns
High level clock Pulse width	$t_{VCKH}$	$4X + 40$		290		240		ns

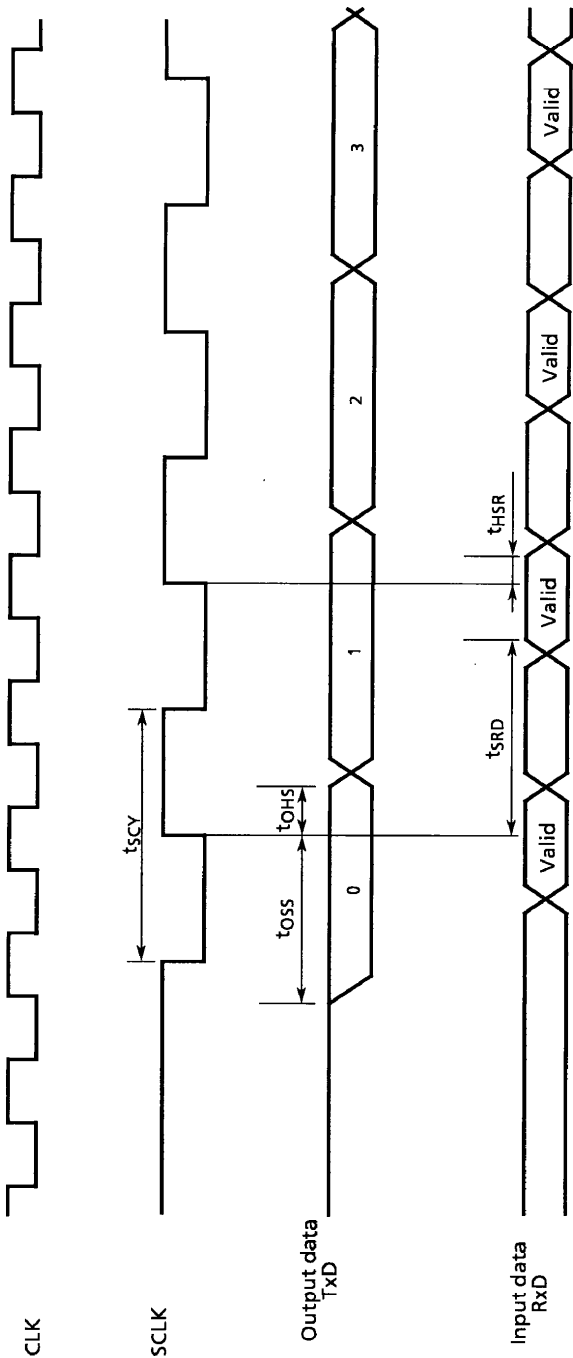
## 4.7 Interrupt Operation

 $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$  (4 to 16 MHz)  $T_A = -20$  to  $70^\circ\text{C}$  (4 to 20 MHz)

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$ , INT0 Low level Pulse width	$t_{INTAL}$	4X		250		200		ns
$\overline{NMI}$ , INT0 High level Pulse width	$t_{INTAH}$	4X		250		200		ns
INT4 to INT7 Low level Pulse width	$t_{INTBL}$	$8X + 100$		600		500		ns
INT4 to INT7 High level Pulse width	$t_{INTBH}$	$8X + 100$		600		500		ns

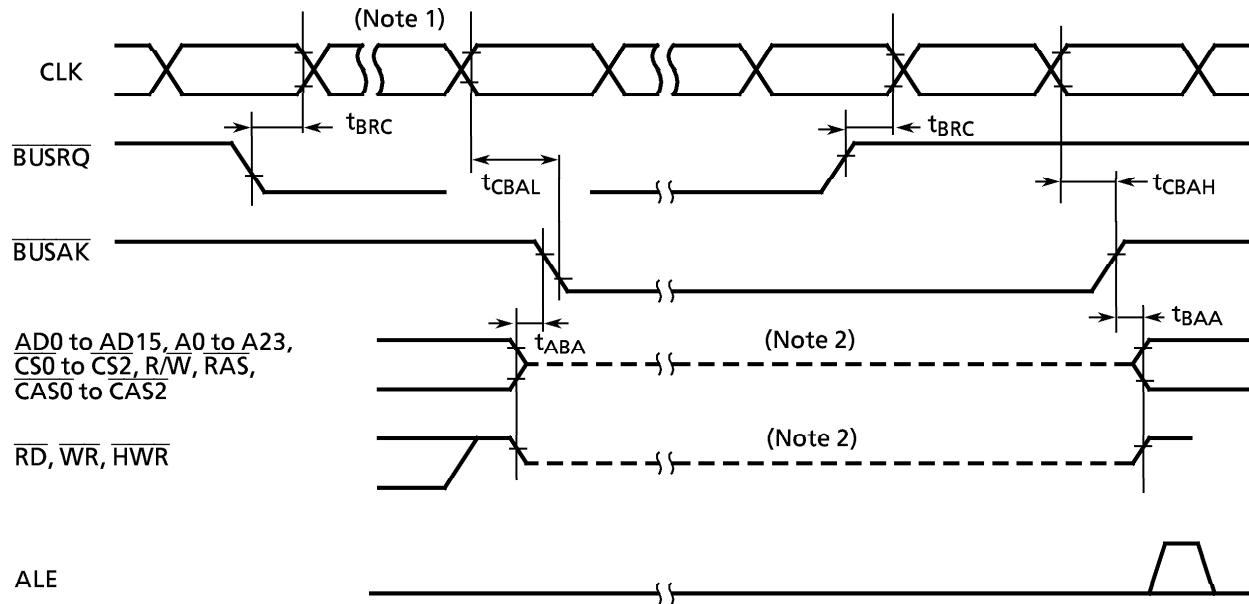


4.8 Timing Chart for I/O Interface Mode



180289

4.9 Timing Chart for Bus Request ( $\overline{\text{BUSRQ}}$ ) / Bus Acknowledge ( $\overline{\text{BUSAK}}$ )



Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$t_{BRC}$	$\overline{\text{BUSRQ}}$ set-up time for CLK	120		120		120		ns
$t_{CBAL}$	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ falling edge		$1.5x + 120$		214		195	ns
$t_{CBAH}$	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ rising edge		$0.5x + 40$		71		65	ns
$t_{ABA}$	Output Buffer is off to $\overline{\text{BUSAK}}$ $\downarrow$	0	80	0	80	0	80	ns
$t_{BAA}$	$\overline{\text{BUSAK}}$ $\uparrow$ to Output Buffer is on.	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the  $\overline{\text{WAIT}}$  request is inactive, when the  $\overline{\text{BUSRQ}}$  is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state. They don't indicate the signal level is fixed. After the bus is released, the signal level is kept dynamically before the bus is released by the external capacitance. Therefore, to fix the signal level by an external resistance under the bus is releasing, the design must be carefully because of the level-fix will be delayed. The internal programmable pull-up/pull-down resistance is switched active/non-active by the internal signal.

4.10 Typical characteristics

$V_{CC}=5\text{ V}$ ,  $T_a=25\text{ }^\circ\text{C}$  unless other wise noted.

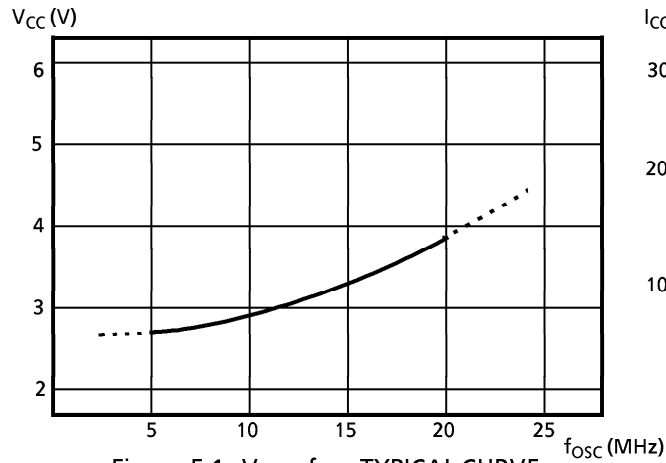


Figure 5.1  $V_{CC} - f_{osc}$  TYPICAL CURVE

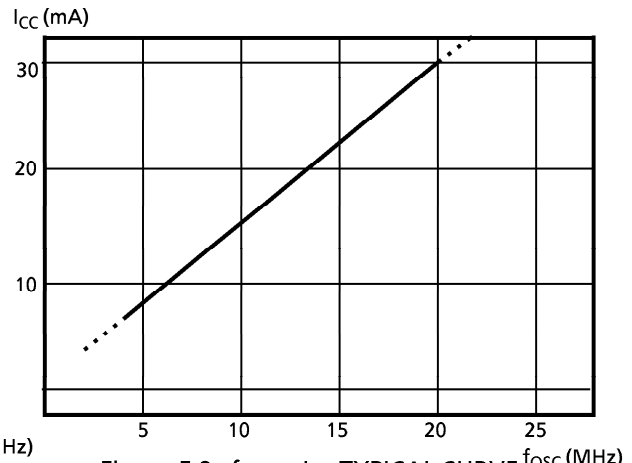


Figure 5.2  $f_{osc} - I_{CC}$  TYPICAL CURVE

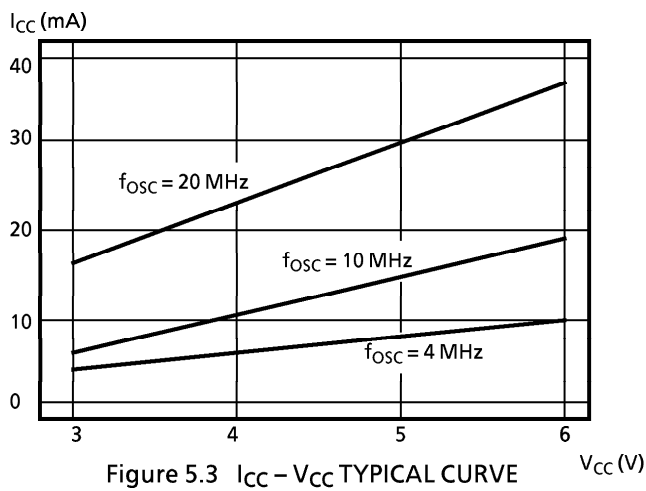


Figure 5.3  $I_{CC} - V_{CC}$  TYPICAL CURVE

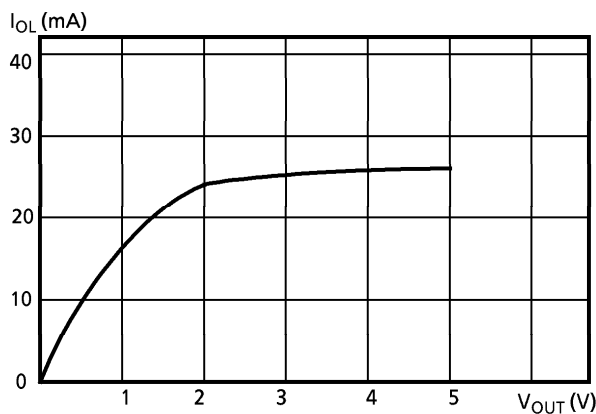


Figure 5.4  $V_{OUT} - I_{OL}$  TYPICAL CURVE

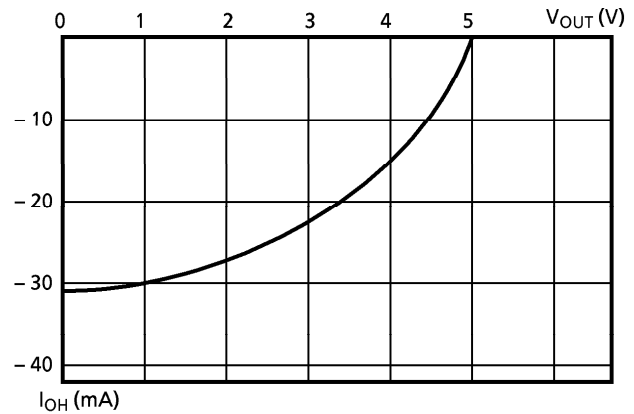


Figure 5.5  $V_{OUT} - I_{OH}$  TYPICAL CURVE