Digital Window Watchdog Timer

Description

The digital window watchdog timer, U5021M, is a CMOS integrated circuit. In applications where safety is critical, it is especially important to monitor the microcontroller. Normal microcontroller operation is indicated by a cyclically transmitted trigger signal which is received by a window watchdog timer within a defined time window. A missing or a wrong trigger signal makes the watchdog timer reset the microcontroller. The IC is tailored for microcontrollers which can work in both full-power and sleep mode. With additional voltage monitoring (power-on reset and supply voltage drop reset), the U5021M offers a complete monitoring solution for microsystems in automotive and industrial applications.

Features

- Low current consumption: I_{DD} < 100 µA
- RC–oscillator
- Internal reset during power up and supply voltage drops (POR)
- “Short” trigger window for active mode “long” trigger window for sleep mode
- Cyclical wake-up of microcontroller in sleep mode
- Trigger input
- Single wake-up input
- Reset output
- Enable output

Ordering Information

Extended Type Number	Package	Remarks
U5021M–NFP	SO8	

Block Diagram

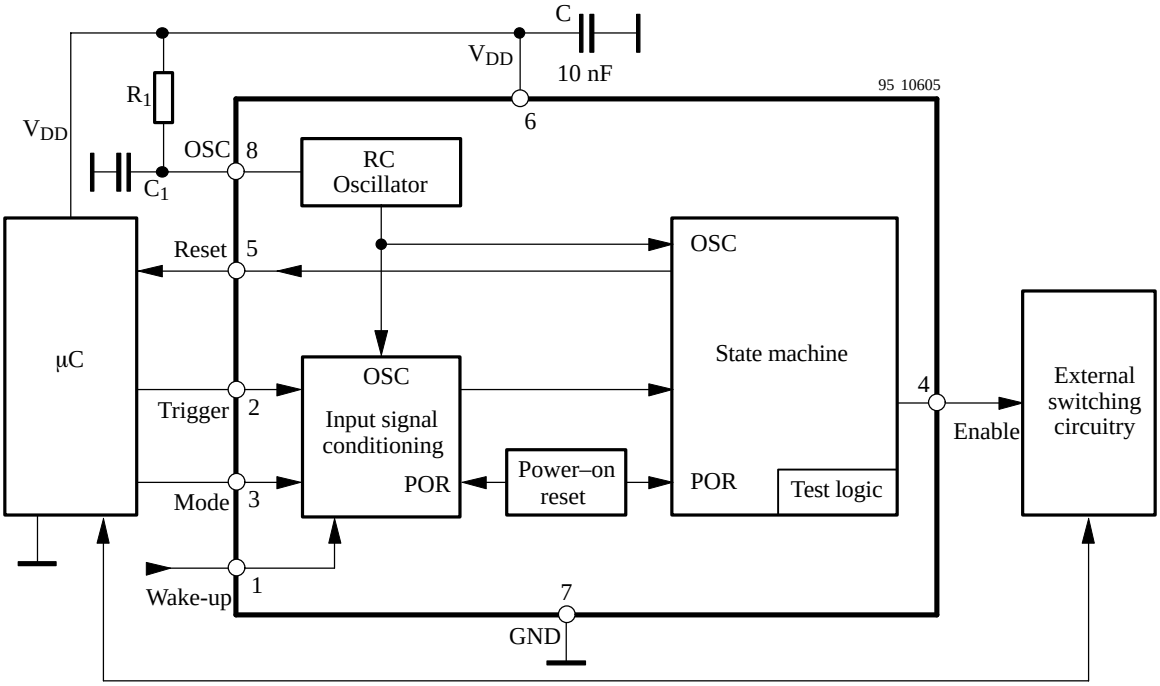

Figure 1. Block diagram with external circuit

Pin Description

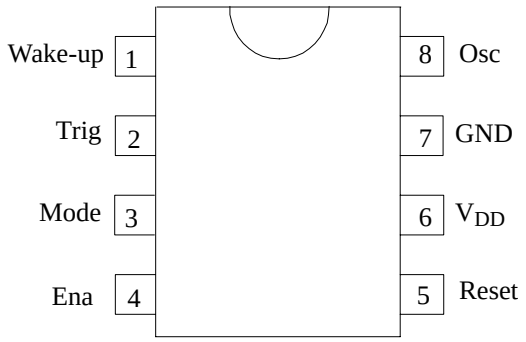

Figure 2. Pinning

Pin	Symbol	Function
1	Wake-up	Wake-up input (pull-down resistor) There is one digitally debounced wake-up input. During the long watchdog window, each signal slope at the input initiates a reset pulse at Pin 5.
2	Trig	Trigger input (pull-up resistor) It is connected to the microprocessor's trigger signal.
3	Mode	Mode input (pull-up resistor) The processor's mode signal initiates the switchover between the long and the short watchdog time.
4	Ena	Enable output (push-pull) It is used for the control of peripheral components. It is activated after the processor triggers three times correctly.
5	Reset	Reset output (open drain) Resets the processor in the case of a trigger error or if a wake-up pulse occurs during the long watchdog period.
6	V_{DD}	Supply voltage
7	GND	Ground, reference voltage
8	Osc	RC oscillator

Functional Description

Supply Voltage, Pin 6

The U5021M requires a stabilized supply voltage V_{DD} = 5 V ± 5% to comply with its electrical characteristic.

An external buffer capacitor of C = 10 nF may be connected between Pin 6 and GND.

RC-Oscillator, Pin 8

The clock frequency, f, can be adjusted with the components R_1 and C_1 according to the formula:

$$f = \frac{1}{t}$$

where $t = 1.35 + 1.57\ R_1\ (C_1 + 0.01)$

R_1 in kΩ, C_1 in nF and t in µs

The clock frequency determines all time periods of the logic part as shown in the last section of the data sheet (timing). With an appropriate selection of components, the clock frequency, f, is nearly independent of the supply voltage, as shown in figure 3. Frequency tolerance Δf_{max} = 10% with R_1 ± 1%, C_1 = ± 5%.

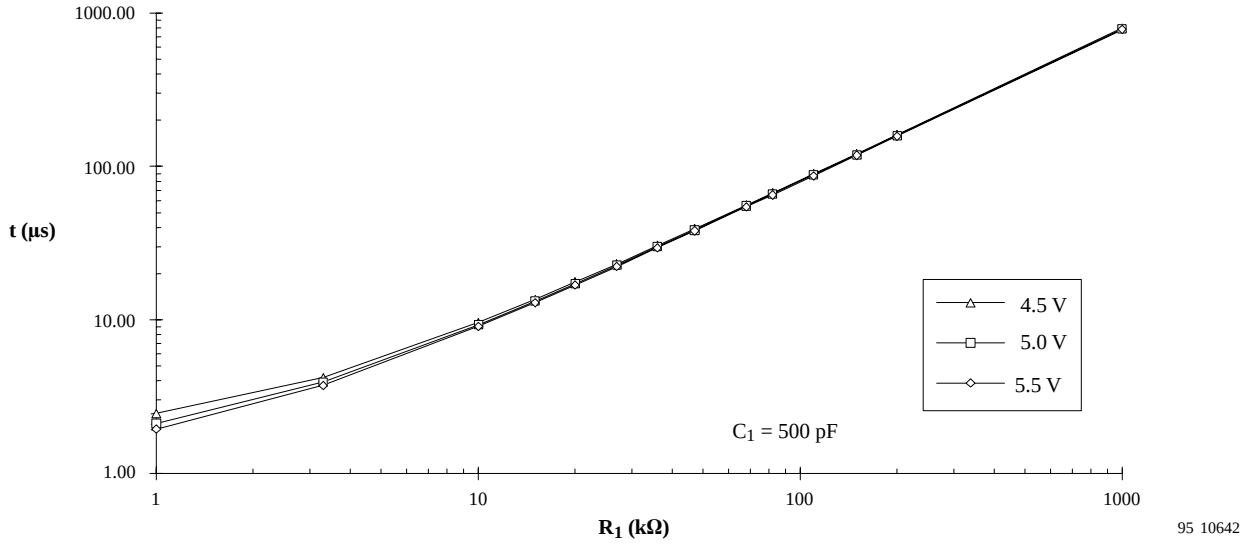

Figure 3. Period t vs. R_1, @ C_1 = 500 pF

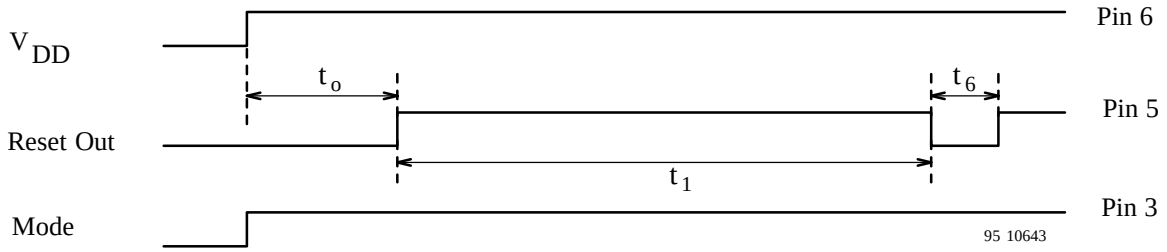

Figure 4. Power-on reset and switch-over mode

Supply Voltage Monitoring, Pin 5

During ramp-up of the supply voltage and in the case of supply-voltage drops the integrated power-on reset (POR) circuitry sets the internal logic to a defined basic status and generates a reset pulse at the reset output, Pin 5. A hysteresis in the POR threshold prevents the circuit from oscillating. During ramp–up of the supply voltage the reset output stays active for t_0 in order to bring the microcontroller into its defined reset status (see figure 4). Pin 5 has an open-drain output.

Switch-over Mode Time, Pin 3

The switch-over mode time enables the synchronous operation of microcontroller and watchdog. After the power-on reset time, the watchdog has to be switched to its monitoring mode by the microcontroller with a “low” signal transmitted to the mode pin (Pin 3) within the time-out period, t_1. If the low signal does not occur within t_1 (see figure 4), the watchdog generates a reset pulse, t_6, and t_1 starts again. Microcontroller and watchdog are synchronized with the switch-over mode time, t_1, each time a reset pulse is generated.

Microcontroller in Active Mode

Monitoring with the “Short” Trigger Window

After the switch-over mode, the watchdog works in the short watchdog mode and expects a trigger pulse from the microcontroller within the defined time window, t_3 (enable time). The watchdog generates a reset pulse which resets the microcontroller if

- the trigger pulse duration is too long,
- the trigger pulse is within the disable time, t_2
- there is no trigger pulse

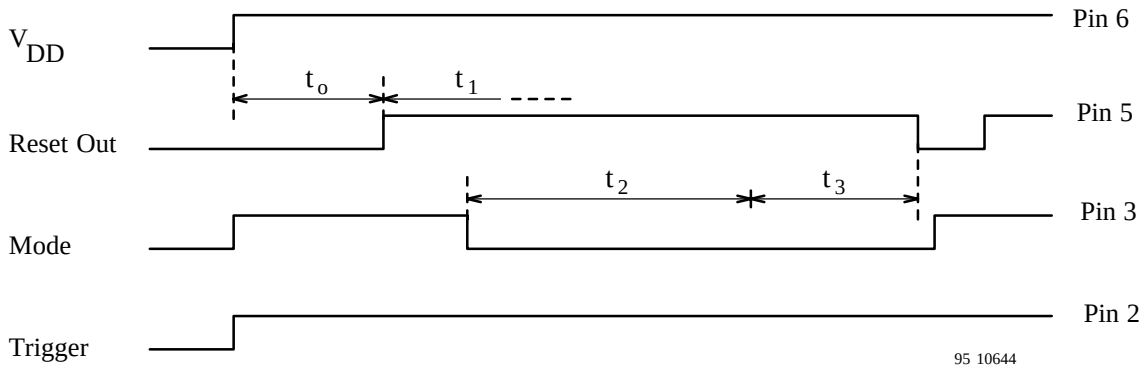

Figure 5. Pulse diagram with no trigger pulse during the short watchdog time

Figure 5 shows the pulse diagram with a missing trigger pulse.

Figure 6 shows a correct trigger sequence. The positive edge of the trigger signal starts a new monitoring cycle with the disable time, t_2. To ensure correct operation of the microcontroller, the watchdog needs to be triggered three times correctly before it sets its enable output. This feature is used to activate or deactivate safety-critical components which have to be switched to a certain condition (emergency status) in the case of a microcontroller malfunction. As soon as there is an incorrect trigger sequence, the enable signal is reset and it takes a sequence of three correct triggers again before enable is active.

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Microcontroller in Sleep Mode

Monitoring with the “Long” Trigger Window

The long watchdog mode allows cyclical wake-up of the microcontroller during sleep mode. As in short watchdog mode, there is a disable time, t_4, and an enable time, t_5, in which a trigger signal is accepted. The watchdog can be switched from the short trigger window to the long trigger window with a “high” potential at the mode pin (Pin 3). In contrast to the short watchdog mode, the time periods are now much longer and the enable output remains inactive so that other components can be switched off to effect a further decrease in current consumption. As soon as a wake-up signal at the wake-up input (Pins 1) is detected, the long watchdog mode ends, a reset pulse wakes-up the sleeping microcontroller and the normal monitoring cycle starts with the mode switch-over time.

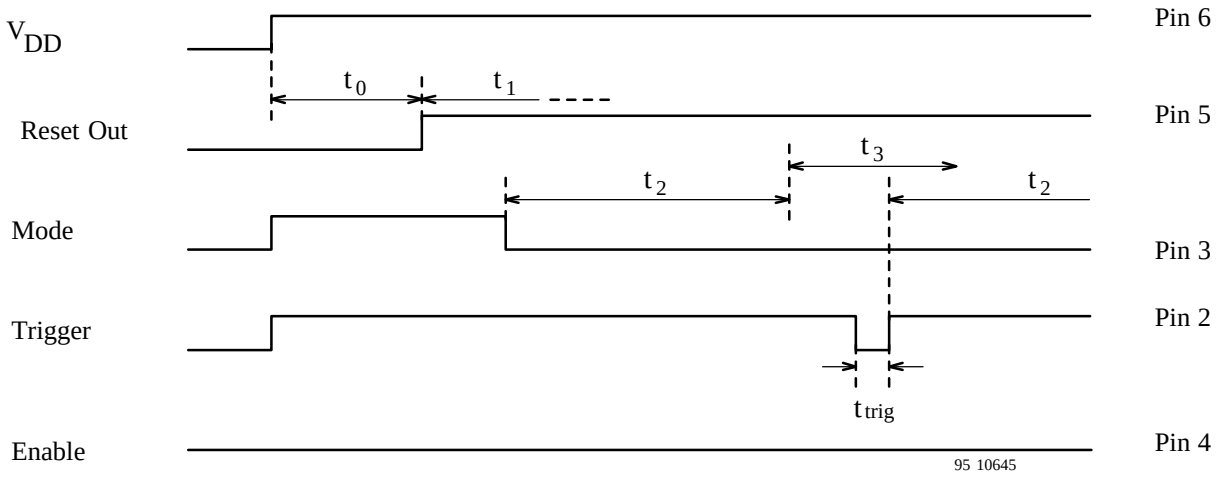


Figure 6. Pulse diagram of a correct trigger sequence during the short watchdog time

Figure 7 shows the switch-over from the short to the long watchdog mode. The wake-up signal during the enable time, t_5, activates a reset pulse, t_6.

The watchdog can be switched back from the long to the short watchdog mode with a low potential at the mode pin (Pin 3).

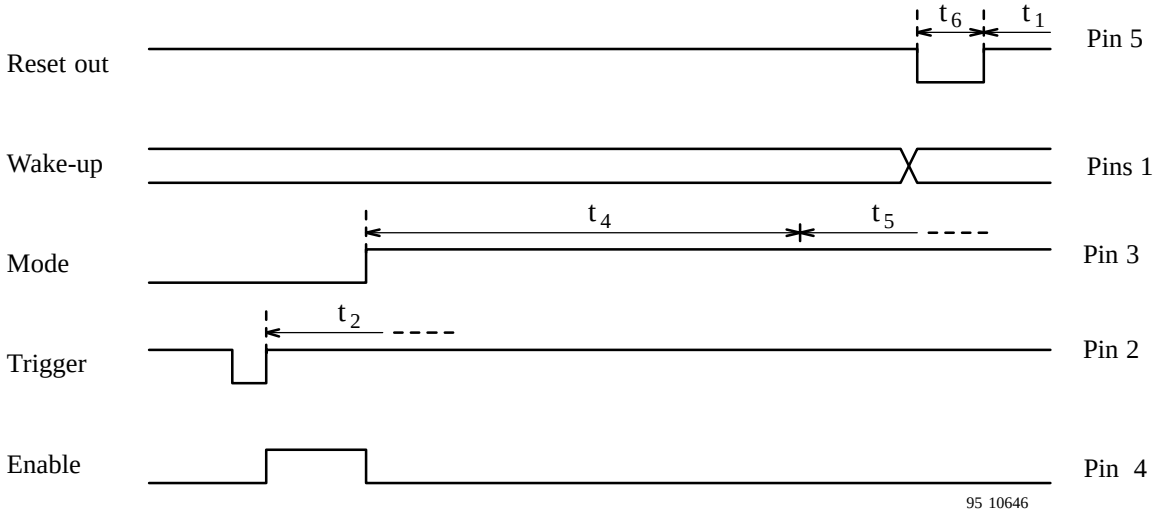
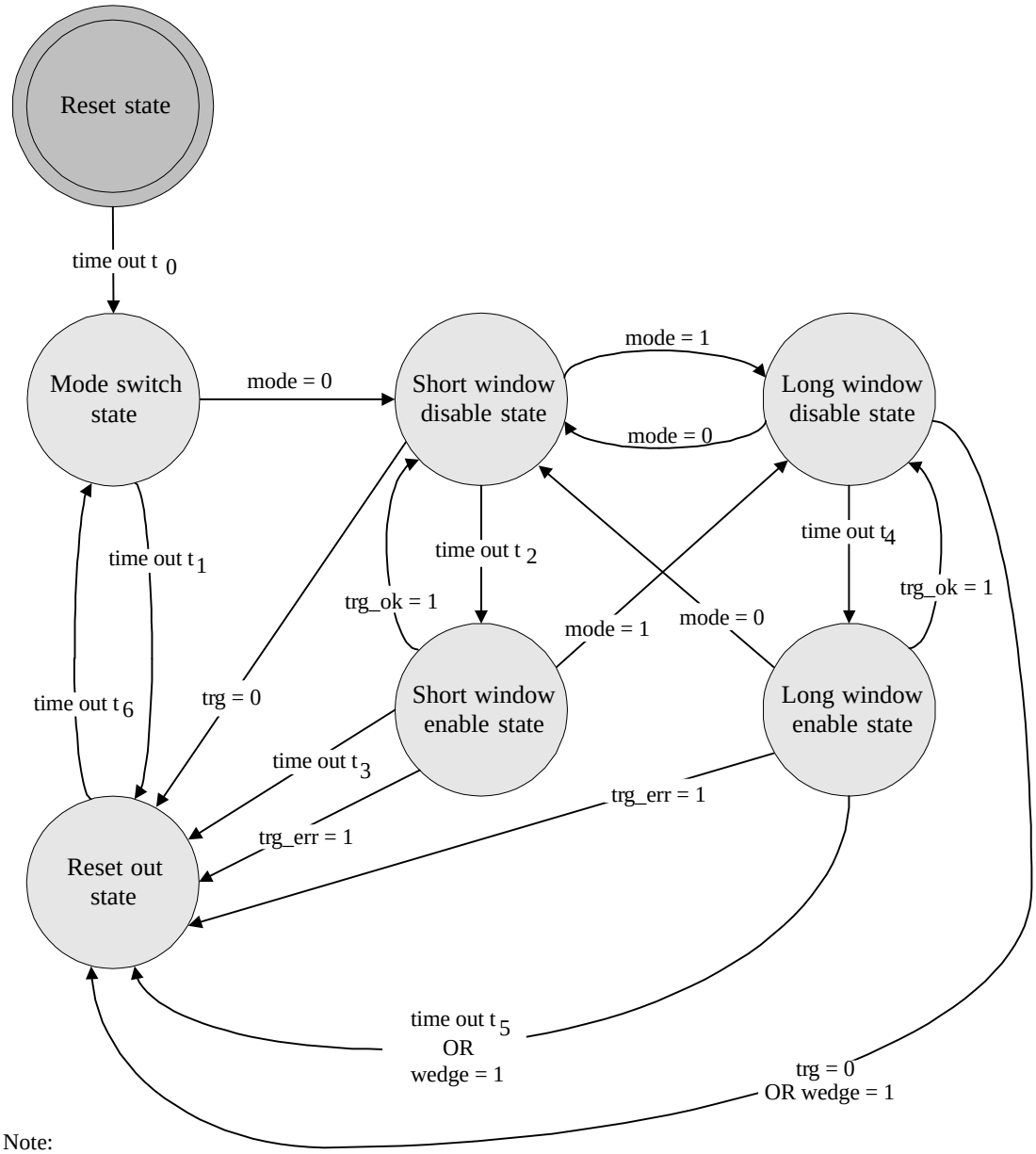


Figure 7. Pulse diagram of the long watchdog time

State Diagram

The kernal of the watchdog is a finite state machine. Figure 8 shows the state diagram. All possible states and transmissions are shown. Many transmissions are controlled by an internal timer. The numbers for the time-outs are the same as on the pulse diagrams.



Note:

”mode” and ”trg” are the debounced input signals from the pins MODE and TRG

trg_ok = 1 after the rising edge of the trg signal

trg_err = 1 when the trg signal low period is too long

wedge = 1 after detecting the debounced changing of an signal level from the WUP pin

every state change restarts the internal timer

Figure 8. State diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	6.5	V
Output current	I_{OUT}	± 2	mA
Input voltage	V_{IN}	–0.4 V to V_{DD} + 0.4 V	V
Ambient temperature range	T_{amb}	–40 to +125	°C
Storage temperature range	T_{stg}	–55 to +150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	180	K/W

Electrical Characteristics

V_{DD} = 5V, T_{amb} = –40 to 125°C, reference point is Pin 7, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 6	V_{DD}	4.5		5.5	V
Current consumption	R_1 = 66 kΩ Pin 6	I_{DD}			60	µA
Power-on reset	Release reset state with rising voltage at Pin 6	V_{POR1}	3.9		4.5	V
	Get reset state with falling voltage at Pin 6	V_{POR2}	3.8		4.4	V
Power-on reset hysteresis		V_{POR_hys}	40		200	mV
Inputs	Pins 1, 2, and 3					
Logical 'high'		V_{IH}	3.4			V
Logical 'low'		V_{IL}			1.6	V
Hysteresis		V_{IN_hys}	0.6		1.4	V
Input voltage range		V_{IN}	–0.3		V_{DD}+0.3	V
Input current	Pins 2 and 3	I_{IN1}	5		20	µA
Input current	Pin 1	I_{IN2}	–20		–5	µA
Outputs						
Max. output current	Pins 4 and 5	I_{OUT}	–2		2	mA
Logical output 'low'	I_{OUT} = –1 mA, Pins 4 and 5	V_{OL}			0.2	V
Logical output 'high'	I_{OUT} = –1 mA, Pin 4	V_{OH}	V_{DD} – 0.2			V
Leakage current	V_{OUT} = 5 V, Pin 5	I_{leak}			2	µA

Electrical Characteristics (continued)

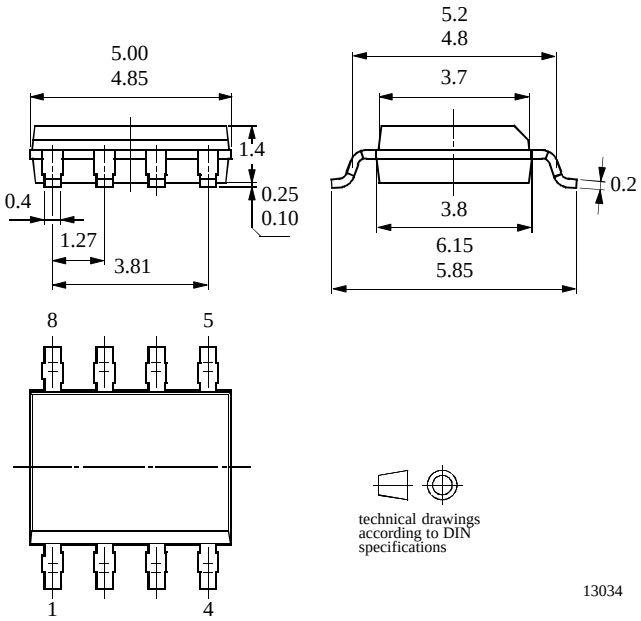
V_{DD} = 5V, T_{amb} = –40 to 125°C, reference point is Pin 7, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Timing						
Frequency deviation *)	R_1 = 66 kΩ, C_1 = 470 pF , V_{DD} = 4.5 to 5.5 V	Δf			5	%
Debounce time	Pins 2 and 3		3		4	cyc
Debounce time	Pin1		96		128	cyc
Max. trigger pulse length		t_{trgmax}		45		cyc
Power-up reset time		t_o		201		cyc
Switch over mode time		t_1		1112		cyc
Disable time	Short watchdog window	t_2		130		cyc
Enable time	Short watchdog window	t_3		124		cyc
Disable time	Long watchdog window	t_4		71970		cyc
Enable time	Long watchdog window	t_5		30002		cyc
Reset-out time		t_6		40		cyc

*) Frequency deviation depends also on the tolerances of the external components

Package Information

Package SO8
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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