PM7325

S/UNI-ATLAS-3200

DATASHEET ERRATA

CONFIDENTIAL

PRELIMINARY

ISSUE 2 : JUNE 2001

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PMC-2000259 (P2)

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Patents

The technology discussed is protected by the following patent:
Canadian Patent Number 2,164,546 issued on April 10, 2001
Relevant patent applications and other patents may also exist.

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	May 2001	Document Creation
2	June 2001	Changed reference to issue 4 from issue 3 of the datasheet.

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1 ISSUE 2 ERRATA

This document is the errata notice for Revision B of the S/UNI-ATLAS-3200 (PM7325-TC) and Issue 4 S/UNI-ATLAS-3200 datasheet. The Issue 4 S/UNI-ATLAS-3200 datasheet (PMC-1990553) and Issue 2 errata supersede all prior editions and versions of the datasheet.

1.1 Device Identification

The information contained in this document applies to the PM7325 S/UNI-ATLAS-3200 Revision B device only. The device revision code is marked at the end of the PMC Fab and Revision Code on the face of the device (as shown in Figure 1). PM7325 S/UNI-ATLAS-3200 Revision B is packaged in a 768 pin Tape BGA package.

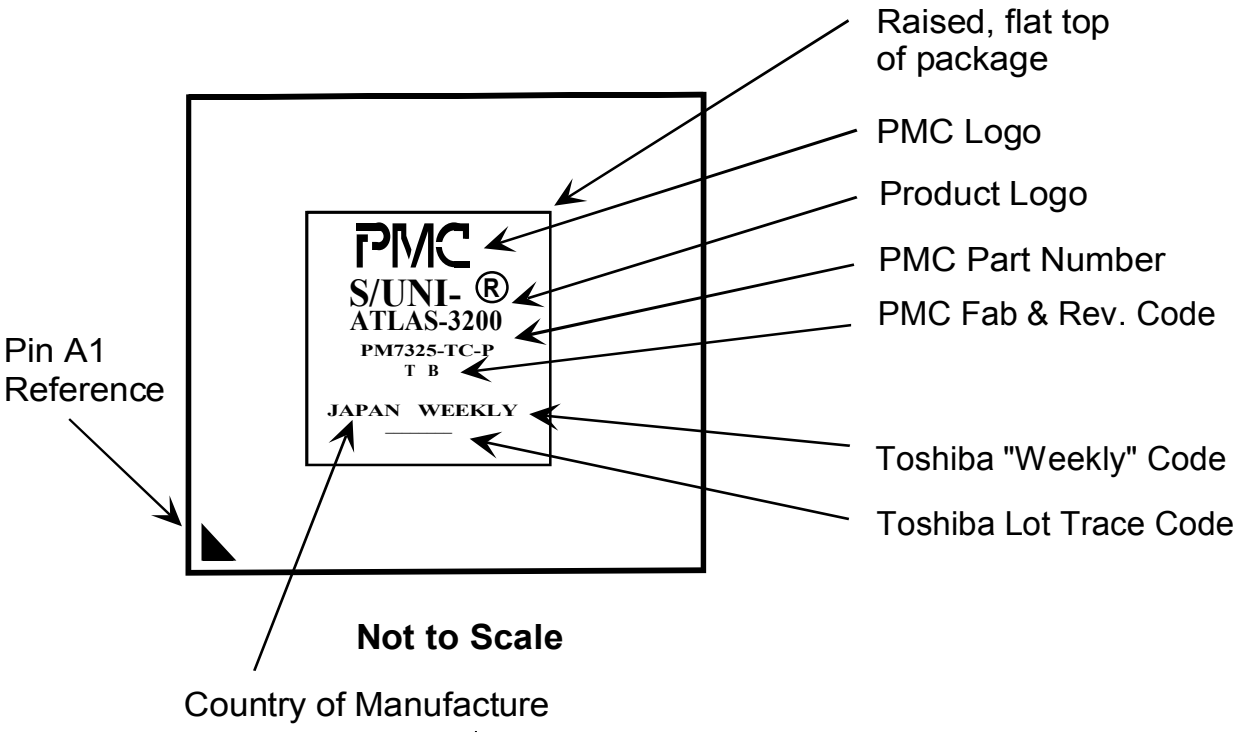

Figure 1 : PM7325 S/UNI-ATLAS-3200 Branding Format

2 DATASHEET DISCREPANCIES

Legend

1. unaltered text is unchanged to add context to changes

2. new material is bold and Italicized

~~3. obsolete material is struck out~~

4. comments specific to this document are in italics

5. A vertical bar in left margin indicates that this is a new item which was not present in the previous issue of this document.

NOTE: All items in Section 2 are documentation changes only.

2.1 Maximum tPul3pl3 Timing

The maximum value for tPul3pl3 in Table 58 of the datasheet is changed to 7.9ns from 6.0ns as shown below:

Table 58: Utopia Level 3/POS-PHY Level 3 AC Timing

Symbol	Description	Min	Max	Units
tPul3pl3	UL3/PL3 Clock to Output Propagation Delay (2)	1.5	***7.9*** ~~6.0~~	ns

2.2 Minimum tSsram Timing

The minimum value for tSsram in Table 60 of the datasheet is changed to 3.5ns from 3.0ns as shown below:

Table 60: SRAM Interface AC Timing

Symbol	Description	Min	Max	Units
tS_{sram}	SDAT, SPAR setup to SYSCLK	***3.5*** ~~3.0~~		ns

Note: For better performance, it is recommended to use a 166MHz Pipelined ZBT SRAM.

2.3 MCIF FIFO Capacity

The capacity of the Microprocessor Cell Interface FIFO (MCIF) extract FIFO is 15 cells rather than 16 cells. The first paragraph text in Section 10.17.5 – Reading Cells is changed to reflect this change:

Cells received on the Input Cell Interface or the Backward Cell Interface can be routed to the ~~16~~***15***-cell Microprocessor Cell Interface FIFO based on the type of cell.

2.4 GFR Non-Compliant Frame Counting

The following text is added under Section 10.7.3 – Guaranteed Frame Rate Policing, CLP conformance test section:

4. CLP conformance test: This test is performed on every cell in a frame, including the EOM. The CLP conformance test can be enabled on a per-connection basis; this is controlled by the CLPCC_CLP1_Discard bit of the Policing Configuration field in the VC Table. If the Start of Frame is a CLP = 1 cell, then any subsequent CLP=0 cell will be tagged ***(though this not be counted as a non-compliant frame, unless the EOP is also tagged).*** If the first cell of the frame is a CLP=0 cell, then if the CLPCC_CLP1_Discard bit is logic 1, any subsequent CLP=1 cell received in the frame will result in a partial packet discard being executed.

2.5 TxLink Interrupt Register Bit Order

The bit positions of the TCAERRI and TERRI bits are reversed in Register 0x282 as shown below:

Register 0x282: TxL Interrupt

Bit	Type	Function	Default
31:8		Unused	X
7		Unused	X
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1	R	~~TERRI~~ ***TCAERRI***	0
0	R	~~TCAERRI~~ ***TERRI***	0

3 FUNCTIONAL DISCREPANCIES

3.1 Non-optimal Throughput Observed for Certain Packet Sizes

3.1.1 RxPhy Performance Based on Calendar Configuration

When the device is configured in the ingress packet-bypass mode, inefficient PL3 operation may arise depending on the RxPhy calendar configuration. This inefficiency causes non-optimal throughput to be observed for certain packet sizes. In particular, the inefficiency is most pronounced when packets just slightly longer than the default PL3 burst length (e.g., 65 bytes) are sent.

3.1.1.1 Software Workaround - Calendar Padding

A simple workaround exists which involves padding the associated calendar. Padding the RxPhy calendar to its maximum length of 128 entries, by repeating the desired calendar several times, greatly enhances the throughput and eliminates much of the inefficiency.

Figure 2 below shows the measured maximum bandwidth versus packet size for the RxPhy interface for a single PHY setup with a single entry calendar and a maximum 128 entry calendar.

The first line series shows a single PHY setup with a single entry calendar. The second line series shows the impact of padding the calendar to 128 entries. Both series are based on tests with a 64-byte output burst size.

The bandwidth of the POS link is also shown as a reference line in the chart below. The upper curve shows the effective throughput of an STS-48c SPE envelope. The second bandwidth curve shows the effective POS data throughput of an STS-48c with an HDLC flag and CRC-16 embedded in the packet. The third bandwidth curve is similar to the second bandwidth curve except that the packet now carries two HDLC flags and a CRC-32. Normally, the HDLC flags and the CRC bytes should be stripped off by the PHY layer device.

Note: The calendar padding workaround has been implemented in PMC-Sierra's beta release version of the device driver. It will pad the RxPhy calendar up to a maximum integer multiple of the original number of entries, not exceeding the 128 entry capacity.

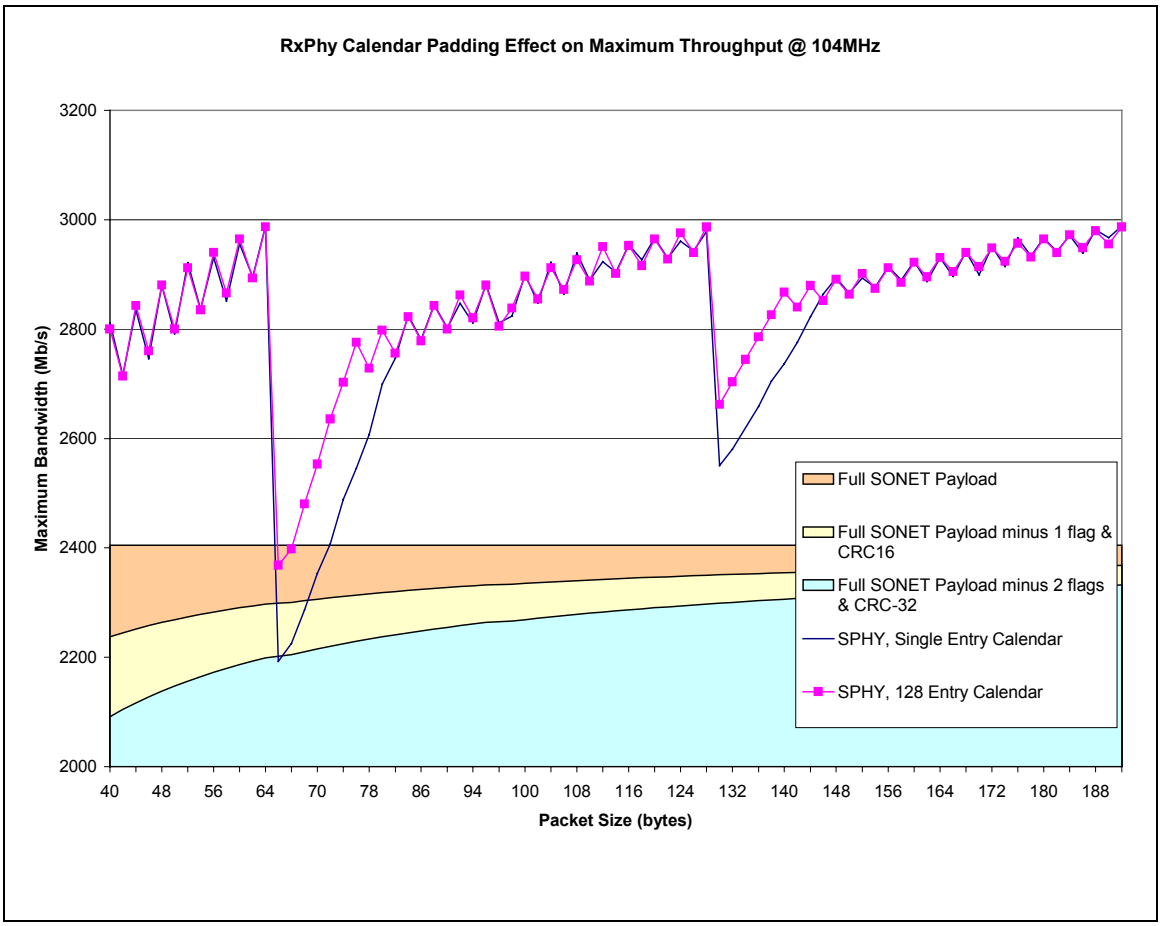

Figure 2: RxPhy Calendar Padding Effect on Throughput

3.1.1.2 Performance with Workaround

With the RxPhy calendar padded to the maximum number of entries, full throughput can be achieved at 104 MHz for all packet sizes greater than 40 bytes, so long as at least a CRC-16 and one HDLC flag is stripped off from each packet by the PHY device.

3.1.1.3 Performance without Workaround

Without the calendar padding, the RxPhy is unable to transmit long strings of 65 to 71 byte packets at full bandwidth. Full throughput can still be achieved as long as the proportion of 65 to 71 byte packets is sufficiently small so that the overspeed from processing other cells or packets outweighs the inefficiency in transmitting the 65 to 71 byte packets. The throughput of ATM cells, particularly if the output cell length is greater than 56 bytes, will also be adversely affected.

3.1.2 RxPhy Performance with Reduced Frequency

When the device is configured in the ingress packet-bypass mode, non-optimal throughput is observed when transmitting back-to-back packets that are 65 or 66 bytes long. This reduction in performance will not reduce throughput below STS-48c for most systems. However, this limits the RxPhy frequency from being reduced to below 101MHz while still maintaining maximum throughput. This problem can be alleviated if a wider variety of packet sizes are transmitted, or by introducing mixed cell/packet traffic, or by increasing the PL3 burst size.

3.1.2.1 Software Workaround - Extending Burst Length

To improve throughput for all packet sizes, the RxPhy output burst size can be increased from the default setting of 64 bytes. This may, however, routinely result in the underrun (UNDI) interrupt being asserted in the Bypass SDQ. Figure 3 below shows the measured maximum bandwidth versus packet size for the RxPhy interface for two burst size settings.

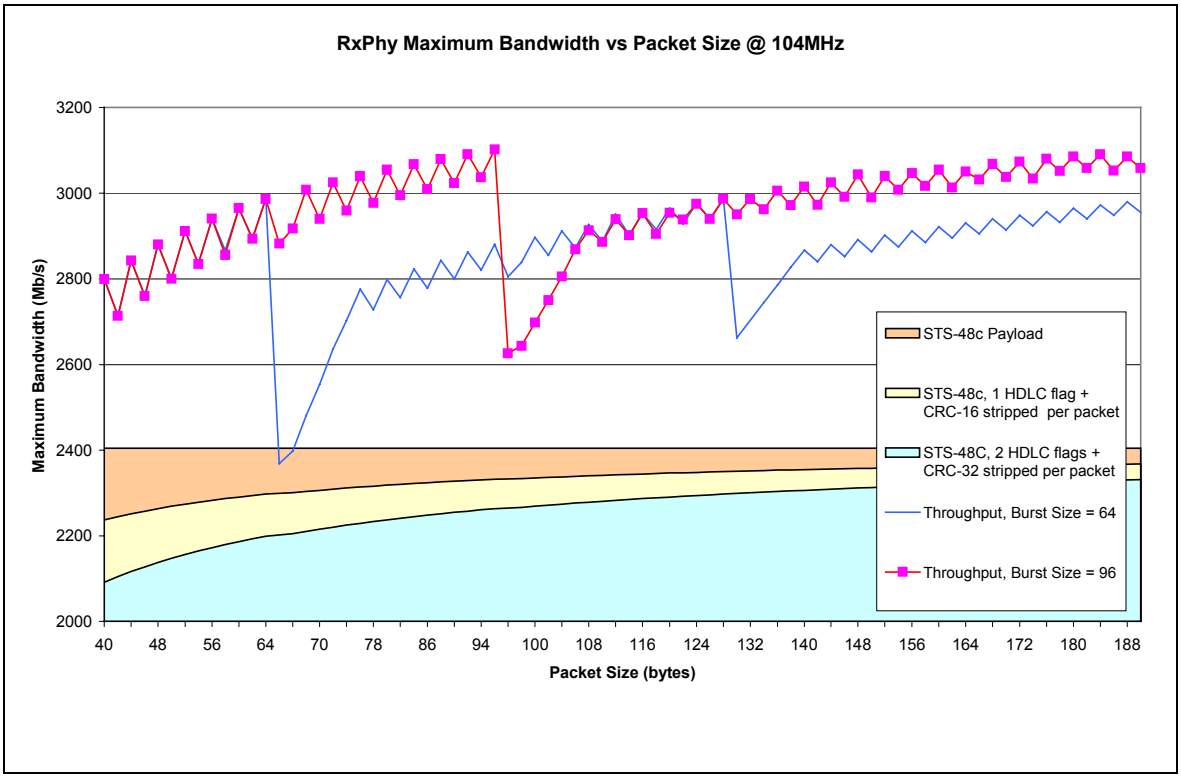

Figure 3: RxPHY Burst Length Effect on Throughput

The first line series shows a single PHY setup with the default burst size of 64 bytes. The second line series shows the impact of increasing the output burst size to 96 bytes.

The bandwidth of the POS link is also shown as a reference line in the chart above. The upper curve shows the effective throughput of an STS-48c SPE envelope. The second bandwidth curve shows the effective POS data throughput of an STS-48c with an HDLC flag and CRC-16 embedded in the packet. The third bandwidth curve is similar to the second bandwidth curve except that the packet now carries two HDLC flags and a CRC-32. Normally, the HDLC flags and the CRC bytes should be stripped off by the PHY layer device.

3.1.2.2 Performance with Workaround

By increasing the burst size to 96 bytes, the minimum throughput for all packets that are over 40 bytes long increases to 2,626 Mbit/s at 104 MHz. This is roughly a 12% speedup over an STS-48c POS data stream with one HDLC flag and CRC-16. The Bypass SDQ Underrun interrupt may, however, routinely be activated.

However, even if packet throughput is sufficient, ATM cell throughput may become the limit if the output cell length is 60 or 64 bytes. An STS-48c contains (780 x 48 x 8000)/53 = 5.651×10^6 cells/sec. The required RxPhy frequency to carry this traffic is (5.651×10^6) x (OutCellLen/4 + 2), where OutCellLen is the output cell length, in bytes. Thus for a 64-byte output cell, the required frequency is 101.7 MHz; for 60 byte cells it is 96.1 MHz.

3.1.2.3 Performance without Workaround

As long as the CRC-16 is stripped off from the packet before it is transmitted to the PHY device, and as long as the calendar is padded out to its maximum size, then full traffic should be carried in the ingress direction with any packet length over 40 bytes. However, if the frequency of the PL3 bus is reduced below 101 MHz, a constant stream of 65-byte packets could no longer be sustained for an extended period of time.

3.1.3 TxLink Performance Based on a Single OC-48c PHY Configuration

When the device is configured in the egress packet-bypass mode while carrying a single OC-48c, non-optimal throughput is observed when transmitting back-to-back packets that are 65 to 71 bytes long. This problem can be alleviated if a wider variety of packet sizes are transmitted, or by introducing mixed cell/packet traffic.

3.1.3.1 Software Workaround – Increasing Burst Size

When transmitting a constant packet size of 65 bytes, the measured bandwidth is 2,186 Mbit/s. To ensure optimal throughput for packet sizes of 65 to 71 bytes, the TxLink output burst size can be increased from the default setting of 64 bytes. This will, however, result in the underrun (UNDI) interrupt being asserted in the Bypass SDQ. Note that, when increasing the burst size, the USE_STPA bit must be set to logic 1 in the ATLAS-3200, and, if interfacing with a S/UNI-MACH48, the corresponding TPAHOLD bit in the MACH48 must be set to logic 1.

Figure 4 below shows the measured maximum bandwidth versus packet size for the TxLink interface for two burst size settings in a single PHY setup.

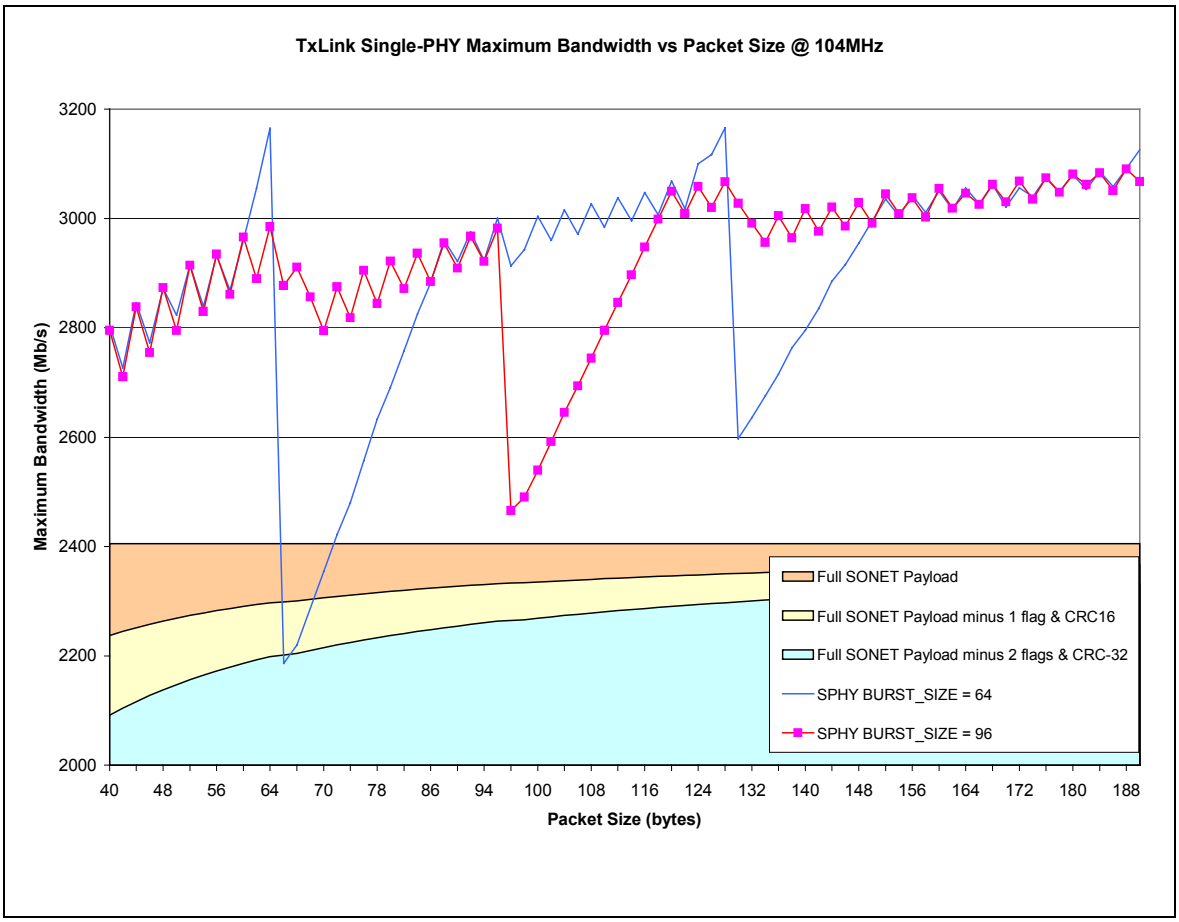

Figure 4: TxLink PL3 Single-PHY Performance

The first line series shows a single PHY setup with the default burst size of 64 bytes. The second line series shows the impact of increasing the output burst size to 96 bytes.

Note: Unlike the RxPhy, the TxLink calendar is required to be of minimum size for best throughput. This is done automatically in PMC-Sierra's beta release version of the device driver. The rates shown in the graph were measured with the TxLink output servicing calendar set to minimum size.

3.1.3.2 Performance with Workaround

With a burst size of 96 bytes, in the single PHY case, the minimum throughput for a packet over 40 bytes long increases to 2,465 Mbits/sec at 104 MHz. This is a speedup of roughly 6% over OC-48c POS with one HDLC flag and CRC-16. The Bypass SDQ Underrun interrupt may, however, routinely be activated.

3.1.3.3 Performance without Workaround

Without the workaround in place, single STS-48c PHY packet bypass is unable to transmit long strings of 65-71 byte cells at full bandwidth. Full throughput is still achieved as long as the proportion of 65-71 byte packets is sufficiently small so that the overspeed from processing other packets outweighs the inefficiency in transmitting the 65-71 byte packets

3.1.4 TxLink Performance Based on a Quad OC-12c PHY Configuration

When the device is configured in the egress packet-bypass mode while carrying four OC-12c flows, non-optimal throughput is observed when transmitting back-to-back packets that are 65-68 bytes long. This problem can be alleviated if a wider variety of packet sizes are transmitted, or by introducing mixed cell/packet traffic, or by increasing the PL3 output burst size.

3.1.4.1 Software Workaround – Increasing Burst Size

When transmitting a constant packet size of 65 bytes, the measured bandwidth is 2,273 Mbit/s. Although this is better than the single PHY case, it is still non-optimal for 65-68 byte packets. To ensure optimal throughput for packet sizes of 65 to 68 bytes, the TxLink output burst size can be increased from the default setting of 64 bytes. This will, however, result in the underrun (UNDI) interrupt being asserted in the Bypass SDQ.

Figure 5 below shows the measured maximum bandwidth versus packet size for the TxLink interface for two burst size settings in a multi-PHY (4 x STS-12) setup. Note that, when increasing the burst size, the USE_STPA bit must be set to logic 1 in the ATLAS-3200, and, if interfacing with a S/UNI-MACH48, the corresponding TPAHOLD bit in the MACH48 must be set to logic 1.

The first line series shows the quad PHY setup with the default burst size of 64 bytes. The second line series shows the impact of increasing the output burst size to 96 bytes. The rates shown in the graph were measured with the TxLink output servicing calendar set to minimum size (4 entries).

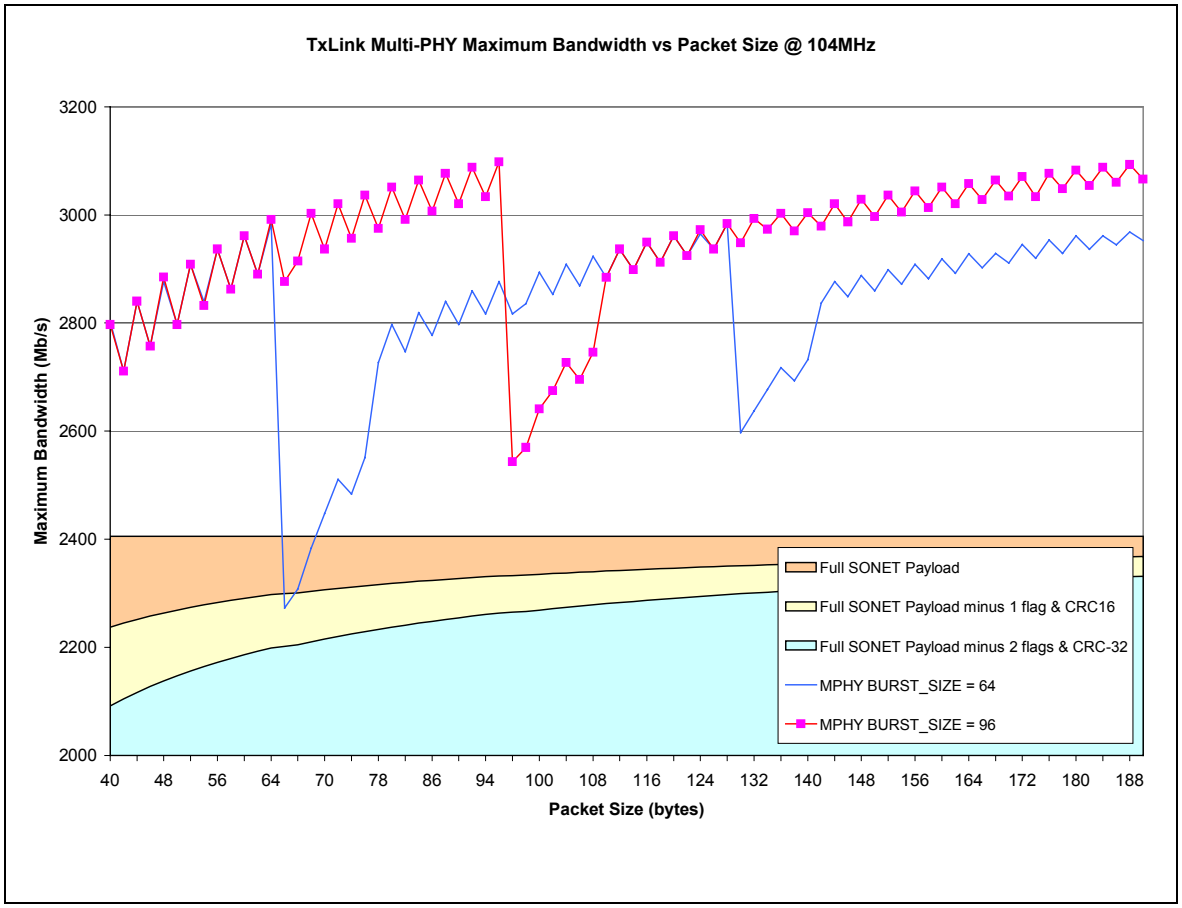

Figure 5: TxLink PL3 Quad PHY Performance

3.1.4.2 Performance with Workaround

With a burst size of 96 bytes in the quad PHY case, the minimum throughput for a packet over 40 bytes long increases to 2,545 Mbit/sec at 104 MHz. This is a

speedup of roughly 9% over OC-48c POS with one HDLC flag and CRC-16. The Bypass SDQ Underrun interrupt may, however, routinely be activated.

3.1.4.3 Performance without Workaround

Without the workaround in place, quad OC-12c PHY packet bypass is unable to transmit long strings of 65-68 byte cells at full bandwidth, unless at least two HDLC flags and a CRC-32 are stripped from each packet by the PHY. Full throughput is still achieved as long as the proportion of 65-68 byte packets is sufficiently small so that the overspeed from processing other packets outweighs the inefficiency in transmitting these 65-68 byte packets.

NOTES

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PMC-2000259(P2) ref PMC-1990553(P4) Issue date: June 2001