2N4199 thru 2N4204

Designer's Data Sheet

Silicon Controlled Rectifiers

Reverse Blocking Triode Thyristors

SCRs
100 AMPERE PULSE
300 thru 800 VOLTS

. . . fast switching, high-voltage Thyristors especially designed for pulse modulator applications in radar and other similar equipment.

- Guaranteed Limits on All Critical Parameters
- High-Voltage: V_{DRM} = 300 to 800 Volts
- Maximum Turn-On Times Specified — 300 to 400 ns
- Repetitive Pulse Current to 100 Amperes
- Stable Switching Characteristics Over an Operating Temperature Range From −65 to +105°C
- Pulse Repetition Rates as High as 20,000 pps
- JAN Versions Available

CASE 63-03
(TO-64)
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage, Note 1 (T_J = 105°C)	V_{RRM}	50	Volts
*Peak Forward Blocking Voltage, Note 1 (T_C = 105°C) 2N4199 2N4200 2N4201 2N4202 2N4203 2N4204	V_{DRM}	300 400 500 600 700 800	Volts
Repetitive Peak On-State Current (PW = 3 μs, Duty Cycle = 0.6%, T_C = 85°C)	I_{TRM}	100	Amps
Continuous On-State Current (T_C = 65°C)	I_T	5	Amps
Current Application Rate, Note 2	di/dt	5000	A/μs
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5	Amps
Peak Gate Voltage — Forward Reverse, Note 3	V_{GFM} V_{GRM}	10 10	Volts
Operating Junction Temperature Range Blocking State Conducting State	T_J	 −65 to +105 −65 to +200	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Stud Torque	—	15	in. lb.

*Indicates JEDEC Registered Data.

Notes: 1. Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. V_{DRM} and V_{RRM} may be applied as a continuous dc voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.

2. Minimum Gate Trigger Pulse: I_G = 200 mA, PW = 1 μs, t_r = 20 ns.

3. Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.

Designers Data for "Worst Case" Conditions — The Designers Data Sheets permit the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

T-25-15

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open) T_C = 105°C	17	I_{DRM}, I_{RRM}	—	2	mA
Gate Trigger Current (Continuous dc) (Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = 25°C) *(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = −65°C)	14	I_{GT}	— —	50 100	mA
Gate Trigger Voltage (Continuous dc) *(Anode Voltage = rated V_{DRM}, R_L = 100 ohms, T_C = 105°C) (Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = 25°C) *(Anode Voltage = 7 Vdc, R_L = 100 ohms, T_C = −65°C)	12	V_{GT}	 0.2 — —	 — 1.5 2	Volts
*Holding Current (Anode Voltage = 7 Vdc, gate open, T_C = 105°C)	18	I_H	3	—	mA
*Forward "On" Voltage (I_{TM} = 5 Adc, PW = 1 ms max, Duty cycle ≤ 1%)	8	V_{TM}	2.6	—	Volts
*Dynamic Forward "On" Voltage (0.5 μs after 50% decay point on dynamic forward voltage waveform) Forward Current: 30 A pulse Gate Pulse: at 200 mA, PW = 1 μs, t_r = 20 ns	7	V_{TM}	—	25	Volts
*Turn-On Time I_{TM} = 30 A					ns
Delay Time — All types	1, 9	t_d	—	200	
Rise Time — 2N4199 and 2N4200	1, 11	t_r	—	200	
2N4201			—	150	
2N4202			—	130	
2N4203 and 2N4204			—	100	
*Pulse Turn-Off Time Test Conditions: PFN discharge; Forward Current = 30 A pulse; Reverse Current = 5 A, T_C = 85°C, dv/dt = 250 V/μs to Rated V_{DRM}; Reverse anode voltage during turn-off interval = 0 V; Reverse gate bias during turn-off interval = 6 V	2, 13	t_q	—	20	μs
*Forward Voltage Application Rate (Linear Rise of Voltage) (T_C = 105°C, gate open, V_D = Rated V_{DRM})	16	dv/dt	250	—	V/μs

*JEDEC Registered Data.

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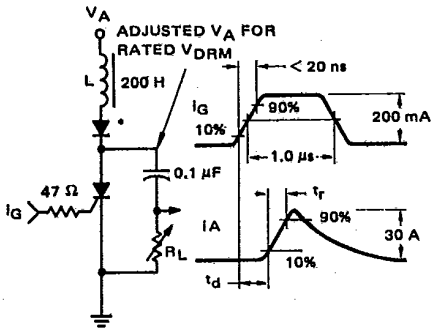
TEST CIRCUITS

FIGURE 1 – TURN-ON TIME



*Two 1N4937 fast-recovery diodes in series each shunted by a 180 kΩ resistor.

FIGURE 2 – TURN-OFF TIME

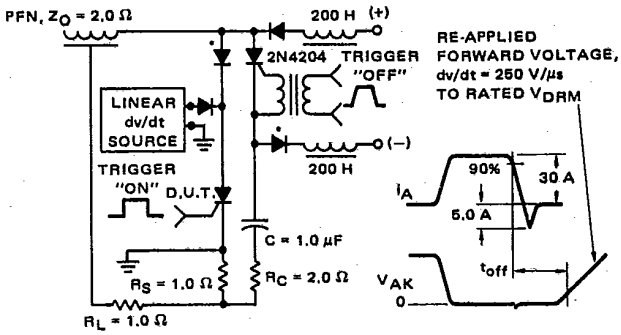


FIGURE 3 – MAXIMUM ALLOWABLE FORWARD PULSE CURRENT

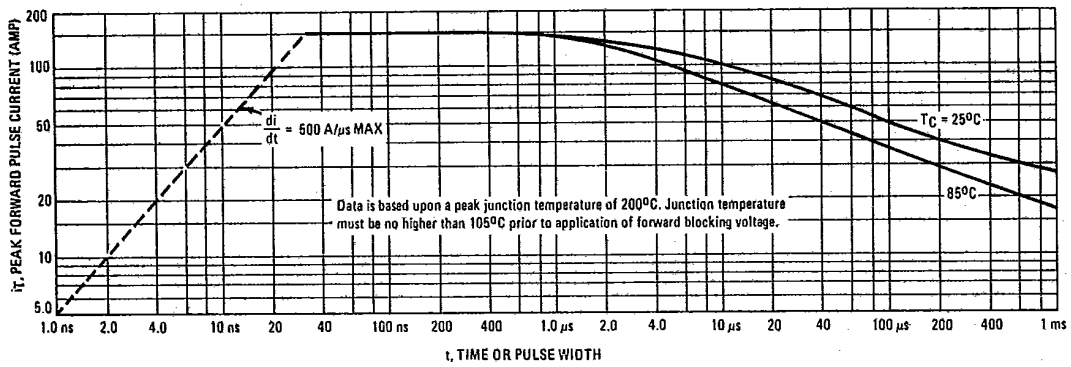


FIGURE 4 – DERATING USING NO SWITCHING LOSSES

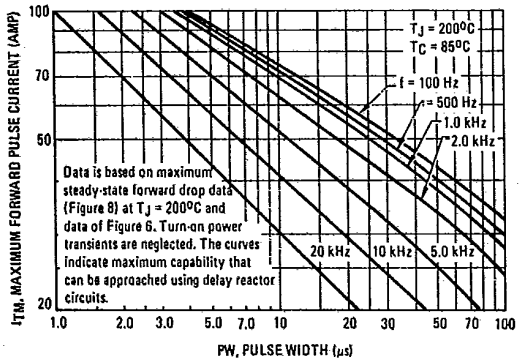


FIGURE 5 – DERATING USING TYPICAL SWITCHING LOSSES

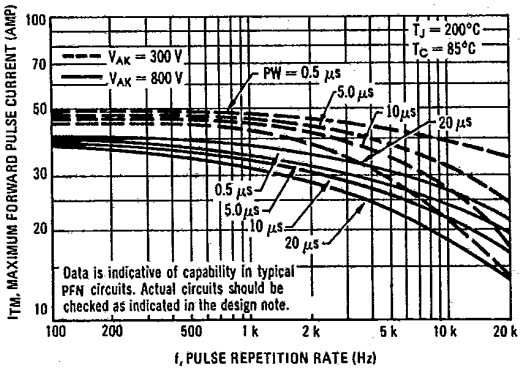


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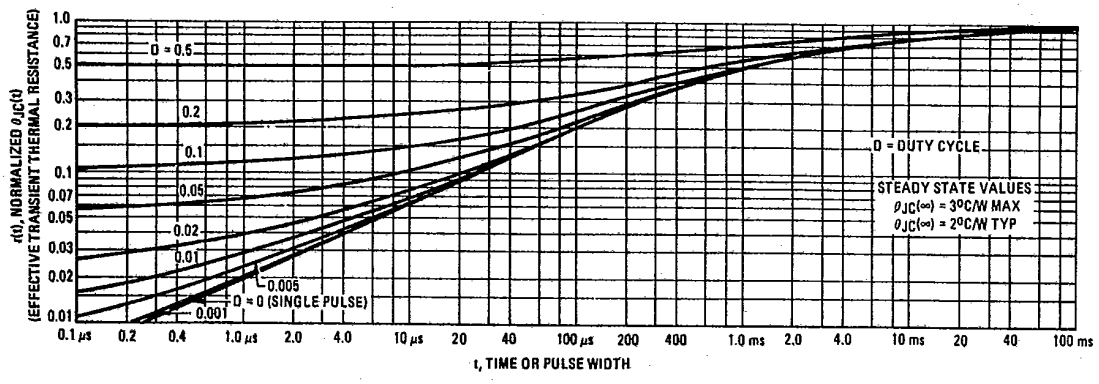
FIGURE 6 – NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE



FORWARD "ON" VOLTAGE DATA

FIGURE 7 – TYPICAL DYNAMIC FORWARD "ON" VOLTAGE

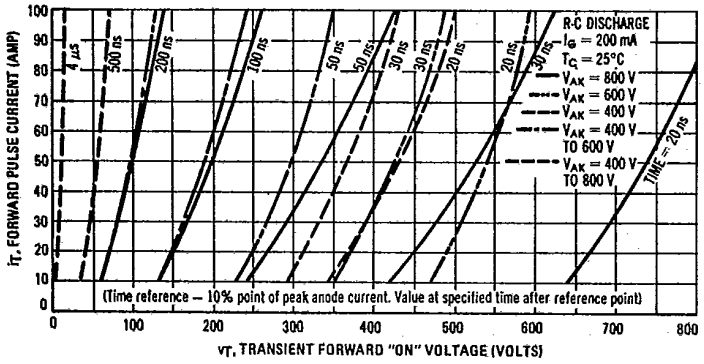
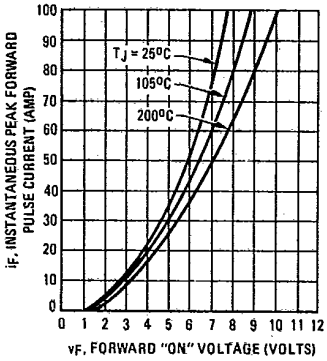


FIGURE 8 – MAXIMUM STEADY-STATE



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DESIGN NOTE CONTINUED

$\Delta T(t_4) = [\,1000\,[0.0205 + (1 - 5.25 \cdot 10^{-3})\,0.27 + 5.25 \cdot 10^{-3} - 0.27] + 700\,[(1 - 7.75 \cdot 10^{-3})\,0.27 + 7.75 \cdot 10^{-3} - 0.27]\,]\,3 = 93.51^{\circ}C$

$\Delta T(t_5) = [\,1000\,[0.032 + (1 - 5.25 \cdot 10^{-3})\,0.27 + 5.25 \cdot 10^{-3} - 0.27 - 0.0205] + 700\,[0.025 + (1 - 7.75 \cdot 10^{-3})\,0.27 + 7.75 \cdot 10^{-3} - 0.27]\,]\,3 = 105.6^{\circ}C$

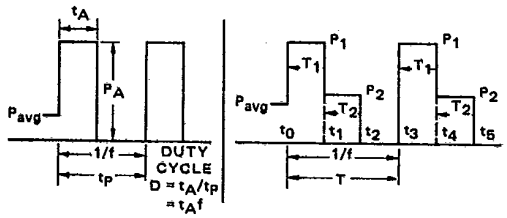


FIGURE A – SIMPLE MODEL FIGURE B – MORE ACCURATE MODEL

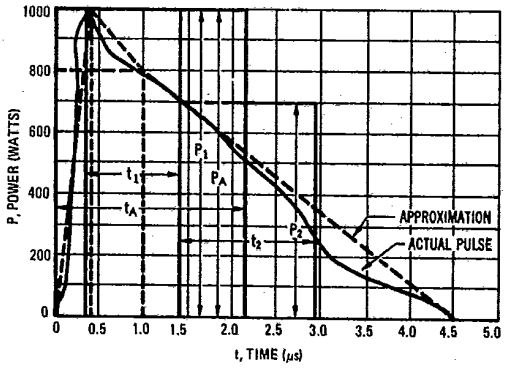


FIGURE C – AN ACTUAL TRANSIENT POWER PULSE

SWITCHING CHARACTERISTICS

FIGURE 9 – DELAY TIME

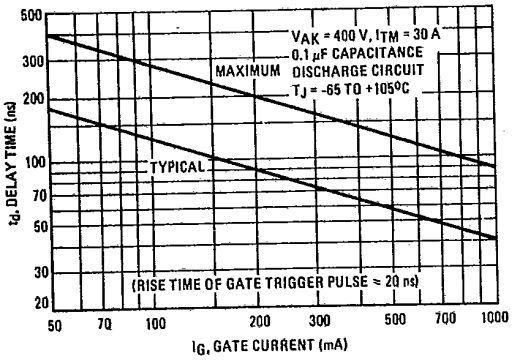


FIGURE 11 – CURRENT RISE TIME

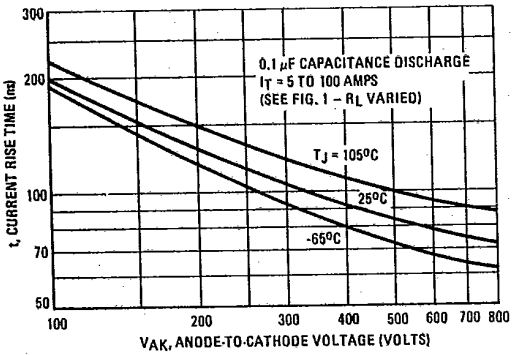
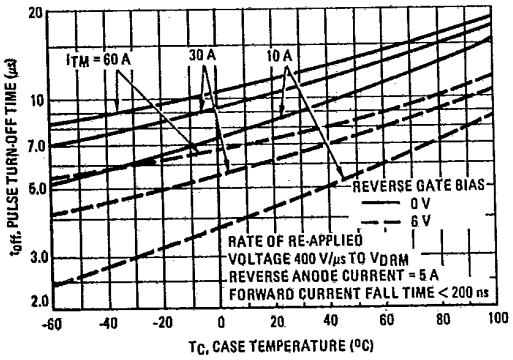


FIGURE 13 – TYPICAL TURN-OFF TIME



TRIGGERING CHARACTERISTICS

FIGURE 10 – TYPICAL PULSE TRIGGER CHARGE/CURRENT

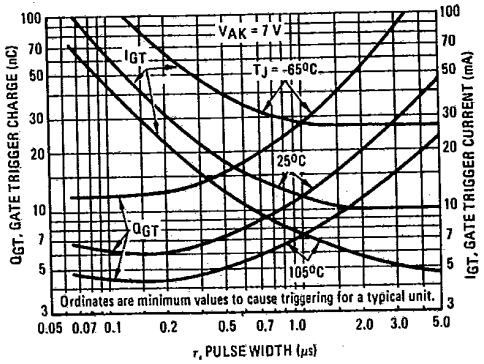


FIGURE 12 – DC GATE TRIGGER VOLTAGE

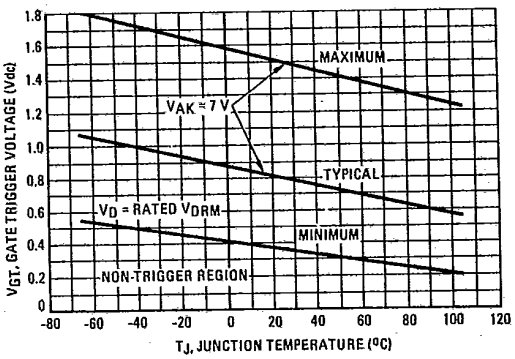


FIGURE 14 – DC GATE TRIGGER CURRENT

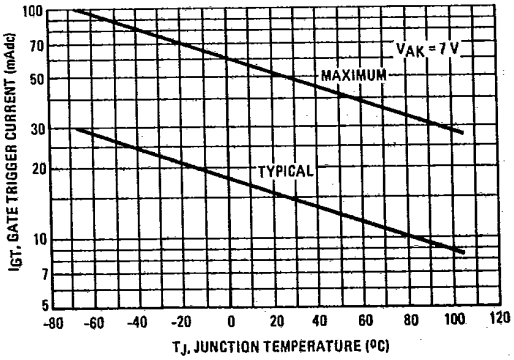


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FIGURE 15 – TYPICAL BLOCKING VOLTAGE DERATING

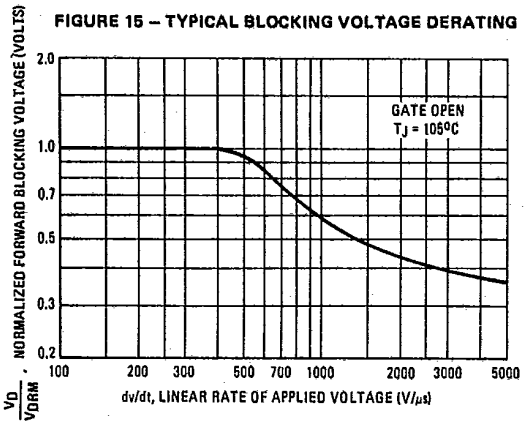

FIGURE 16 – TYPICAL LINEAR dv/dt CAPABILITY

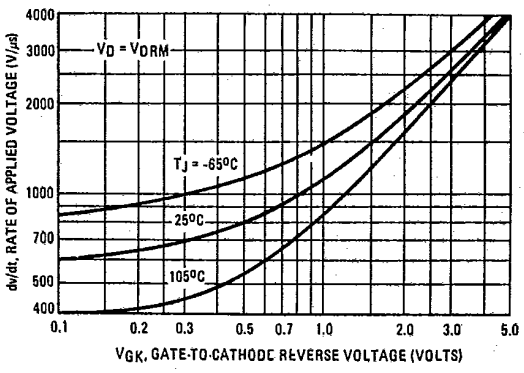

FIGURE 17 – FORWARD BLOCKING CURRENT

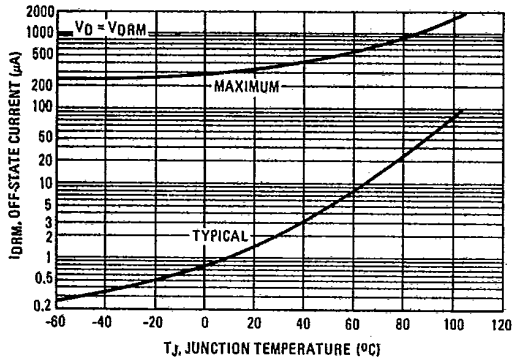

FIGURE 18 – HOLDING CURRENT

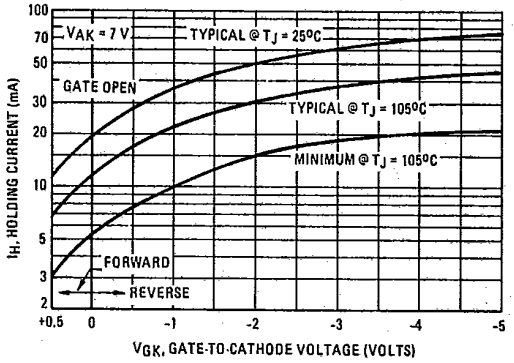

FIGURE 19 – TYPICAL ANODE-TO-CATHODE CAPACITANCE

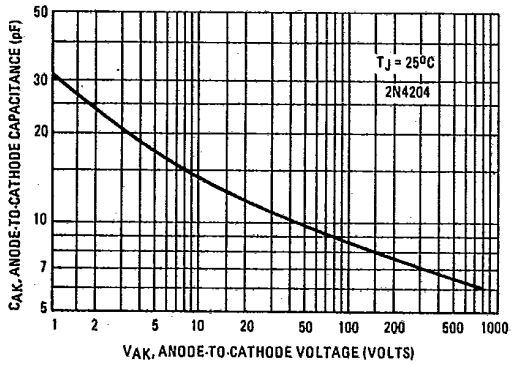

FIGURE 20 – TYPICAL GATE-TO-CATHODE CAPACITANCE