Features

- **Input Voltage: 8 V to 40 V**
- **Output Voltage Linear Regulator: 5 V/50 mA/3 mA**
- **ON_NOFF (High Active) Input**
- **Window Watchdog**
- **OFF Mode Quiescent current < 10 µA**
- **Standby Mode Quiescent Current < 30 µA**
- **Temperature Range: -40° C to 125°C**
- **Reset Logic**
- **Select Pin Standby/OFF Mode**

Description

The ATA6405 is a fully integrated system voltage supply IC. The device is designed for the 12/24 V board voltage system in a motor vehicle. In order to minimize power consumption, a switching regulator generates a voltage for supplying the internal linear regulator with a 5 V output voltage for microcontrollers.

To monitor the microcontroller, provision has been made for a window watchdog feature incorporating a reset logic function. The voltage system IC has three modes: active, Standby and OFF. One control input serves to facilitate the selection between the active and Standby modes. Another input permits the selection between the Standby and OFF modes. In the OFF mode, a maximum quiescent current of less than 10 µA flows through the system and in Standby mode quiescent current less than 30 µA.

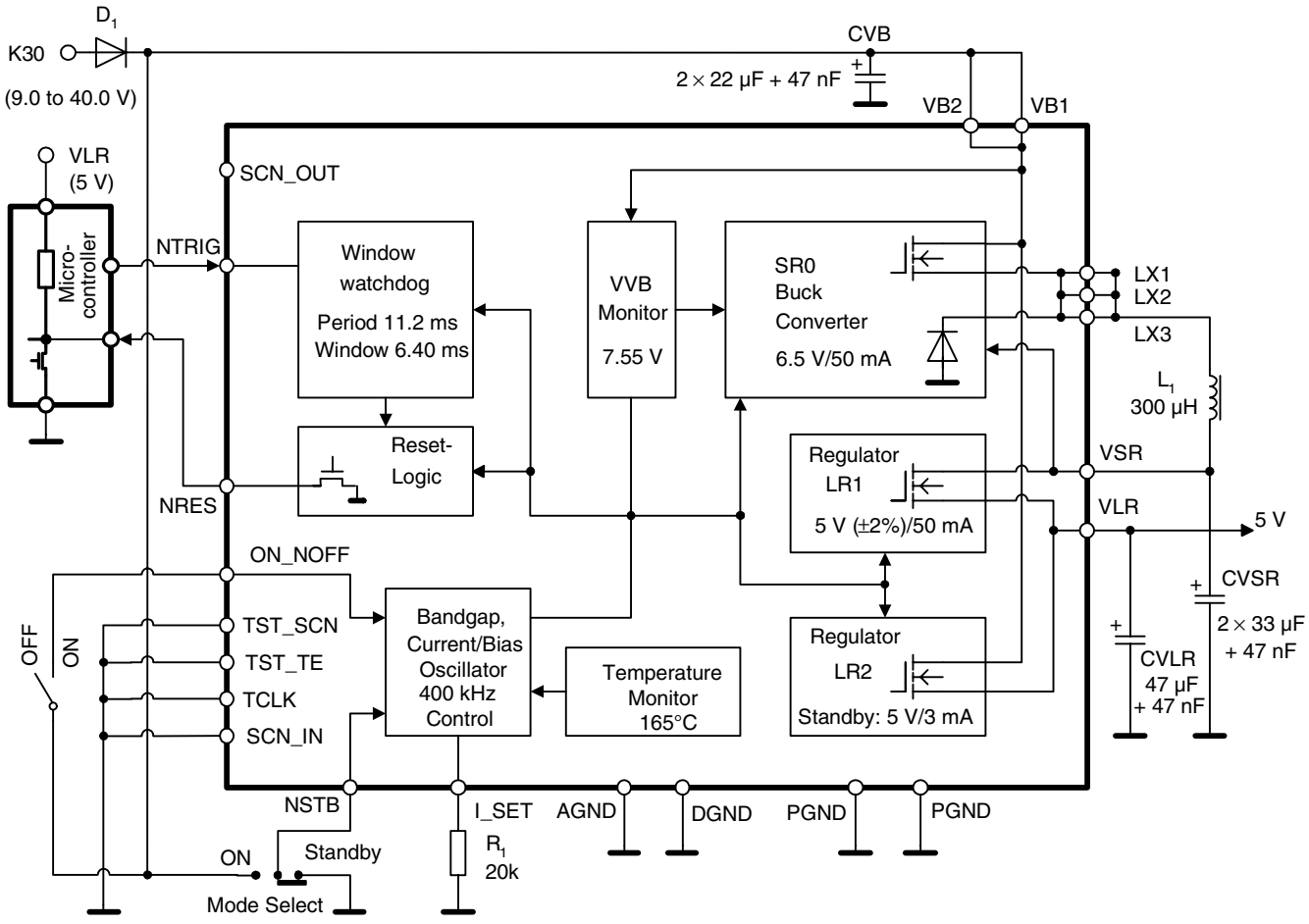
12/24 V System Power Supply IC

ATA6405

Preliminary

Rev. 4737A–AUTO–06/04

Block Diagram/Application Circuit

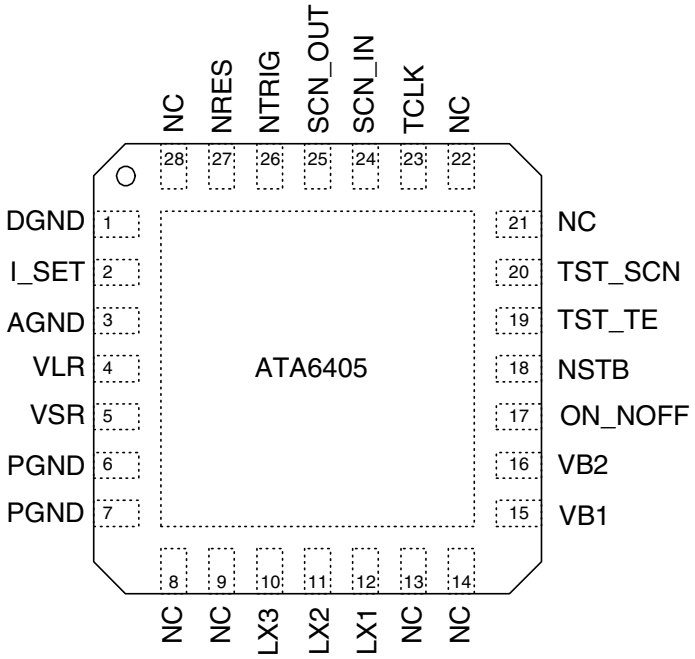


Application Notes

1. It is strongly recommended to connect the blocking capacitors at VB1, VB2, VSR, VLR as closely as possible to the pins PGND, AGND.
2. It is strongly recommended to use capacitors with very low ESR.
3. The 47 nF capacitors are of ceramic types.
4. It is strongly recommended to connect the resistor R_1 as closely as possible to the pins I_SET and AGND.

Pin Configuration

Figure 1. Pinning QFN28 7x7 (pitch 0.8 mm)



Pin Description

Pin	Symbol	Function	Remarks
1	DGND	Grounding connection for digital stages	
2	I_SET	Connection for reference resistance	
3	AGND	Grounding connection for analog stages	
4	VLR	Output from LR1 Output from LR2	5 V/50 mA (ON_mode) 5 V/3 mA (Standby mode)
5	VSR	Feedback input of switching regulator and input of linear regulator LR1	
6	PGND	Grounding connection for power stages	
7	PGND	Grounding connection for power stages	
8	NC	Not connected	
9	NC	Not connected	
10	LX3	Switching output of switching regulator	
11	LX2	Switching output of switching regulator	
12	LX1	Switching output of switching regulator	
13	NC	Not connected	
14	NC	Not connected	
15	VB1	Voltage supply	
16	VB2	Voltage supply	
17	ON_NOFF	Input for selecting between ON and OFF or Standby mode	Connector to VB ⇒ ON mode LOW ⇒ OFF mode

Pin Description (Continued)

Pin	Symbol	Function	Remarks
18	NSTB	Input for selecting the OFF- or Standby mode	Connector to VB ⇒ OFF mode LOW ⇒Standby mode
19	TST_TE	Connections for test purposes	
20	TST_SCN	Connections for test purposes	
21	NC	Not connected	
22	NC	Not connected	
23	TCLK	Connections for test purposes	
24	SCN_IN	Connections for test purposes	
25	SCN_OUT	Connections for test purposes	
26	NTRIG	Trigger input for watchdog	Low - active, slope L/H
27	NRES	Reset output	Low - active
28	NC	Not connected	

Functional Description

The system voltage supply IC described here is designed for the 12/24V board voltage supply systems in motor vehicles. To minimize power losses, provision is made for a step-down type switching regulator to transform the battery voltage to the lowest possible initial value so as to supply the internal linear regulator with 5V. The linear regulator is equipped with monitors controlling different voltages, currents and the temperature. Accuracy of the regulators and monitors is provided by a bandgap acting in conjunction with an external reference resistance on pin I_SET. In addition to the voltage regulators, the system is further enhanced by a monitoring and control feature for microcontrollers designed in the form of a window watchdog geared to the reset logic system. A switching input is provided for switching the system on and off. Another input controlling the switched-off state serves to determine whether the system is to be completely switched off (OFF mode) or whether the Standby mode is to be enabled, in which case minimum supply of the microcontroller on pin VLR is maintained.

General Features

This product is designed for continuous operation on terminal 30 of a motor vehicle board supply system. Accordingly, attention has been paid to ensuring minimum current consumption in the OFF mode. The rise in supply voltage when connected to terminal 30 or when connecting up a battery must not be allowed to fall below 2V/ms. This applies to the process of assembly and not to normal operation where minimum supply voltage is ensured even when power fades occurs during the starting phase.

Operating Modes: ON/OFF/Standby

These operating modes can be set via the ON_NOFF and NSTB pins. Connecting pin ON_NOFF to pin VB results in the ON mode being set irrespective of the NSTB pin. If the ON_NOFF pin remains unconnected, either the OFF mode or Standby mode will be set depending on the NSTB pin. Connection of NSTB to VB results int the OFF mode being set. On the other hand, connecting the NSTB pin to ground potential will result in the Standby mode being set provided that the ON mode was previously enabled. The NSTB pin is designed for permanent wiring depending on the desired mode of functioning.

Operating Sequence

Whenever a voltage having a typically greater value than 7.55 V is applied to the VB pin, the switching regulator can be run up (after a brief initialization phase of approximately 100 µs) by switching from the OFF mode to the ON mode. As soon as transient build-up is just about to transpire, the LR1 linear regulator is automatically switched on, applying a typical output voltage of 5.6 V to the VSR pin.

As long as transient build-up has not yet taken place on the LR1 linear regulator, a reset will be put out on the NRES pin (reset for the microcontroller supplied by the linear regulator). As soon as the typical output voltage of 4.75 V has been exceeded on the VLR pin, the reset will terminate with a delay of approximately 10 ms. This period covers the transient build-up phase on the oscillator of the microcontroller.

In the event pin VLR falls below the typical limiting values, a reset will be put out. In the event of excess temperature occurring or if the supply voltage falls below the specified limiting value, both voltage regulators will be immobilized. This will also lead indirectly to the reset state, which will remain in force until pin VB voltage drops to approximately 2.5 V.

The further sequence of operations after termination of the ON mode unleashed by switching to ON_NOFF will depend on the wiring of the NSTB pin (also refer to the previous description). The switching regulator and linear regulator are switched off irrespective of the NSTB pin. If the Standby mode has been selected, the first linear regulator (LR1) will be substituted by a second linear regulator of lower power capacity, this being fed directly via the VB pin. For minimized current consumption all further functions will switched off. These are the internal supply, the oscillator with the related voltage monitoring controllers, the temperature controlling monitor and the watchdog. Enabling of the Standby mode is only possible after an ON-MODE phase. Initial application of the supply voltage will prove insufficient.

With the transfer from the Standby to the ON mode, activated by the switching pin ON_NOFF, the pin NRES remains high in the first time (with external resistor). Due to the functionality there is the same procedure as the one at the end of the generation of the reset output (LOW HIGH transmission at NRES). Also see section “RESET” and “Watchdog” on page 6.

Reset

The purpose of the reset function is to transform the microcontroller to be monitored into a predefined state. In order to achieve this, the NRES pin is drawn internally (or externally) on ground potential. In the OFF mode the reset signal is active permanently. After switching into the ON mode the reset signal remains for 10 ms, typically, after transient build-up of all voltage regulators.

Outputting of the reset in the ON mode may be triggered due to a variety of different reasons. In case of undervoltage at pin VLR the reset occurs immediately. The turn-off delay is typically 10 ms and starts with the end of the event. The activation of the watchdog generates a reset of 10 ms. Undervoltage at pin VB or overtemperature will switch off all voltage regulators and a reset is generated due to undervoltage at pin VLR. With the changeover from the ON mode to the Standby mode the reset is locked in any time. The reset is also locked with the return to the ON mode as long as all voltage regulators have finished the transient build-up.

Oscillator

The task of the oscillator is to provide system timing for the switching regulator as well as a timing basis for all counting and delay functions, including those of the watchdog system. It is designed in the form of an RC oscillator, the frequency of which is governed by the tolerances of integrated capacity and the properties of external resistance on pin I_SET. Temperature dependence is better than 300 ppm/°C subject to corresponding selection of external resistance. To minimize interference in the radio-broadcasting band, the typical frequency has been permanently set to 400 kHz.

Switching Regulator SR

From the variable supply voltage present on the VB pin, the SR switching regulator generates a typical output voltage of 6.5 V on the VSR pin. The latter acts as a feedback input for the switching regulator and also as an input for the LR1 linear regulator. Typical loading capacity is laid out for 50 mA. The current limitation is fixed at 100 mA. An external capacitor is needed to suppress transients and to ensure a normal input voltage for LR1. The ESR of the capacitor has to be considered due to the ripple. If the ripple is too high the voltage monitor at pin VSR will not release LR1.

The operating frequency is bled off from an integrated RC oscillator, whose frequency has been set at 400 kHz. This frequency serves to ensure minimum possible interference in the radio broadcasting bands. In this context, the slope rate on the circuit output has been selected in such a way that an optimum state is achieved between the efficiency factor and freedom from interference.

Linear Regulators LR1, LR2

The linear regulator LR1 provides a typical supply voltage of 5.0 V on the VLR pin. The input voltage is provided on the VSR pin (output of switching regulator). An internal current limiter is set to approximately 70 mA. This regulator is only enabled in the ON mode.

When changing from the ON mode to the Standby mode, linear regulator LR2 is enabled, which draws its input current directly from the VB pin, thus maintaining the typical output voltage of 5.0 V on the VLR pin up to a current of approximately 3 mA. The current limitation is fixed at 7 mA. An external capacitor needs to be added at pin VLR in accordance to the load of the microcontroller to avoid generating a reset of the voltage monitor controller.

Pin SCN OUT

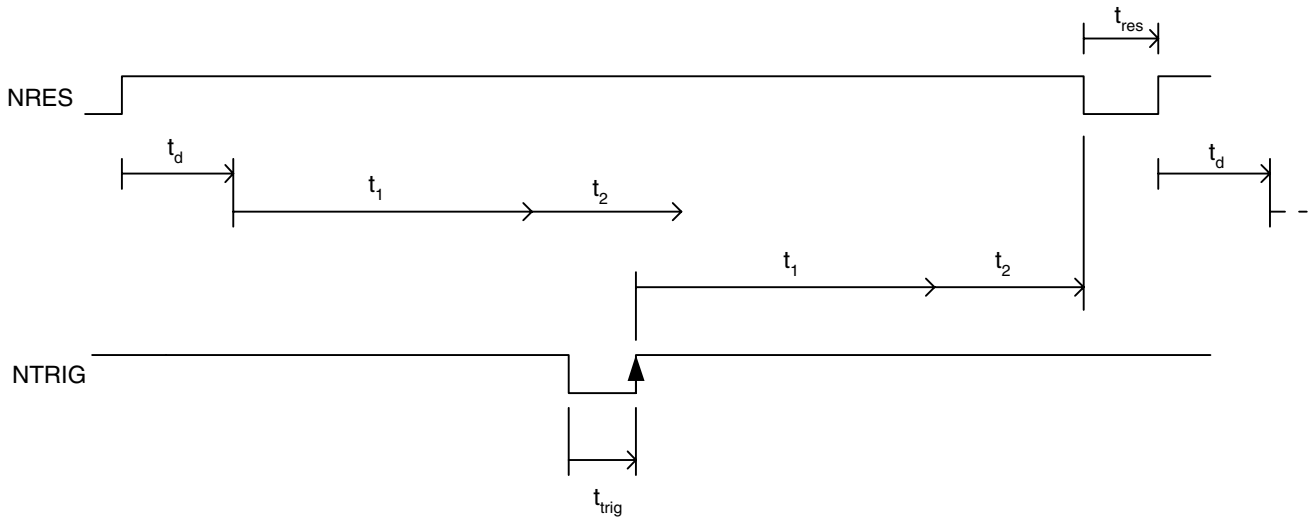
A high level in the ON mode at this pin indicates undervoltage detection at pin VB or overtemperature of the device.

Watchdog

The watchdog anticipates a triggering signal from the microcontroller at the NTRIG input within a recurrent time window. On the basis of this low-active (or alternatively high-active) signal, evaluation of the low slope (or high slope) takes place, however only if a minimum dwell time t_{trig} is exceeded. If no such triggering signal is received, output of a reset will take place. Alternatively, outputting of a reset may take place if t_{trig} exceeds a predefined maximum value. The timing basis of the watchdog is provided by the internal RC oscillator.

Detailed Description of the Watchdog Function

Figure 2. Watchdog Sequence



WD sequence (typically): t_1 = 8.0 ms t_2 = 6.4 ms

After completion of the reset function (low/high slope on NRES) a lead time t_d follows (e.g. for setups) of typically 40 µs before the actual watchdog sequence begins. Times t_1 and t_2 form a part of the watchdog sequence and assume a fixed relationship to one another. A triggering signal from the microcontroller is anticipated within the timeframe of t_2 (6.4 ms). Of decisive importance in this case is the low/high slope after the minimum dwell time t_{trig} of typically 40 µs. This slope serves to restart the watchdog sequence. Should the triggering signal fail to emerge, the NRES output will be drawn on ground potential applying the time duration t_{res} of typically 10 ms. A reset situation is likewise unleashed if the triggering signal emerges within the timeframe of t_1 (8 ms) or alternatively if t_{trig} exceeds the time of 100 µs.

An example of how the above time values are defined is given in the first variant. However, the time values can, on principle, be selected by the mask function. A 6-bit counter is available for t_{trig} and a 16-bit counter for t_d, t_1, t_2, t_{res}. In the same way, orientation of the trigger pulse (low- or high-active) is selectable by the mask function.

The original time basis is defaulted by the internal oscillator. The time basis T_{wd} for the watchdog is obtained by applying a division ratio of 1:4. All the times indicated above are multiples of T_{wd}.

Oscillator cycle duration: $T_{osc} = 1/f_{osc}$ = 1/400 kHz ±Tol. = 2.50 µs ±Tol.

Time basis for watchdog: $T_{wd} = 4 \times T_{osc}$ = 10 µs (typical)

The above time values and oscillator tolerances result in a typical triggering frequency based on T = 10.56 ms ±0.94 ms.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_{vb}	-0.35	40	V
Output voltage LX	V_{out}	-1.0	V_{vb} + 0.35	V
Input voltage regulator LR	V_{in}	-0.35	8 + 0.35	V
Output voltage regulator LR	V_{out}	-0.35	V_{sr} + 0.35	V
Output voltage pin NRES	V_{out}	-0.35	V_{vlr} + 0.35	V
Output current pin I_SET	I_{out}		1.0	mA
Input voltage NTRIG	V_{in}	-0.35	V_{vlr} + 0.35	V
Input voltage ON_NOFF, NSTB	V_{in}	-0.35	V_{vb} + 0.35	V
Junction temperature	T_j	-40	150	°C
Storage temperature	T_{stg}	-55	150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction to case[1]	R_{thJC}	10	K/W
Junction to ambient	R_{thJA}	130	K/W

Note: 1. Chip soldered on metal plate

Operating Range

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_{vb}	8	40	V
Ambient Temperature	T_{amb}	-40	+125	°C

Electrical Characteristics

V_{vb} = 8 V to 40 V; T_{amb} = -40°C to 125°C; reference point is pin AGND.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply**								
1.1	Input current	ON mode No load on SR, LR	VB	I_{vb}			10	mA	A
1.2	Input current	OFF mode	VB	I_{vb}			10	µA	A
1.3	Input current	Standby mode	VB	I_{vb}			30	µA	A
1.4	Dissipated power	ON mode		P			0.5	W	D
2	**Voltage Regulator SR**								
2.1	Output voltage	I_{VSR} = 0 to 50 mA	VSR	V_{SR}	6.1	6.5	7.1	V	A
3	**Voltage Regulator LR1**								
3.1	Output voltage 5V	I_{VLR} = 0 to 50 mA	VLR	V_{LR1}	4.90	5V	5.10	V	A
4	**Voltage Regulator LR2**								
4.1	Output voltage 5V	I_{VLR} = 0 to 3 mA	VLR	V_{LR2}	4.50	5V	5.50	V	A
5	**Voltage Monitor VB**								
5.1	Enable threshold voltage		VB	V_{th}	7.4	7.55	7.7	V	A
5.2	Hysteresis		VB	V_{hy}		0.1		V	A
6	**Voltage Monitor VSR**								
6.1	Enable threshold voltage		VSR	V_{th}	5.48	5.6	5.72	V	A
6.2	Hysteresis		VSR	V_{hy}		0.1		V	A
7	**Voltage Monitor VLR**								
7.1	Enable threshold voltage		VLR	V_{th}	4.65	4.75	4.85	V	A
7.2	Hysteresis		VLR	V_{hy}		0.1		V	A
8	**Temperature Monitor**								
8.1	Disable threshold			T_{th}		165		°C	C
8.2	Hysteresis			T_{hy}		15		°C	C
9	**Logic**								
9.1	High input voltage		NTRIG	V_{ih}	4.0			V	A
9.2	Low input voltage		NTRIG	V_{il}			0.4	V	A
9.3	Input current	V_{in} = 5 V	NTRIG	I_{in}			1.0	µA	A
9.4	Input current	V_{in} = 0 V	NTRIG	I_{in}	-1.0			µA	A
9.5	High input voltage		ON_NOFF, NSTB	V_{ih}	7.0			V	A
9.6	Low input voltage		ON_NOFF, NSTB	V_{il}			0.4	V	A
9.7	Input current	V_{in} = 40 V	ON_NOFF	I_{in}	197		983	µA	A
9.8	Input current	V_{in} = 4 V	ON_NOFF	I_{in}	3.1		15	µA	A
9.9	Input current	V_{in} = 0.4 V	ON_NOFF	I_{in}	0.5		1	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{vb} = 8 V to 40 V; T_{amb} = -40°C to 125°C; reference point is pin AGND.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.10	Input current	V_{in} = 40 V	NSTB	I_{in}	0.5		1	µA	A
9.11	Input current	V_{in} = 4 V	NSTB	I_{in}	0.5		1	µA	A
9.12	Input current	V_{in} = 0.4 V	NSTB	I_{in}	-2		-1	µA	A
9.13	Low output voltage	I_{out} = -1 mA	NRES	V_{ol}			0.4	V	A
9.14	High output voltage	I_{out} = -5 mA	SCN_OUT	V_{oh}	4.6			V	A
9.15	Low output voltage	I_{out} = 5 mA	SCN_OUT	V_{ol}			0.4	V	A
10	**Oscillator/Watchdog**								
10.1	Oscillator period time		LX	T_{osc}	2.0	2.50	3.0	µs	A
10.2	WD time base			T_{wd}	8.0	10.0	12.0	µs	D
10.3	WD pre-period			t_d		4		T_{wd}	D
10.4	WD disable time			t_1		800		T_{wd}	A
10.5	WD enable time			t_2		640		T_{wd}	A
10.6	Reset-out time			t_{res}		1000		T_{wd}	A
10.7	Trigger pulse		NTRIG	t_{trig}	4		10	T_{wd}	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Noise and Surge Immunity

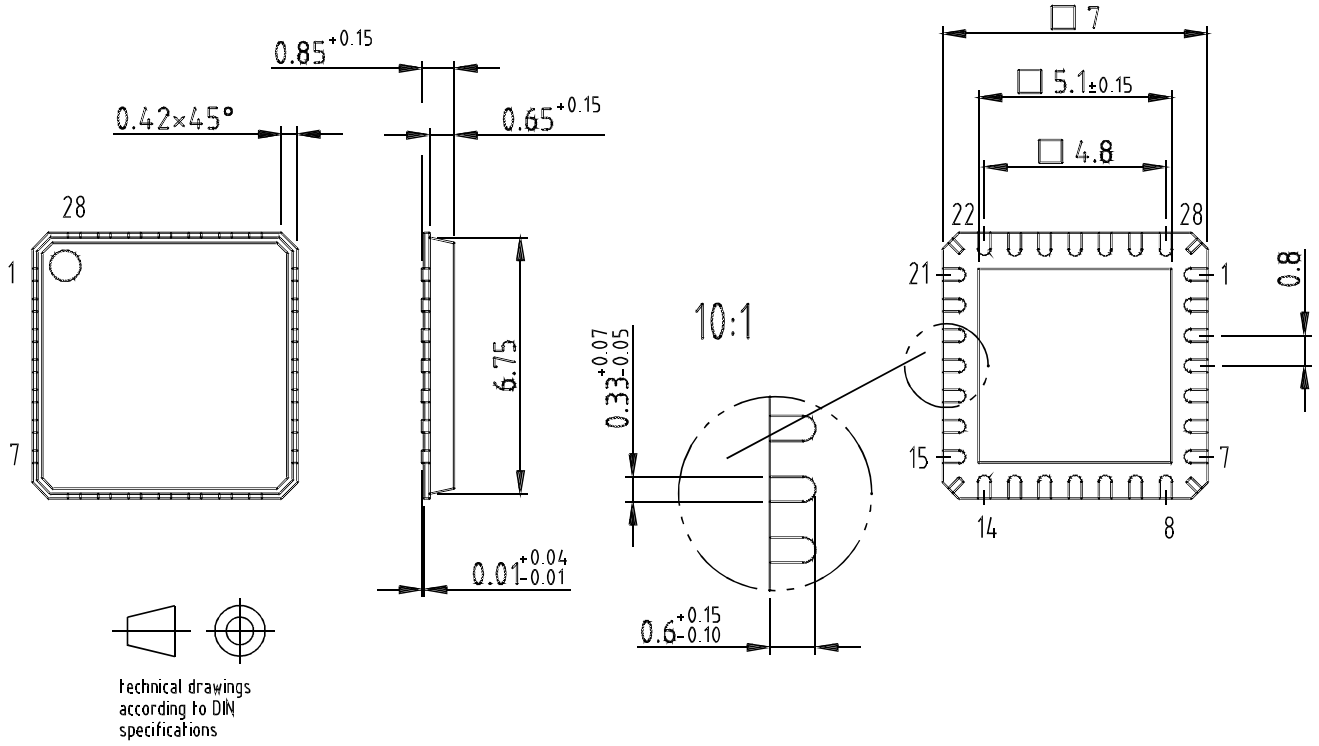
Parameter	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4
Interference suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model)	MIL-STD-883D Method 3015.7	1.5 kV
ESD (Machine Model)	EOS/ESD – S 5.2	200 V

Ordering Information

Extended Type Number	Package	Remarks
ATA6405-PKQ	QFN28	Voltage Regulator

Package Information

Package: QFN 28 - 7x7
Exposed pad 5.1x5.1
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm



Drawing-No.: 6.543-5073.01-4
Issue: 3; 24.01.03

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