

8bit 12ch D/A converter

BH2221FV

BH2221FV is an 8bit D/A converter for electronic adjustment. The 12-channel DC output voltage can be independently controlled by three-wire serial interface from micro-controller. The D/A converter can generate without loss by Rail-to-Rail output within the setting voltage. The built-in power ON reset circuit keeps the output state Low after the power is ON and prevents the unstable output state.

●Applications

The voltage adjustment for DVC, DSC etc.

●Features

- 1) 8bit 12-channel D/A converters adopting R-2R system.
- 2) The full scale output voltage range : 2.7V~5.5V.
- 3) 3-wire 12-bit serial interface.
- 4) POWER ON RESET circuit.
- 5) SSOP-B20 package.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	-0.3~+7.0	V
Maximum output voltage	V _{IN}	-0.3~V _{CC}	V
Storage temperature	T _{stg}	-55~+125	°C
Power dissipation	P _d	400 *	mW

*Reduced by 4mW for each increase in Ta of 1°C over 25°C.

©This product is not designed for protection against radioactive rays.

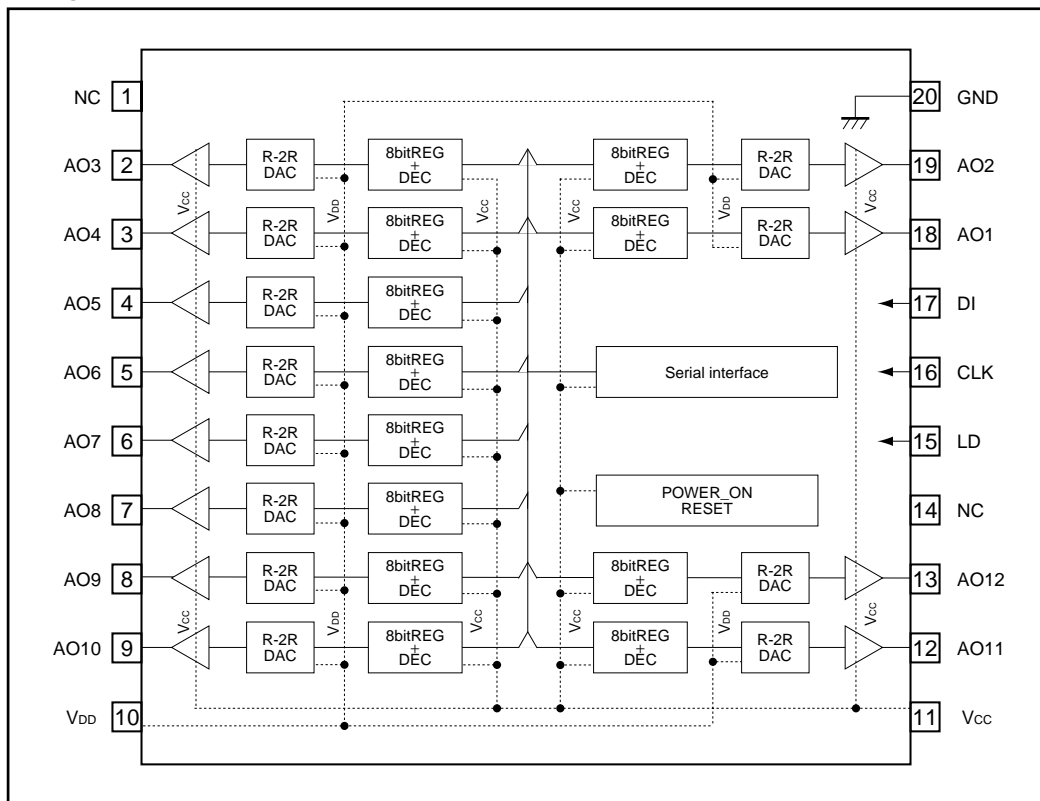
●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
V _{CC} supply voltage	V _{CC}	2.7	–	5.5	V
V _{DD} supply voltage	V _{DD}	2.7	–	V _{CC}	V
Analog output source current	I _{OL}	–	–	1.0	mA
Analog output sink current	I _{OH}	–	–	1.0	mA
Operating temperature range	T _{opr}	-20	–	85	°C
Clock frequency	FSCLK	–	1.0	–	MHz
Limit load capacitance	CL	–	–	0.1	μF

Please set to V_{CC} ≥ V_{DD}.

Standard ICs

●Block diagram



●Pin descriptions

Pin No.	Pin name	In / Out	Functions
1	NC	–	No connected
2	AO3	OUT	Analog output pins
3	AO4	OUT	
4	AO5	OUT	
5	AO6	OUT	
6	AO7	OUT	
7	AO8	OUT	
8	AO9	OUT	
9	AO10	OUT	
10	V _{DD}	–	Power supply pin
11	V _{CC}	–	Power supply pin
12	AO11	OUT	Analog output pins
13	AO12	OUT	
14	NC	–	No connected
15	LD	IN	Serial Load input pin
16	CLK	IN	Serial Clock input pin
17	DI	IN	Serial Data input pin
18	AO1	OUT	Analog output pins
19	AO2	OUT	
20	GND	–	Common GND pin

Standard ICs

●Electrical characteristics (unless otherwise noted, Ta=25°C, Vcc=3.0V, VDD=3.0V, RL=OPEN, CL=0pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Operating current> (80H set)						
Vcc system	Icc	–	0.6	1.5	mA	CLK=1MHz
VDD system	IDD	–	1.0	2.0	mA	
<Logic interface>						
Input low voltage	VIL	GND	–	0.2Vcc	V	
Input high voltage	VIH	0.8Vcc	–	Vcc	V	
Input low current	IIL	–	–	10	μA	
Input high current	IIH	–	–	10	μA	
<Buffer amplifier>						
Minimum output voltage	ZS1	GND	–	0.1	V	00H set IOH=0.0mA
	ZS2	GND	–	0.2	V	00H set IOH=0.5mA
	ZS3	GND	–	0.3	V	00H set IOH=1.0mA
Maximum output voltage	FS1	Vcc –0.1	–	Vcc	V	FFH set IOL=0.0mA
	FS2	Vcc –0.2	–	Vcc	V	FFH set IOL=0.5mA
	FS3	Vcc –0.3	–	Vcc	V	FFH set IOL=1.0mA
<DAC accuracy>						
Resolution	RES	–	8	–	bit	
Differential nonlinearity error	DNL	–1.0	–	1.0	LSB	Input code 02H~FDH
Nonlinearity error	INL	–1.5	–	1.5	LSB	Input code 02H~FDH

●Circuit operation

(1) Power on reset

This LSI has a power on reset circuit that sets an analog output to low level in Vcc power stand-up.

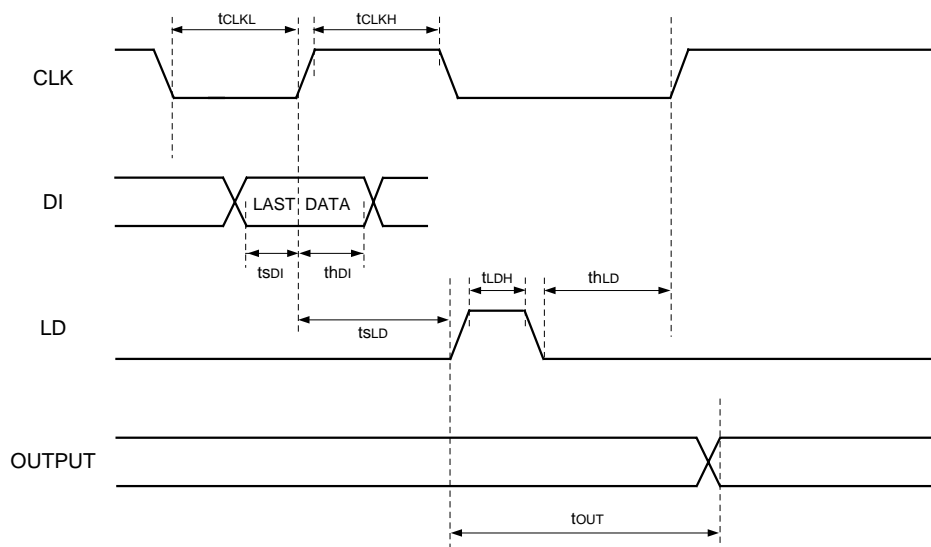
Please be sure that the time constant meets below condition, because the output is undefined when Vcc power stand up too rapidly.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Vcc supply voltage rise time	trVcc	10	–	–	ms	Vcc=0→2.7V
Power on reset voltage	VPOR	–	1.9	–	V	

Standard ICs

(2) Conditions of operating timing (unless otherwise noted, $T_a=25^\circ\text{C}$, $V_{CC}=3.0\text{V}$, $V_{DD}=3.0\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK L level pulse width	tCLKL	200	–	–	ns	
CLK H level pulse width	tCLKH	200	–	–	ns	
DI setup time	tsDI	30	–	–	ns	
DI hold time	thDI	60	–	–	ns	
LD setup time	tsLD	200	–	–	ns	
LD hold time	thLD	100	–	–	ns	
LD "H" level pulse width	tLDH	100	–	–	ns	
Analog output delay time	tOUT	–	–	300	μs	$C_L=50\text{pF}$, $R_L=10\text{k}\Omega$



Standard ICs

(3) Command sending

Control command is 3wire 12bit serial interface. (MSB first)

Data is taken in with the rise edge of the CLK and output data is fixed in the LD high section.

Data is maintained in the LD low section.

LSB (LAST)

MSB (FIRST)

Data set								Channel select			
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

•Data set

D0	D1	D2	D3	D4	D5	D6	D7	Analog output voltage level
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(Vcc-GND) / 256×1
0	1	0	0	0	0	0	0	(Vcc-GND) / 256×2
1	1	0	0	0	0	0	0	(Vcc-GND) / 256×3
0	0	1	0	0	0	0	0	(Vcc-GND) / 256×4
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(Vcc-GND) / 256×254
1	1	1	1	1	1	1	1	(Vcc-GND) / 256×255

•Channel select

D8	D9	D10	D11	Adress select
0	0	0	0	Don't Care
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7
1	0	0	0	AO8
1	0	0	1	AO9
1	0	1	0	AO10
1	0	1	1	AO11
1	1	0	0	AO12
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

Standard ICs

●Operation notes

(1) Regarding to the DNL & INL

This item is guaranteed under below condition.

Input code 02H~FDH

(2) Regarding to the setting of the each voltage

Set the V_{CC} , V_{DD} to become the following condition.

When not satisfied, unnecessary current flows or D/A conversion is not correct.

$$V_{CC} \geq V_{DD}$$

And the minimum output voltage of this LSI is fixed to the GND level.

(3) Regarding to the power on reset function

This function operates detecting the voltage level of the V_{CC} .

So, if the voltage level of the V_{CC} become less than power on reset voltage when working, it is a possibility that the outputs become reset condition.

●External dimensions (Units : mm)

