agere systems

Preliminary Data Sheet
April 2004

TruePHY™ ET1011
Gigabit Ethernet Transceiver

Features

- 10Base-T, 100Base-TX, and 1000Base-T gigabit Ethernet transceiver:
  - — 0.13 µm process
  - — 128-pin TQFP:
    - ❑ RGMII, GMII, MII, RTBI, and TBI interfaces to MAC or switch
  - — 68-pin MLCC:
    - ❑ RGMII and RTBI interfaces to MAC or switch
- Low power consumption:
  - — Less than 750 mW in 1000Base-T mode
  - — Advanced power management
  - — ACPI compliant wake-on-LAN support
- Oversampling architecture to improve signal integrity and SNR
- Optimized, extended performance echo and NEXT filters
- All digital baseline wander correction
- Digital PGA control
- On-chip diagnostic support
- Automatic speed negotiation
- Automatic speed downshift
- Single supply 3.3 V or 2.5 V operation:
  - — On-chip regulator controllers
  - — 3.3 V or 2.5 V digital I/O
  - — 1.0 V core power supplies
  - — 1.8 V or 2.5 V for transformer center tap
- JTAG

Introduction

Agere Systems ET1011 is a gigabit Ethernet transceiver fabricated on a single CMOS chip. Packaged in either a 128-pin TQFP or a 68-pin MLCC, the ET1011 is built on 0.13 µm technology for low power consumption and application in server and desktop NIC cards. It features single power supply operation using on-chip regulator controllers. The 10/100/1000Base-T device is fully compliant with *IEEE*® 802.3, 802.3u, and 802.3ab standards.

The ET1011 uses an oversampling architecture to gather more signal energy from the communication channel than possible with traditional architectures. The additional signal energy or analog complexity transfers into the digital domain. The result is an analog front end that delivers robust operation, reduced cost, and lower power consumption than traditional architectures.

Using oversampling has allowed for the implementation of a fractionally spaced equalizer, which provides better equalization and has greater immunity to timing jitter, resulting in better signal-to-noise ratio (SNR) and thus improved BER. In addition, advanced timing algorithms are used to enable operation over a wider range of cabling plants.

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Functional Description

Agere Systems ET1011 is a gigabit Ethernet transceiver that simultaneously transmits and receives on each of the four UTP pairs of category 5 cable (signal dimensions or channels A, B, C, and D) at 125 Msymbols/s using five-level pulse amplitude modulation (PAM). Figure 1 is a block diagram of its basic configuration.

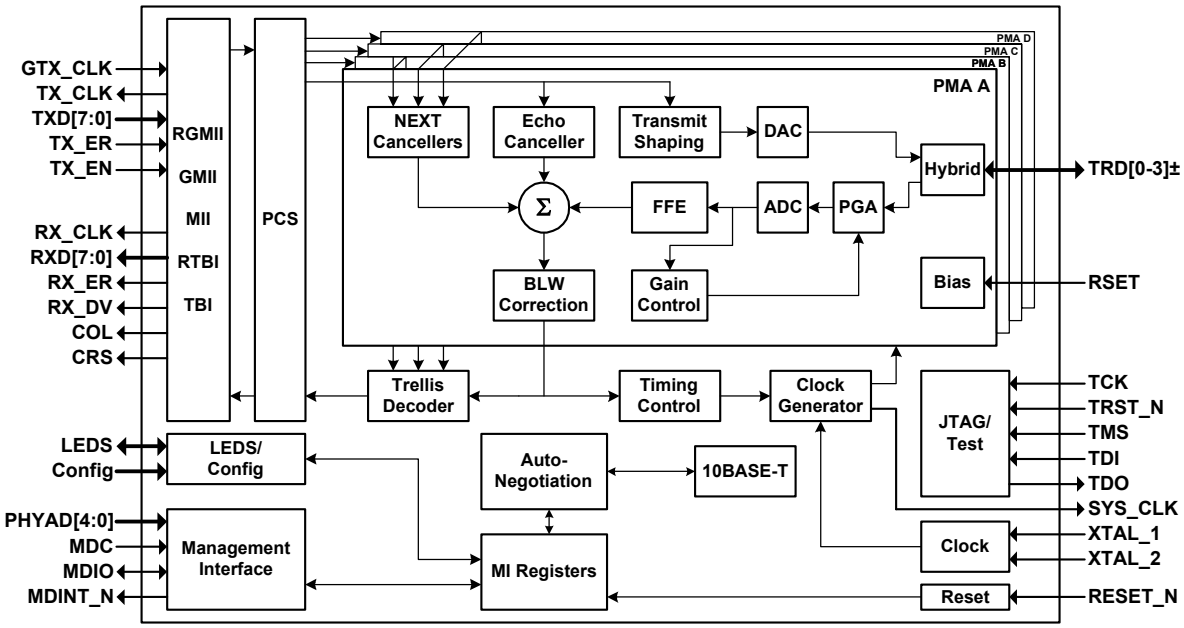

Figure 1. ET1011 Block Diagram

Oversampling Architecture

The ET1011 architecture uses oversampling techniques to sample at two times the symbol rate. A fractionally spaced feed forward equalizer (FFE) adapts to remove intersymbol interference (ISI) and to shape the spectrum of the received signal to maximize the (SNR) at the trellis decoder input. The FFE equalizes the channel to a fixed target response. Oversampling enables the use of a fractionally spaced equalizer (FSE) structure for the FFE, resulting in symbol rate clocking for both the FFE and the rest of the receiver. This provides robust operation and substantial power savings.

Automatic Speed Downshift

Automatic speed downshift is an enhanced feature of autonegotiation that allows the ET1011 to:

- Fallback in speed, based on cabling conditions or link partner abilities.
- Operate over CAT-3 cabling (in 10Base-T mode).
- Operate over two-pair CAT-5 cabling (in 100Base-TX mode).

For speed fallback, the ET1011 first tries to autonegotiate by advertising 1000Base-T capability. After a number of failed attempts to bring up the link, the ET1011 falls back to advertising 100Base-TX and restarts the autonegotiation process. This process continues through all speeds down to 10Base-T. At this point, there are no lower speeds to try and so the host enables all technologies and starts again.

PHY configuration register, address 22, bits 11and 10 enable automatic speed downshift and specifies if fallback to 10Base-T is allowed. PHY control register, address 23, bits 11and 12 specify the number of failed attempts before downshift (programmable to 1, 2, 3, or 4 attempts).

Functional Description (continued)

Transmit Functions

1000Base-T Encoder

In 1000Base-T mode, the ET1011 translates 8-bit data from the MAC interfaces into a code group of four quinary symbols that are then transmitted by the PMA as 4D five-level PAM signals over the four pairs of CAT-5 cable.

100Base-TX Encoder

In 100Base-TX mode, 4-bit data from the media independent interface (MII) is 4B/5B encoded to output 5-bit serial data at 125 MHz. The bit stream is sent to a scrambler, and then encoded to a three-level MLT3 sequence that is then transmitted by the PMA.

10Base-T Encoder

In 10Base-T mode, the ET1011 transmits and receives Manchester-encoded data.

Receive Functions

Decoder 1000Base-T

In 1000Base-T mode, the PMA recovers the 4D PAM signals after compensating for the cabling conditions. The resulting code group is decoded to 8-bit data. Data stream delimiters are translated appropriately, and the data is output to the receive data pins of the MAC interfaces. The GMII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 100Base-TX

In 100Base-TX mode, the PMA recovers the three-level MLT3 sequence that is descrambled and 5B/4B decoded to 4-bit data. This is output to the MII receive data pins after data stream delimiters have been translated appropriately. The MII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 10Base-T

In 10Base-T mode, the ET1011 decodes the Manchester-encoded received signal.

Hybrid

The hybrid subtracts the transmitted signal from the input signal allowing full-duplex operation on each of the twisted-pair cables.

Programmable Gain Amplifier (PGA)

The PGA operates on the received signal in the analog domain prior to the analog-to-digital converter (ADC). The gain control module monitors the signal at the output of the ADC in the digital domain to control the PGA. It implements a gain that maximizes the signal at the ADC while ensuring that no hard clipping occurs.

Clock Generator

A clock generator circuit uses the 25 MHz input clock signal and a phase-locked loop (PLL) circuit to generate all the required internal analog and digital clocks. A 125 MHz system clock is also generated and is available as an output clock.

Analog-to-Digital Converter

The ADC operates at 250 MHz oversampling at twice the symbol rate in 1000Base-T and 100Base-TX. This enables innovative timing recovery and fractional skew correction and has allowed transfer of analog complexity to the digital domain.

Timing Recovery/Generation

The timing recovery and generator block creates transmit and receive clocks for all modes of operation. In transmit mode, the 10Base-T and 100Base-TX modes use the 25 MHz clock input. While in receive mode, the input clock is locked to the receive data stream. 1000Base-T is implemented using a master-slave timing scheme, where the master transmit and receive are locked to the 25 MHz clock input, and the slave acquires timing information from the receive data stream. Timing recovery is accomplished by first acquiring lock on one channel and then making use of the constant phase relationship between channels to lock on the other pairs, resulting in a simplified PLL architecture. Timing shifts due to changing environmental conditions are tracked by the ET1011.

Functional Description (continued)

Adaptive Fractionally Spaced Equalizer

The ET1011's unique oversampling architecture employs an FSE in place of the traditional FFE structure. This results in robust equalization of the communications channel, which translates to superior bit error rate (BER) performance over the widest variety of worst-case cabling scenarios. The all-digital equalizer automatically adapts to changing conditions.

Echo and Crosstalk Cancellers

Since the four twisted pairs are bundled together and not insulated from each other in Gigabit Ethernet, each of the transmitted signals is coupled onto the three other cables and is seen at the receiver as near-end crosstalk (NEXT). A hybrid circuit is used to transmit and receive simultaneously on each pair. If the transmitter is not perfectly matched to the line, a signal component will be reflected back as an echo. Reflections can also occur at other connectors or cable imperfections. The ET1011 cancels echo and NEXT by subtracting an estimate of these signals from the equalizer output.

Baseline Wander Correction

A known issue for 1000Base-T and 100Base-TX is that the transformer attenuates at low frequencies. As a result, when a large number of symbols of the same sign are transmitted consecutively, the signal at the receiver gradually dies away. This effect is called baseline wander. By employing a circuit that continuously monitors and compensates for this effect, the probability of encountering a receive symbol error is reduced.

Autonegotiation

Autonegotiation is implemented in accordance with *IEEE* 802.3. The device supports 10Base-T, 100Base-TX, and 1000Base-T and can autonegotiate between them in either half- or full-duplex mode. It can also parallel detect 10Base-T or 100Base-TX. If autonegotiation is disabled, a 10Base-T or 100Base-TX link can be manually selected via the *IEEE* MII registers.

Pair Skew Correction

In gigabit Ethernet, pair skew (timing differences between pairs of cable) can result from differences in length or manufacturing variations between the four individual twisted-pair cables. The ET1011 automatically corrects for both integer and fractional symbol timing differences between pairs.

Automatic MDI Crossover

During autonegotiation, the ET1011 automatically detects and sets the required MDI configuration so that the remote transmitter is connected to the local receiver and vice versa. This eliminates the need for crossover cables or crosswired (MDIX) ports. If the remote device also implements automatic MDI crossover, and/or the crossover is implemented in the cable, the crossover algorithm ensures that only one element implements the required crossover.

Polarity Inversion Correction

In addition to automatic MDI crossover that is necessary for autonegotiation, 10Base-T, and 100Base-TX operation, the ET1011 automatically corrects crossover of the additional two pairs used in 1000Base-T. Polarity inversion on all pairs is also corrected. Both of these effects may arise if the cabling has been incorrectly wired.

Carrier Sense (128-pin TQFP only)

The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011 whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is nonidle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.

Functional Description (continued)

Link Monitor

1000Base-T

Once 1000Base-T is autonegotiated and the link is established, both link partners continuously monitor their local receiver status. If the master device determines a problem with its receiver, it signals the slave and both devices cease transmitting data but transmit IDLE. If the master retrains its receiver within 750 ms, then normal operation recommences. Otherwise, both devices restart autonegotiation.

If the slave device determines a problem with its receiver, it ceases transmitting and expects the master to transmit the IDLE sequence. If the slave retrains its receiver within 350 ms, normal operation recommences when the master signals that its receiver is ready. If either receiver fails to reacquire, then autonegotiation is restarted.

100Base-TX

In 100Base-TX mode, the ET1011 monitors the link and determines the link quality based on signal energy, mean square error and scrambler lock. If the link quality is deemed insufficient, transmit and receive data are disabled. If the link had been autonegotiated then control is handed back to autonegotiation. If the link had been manually set, the 100Base-TX receiver is retrained, and the transmitter is set to transmit idle. Once the link quality has been recovered, data transmit and receive are enabled.

10Base-T

In 10Base-T mode, the ET1011 monitors the link and determines the link quality based on the presence of valid link pulses. If the link is deemed to have failed and the link had been autonegotiated, then control is handed back to autonegotiation. If the link had been manually set, the ET1011 continues to try to reestablish the link.

Functional Description (continued)

Loopback Mode

Enabling loopback mode allows in-circuit testing of the ET1011's digital and analog data path.

The ET1011 provides several options for loopback that test and verify various functional blocks within the PHY. These are digital loopback and analog loopback. Figure 2 is a block diagram that shows the PHY loopback functionality.

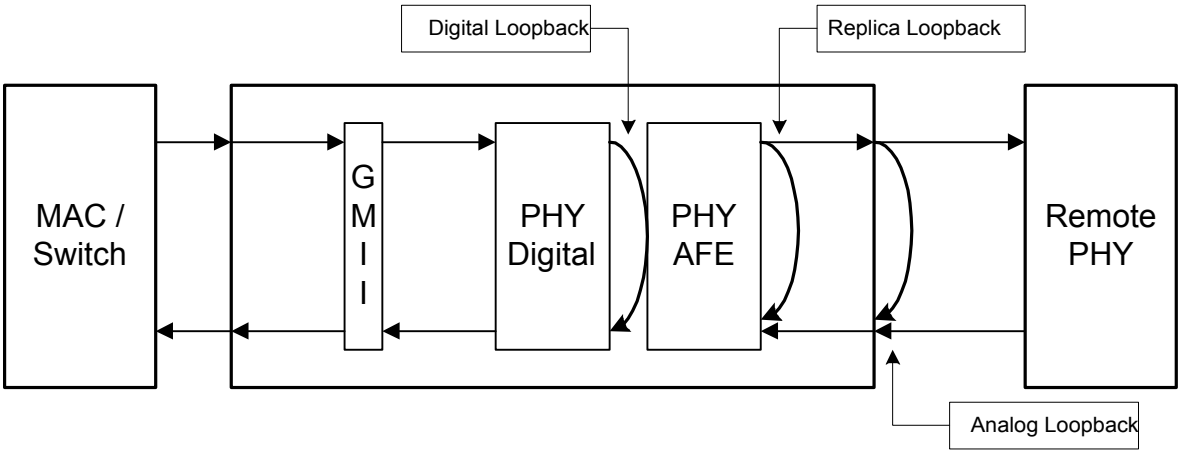

Figure 2. Loopback Functionality

The loopback mode is selected by setting the respective bit in the PHY loopback control register (MII register address 19, bits 9:15). The default loopback mode is digital MII loopback. Loopback is enabled by writing to the PHY control register, address 0, bit 14.

Functional Description (continued)

Digital Loopback

Digital loopback provides the ability to loop the transmitted data back to the receiver at various internal points between the MAC interface and the analog front end (AFE) circuitry. The point at which the data is looped back is selected using the loopback control register (address 19) with the following options being available: MII, PCS, PMD and all digital. Selecting the MII option gives a simple loopback with minimal latency where the data is looped back directly at the media-independent interface. This loopback is currently set as the default, but it should be noted that it only exercises a small percentage of the PHY circuitry. When the all digital option is selected, the transmitted data is looped back at the interface between the digital and the analog circuitry. thereby exercising a high percentage of the digital logic. The PCS and PMD options represent intermediate points between the two extremes. Figure 3 shows a block diagram of digital loopback.

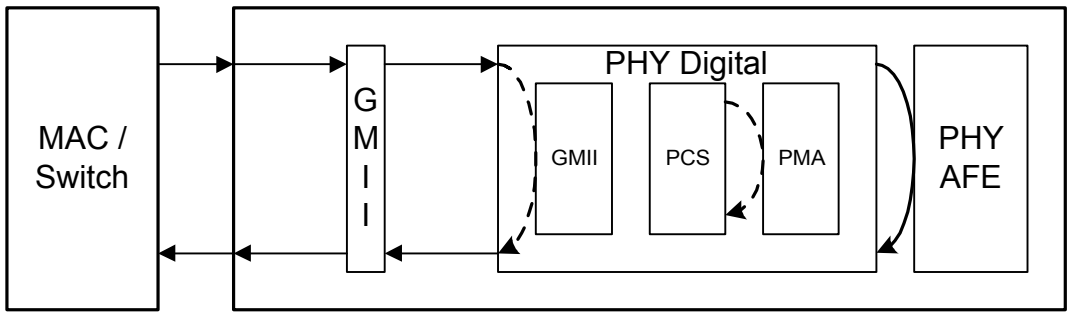

Figure 3. Digital Loopback

Functional Description (continued)

Analog Loopback

Analog loopback provides the ability to loop the transmitted signal back to the receiver within the AFE. The point at which the signal is looped back is selected using the loopback control register with the following options being provided: replica and line driver.

Selecting the replica option causes the transmitted signal to be looped back through the replica generation circuitry of the on-chip hybrid, thereby allowing most of the digital and analog circuitry to be exercised. This loopback mode may be used even when the device is connected to a network because nothing is transmitted to or received from the MDI in this case.

The most thorough loopback test available without the cooperation of a link partner is provided by selecting the line driver option where the PHY transmits to and receives from the MDI. However, in general, this loopback may not be used when the device is connected to a network because it could cause an unanticipated response from the link partner. Figure 4 shows a block diagram of replica analog loopback and Figure 5 shows a block diagram of line driver analog loopback.

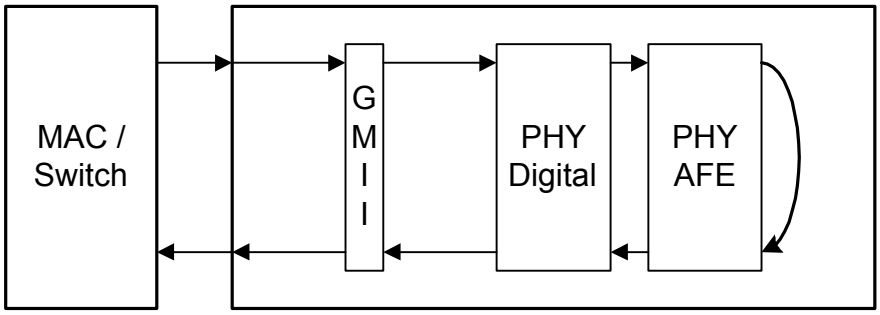

Figure 4. Replica Analog Loopback

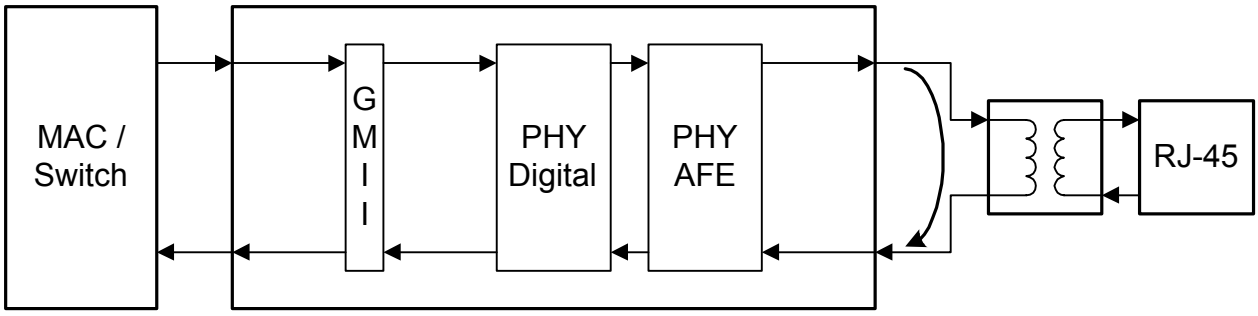

Figure 5. Line Driver Analog Loopback

Functional Description (continued)

LEDs

Seven status LEDs are provided. These can be used to indicate speed of operation, duplex mode, link status, etc. There is a very high degree of programmability allowed. Hence, the LEDs can be programmed to different status functions from their default value, or they can be controlled directly from the MII register interface. The LED signal pins can also be used for general-purpose I/O if not needed for LED indication.

Note: The 68-pin MLCC has only two LEDs. Both can be programmed through MII register 28 to provide all speed indications as well as link and activity indications.

Resetting the ET1011

The ET1011 provides the ability to reset the device by hardware (pin RESET_N) or via software through the management interface. A hardware reset is accomplished by driving the active-low pin RESET_N to 0 volts for a minimum of 1 μs. The configuration pins and the physical address configuration are read during a hardware reset.

A software reset is accomplished by setting bit 15 of the control register (MII register address 0 bit 15). The configuration pins and the physical address configuration are not read during software reset.

Low-Power Modes

The ET1011 supports a number of powerdown modes.

Hardware Powerdown Mode

Hardware powerdown is entered when the COMA signal is driven high. In hardware powerdown, all PHY functions (analog and digital) are disabled. During hardware powerdown, SYS_CLK is not available and the MII registers are not accessible.

At exit from hardware powerdown, the ET1011 does the following:

- Initializes all analog circuits including the PLL.
- Initializes all digital logic and state machines.
- Reads and latches the PHY address pins.
- Initializes all MII registers to their default values (H/W configuration pins are reread).

Software Powerdown Mode

Software powerdown is entered when bit 11 of the control register (MII register address 0 bit 11) is set. In software powerdown, all PHY functions except the serial management interface and clock circuitry are disabled. The MII registers can be read or written. If the system clock output is enabled (MII register address 22 bit 4), the 125 MHz system clock will still be available for use by the MAC on pin SYS_CLK.

At exit from software powerdown, the ET1011 does the following:

- Initializes all digital logic and state machines.

Note: At exit from software powerdown, the H/W configuration pins and the PHY address pins are not reread and the MII registers are not reset to their default values. These operations are only done during reset or recovery from hardware powerdown.

Wake-On-LAN Powerdown Mode

ACPI power consumption compliant Wake-On-LAN mode is implemented on the ET1011 by using the *IEEE* standard MII registers to put the PHY into 10Base-T or 100Base-TX modes. Clearing the advertisement of 1000Base-T (MII register address 9 bits 8, 9) and setting the desired 10Base-T and 100Base-TX advertisement (MII register address 4 bits 5-8) activates this feature. This must be followed by an autonegotiation restart via the control register (MII register address 0 bit 9).

Low-Power Energy-Detect Mode

When COMA is asserted, low-power energy-detect (LPED) mode is enabled if LPED_EN_N is low. In this mode, the PHY monitors the cable for energy. If energy is detected, the MDINT_N pin is asserted. The PHY exits from LPED mode when COMA is deasserted.
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Pin Information

Pin Diagram, 128-Pin TQFP

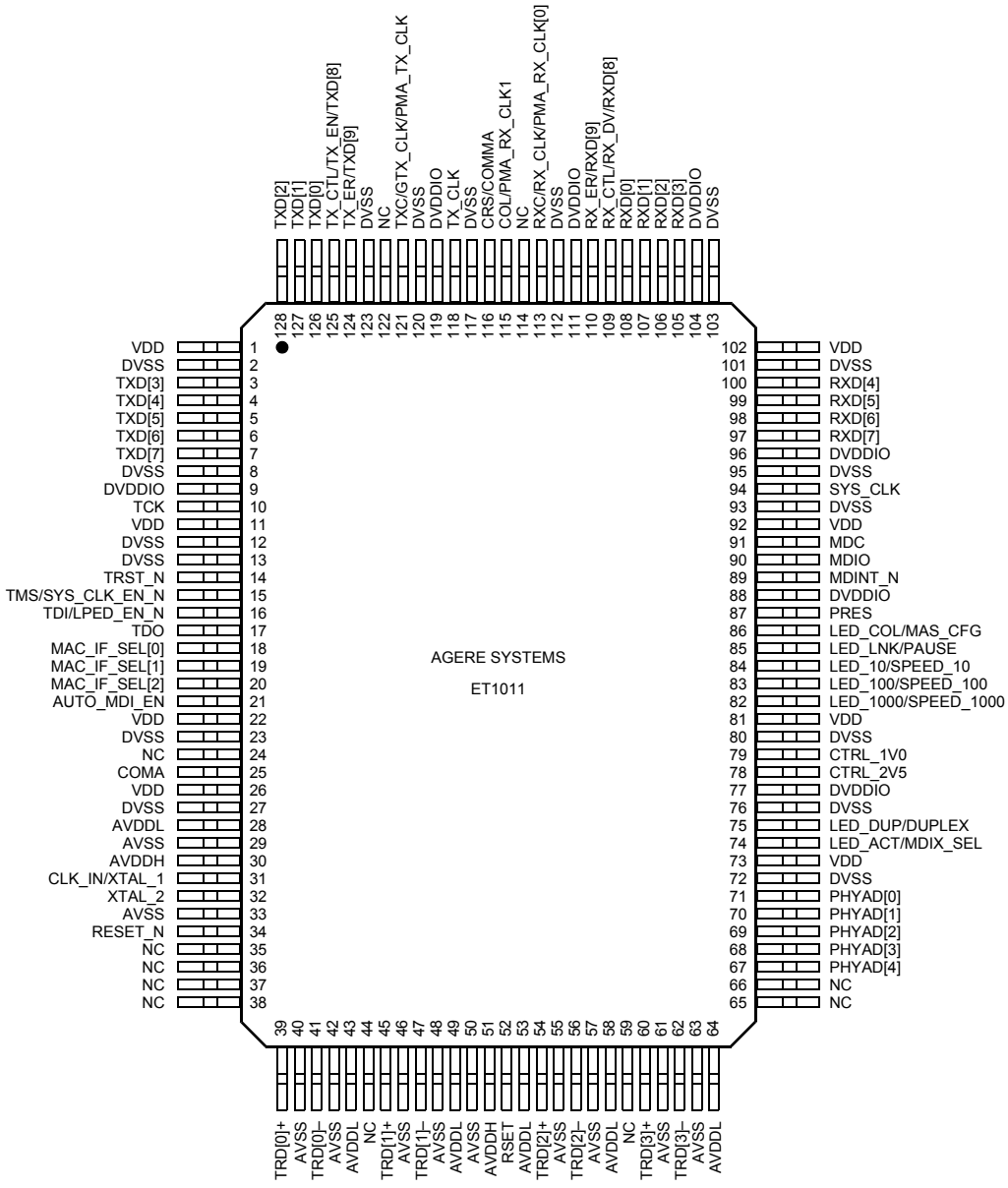


Figure 6. Pin Diagram for ET1011 in 128-Pin TQFP Package (Top View)

Pin Information (continued)

Pin Diagram, 68-Pin MLCC

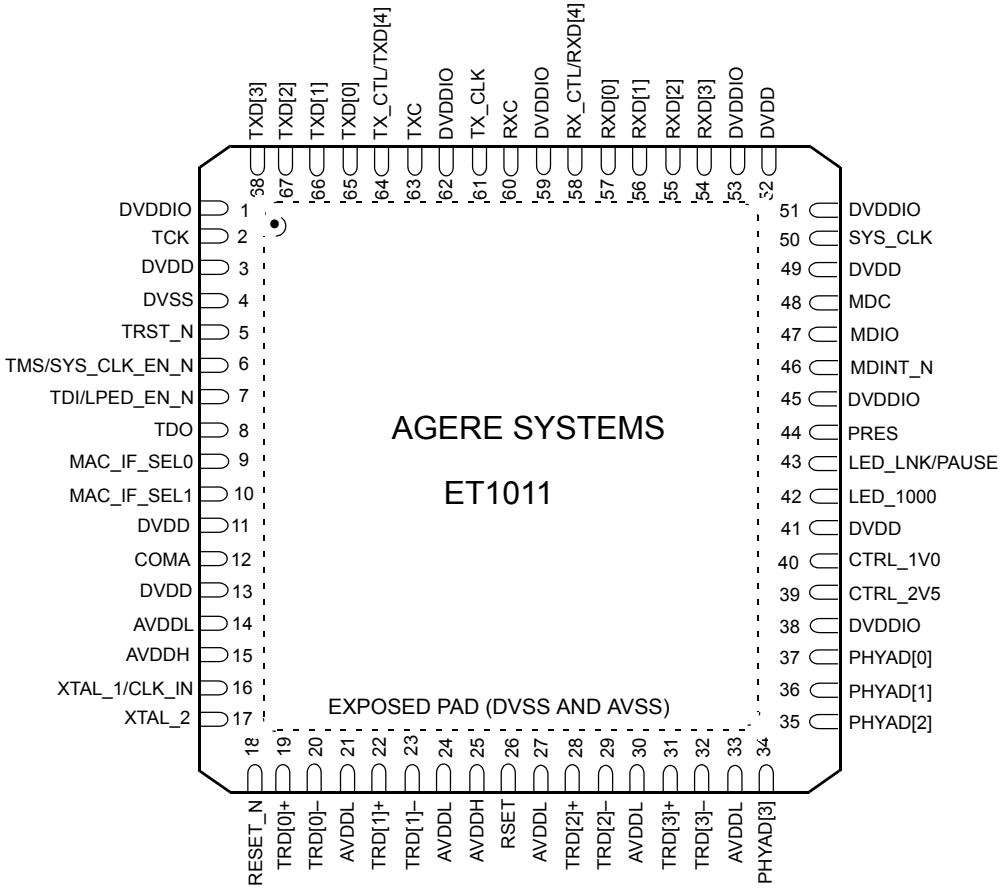


Figure 7. Pin Diagram for ET1011 in 68-Pin MLCC Package (Top View)

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC

Table 1. Agere Systems ET1011 Device Signals by Interface, 128-Pin TQFP and 68-Pin MLCC

Name	Description	Pad Type	Hyst./ Open-Drain	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-TQFP	Pin # 68-MLCC
MAC: GMII—Gigabit Media Independent Interface (128-pin TQFP only)								
GTX_CLK	GMII transmit clock	I	H	—	—	—	121	—
TX_ER	Transmit error	I	H	—	—	—	124	—
TX_EN	Transmit enable	I	H	—	—	—	125	—
TXD[7:0]	Transmit data bits	I	H	—	—	—	126, 127, 128, 3, 4, 5, 6, 7	—
RX_CLK	Receive clock	O	—	—	Z	—	113	—
RX_ER	Receive error	O	—	—	Z	—	110	—
RX_DV	Receive data valid	O	—	—	Z	—	109	—
RXD[7:0]	Receive data bits	O	—	—	Z	—	108, 107, 106, 105, 100, 99, 98, 97	—
CRS	Carrier sense	O	—	—	Z	—	116	—
COL	Collision detect	O	—	—	Z	—	115	—
MAC: RGMII—Reduced Gigabit Media Independent Interface								
TXC	RGMII transmit clock	I	H	—	—	—	121	63
TXD[3:0]	Transmit data bits	I	H	—	—	—	126, 127, 128, 3	68, 67, 66, 65
TX_CTL	Transmit control	I	H	—	—	—	125	64
RXC	Receive clock	O	—	—	Z	—	113	60
RXD[3:0]	Receive data bits	O	—	—	Z	—	108, 107, 106, 105	54, 55, 56, 57
RX_CTL	Receive control	O	—	—	Z	—	109	58
MAC: MII—Media Independent Interface (128-pin TQFP only)								
TX_CLK	MII transmit clock	O	—	—	Z	—	118	—
TX_ER	Transmit error	I	H	—	—	—	124	—
TX_EN	Transmit enable	I	H	—	—	—	125	—
TXD[3:0]	Transmit data bits	I	H	—	—	—	126, 127, 128, 3	—
RX_CLK	Receive clock	O	—	—	Z	—	113	—
RX_ER	Receive error	O	—	—	Z	—	110	—
RX_DV	Receive data valid	O	—	—	Z	—	109	—
RXD[3:0]	Receive data bits	O	—	—	Z	—	108, 107, 106, 105	—
CRS	Carrier sense	O	—	—	Z	—	116	—
COL	Collision detect	O	—	—	Z	—	115	—

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC (continued)

Table 1. Agere Systems ET1011 Device Signals by Interface, 128-Pin TQFP and 68-Pin MLCC (continued)

Name	Description	Pad Type	Hyst./ Open-Drain	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-TQFP	Pin # 68-MLCC
MAC: TBI—Ten-Bit Interface (128-pin TQFP only)								
PMA_ TX_CLK	TBI transmit clock	I	H	—	—	—	121	—
TXD[9:0]	Transmit data bits	I	H	—	—	—	126, 127, 128, 3, 4, 5, 6, 7, 125, 124	—
PMA_RX_CLK[0]	TBI receive clock	O	—	—	Z	—	113	—
RXD[9:0]	Receive data bits	O	—	—	Z	—	108, 107, 106, 105, 100, 99, 98, 97, 109, 110	—
PMA_RX_ CLK[1]	TBI receive clock	O	—	—	Z	—	115	—
COMMA	Valid comma detect	I	H	—	—	—	116	—
MAC: RTBI—Reduced Ten-Bit Interface								
TXC	RTBI transmit clock	I	H	—	—	—	121	63
TXD[4:0]	Transmit data bits	I	H	—	—	—	4, 3, 128, 127, 126	68, 67, 66, 65 64
RXC	RTBI receive clock	O	—	—	Z	—	113	60
RXD[4:0]	Receive data bits	O	—	—	Z	—	108, 107, 106, 105, 109	58, 54, 55, 56, 57
MDI: Transformer Interface								
TRD[0]+	Transmit and receive differential pair	I/O	—	—	—	A	39	19
TRD[0]–							41	20
TRD[1]+	Transmit and receive differential pair	I/O	—	—	—	A	45	22
TRD[1]–							47	23
TRD[2]+	Transmit and receive differential pair	I/O	—	—	—	A	54	28
TRD[2]–							56	29
TRD[3]+	Transmit and receive differential pair	I/O	—	—	—	A	60	31
TRD[3]–							62	32
RSET	Analog reference resistor	I/O	—	—	—	A	52	26

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC (continued)

Table 1. Agere Systems ET1011 Device Signals by Interface, 128-Pin TQFP and 68-Pin MLCC (continued)

Name	Description	Pad Type	Hyst./ Open-Drain	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-TQFP	Pin # 68-MLCC
Management Interface								
PHYAD[4:0]	PHY address 4—1	I	—	Pull-down	—	—	70, 71, 69, 68, 67	34, 35, 36, 37 PHYAD [3:0]
	PHY address 0	I	—	Pull-up	—	—		
MDC	Management interface clock	I	—	Pull-down	—	—	91	48
MDIO	Management data I/O	I/O	—	Pull-up	—	—	90	47
MDINT_N	Management interface interrupt	O	OD	—	—	—	89	46
Configuration[1]								
SPEED_1000	1000Base-T speed select	I	—	Pull-up	—	—	82	—
SPEED_100	100Base-TX speed select	I	—	Pull-up	—	—	83	—
SPEED_10	10Base-T speed select	I	—	Pull-up	—	—	84	—
DUPLEX	Half- or full-duplex configuration	I	—	Pull-up	—	—	75	—
AUTO_MDI_EN	Auto-MDI detection enable	I	—	Pull-up	—	—	21	—
MDIX_SEL	MDI/MDI-X autodetection	I	—	Pull-down	—	—	74	—
MAS_CFG	Master slave configuration	I	—	Pull-down	—	—	86	—
PAUSE	Pause mode	I	—	Pull-down	—	—	85	43
MAC_IF_SEL[1]	MAC interface select 1	I	—	Pull-down	—	—	19	10
MAC_IF_SEL[2]	MAC interface select 2	I	—	Pull-down	—	—	20	—
SYS_CLK_EN_N	System clock enable	I	—	Pull-up	—	—	15	6
LPED_EN_N	Low power energy detection enable	I	—	Pull-up	—	—	16	7
PRES	Precision resistor	I	—	—	—	—	87	44

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC (continued)

Table 1. Agere Systems ET1011 Device Signals by Interface, 128-Pin TQFP and 68-Pin MLCC (continued)

Name	Description	Pad Type	Hyst./ Open-Drain	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-TQFP	Pin # 68-MLCC
LED Interface								
LED_1000	1000Base-T LED	O	—	Pull-up	—	—	82	42
LED_100	100Base-TX LED	O	—	Pull-up	—	—	83	—
LED_10	10Base-T LED	O	—	Pull-up	—	—	84	—
LED_DUP	Duplex LED	O	—	Pull-up	—	—	75	—
LED_LNK	Link established LED	O	—	Pull-down	—	—	85	43
LED_COL	Collision LED	O	—	Pull-down	—	—	86	—
LED_ACT	Transmit and receive activity	O	—	Pull-down	—	—	74	—
JTAG								
TCK	Test clock	I	—	—	—	—	10	2
TRST_N	Test reset	I	H	Pull-down	—	—	14	5
TMS	Test mode select	I	—	Pull-up	—	—	15	6
TDI	Test data input	I	—	Pull-up	—	—	16	7
TDO	Test data output	O	—	Pull-up	—	—	17	8
Clocking and Reset								
CLK_IN	Reference clock input	I/O	—	—	—	A	31	16
XTAL_1	Reference crystal input	I/O	—	—	—	A	31	16
XTAL_2	Reference crystal	I/O	—	—	—	A	32	17
SYS_CLK	System clock	O	—	—	—	—	94	50
RESET_N	Reset	I	—	—	—	—	34	18
COMA	Hardware powerdown	I	—	Pull-down	—	—	25	12
Regulator Control								
CTRL_1V0	Regulator control 1.0 V	O	—	—	—	A	79	40
CTRL_2V5	Regulator control 2.5 V	O	—	—	—	A	78	39

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC (continued)

Table 1. Agere Systems ET1011 Device Signals by Interface, 128-Pin TQFP and 68-Pin MLCC (continued)

Name	Description	Pad Type	Hyst./ Open-Drain	Internal Pull-Up/ Pull-Down	3-State	Analog	Pin # 128-TQFP	Pin # 68-MLCC
Power, Ground, and No Connect								
DVDDIO	Digital I/O 2.5 V or 3.3 V supply	V_{DD}	—	—	—	—	9, 77, 88, 96, 104, 111, 119	1, 38, 45, 51, 53, 59, 62
VDD	Digital core 1.0 V supply	V_{DD}	—	—	—	—	1, 11, 22, 26, 73, 81, 92, 102	3, 11, 13, 41, 49, 52
DVSS[2]	Digital ground	V_{SS}	—	—	—	—	2, 4, 8, 12, 13, 23, 27, 72, 76, 80, 93, 95, 101, 103, 112, 117, 120, 123	4
AVDDH	Analog power 2.5 V	V_{DD}	—	—	—	—	30, 51	15, 25
AVDDL	Analog power 1.0 V	V_{DD}	—	—	—	—	28, 43, 49, 53, 58, 64	14, 21, 24, 27, 30, 33
AVSS[2]	Analog ground	V_{SS}	—	—	—	—	29, 33, 40, 42, 46, 48, 50, 55, 57, 61, 63	—
NC	Reserved—do not connect	—	—	—	—	—	24, 35, 36, 37, 38, 44, 59, 65, 66, 114, 122	—

1. Configuration signals are multiplexed with the LED controls. During a reset, the status of the configuration pins are latched and used to set the configuration and later to select the polarity to drive the LEDs.
2. For the 68-MLCC, all AVss and DVss pins share a common ground pin (pad) in the center of the device.

Pin Information (continued)

Pin Descriptions, 128-Pin TQFP and 68-Pin MLCC (continued)

Table 2. Multiplexed Signals on the ET1011

Default	Pin # 128-TQFP	Pin # 68-MLCC	Alternate
COL	115	—	COL[1, 6]
			PMA_RX_CLK[1][2]
CRS	116	—	CRS[1, 6]
			COMMA[2]
GTX_CLK	121	—	GTX_CLK[1]
			PMA_TX_CLK[2]
			TXC[3, 4]
LED_ACT	74	—	LED_ACT
			MDIX_SEL[5]
LED_COL	86	—	LED_COL
			MAS_CFG[5]
LED_DUP	75	—	LED_DUP
			DUPLEX[5]
LED_LNK	85	—	LED_LNK
			PAUSE[5]
LED_1000	82	—	LED_1000
			SPEED_1000[5]
LED_100	83	—	LED_100
			SPEED_100[5]
LED_10	84	—	LED_10
			SPEED_10[5]
RX_CLK	113	—	RX_CLK[1, 6]
			PMA_RX_CLK[0][2]
			RXC[3, 4]
RX_ER	110	—	RX_ER[1, 6]
			RXD[9][2]
RX_DV	109	—	RX_DV[1, 6]
			RXD[8][2]
			RX_CTL[3]
TDI	16	7	TDI
			LPED_EN_N[5]
TMS	15	6	TMS
			SYS_CLK_EN_N[5]
TX_ER	124	—	TX_ER[1, 6]
			TXD[9][2]
TX_EN	125	—	TX_EN[1, 6]
			TXD[8][2]
XTAL_1	31	16	XTAL_1
			CLK_IN

1. GMII signal.
2. TBI signal.
3. RGMII signal.
4. RTBI signal.
5. Reset/configuration signal.
6. MII signal.

Hardware Interfaces

The following hardware interfaces are included on the ET1011 gigabit Ethernet transceiver:

- MAC interfaces:
  - — GMII (128-pin TQFP only)
  - — RGMII
  - — MII (128-pin TQFP only)
  - — TBI (128-pin TQFP only)
  - — RTBI
- Media dependent interface
- Management interface
- Configuration interface
- LED interface
- Clock and reset signals
- JTAG interface
- Regulator control
- Power and ground signals

Several of the pins of the MAC interface are multiplexed, but they are designed to be interchangeable so that the device can change the MAC interface once the transmission capabilities (1000Base-T, 100Base-TX, and 10Base-T) are established.

The following diagram shows the various interfaces on each ET1011 and how they connect to the MAC and other support devices in a typical application.

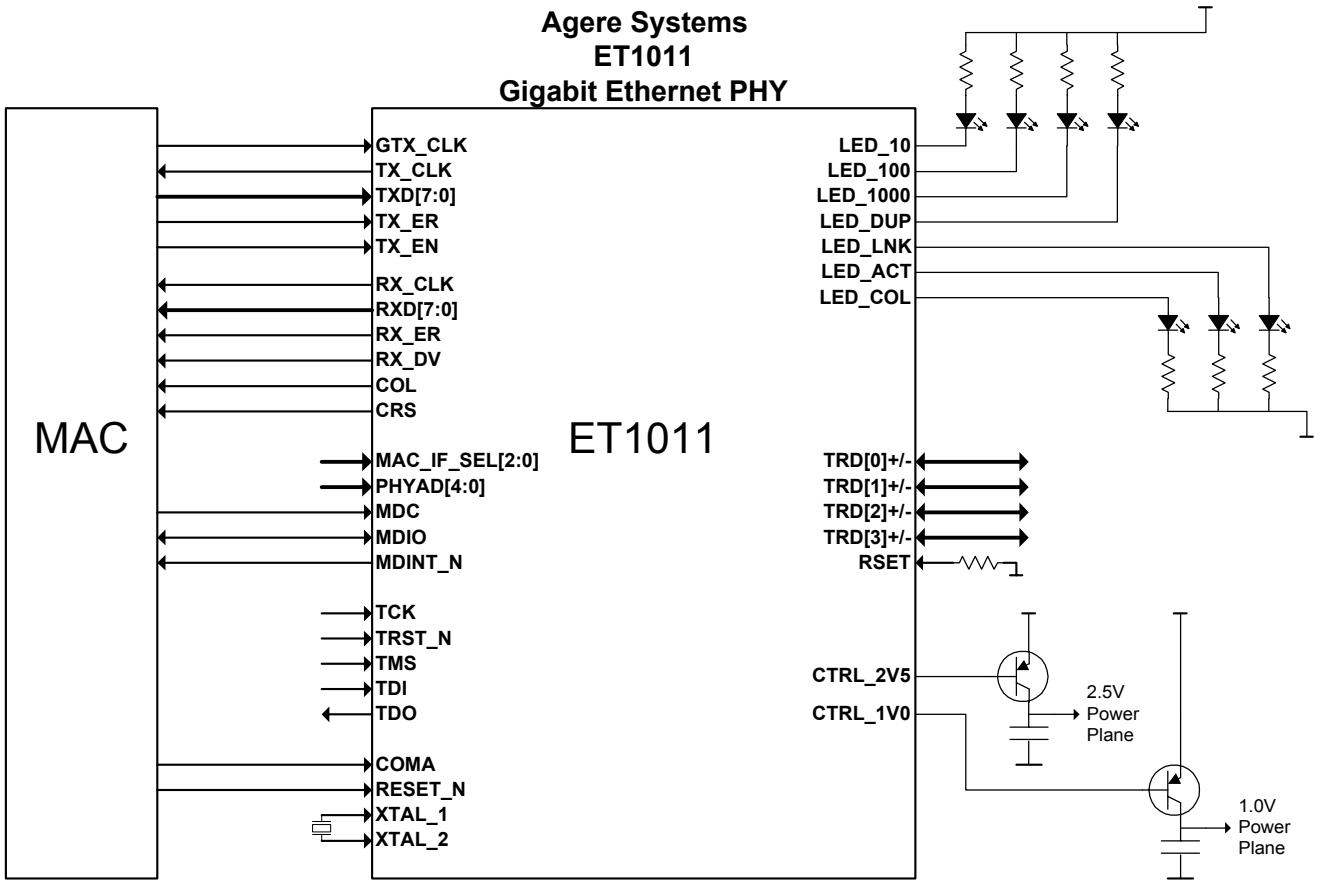


Figure 8. ET1011 Gigabit Ethernet Card Block Diagram

Hardware Interfaces (continued)

MAC Interface

The ET1011 supports RGMII, GMII, MII, RTBI, and TBI interfaces to the MAC. The MAC interface mode is selected via the hardware configuration pins, MAC_IF_SEL[2:0].

Gigabit Media Independent Interface (GMII) (128-pin TQFP only)

The GMII is fully compliant with *IEEE* 802.3 clause 35. The GMII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 000.

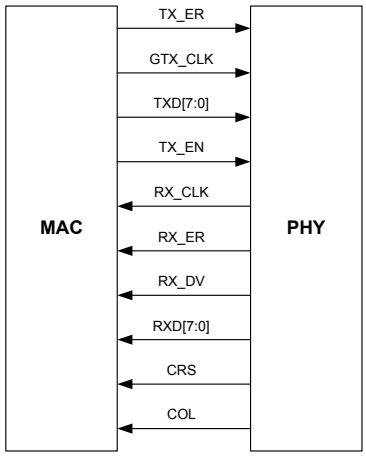


Figure 9. GMII MAC-PHY Signals

Table 3. GMII Signal Description (1000Base-T Mode) (128-pin TQFP Only)

Pin Name	Pin # 128 TQFP	Pin Description	Functional Description
GTX_CLK	121	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation or when operating in modes other than 1000Base-T.
TX_ER	124	Transmit error	The MAC drives this signal high to indicate a transmit coding error.
TX_EN	125	Transmit enable	The MAC drives this signal high to indicate that data is available on the transmit data bus.
TXD[7:0]	126, 127, 128, 3, 4, 5, 6, 7	Transmit data bits 7—0	The MAC transmits data synchronized with RX_CLK to the ET1011 for transmission on the media dependent (transformer) interface.
RX_CLK	113	Receive clock	The ET1011 generates a 125 MHz clock to synchronize receive data.
RX_ER	110	Receive error	The ET1011 drives RX_ER to indicate that an error was detected in the frame that was received and is being transmitted to the MAC.
RX_DV	109	Receive data valid	The ET1011 drives RX_DV to indicate that it is sending recovered and decoded data to the MAC.
RXD[7:0]	108, 107, 106, 105, 100, 99, 98, 97	Receive data	The ET1011 transmits data that is synchronized with RX_CLK to the MAC.
CRS	116	Carrier sense	The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011 whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is nonidle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.
COL	115	Collision detect	In 10Base-T, 100Base-TX, and 1000Base-T half-duplex modes, COL is asserted when both transmit and receive media are nonidle.

Hardware Interfaces (continued)

Reduced Gigabit Media Independent Interface (RGMII)

The RGMII interface is fully compliant with the RGMII Rev. 1.3 specification. The RGMII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 100 (trace delay) or 110 (DLL delay).

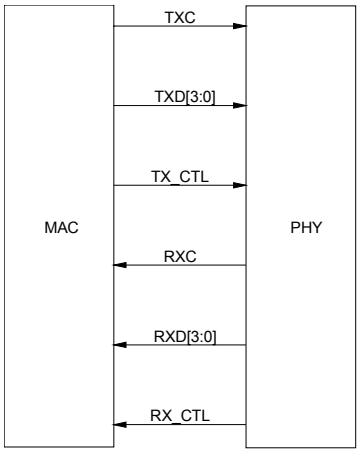


Figure 10. RGMII MAC-PHY Signals

Table 4. RGMII Signal Description (1000Base-T Mode)

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
TXC	121	63	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation or when operating in modes other than 1000Base-T. To obtain the 1 gigabit transmission rate, the MAC uses both the positive and negative clock transitions.
TXD[3:0]	126, 127, 128, 3	68, 67, 66, 65	Transmit data bits	The MAC transmits data synchronized with RX_CLK to the ET1011 for transmission on the media dependent (transformer) interface. The MAC sends data in two 4-bit nibbles.
TX_CTL	125	64	Transmit control	The MAC transmits control signals across this line (TX_ER and TX_EN). The MAC transmits TX_EN[1] on a positive transition of TXC and TX_EN and TX_ER[1] on the negative transition of TXC.
RXC	113	60	Receive clock	The ET1011 generates a 125 MHz clock to synchronize receive data. To obtain the 1 gigabit transmission rate, the ET1011 uses both the positive and negative clock transitions.
RXD[3:0]	108, 107, 106, 105,	54, 55, 56, 57	Receive data	The ET1011 transmits data that is synchronized with RX_CLK to the MAC. The ET1011 sends data in two 4-bit nibbles.
RX_CTL	109	58	Receive control	The ET1011 transmits control signals across this line (RX_ER and RX_EN). The ET1011 transmits RX_DV[1] on a positive transition of RXC and RX_EN[1] and RX_ER[1] on the negative transition of TXC.

1. Reference the GMII interface for description of the following parameters: TX_EN, TX_ER, RX_DV, RX_EN, and RX_ER.

Hardware Interfaces (continued)

Media Independent Interface (MII) (128-pin TQFP only)

The MII is fully compliant with *IEEE* 802.3 clause 22. The MII interface mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 000.

In 100Base-TX and 10Base-T mode, the RXD[7:4] pins are driven low by the ET1011 and the TXD[7:4] pins are ignored. They should not be left floating but should be set either high or low. In the MII interface mode, the GTX_CLK pin may be held low.

An alternative to the standard MII is provided when operating in 10Base-T or 100Base-TX mode by setting hardware configuration pins MAC_IF_SEL[2:0] = 010. In this alternative interface, the MAC provides a reference clock at 2.5 MHz or 25 MHz at the GTX_CLK pin. The ET1011 then uses a FIFO to resynchronize data presented synchronously with this reference clock.

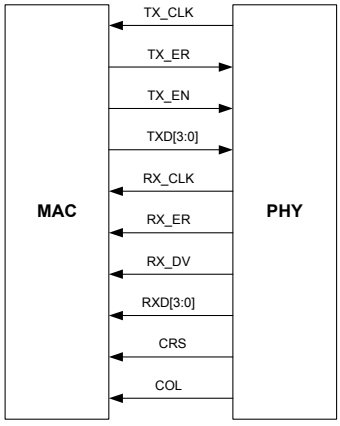


Figure 11. MII Signals

Table 5. MII Interface (100Base-TX and 10Base-T) (128-pin TQFP Only)

Pin Name	Pin # 128 TQFP	Pin Description	Functional Description
TX_CLK	118	Transmit clock	In 100Base-TX mode, the ET1011 generates 25 MHz reference clocks and in 10Base-T mode provides 2.5 MHz reference clocks. MAC_IF_SEL[2:0] = 000—this is default behavior.
GTX_CLK	121	Alternate transmit clock	In 100Base-TX mode, the MAC generates the 25 MHz reference clock and in 10Base-T mode provides a 2.5 MHz reference clock. MAC_IF_SEL[2:0] = 010.
TX_ER	124	Transmit error	The MAC drives this signal high to indicate a transmit coding error.
TX_EN	125	Transmit enable	The MAC drives this signal high to indicate that data is available on the transmit data bus.
TXD[3:0]	126, 127, 128, 3	Transmit data bits	The MAC transmits data synchronized with TX_CLK to the ET1011 for transmission on the media dependent (transformer) interface.
RX_CLK	113	Receive clock	In 100Base-TX mode, the ET1011 generates 25 MHz reference clocks and in 10Base-T mode provides 2.5 MHz reference clocks.
RX_ER	110	Receive error	The ET1011 drives RX_ER to indicate that an error was detected in the frame that was received and is being transmitted to the MAC.
RX_DV	109	Receive data valid	The ET1011 drives RX_DV to indicate that it is sending recovered and decoded data to the MAC.
RXD[3:0]	108, 107, 106, 105	Receive data bits	The ET1011 transmits data synchronized with RX_CLK to the MAC.
CRS	116	Carrier sense	The carrier sense signal (CRS) of the MAC interface is asserted by the ET1011 whenever the receive medium is nonidle. In half-duplex mode, CRS may also be asserted when the transmit medium is non-idle. The CRS may be enabled on transmit in half-duplex mode by writing to the PHY configuration register, address 22, bit 15.
COL	115	Collision detect	In 10Base-T, 100Base-TX, and 1000Base-T half-duplex modes, COL is asserted when both transmit and receive media are nonidle.

Hardware Interfaces (continued)

Ten-Bit Interface (TBI) (128-pin TQFP only)

The TBI is fully compliant with *IEEE* 802.3 clause 36. It may be used as an alternative to the GMII in 1000Base-T mode. The TBI mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 001.

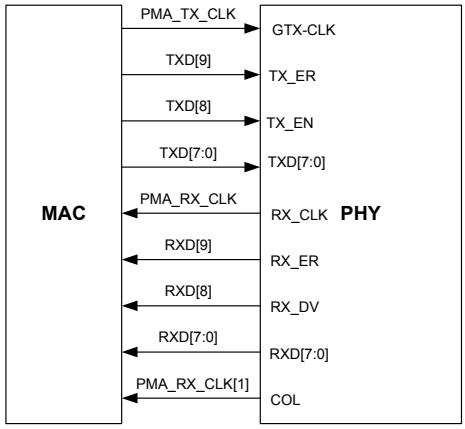


Figure 12. Ten-Bit Interface

Table 6. Ten-Bit Interface (1000Base-T) (128-pin TQFP Only)

Pin Name	Pin # 128 TQFP	Pin Description	Functional Description
PMA_TX _CLK	121	TBI transmit clock	The MAC drives this 125 MHz clock signal and should be held low during autonegotiation or when operating in modes other than 1000Base-T.
TXD[9:0]	126, 127, 128, 3, 4, 5, 6, 7, 125, 124	Transmit data bits	The MAC transmits data synchronized with PMA_TX_CLK to the ET1011 for transmission on the media dependent (transformer) interface.
PMA_RX_CLK[0]	113	Receive clock	The ET1011 generates a 62.5 MHz clock to synchronize receive data for the odd code group. This signal is 180 degrees out of phase from PMA_RX_CLK[1].
RXD[9:0]	108, 107, 106, 105, 100, 99, 98, 97, 109, 110	Receive data bits	The ET1011 transmits data that is synchronized with PMA_RX_CLK[0] to the MAC.
PMA_RX_CLK[1]	115	Receive clock	The ET1011 generates a 62.5 MHz clock to synchronize receive data for the even code group. This signal is 180 degrees out of phase from PMA_RX_CLK[0].

Hardware Interfaces (continued)

Reduced Ten-Bit Interface (RTBI)

The RTBI is fully compliant with RGMII rev 1.3 specification. The RTBI mode is selected by setting the hardware configuration pins MAC_IF_SEL[2:0] = 101 (trace delay) or 111 (DLL delay).

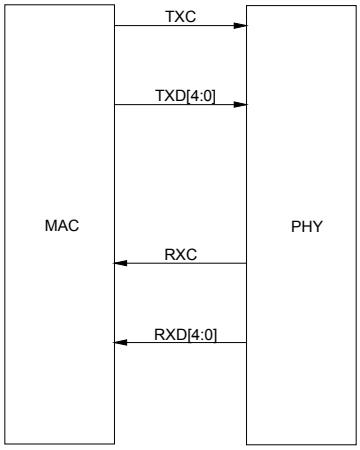


Figure 13. Reduced Ten-Bit Interface

Table 7. RTBI Signal Description (1000Base-T Mode)

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
TXC	121	63	Transmit clock	The MAC drives this 125 MHz clock signal that is held low during autonegotiation or when operating in modes other than 1000Base-T.
TXD[4:0]	4, 3, 128, 127, 126	68, 67, 66, 65, 64	Transmit data bits	The MAC transmits data synchronized with TXC to the ET1011 for transmission on the media dependent (transformer) interface.
RXC	113	60	Receive clock	The ET1011 generates a 125 MHz clock to synchronize receive data.
RXD[4:0]	108, 107, 106, 105, 109	54, 55, 56, 57, 58	Receive data	The ET1011 transmits data that is synchronized with RXC to the MAC.

Hardware Interfaces (continued)

Management Interface

Serial Management Interface

The MII management interface (MI) provides a simple, two-wire serial interface between the MAC and the PHY to allow access to control and status information in the internal registers of the ET1011. The interface is compliant with *IEEE* 802.3 clause 22 and is compatible with the clause 45.3, enabling the two systems to co-exist on the same MDIO bus.

Management Frame Structure

Frames transmitted on the MI have the following structure.

Table 8. Management Frame Structure

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1 . . . 1	01	10	aaaaa	rrrrr	ZO	d . . . d	Z
Write	1 . . . 1	01	01	aaaaa	rrrrr	10	d . . . d	Z

- **PRE** (preamble): At the beginning of each transaction, the MAC may send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. The ET1011 supports MF preamble suppression, and thus the MAC may initiate management frames with the ST (start of frame) pattern.
- **ST** (start of frame): The start of frame is indicated by a <01> pattern. This pattern ensures transitions from the default logic one line state to zero and back to one. When a clause 45 start of frame <00> is received, the frame is ignored
- **OP** (operation code): The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.
- **PHYAD** (phy address): The PHY address is 5 bits. The first PHY address bit transmitted and received is the MSB of the address. Only the PHY that is addressed will respond to the MI operation.
- **REGAD** (register address): The register address is 5 bits. The first register address bit transmitted and received is the MSB of the address.
- **TA** (turnaround): The turnaround time is a 2-bit time spacing between the register address field and the data field of a management frame to avoid contention during a read transaction. For a read transaction, the PHY remains in a high-impedance state for the first bit time of the turnaround and drives a zero bit during the second bit time of the turnaround. During a write transaction, the PHY expects a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround.
- **DATA** (data): The data field is 16 bits. The first data bit transmitted and received is the MSB of the register being addressed.
- **IDLE** (idle condition): The IDLE condition on MDIO is a high-impedance state, and the ET1011 internal pull-up resistor will pull the MDIO line to logic one.

Hardware Interfaces (continued)

Table 9. Management Interface

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
PHYAD [4:0]	71, 70, 69, 68, 67	34, 35, 36, 37 (PHYAD [3:0])	PHY Address	The physical address of the ET1011 is configured at reset by the current state of the PHYAD[4:0] pins. Once these pins have been latched in at reset, the ET1011 is accessible via the management interface at the configured address. The default address is set to 1 by internal pull up/downs. These may be overridden by external pull-up/downs. The valid range is 0 to 31[1].
MDC	91	48	Management Interface Clock	The management data clock (MDC) is a reference for the data signal and is generated by the MAC. It should be turned off when the MI is not being used. This pin has an internal pull-down resistor. MDC is nominally 2.5 MHz, and can work up to a maximum of 12.5 MHz.
MDIO	90	47	Management Data I/O	The management data input/output (MDIO) is a bidirectional data signal between the MAC and one or more PHYs. MDIO is a 3-state pin that allows either the MAC or the selected PHY to drive this signal. This pin has an internal pull-up resistor. An external pull-up resistor should also be used, the exact value depending on the number of PHYs sharing the MDIO signal. Data signals written by the MAC are sampled by the PHY synchronously with respect to the MDC. Data signals written by the PHY are generated synchronously with respect to the MDC. This pin requires an external pull-up (1 kΩ to 10 kΩ).
MDINT_N	89	46	Management Interface Interrupt	This pin is active-low and indicates an unmasked management interrupt. This pin requires an external pull-up resistor (1 kΩ to 4.7 kΩ).

1. PHYAD description applies to the 128-TQFP only. For the 68-MLCC, the valid range will be 0—15.

Management Interrupt

The ET1011 is capable of generating hardware interrupts on pin MDINT_N in response to a variety of user-selectable conditions. MDINT_N is an open-drain, active-low signal that can be wire-ORed with several other ET1011 devices. A single 2.2 kΩ pull-up resistor is recommended for this wire-OR configuration.

When an interrupt occurs, the system can poll the status of the interrupt status register on each device to determine the origin of the interrupt. There are nine conditions that can be selected to generate an interrupt:

- Autonegotiation status change
- Autonegotiation page received
- FIFO overflow/underflow
- Link status change
- High bit-error rate
- Full error counter
- Local/remote rx status change
- Automatic speed downshift occurred
- MDIO synchronization lost

The ET1011 is configured to generate an interrupt based on any of these conditions by use of the interrupt mask register (MII register 24). By setting the corresponding bit in the interrupt mask register for the desired condition, the ET1011 will generate the desired interrupt. The ET1011 can be polled on the status of an activated interrupt condition by accessing MII register interrupt status register (MII register 25). If this condition has occurred, the corresponding bit in the interrupt status register will be set. The interrupt status register is self-clearing on a read operation.

Hardware Interfaces (continued)

Configuration Interface

The hardware configuration pins initialize the ET1011 at poweron and reset. The configuration is latched during initialization and stored. These pins set the default value of their corresponding MII register bits.

Some configuration inputs are shared with LED pins. The hardware configuration and LED pins are read on initial powerup of the ET1011, during a hardware reset and during recovery from hardware powerdown. The logic value at the pin is sensed and latched. After RESET_N has been deasserted (raised high), the shared configuration pins become outputs that are used to drive LEDs.

Note: The 68-MLCC, unlike its 128-TQFP counterpart, offers comparatively limited hardware configuration capabilities. It only has PAUSE, SYS_CLK_EN_N, and LPED_EN_N configuration pins. Most configuration settings are established via registers.

Autonegotiation: Speed and Duplex Selection

The ET1011 supports 10Base-T, 100Base-TX, and 1000Base-T modes in both full and half duplex. For the purpose of autonegotiation, the *IEEE* defines a technology as a combination of speed and duplex capability. The PHY can be configured to advertise a subset of the available technologies as shown in Table 10.

Once autonegotiation is completed, an attempt is made to bring up a link with the highest common denominator technology.

Table 10. Autonegotiation Modes

SP_1000	SP_100	SP_10	DUPLEX	Autonegotiation Mode
0	0	1	0	Advertise only 10Base-T, half duplex.
0	0	1	1	Advertise only 10Base-T, full duplex.
0	1	0	0	Advertise only 100Base-TX, half duplex.
0	1	0	1	Advertise only 100Base-TX, full duplex.
1	0	0	0	Advertise only 1000Base-T, half duplex.
1	0	0	1	Advertise only 1000Base-T, full duplex.
0	1	1	0	Advertise 10Base-T and 100Base-TX, half duplex.
0	1	1	1	Advertise 10Base-T and 100Base-TX, full duplex.
1	0	1	0	Advertise 10Base-T and 1000Base-T, half duplex.
1	0	1	1	Advertise 10Base-T and 1000Base-T, full duplex.
1	1	0	0	Advertise 100Base-TX and 1000Base-T, half duplex.
1	1	0	1	Advertise 100Base-TX and 1000Base-T, full duplex.
1	1	1	0	Advertise all capabilities, half duplex.
1	1	1	1	Advertise all capabilities, full duplex.

Autonegotiation can be disabled and the technology forced by writing to the control register (MI register address 0, bits 12). This causes the PHY to transmit and receive in accordance with the selected technology irrespective of the capability of the link partner. Disabling autonegotiation is not recommended.

Hardware Interfaces (continued)

Autonegotiation: Master/Slave Configuration

A PHY can advertise a preference for master or slave. The hardware configuration pin MAS_CFG sets the preference as shown in Table 11. If both PHYs advertise the same master/slave preference, the master/slave configuration is resolved during autonegotiation as described in the *IEEE* standards.

Table 11. Master/Slave Preference

MAS_CFG	Autonegegotiation Master/Slave Mode
0	Autonegotiation, advertise slave preference.
1	Autonegotiation, advertise master preference.

The PHY can be manually configured for master or slave by writing to the 1000Base-T control register (MI register address 9, bits 12 and 11). If both PHYs are manually configured to the same master/slave setting, a 1000Base-T link cannot be established. Manual master/slave configuration is not recommended.

Hardware Interfaces (continued)

Autonegotiation: MDI/MDI-X Configuration

The PHY can be configured to automatically detect MDI/MDI-X configuration, or the MDI/MDI-X configuration can be forced as shown in Table 12.

Table 12. MDI/MDI-X Configuration

AUTO_MDI_EN	MDI_SEL	MDI/MDI-X Configuration
1	X	Automatic MDI/MDI-X detection.
0	0	MDI configuration (NIC/DTE).
0	1	MDI-X configuration (switch).

Table 13. Configuration Signals

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
SPEED_1000	82	—	Speed 1000	The speed configuration pins set the default advertised speed. The assertion of each input enables advertisement of the corresponding speed to the remote end. SPEED_1000 → Advertise 1000Base-T SPEED_100 → Advertise 100Base-TX SPEED_10 → Advertise 10Base-T The default is to advertise all three speeds.
SPEED_100	83	—	Speed 100	
SPEED_10	84	—	Speed 10	
DUPLEX	75	—	Duplex	DUPLEX selects the duplex mode to be advertised (half or both half and full). 0 = Advertise half duplex. 1 = Advertise both half and full duplex (default).
SYS_CLK_EN_N	15	6	SYS_CLK Enable	Enables the system clock. 0 = SYS_CLK enabled. 1 = SYS_CLK disabled (default).
MAS_CFG	86	—	Master slave configuration	This input determines the master/slave preference. 0 = Advertise a preference to operate as slave (default). 1 = Advertise a preference to operate as master.

Hardware Interfaces (continued)

Table 13. Configuration Signals (continued)

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
PAUSE	85	43	Pause	This input sets the pause mode. If PAUSE is asserted, full-duplex pause and asymmetric pause operation are advertised. 0 = Don't advertise pause (default). 1 = Advertise full-duplex pause and asymmetric pause.
AUTO_MDI_EN	21	—	Autoconfigure MDI/MDI-X	These inputs determine the MDI/MDI-X configuration. If AUTO_MDI_EN is asserted, automatic MDI/MDI-X detection is enabled and the MDI/MDI-X configuration is determined by the PHY automatically. The MDIX_SEL signal is ignored. If AUTO_MDI_EN is not asserted, MDIX_SEL determines the MDI/MDI-X configuration and MDIX_SEL high sets the MDI-X configuration or MDIX_SEL low sets the MDI configuration. **Autoconfigure MDI/MDI-X** 0 = Automatic MDI/MDI-X detection disabled. 1 = Automatic MDI/MDI-X detection enabled (default). **MDI/MDI-X Selection** 0 = MDI configuration (default). 1 = MDI-X configuration mode.
MDIX_SEL	74	—	MDI/MDI-X Selection	

Hardware Interfaces (continued)

Table 13. Configuration Signals (continued)

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
MAC_IF_ SEL[2:0]	18 19 20	10 9 (MAC_IF_ SEL[1:0] (See Note 1.)	MAC Interface Mode	This input selects the desired MAC interface mode. Configure the MAC during reset as follows: 000 = GMII/MII (128-TQFP default). 001 = TBI. 010 = GMII/MII (clocked by GTX_CLK instead of TX_CLK) 011 = Reserved. 100 = RGMII/RMII (trace delay; 68-MLCC default). 101 = RTBI (trace delay). 110 = RGMII/RMII (DLL delay). 111 = RTBI (DLL delay).
LPED_EN_N	16	7	Low Power Energy Detection Enable	LPED_EN_N enables the low-power energy-detect (LPED) mode when COMA is asserted. When the PHY is in LPED mode, it can wake the MAC/controller (instead of *Magic Packet*) by asserting the MDINT_N pin to indicate the presence of cable energy. 0 = Low-power energy-detect mode enable. 1 = Low-power energy-detect mode disabled (default).
PRES	87	44	Precision Resistor	Connect a 1.0 kΩ precision resistor to ground to set termination for all digital I/O's.

1. In the 68-MLCC, MAC_IF_SEL 2 (=1) will be set internally.

LEDs Interface

The ET1011 is capable of sinking or sourcing current to drive LEDs. These LEDs are used to provide link status information to the user. The ET1011 is capable of automatically sensing the polarity of the LEDs. The device determines the active sense of the LED based upon the input that is latched during configuration. Thus, if logic 1 is read, the device will drive the pin to ground to activate the LED; otherwise, it will drive the pin to supply to activate the LED.

The LEDs can be programmed to stretch out events to either 28, 60, or 100 ms. This makes very short events more visible to the user. All LEDs can be programmed to be on, off, or blink instead of the default status function. This is useful for alternative function indication under host processor control: for example, a system error during power-on self-check. Four of the LEDs (LED_ACT, LED_LNK[1], LED_100 and LED_1000[1]) can be programmed to indicate one of thirteen different status functions instead of the default status function:

- 1000Base-T
- 100Base-TX
- 10Base-T
- 1000Base-T (on) and 100Base-TX (blink)
- Link established
- Transmit activity
- Receive activity
- Transmit or receive activity
- Full duplex
- Collision
- Link established (on) and activity (blink)
- Link established (on) and receive activity (blink)
- Full duplex (on) and collision (blink)

The LED drivers can be configured by use of LED control register 1 and LED control register 2 (MII registers 27—28).

1. Only LED_LNK and LED_1000 are available in the 68-pin MLCC.

Hardware Interfaces (continued)

Table 14. LED

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
LED_1000	82	42	1000Base-T LED	This LED indicates that the device is operating in 1000Base-T mode. Setting can be overridden.
LED_100	83	—	100Base-TX LED	This LED indicates that the device is operating in 100Base-TX mode. Setting can be overridden.
LED_10	84	—	10Base-T LED	This LED indicates that the device is operating in 10Base-T mode. Setting can be overridden.
LED_DUP	75	—	Duplex LED	This LED indicates that the device is operating in full-duplex mode. Setting can be overridden.
LED_LNK	85	43	Link Established LED	This LED indicates that the link is established. Setting can be overridden.
LED_COL	86	—	Collision LED	This LED indicates that both transmit and receive activity is occurring in half-duplex mode. Setting can be overridden.
LED_ACT	74	—	Transmit/Receive Activity LED	This LED indicates that there is transmit or receive activity. Setting can be overridden.

Hardware Interfaces (continued)

Media-Dependent Interface: Transformer Interface

Table 15. Transformer Interface Signals

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
TRD[0]+ TRD[0]–	39 41	19 20	Transmit and Receive Differential Pair 0	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occur simultaneously at TRD[0]±. In 10Base-T and 100Base-TX modes, TRD[0]± are used to transmit when operating in the MDI configuration and to receive when operating in the MDI-X configuration. The PHY automatically determines the appropriate MDI/MDI-X configuration.
TRD[1]+ TRD[1]–	45 47	21 22	Transmit/Receive Differential Pair 1	Connect this signal pair through a transformer to the media dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[1]±. In 10Base-T and 100Base-TX modes, TRD[1]± are used to receive when operating in the MDI configuration and to transmit when operating in the MDI-X configuration. The PHY automatically determines the appropriate MDI/MDI-X configuration.
TRD[2]+ TRD[2]–	54 56	28 29	Transmit/Receive Differential Pair 2	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[2]±. In 10Base-T and 100Base-TX modes, TRD[2]± are unused.
TRD[3]+ TRD[3]–	60 62	31 32	Transit/Receive Differential Pair 3	Connect this signal pair through a transformer to the media-dependent interface. In 1000Base-T mode, transmit and receive occurs simultaneously at TRD[3]±. In 10Base-T and 100Base-TX modes, TRD[3]± are unused.
RSET	52	26	Analog Reference Resistor	RSET sets an absolute value reference current for the transmitter. Connect this signal to analog ground through a precision 6.34 kΩ 1% resistor.

Hardware Interfaces (continued)

Clocking and Reset

Table 16. Clocking and Reset

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
CLK_IN	31	16	Reference Clock Input	Connect this signal to a 25 MHz clock input (CLK_IN) or a 25 MHz ± 50 ppm tolerance crystal (XTAL_1).
XTAL_1	31	16	Reference Crystal Input	
XTAL_2	32	17	Reference Crystal Input	Connect this signal to a 25 MHz ± 50 ppm tolerance crystal. Float this signal if an external clock is used (CLK_IN).
SYS_CLK	94	50	System Clock	Use this signal to supply a 125 MHz clock to the MAC. By default, the SYS_CLK output is disabled. The SYS_CLK output can be enabled by asserting the SYS_CLK_EN_N pin or via the management interface.
RESET_N	34	18	Reset	Drive RESET_N low for 1 μs to initiate a hardware reset. The ET1011 completes all reset operations within 5 ms of this signal returning to a high state. The configuration pins and the physical address configuration are read during a hardware reset.
COMA	25	12	Hardware Powerdown	Drive COMA high to initiate a hardware powerdown. The ET1011 completes all reset operations within 5 ms of this signal returning to a low state. All hardware functions are disabled during a hardware powerdown. The configuration pins and the physical address configuration are read during a hardware powerdown.

Hardware Interfaces (continued)

JTAG

The ET1011 has a standard *IEEE* 1149.1 JTAG test interface. The interface provides extensive test and diagnostics capability. It contains internal circuitry that allows the device to be controlled through the JTAG port to provide on-chip, in-circuit emulation.

The JTAG interface is a bidirectional serial interface with its own reset strobe (TRST_N). The reset strobe can be used independently to reset the JTAG state machine but must be used during a power-on reset (see Reset Timing on page 73). The only exception is when the JTAG interface is not being used. In this scenario, connect the reset strobe to ground to keep the interface in the reset state.

Table 17. JTAG Test Interface

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
TDI	16	7	Test Data Input	This signal is the JTAG serial input. All instructions and scanned data are input using this pin. This pin has an internal pull-up resistor.
TDO	17	8	Test Data Output	This signal is the JTAG serial output. Scanned data and status bits are output using this pin.This pin has an internal pull-up resistor.
TCK	10	2	Test Clock	This signal is the JTAG serial shift clock. It clocks all of the data that passes through the port on TDI and TDO.
TMS	15	6	Test Mode Select	This signal is the JTAG test mode control. This pin has an internal pull-up resistor.
TRST_N	14	5	Test Reset (Jtag Reset)	A high-to-low transition on this signal causes the JTAG TAP controller to enter the reset state. This pin has an internal pull-down resistor.

Regulator Control

The ET1011 has two on-chip regulator controllers. This allows the device to be powered from a single supply, either 3.3 V or 2.5 V. The on-chip regulator control circuits provide output control voltages that are used to control two external transistors and thus provide regulated 1.0 V and 2.5 V supplies.

Table 18. Regulator Control Interface

Pin Name	Pin # 128-TQFP	Pin # 68-MLCC	Pin Description	Functional Description
CTRL_1V0	79	40	Regulator Control for 1.0 V	This is the regulator output control voltage for the 1.0 V supply. It is used to control an external transistor and thus provide a regulated 1.0 V supply.
CTRL_2V5	78	39	Regulator Control for 2.5 V	This is the regulator output control voltage for the 2.5 V supply. It is used to control an external transistor and thus provide a regulated 2.5 V supply.

Hardware Interfaces (continued)

Regulator Control (continued)

The ET1011 digital and analog core operates at 1.0 V. The analog I/O operates at 2.5 V. The digital I/O can operate at either 3.3 V or 2.5 V. The GMII interface operates at 3.3 V and the RGMII interface operates at 2.5 V. The on-chip regulator control allows the device to be operated from a wide variety of external supply combinations. When more than one external supply is available, one or both of the regulator control circuits may be left unused. Table 19 lists example combinations of available external supplies and shows how the on-chip regulator control may be used to provide the required supplies.

Table 19. Supply Voltage Combinations

Available External Supplies	AVDDL	DVDD	AVDDH	DVDDIO	Description
3.3 V only	1.0	1.0	2.5	3.3 or 2.5	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 1.0 V and 2.5 V.
2.5 V only	1.0	1.0	2.5	2.5	Digital I/O is 2.5 V. Regulator control is used to provide 1.0 V.
3.3 V and 1.0 V	1.0	1.0	2.5	3.3 or 2.5	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 2.5 V.
2.5 V and 1.0 V	1.0	1.0	2.5	2.5	Digital I/O is 2.5 V. Regulator control is not required.
3.3 V and 2.5 V	1.0	1.0	2.5	3.3 or 2.5	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is used to provide 1.0 V.
3.3 V, 2.5 V, and 1.0 V	1.0	1.0	2.5	3.3 or 2.5	Digital I/O can be either 3.3 V or 2.5 V. Regulator control is not required.

Power, Ground, and No Connect

Table 20. Power, Ground, and No Connect

Pin Name	Pin Description	Functional Description
DVDDIO	V_{DD}	Digital I/O 3.3 V or 2.5 V supply.
DVDD	V_{DD}	Digital core 1.0 V supply.
DVSS	V_{SS}	Digital ground[1].
AVDDH	V_{DD}	Analog power 2.5 V.
AVDDL	V_{DD}	Analog power 1.0 V.
AVSS	V_{SS}	Analog ground[1].
NC	No Connect	Reserved—do not connect.

1. For the 68-MLCC, all AVSS and DVSS pins share a common ground pin (exposed pad) in the center of the device.

Cable Diagnostics

The ET1011 has on-chip cable diagnostics. The cable analysis uses two distinct methods for evaluating the cable: link analysis and time domain reflectometry (TDR) analysis. This analysis can be used to detect cable impairments that may be preventing a gigabit link or affecting performance.

When there is a link active, the link analysis can detect cable length, link quality, pair skew, pair swaps (MDI/MDI-X configuration), and polarity reversal. When there is no link, TDR can detect cable faults (open circuit, short circuit), distance to the fault, pair fault is on, cable length, pair skew, and excessive crosstalk. Table 21 summarizes the specifications of the cable diagnostic functions.

Table 21. Cable Diagnostic Functions

Feature	Description	10	100	1000	Term	Unterm	Analysis
Detection of Cable Fault on Any Pair	Cable open	—	—	—	✓	✓	Line Probing
	Cable short	—	—	—	✓	✓	
	Indicate distance to fault	—	—	—	±2 m	±2 m	
	Pair swaps	✓	✓	✓[1]	—	—	Link Analysis
Detect Polarity Reversal	—	✓	—[2]	✓	—	—	Link Analysis
Good Cable with Link	Indicate length	—	±5 m	±5 m	—	—	Link Analysis
Good Cable Without Link	Indicate length	—	—	—	±5 m[3]	±2 m	Line Probing
Pair Skew with Link	Detect excessive, >50 ns	—	—	✓	—	—	Link Analysis
Pair Skew Without Link	Detect excessive, >50 ns	—	—	—	✓[3]	✓	Line Probing
Excessive Crosstalk	Cable quality or split pairs	—	—	—	✓	✓	Line Probing

1. Pair swaps on C and D as well as pairs A and B are reported.
2. Polarity reversal in 100Base-TX is not detected because MLT-3 signaling is polarity insensitive.
3. If the magnitude of the peak reflection is greater than 15% of an open circuit.

Register Description

Register Address Map

Table 22. Register Address Map

Address	Description
0	Control register.
1	Status register.
2	PHY identifier register 1.
3	PHY identifier register 2.
4	Autonegotiation advertisement register.
5	Autonegotiation link partner ability register.
6	Autonegotiation expansion register.
7	Autonegotiation next page transmit register.
8	Link partner next page register.
9	1000Base-T control register.
10	1000Base-T status register.
11—14	Reserved.
15	Extended status register.
16—18	Reserved.
19	Loopback control register.
20	Reserved.
21	Register management (MI) control register.
22	PHY configuration register.
23	PHY control register.
24	Interrupt mask register.
25	Interrupt status register.
26	PHY status register.
27	LED control register 1.
28	LED control register 2.
29-31	Reserved.

Table 23. Register Type Definition

Type	Description
LL	Latching low.
LH	Latching high.
R/W	Read write. Register can be read or written.
RO	Read only. Register is read only. Writes to register are ignored.
SC	Self-clearing. Register is self-clearing; if a one is written, the register will automatically clear to zero after the function is completed.

Register Description (continued)

Register Functions/Settings

Table 24. Control Register—Address 0

Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reset	1 = PHY reset. 0 = Normal operation.	R/W SC	0	1
14	Loopback	1 = Enable loopback. 0 = Disable loopback.	R/W	0	2
13	Speed Selection (LSB)	Bit 6,13. 11 = Reserved. 10 = 1000 Mbits/s. 01 = 100 Mbits/s. 00 = 10 Mbits/s.	R/W	SPEED_1000 SPEED_100 SPEED_10	3
12	Autonegotiation Enable	1 = Enable autonegotiation process. 0 = Disable autonegotiation process.	R/W	1	4
11	Powerdown	1 = Powerdown. 0 = Normal operation.	R/W	0	—
10	Isolate	1 = Isolate PHY from MII. 0 = Normal operation.	R/W	0	5
9	Restart Autonegotiation	1 = Restart autonegotiation process. 0 = Normal operation.	R/W SC	0	—
8	Duplex Mode	1 = Full duplex. 0 = Half duplex.	R/W	DUPLEX	6
7	Collision Test	1 = Enable collision test. 0 = Disable collision test.	R/W	0	7
6	Speed Selection (MSB)	See bit 13.	R/W	See bit 13	3
5:0	Reserved	—	RO	0	—

1. The reset bit is automatically cleared upon completion of the reset sequence. This bit is set to 1 during reset.
2. This is the master enable for digital and analog loopback as defined by the standard. The exact type of loopback is determined by the loopback control register (address 19).
3. The speed selection address 0 bits 13 and 6 may be used to configure the link manually. Setting these bits has no effect unless address 0 bit 12 is clear. The speed bits are set by the SPEED_10, SPEED_100, and SPEED_1000 pins at reset.
4. When this bit is cleared, the link configuration is determined manually.
5. Setting this bit isolates the PHY from the MII, GMII, or RGMII interfaces.
6. This bit may be used to configure the link manually. Setting this bit has no effect unless address 0 bit 12 is clear. Duplex is set on reset by the DUPLEX pin.
7. Enables *IEEE* 22.2.4.1.9 collision test.

Register Description (continued)

Table 25. Status Register—Address 1

Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	100Base-T4	0 = Not 100Base-T4 capable.	RO	0	1
14	100Base-X Full Duplex	1 = 100Base-X full-duplex capable. 0 = Not 100Base-X full-duplex capable.	RO	SPEED_100 and DUPLEX	2
13	100Base-X Half Duplex	1 = 100Base-X half-duplex capable. 0 = Not 100Base-X half-duplex capable.	RO	SPEED_100	2
12	10Base-T Full-Duplex	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	RO	SPEED_10 and DUPLEX	2
11	10Base-T Half-Duplex	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	RO	SPEED_10	2
10	100Base-T2 Full-Duplex	0 = Not 100Base-T2 full-duplex capable.	RO	0	—
9	100Base-T2 Half-Duplex	0 = Not 100Base-T2 half-duplex capable.	RO	0	—
8	Extended Status	1 = Extended status information in register 0Fh.	RO	1	—
7	Reserved	—	RO	—	—
6	MF Preamble Suppression	1 = Preamble suppressed management frames accepted.	RO	1	—
5	Autonegotiation Complete	1 = Autonegotiation process complete. 0 = Autonegotiation process not complete.	RO	0	3
4	Remote Fault	1 = Remote fault detected. 0 = No remote fault detected.	RO LH	0	4
3	Autonegotiation Ability	1 = Autonegotiation capable. 0 = Not autonegotiation capable.	RO	1	—
2	Link Status	1 = Link is up. 0 = Link is down.	RO LL	0	5
1	Jabber Detect	1 = Jabber condition detected. 0 = No jabber condition detected.	RO LH	0	—
0	Extended Capability	1 = Extended register capabilities.	RO	1	6

1. The ET1011 does not support 100Base-T4 or 100Base-T2, therefore, these register bits will always be set to zero.
2. These bits receive values from the SPEED_10, SPEED_100, SPEED_1000, and DUPLEX pins during reset as follows:

Register Bit	Configuration Pin Combination
14	SPEED_100 and DUPLEX
13	SPEED_100
12	SPEED_10 and DUPLEX
11	SPEED_10

3. Upon completion of autonegotiation, this bit becomes set.
4. This bit indicates that a remote fault has been detected. Once set, it remains set until it is cleared by reading register 1 via the management interface or by PHY reset.
5. This bit indicates that a valid link has been established. Once cleared due to link failure, this bit will remain cleared until register 1 is read via the management interface.
6. Indicates that the PHY provides an extended set of capabilities that may be accessed through the extended register set. For a PHY that incorporates a GMII/RGMII, the extended register set consists of all management registers except registers 0, 1, and 15.

Register Description (continued)

Table 26. PHY Identifier Register 1—Address 2

PHY Identifier Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	PHY Identifier Bits 3:18	Organizationally unique identifier (OUI), bits 3:18.	RO	0x0282	1

Table 27. PHY Identifier Register 2—Address 3

PHY Identifier Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:10	PHY Identifier Bits 19:24	Organizationally unique identifier (OUI), bits 19:24.	RO	111100	1
9:4	Model Number	Model number = 1.	RO	000001	—
3:0	Revision Number	Revision number = 2.	RO	0010	—

1. Agere's OUI is 00-05-3D.

Register Description (continued)

Table 28. Autonegotiation Advertisement Register—Address 4

Autonegotiation Advertisement Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Advertise next page ability supported. 0 = Advertise next page ability not supported.	R/W	0	—
14	Reserved	—	RO	0	—
13	Remote Fault	1 = Advertise remote fault detected. 0 = Advertise no remote fault detected.	R/W	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Advertise asymmetric pause ability. 0 = Advertise no asymmetric pause ability.	R/W	PAUSE	1
10	Pause Capable	1 = Capable of full-duplex pause operation. 0 = Not capable of pause operation.	R/W	PAUSE	1
9	100Base-T4 Capability	1 = 100Base-T4 capable. 0 = Not 100Base-T4 capable.	R/W	0	2
8	100Base-TX Full-Duplex Capable	1 = 100Base-TX full-duplex capable. 0 = Not 100Base-TX full-duplex capable.	R/W	SPEED_100 and DUPLEX	3
7	100Base-TX Half-Duplex Capable	1 = 100Base-TX half-duplex capable. 0 = Not 100Base-TX half-duplex capable.	R/W	SPEED_100	3
6	10Base-T Full-Duplex Capable	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	R/W	SPEED_10 and DUPLEX	3
5	10Base-T Half-Duplex Capable	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	R/W	SPEED_10	3
4:0	Selector Field	00001 = IEEE 802.3 CSMA/CD.	R/W	00001	—

1. Value read from PAUSE on reset.
2. The ET1011 does not support 100Base-T4, so the default value of this register bit is zero.
3. These bits receive values from the configuration pins upon reset as follows:

Register Bit	Configuration Pin Combination
8	SPEED_100 and DUPLEX
7	SPEED_100
6	SPEED_10 and DUPLEX
5	SPEED_10

Note: Any write to this register prior to the completion of autonegotiation is followed by a restart of autonegotiation. Also note that this register is not updated following autonegotiation.

Register Description (continued)

Table 29. Autonegotiation Link Partner Ability Register—Address 5

Autonegotiation Link Partner Ability Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next page	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	RO	0	—
14	Acknowledge	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	RO	0	—
13	Remote Fault	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	RO	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Link partner desired asymmetric pause. 0 = Link partner does not desire asymmetric pause.	RO	0	—
10	Pause Capable	1 = Link partner capable of full-duplex pause operation. 0 = Link partner is not capable of pause operation.	RO	0	—
9	100Base-T4 Capability	1 = Link partner is 100Base-T4 capable. 0 = Link partner is not 100Base-T4 capable.	RO	0	—
8	100Base-TX Full-Duplex Capable	1 = Link partner is 100Base-TX full-duplex capable. 0 = Link partner is not 100Base-TX full-duplex capable.	RO	0	—
7	100Base-TX Half-Duplex Capable	1 = Link partner is 100Base-TX half-duplex capable. 0 = Link partner is not 100Base-TX half-duplex capable.	RO	0	—
6	10Base-T Full-Duplex Capable	1 = Link partner is 10Base-T full-duplex capable. 0 = Link partner is not 10Base-T full-duplex capable.	RO	0	—
5	10Base-T Half-Duplex Capable	1 = Link partner is 10Base-T half-duplex capable. 0 = Link partner is not 10Base-T half-duplex capable.	RO	0	—
4:0	Protocol Selector Field	Link partner protocol selector field.	RO	0	—

Register Description (continued)

Table 30. Autonegotiation Expansion Register—Address 6

Autonegotiation Expansion Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:5	Reserved	—	RO	—	—
4	Parallel Detection Fault	1 = Parallel link fault detected. 0 = Parallel link fault not detected.	RO LH	0	—
3	Link Partner Next Page Ability	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	RO	0	—
2	Next Page Capability	1 = Local device has next page capability. 0 = Local device does not have next page capability.	RO LH	1	—
1	Page Received	1 = New page has been received from link partner. 0 = New page has not been received.	RO LH	0	—
0	Link Partner Autonegotiation Ability	1 = Link partner has autonegotiation capability. 0 = Link partner does not have autonegotiation capability.	RO	0	—

Table 31. Autonegotiation Next Page Transmit Register—Address 7

Autonegotiation Next Page Transmit Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	R/W	0	—
14	Reserved	—	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	1	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	1	—

Register Description (continued)

Table 32. Link Partner Next Page Register—Address 8

Link Partner Next Page Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	RO	0	—
14	Acknowledge	1 = Acknowledge. 0 = No acknowledge.	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	0	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	0	—

Register Description (continued)

Table 33. 1000 Base-T Control Register—Address 9

1000Base-T Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:13	Test Mode	000 = Normal mode. 001 = Test mode 1—transmit waveform test. 010 = Test mode 2—master transmit jitter test. 011 = Test mode 3—slave transmit jitter test (slave mode). 100 = Test mode 4—transmit distortion test. 101, 110, 111 = Reserved.	R/W	000	—
12	Master/Slave Configuration Enable	1 = Enable master/slave configuration. 0 = Automatic master/slave configuration.	R/W	0	—
11	Master/Slave Configuration Value	1 = Configure PHY as master. 0 = Configure PHY as slave.	R/W	MAS_CFG	1
10	Port Type	1 = Prefer multiport device (master). 0 = Prefer single-port device (slave).	R/W	MAS_CFG	2
9	Advertise 1000Base-T Full-duplex Capability	1 = Advertise 1000Base-T full-duplex capability. 0 = Advertise no 1000Base-T full-duplex capability.	R/W	SPEED_1000 and DUPLEX	3
8	Advertise 1000Base-T Half-duplex Capability	1 = Advertise 1000Base-T half-duplex capability. 0 = Advertise no 1000Base-T half-duplex capability.	R/W	SPEED_1000	4
7:0	Reserved	—	RO	9.7:0	—

1. Value read from MAS_CFG pin at reset. Setting this bit has no effect unless address 9 bit 12 is set.
2. Value read from MAS_CFG at reset.
3. Value is a result of (SPEED_1000 and DUPLEX) pins at reset.
4. Value read from SPEED_1000 pin at reset.

Note: Logically, bits 12:8 may be regarded as an extension of the technology ability field of register 4.

Register Description (continued)

Table 34. 1000Base-T Status Register—Address 10

1000Base-T Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Master/ Slave Configuration Fault	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	RO, LH, SC	0	1
14	Master/Slave Configuration Resolution	1 = Local PHY resolved to master. 0 = Local PHY resolved to slave.	RO	0	2
13	Local Receiver Status	1 = Local receiver okay. 0 = Local receiver not okay.	RO	0	—
12	Remote Receiver Status	1 = Remote receiver okay. 0 = Remote receiver not okay.	RO	0	—
11	Link Partner 1000Base-T Full-duplex Capability	1 = Link partner is capable of 1000Base-T full duplex. 0 = Link partner not 1000Base-T full-duplex capable.	RO	0	3
10	Link Partner 1000Base-T Half-duplex Capability	1 = Link partner is 1000Base-T half-duplex capable. 0 = Link partner not 1000Base-T half-duplex capable.	RO	0	3
9:8	Reserved	—	RO		—
7:0	Idle Error Count	MSB of idle error count.	RO	0	4

1. Once set, this bit remains set until cleared by the following actions:
   - Read of register 10 via the management interface.
   - Reset.
   - Completion of autonegotiation.
   - Enable of autonegotiation.
2. This bit is not valid when bit 15 is set.
3. Note that logically, bits 11:10 may be regarded as an extension of the technology ability field of register 5.
4. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and both local and remote receiver status are OK. The count is held at 255 in the event of overflow and is reset to zero by reading register 10 via the management interface or by reset.

Register Description (continued)

Table 35. Reserved Registers—Addresses 11—14

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Table 36. Extended Status Register—Address 15

Extended Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	1000Base-X Full-duplex	0 = Not 1000Base-X full-duplex capable.	RO	0	1
14	1000Base-X Half-duplex	0 = Not 1000Base-X half-duplex capable.	RO	0	—
13	1000Base-T Full-duplex	1 = 1000Base-T full-duplex capable. 0 = Not 1000Base-T full-duplex capable.	RO	SPEED_1000 and DUPLEX	2
12	1000Base-T Half-duplex	1 = 1000Base-T half-duplex capable. 0 = Not 1000Base-T half-duplex capable.	RO	SPEED_1000	3
11:0	Reserved	—	RO	0	—

1. 1000Base-X not supported.
2. Value is a result of (SPEED_1000 and DUPLEX) pins at reset.
3. Value read from SPEED_1000 pin at reset.

Table 37. Reserved Registers—Addresses 16—18

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Register Description (continued)

Table 38. Loopback Control Register—Address 19

Loopback Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	MII Enable	1 = Use MII loopback. 0 = MII loopback disabled.	R/W	1	—
14	PCS Enable	1 = Use PCS loopback. 0 = PCS loopback disabled.	R/W	0	—
13	PMD Enable	1 = Use PMD loopback. 0 = PMD loopback disabled.	R/W	0	1
12	All Digital Enable	1 = Use all digital loopback. 0 = All digital loopback disabled.	R/W	0	—
11	Replica Enable	1 = Use replica loopback. 0 = Replica loopback disabled.	R/W	0	—
10	Line Driver Enable	1 = Use line driver loopback. 0 = Line driver loopback disabled.	R/W	0	—
9:0	Reserved	—	—	—	—

1. Only for 100Base-TX.

Register Description (continued)

Table 39. Reserved Registers—Address 20

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Table 40. Management Interface (MI) Control Register—Address 21

Management Interface (MI) Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:11	Reserved	—	—	—	—
10:4	MI Error Counter	MI transaction error count (00-7F).	RO	00	—
3	Reserved	—	—	—	—
2	Ignore 10G Frames	1 = Management frames with ST = <00> are ignored. 0 = Management frames with ST = <00> are treated as wrong frames	R/W	1	—
1	Reserved	—	—	—	—
0	Preamble Suppression Enable	1 = MI preamble is ignored. 0 = MI preamble is required.	R/W	1	—

Register Description (continued)

Table 41. PHY Configuration Register—Address 22

PHY Configuration Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	CRS Transmit Enable	1 = Enable CRS on transmit in half-duplex mode. 0 = Disable CRS on transmit.	R/W	0	—
14	Reserved	—	—	—	—
13:12	Transmit FIFO depth (1000Base-T)	00 = ±8. 01 = ±16. 10 = ±24. 11 = ±32.	R/W	01	—
11:10	Automatic Speed Downshift Mode	00 = Disable automatic speed downshift. 01 = 10Base-T downshift enabled. 10 = 100Base-TX downshift enabled. 11 = 100Base-TX and 10Base-T enabled.	R/W	11	1
9	TBI Detect Select	1 = CRS pin outputs comma detect. 0 = CRS pin outputs link status detect	R/W	0	—
8	TBI Rate Select	1 = Output 125 MHz clock on RX_CLK while COL is held low (full rate). 0 = Output even/odd clocks on RX_CLK/COL	R/W	0	—
7	Alternate Next-Page	1 = Enables manual control of 1000Base-T next pages only. 0 = Normal operation of 1000Base-T next page exchange	R/W	0	—
6	Group MDIO Mode Enable	1 = Enable group MDIO mode. 0 = Disable Group MDIO mode.	R/W	0	—
5	Transmit Clock Enable	1 = Enable output of 1000Base-T transmit clock (TX_CLK pin). 0 = Disable output.	R/W	0	—
4	System Clock Enable	1 = Enable output of 125 MHz reference clock (SYS_CLK pin). 0 = Disable output of 125 MHz reference clock.	R/W	$\overline{\text{SYS\_CLK\_EN\_N}}$	2
3	Reserved	—	—	—	—
2:0	MAC Interface Mode Select	000 = GMII/MII 001 = TBI 010 = GMII/MII clocked by GTX_CLK instead of TX_CLK 011 = Reserved. 100 = RGMII/RMII (trace delay). 101 = RTBI (trace delay). 110 = RGMII/RMII (DLL delay). 111 = RTBI (DLL delay).	R/W	MAC_IF_SEL [2:0]	3

1. If automatic speed downshift is enabled and the PHY fails to autonegotiate at 1000Base-T, the PHY will fall back to attempt connection at 100Base-TX and, subsequently, 10Base-T. This cycle will repeat. If the link is broken at any speed, the PHY will restart this process by reattempting connection at the highest possible speed (e.g., 1000Base-T).
2. Value is read from inversion of SYS_CLK_EN_N at reset.
3. For the 68-pin MLCC, only RGMII/RMII and RTBI modes/options are supported.

Register Description (continued)

Table 42. PHY Control Register—Address 23

PHY Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reserved	—	—	—	—
14	TDR_EN	1 = Enable cable diagnostics. 0 = Disable cable diagnostics.	R/W	0	1
13	Reserved	—	—	—	—
12:11	Automatic Speed Downshift Attempts Before Downshift	00 = 1. 01 = 2. 10 = 3. 11 = 4.	R/W	01	—
10:6	Reserved	—	—	—	—
5	Jabber (10Base-T)	1 = Disable jabber. 0 = Normal operation.	R/W	0	—
4	SQE (10Base-T)	1 = Enable heartbeat. 0 = Disable heartbeat.	R/W	0	—
3	TP_LOOPBACK (10Base-T)	1 = Disable TP loopback during half-duplex. 0 = Normal operation.	R/W	1	—
2	Preamble Generation Enable	1 = Enable preamble generation for 10Base-T. 0 = Disable preamble generation for 10Base-T.	R/W	1	—
1	Reserved	—	—	—	—
0	Force Interrupt	1 = Assert MDINT_N pin. 0 = Deassert MDINT_N pin.	R/W	0	—

1. If TDR is enabled, the PHY can implement cable diagnostics and IP phone detection.

Register Description (continued)

Table 43. Interrupt Mask Register—Address 24

Interrupt Mask Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:10	Reserved	—	—	—	—
9	MDIO Sync Lost	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
8	Autonegotiation Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
7	High Bit-Error Rate	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
6	Next Page Received	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
5	Error Counter Full	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
4	FIFO Overflow/ Underflow	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
3	Receive Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
2	Link Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
1	Automatic Speed Downshift	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
0	Interrupt Enable	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—

Register Description (continued)

Table 44. Interrupt Status Register—Address 25

Interrupt Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:10	Reserved	—	—	—	—
9	MDIO Sync Lost	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	1
8	Autonegotiation Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
7	High Bit-Error Rate	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
6	Next Page Received	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
5	Error Counter Full	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
4	FIFO Overflow/ Underflow	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
3	Receive Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
2	Link Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
1	Automatic Speed Downshift	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
0	MII Interrupt Pending	1 = Interrupt pending. 0 = No interrupt pending.	RO SC	0	2

1. If the management frame preamble is suppressed (MF preamble suppression, register 0, bit 6), it is possible for the PHY to lose synchronization if there is a glitch at the interface. The PHY can recover if a single frame with a preamble is sent to the PHY. The MDIO sync lost interrupt can be used to detect loss of synchronization and thus enable recovery.
2. The MII interrupt pending bit is not masked by interrupt enable bit (interrupt mask register, address 24 bit 0). This bit is inverted and provided as an output on MDINT_N, gated by interrupt enable bit.

Register Description (continued)

Table 45. PHY Status Register—Address 26

PHY Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reserved	—	—	—	—
14:13	Autonegotiation Fault Status	10 = Master/slave autonegotiation fault. 01 = Parallel detect autonegotiation fault. 00 = No autonegotiation fault.	RO	00	—
12	Autonegotiation Status	1 = Autonegotiation is complete. 0 = Autonegotiation not complete.	RO	0	—
11	MDI-X Status	1 = MDI-X configuration. 0 = MDI configuration.	RO	0	—
10	Polarity Status	1 = Polarity is normal (10Base-T only). 0 = Polarity is inverted (10Base-T only).	RO	1	—
9:8	Speed Status	11 = Undetermined. 10 = 1000Base-T. 01 = 100Base-TX. 00 = 10Base-T.	RO	11	—
7	Duplex Status	1 = Full duplex. 0 = Half duplex.	RO	0	—
6	Link Status	1 = Link is up. 0 = Link is down.	RO	0	—
5	Transmit Status	1 = PHY is transmitting a packet. 0 = PHY is not transmitting a packet.	RO	0	—
4	Receive Status	1 = PHY is receiving a packet. 0 = PHY is not receiving a packet.	RO	0	—
3	Collision Status	1 = Collision is occurring. 0 = Collision not occurring.	RO	0	—
2	Autonegotiation Enabled	1 = Both partners have autonegotiation enabled. 0 = Both partners do not have autonegotiation enabled.	RO	0	—
1	PAUSE Enabled	1 = Link partner advertised PAUSE mode enabled. 0 = Link partner advertised PAUSE mode disabled.	RO	0	—
0	Asymmetric Direction	1 = Link partner advertised direction is symmetric. 0 = Link partner advertised that direction is asymmetric.	RO	0	—

Register Description (continued)

Table 46. LED Control Register 1—Address 27

LED Control Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	Reserved	—	—	—	—
13:12	Duplex Indication LED	00 = Full duplex. 01 = Blink. 10 = On. 11 = Off.	R/W	00	1
11:10	10Base-T LED	00 = 10Base-T operation. 01 = Blink. 10 = On. 11 = Off.	R/W	00	1
9:8	Collision Indication LED	00 = Collision indication. 01 = Blink. 10 = On. 11 = Off.	R/W	00	1
7:6	Reserved	—	—	—	—
5.4	Reserved	—	—	—	—
3:2	LED Pulse Duration	00 = Stretch LED events to 28 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00	—
1	Pulse Stretch 1	1 = Enable pulse stretching of LED functions: 1000Base-T, 100Base-TX, 10Base-T, link, and duplex. 0 = Disable pulse stretching of LED functions: 1000Base-T, 100Base-TX, 10Base-T, link, and duplex.	R/W	0	—
0	Pulse Stretch 0	1 = Enable pulse stretching of LED functions: transmit activity, receive activity, and collision. 0 = Disable pulse stretching of LED functions: transmit activity, receive activity, and collision.	R/W	1	—

1. Not applicable in the 68-pin MLCC.

Register Description (continued)

Table 47. LED Control Register 2—Address 28

LED Control Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:12	Transmit/ Receive LED	0000 = 1000Base-T. 0001 = 100Base-TX. 0010 = 10Base-T. 0011 = 1000Base-T on, 100Base-TX blink. 0100 = Link established. 0101 = Transmit. 0110 = Receive. 0111 = Transmit or receive activity. 1000 = Full duplex. 1001 = Collision. 1010 = Link established (on) and activity (blink). 1011 = Link established (on) and receive (blink). 1100 = Full duplex (on) and collision (blink). 1101 = Blink. 1110 = On. 1111 = Off.	R/W	0111	1
11:8	Link LED	As per 15:12.	R/W	0100	—
7:4	100Base-TX LED	As per 15:12.	R/W	0001	1
3:0	1000Base-T LED	As per 15:12.	R/W	0000	—

1. Not applicable in the 68-MLCC.

Table 48. Reserved Registers—Addresses 29—31

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 49. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	—	4.2	V
Supply Voltage (1.0 V analog)	AV_{DDL}	—	1.2	V
Supply Voltage (3.3 V/2.5 V digital)	DV_{DDIO}	—	4.2	V
Supply Voltage (1.0 V digital)	V_{DD}	—	1.2	V
ESD Protection	V_{ESD}	—	2000	V
Storage Temperature	T_{STORE}	–40	125	° C

Recommended Operating Conditions

Table 50. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	2.38	2.62	V
Supply Voltage (1.0 V analog)	AV_{DDL}	0.95	1.05	V
Supply Voltage (3.3 V digital)[1]	DV_{DDIO}	3.14	3.46	V
Supply Voltage (2.5 V digital)[1]	DV_{DDIO}	2.38	2.62	V
Supply Voltage (1.0 V digital)	V_{DD}	0.95	1.05	V
Ambient Operating Temperature	T_A	0	70	° C
Maximum Junction Temperature	T_J	0	125	° C
Thermal Characteristics, 128 TQFP (JDEC 3 in. x 4.5 in. 4-layer PCB, 0 m/s airflow)	T_{JA}	TBD	TBD	° C/W
Thermal Characteristics, 68 MLCC (JDEC 3 in. x 4.5 in. 4-layer PCB, 0 m/s airflow)	T_{JA}	TBD	TBD	° C/W

1. The part can operate at either 3.3 V (typically for an GMII interface) or 2.5 V (typically for an RGMII interface).

Electrical Specifications (continued)

Device Electrical Characteristics

Table 51. Device Characteristics—3.3 V Digital I/O Supply (DV_{DDIO})

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage (GMII input pins)	V_{IL}	–0.3	—	0.8	V
Input Low Voltage (all other digital input pins)	V_{IL}	–0.3	—	0.8	V
Input High Voltage (GMII input pins)	V_{IH}	2.0	—	3.6	V
Input High Voltage (all other digital input pins)	V_{IH}	2.0	—	3.6	V
Output Low Voltage (GMII output pins)	V_{OL}	—	—	0.4	V
Output Low Voltage (all other digital output pins)	V_{OL}	—	—	0.4	V
Output High Voltage (GMII output pins)	V_{OH}	2.4	—	—	V
Output High Voltage (all other digital output pins)	V_{OH}	2.4	—	—	V
Differential Output Voltage (analog MDI pins 1000Base-T)	V_{ODIFF}	0.67	0.75	0.82	V
Differential Output Voltage (analog MDI pins 100Base-TX)	V_{ODIFF}	0.95	1.0	1.05	V
Differential Output Voltage (analog MDI pins 10Base-T)	V_{ODIFF}	2.2	2.5	2.8	V
Bias Voltage	V_{BIAS}	—	1.2	—	V

Table 52. Device Characteristics—2.5 V Digital I/O Supply (DV_{DDIO})

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage (GMII input pins)	V_{IL}	–0.3	—	0.7	V
Input Low Voltage (all other digital input pins)	V_{IL}	–0.3	—	0.7	V
Input High Voltage (GMII input pins)	V_{IH}	1.7	—	2.8	V
Input High Voltage (all other digital input pins)	V_{IH}	1.7	—	2.8	V
Output Low Voltage (GMII output pins)	V_{OL}	—	—	0.4	V
Output Low Voltage (all other digital output pins)	V_{OL}	—	—	0.4	V
Output High Voltage (GMII output pins)	V_{OH}	2.0	—	—	V
Output High Voltage (all other digital output pins)	V_{OH}	2.0	—	—	V
Differential Output Voltage (analog MDI pins 1000Base-T)	V_{ODIFF}	0.67	0.75	0.82	V
Differential Output Voltage (analog MDI pins 100Base-TX)	V_{ODIFF}	0.95	1.0	1.05	V
Differential Output Voltage (analog MDI pins 10Base-T)	V_{ODIFF}	2.2	2.5	2.8	V
Bias Voltage	V_{BIAS}	—	1.2	—	V

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 53. Current Consumption GMII/RGMII 1000Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (3.3 V/2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA

Table 54. Current Consumption MII/RMII 100Base-TX

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (3.3 V/2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA

Table 55. Current Consumption MII/RMII 10Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (3.3 V/2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA

Timing Specification

GMII 1000Base-T Transmit Timing (128-pin TQFP only)

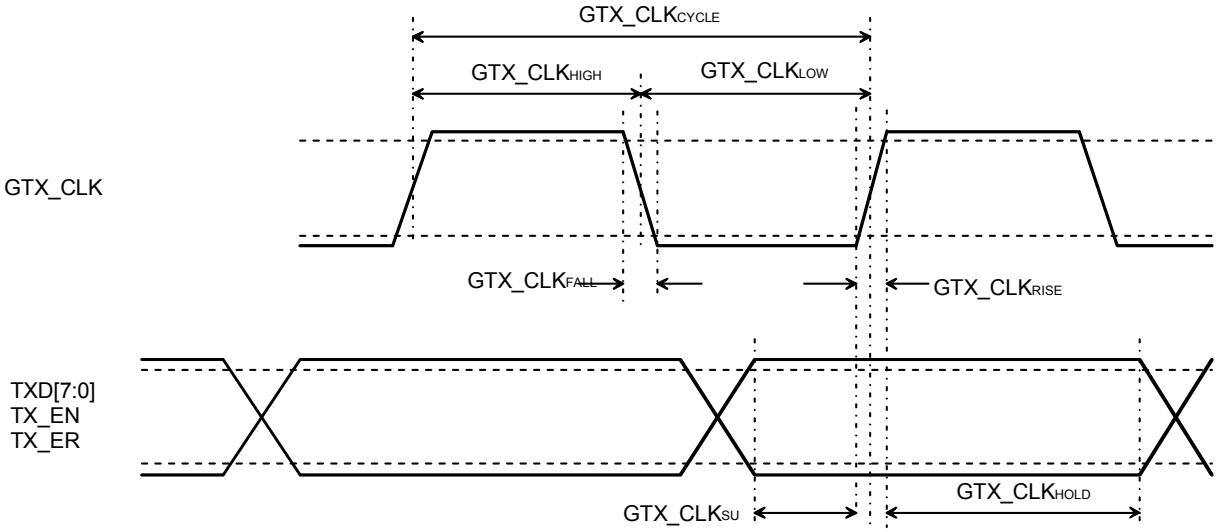


Figure 14. GMII 1000Base-T Transmit Timing

Table 56. GMII 1000Base-T Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
GTX_CLK Cycle Time	GTX_CLKCYCLE	7.5	—	8.5	ns
GTX_CLK High Time	GTX_CLKHIGH	2.5	—	—	ns
GTX_CLK Low Time	GTX_CLKLOW	2.5	—	—	ns
GTX_CLK Rise Time	GTX_CLKRISE	—	—	1.0	ns
GTX_CLK Fall Time	GTX_CLKFALL	—	—	1.0	ns
GMII Input Signal Setup Time to GTX_CLK	GTX_CLKSU	2.0	—	—	ns
GMII Input Signal Hold Time to GTX_CLK	GTX_CLKHOLD	0.0	—	—	ns

Timing Specification (continued)

GMII 1000Base-T Receive Timing (128-pin TQFP only)

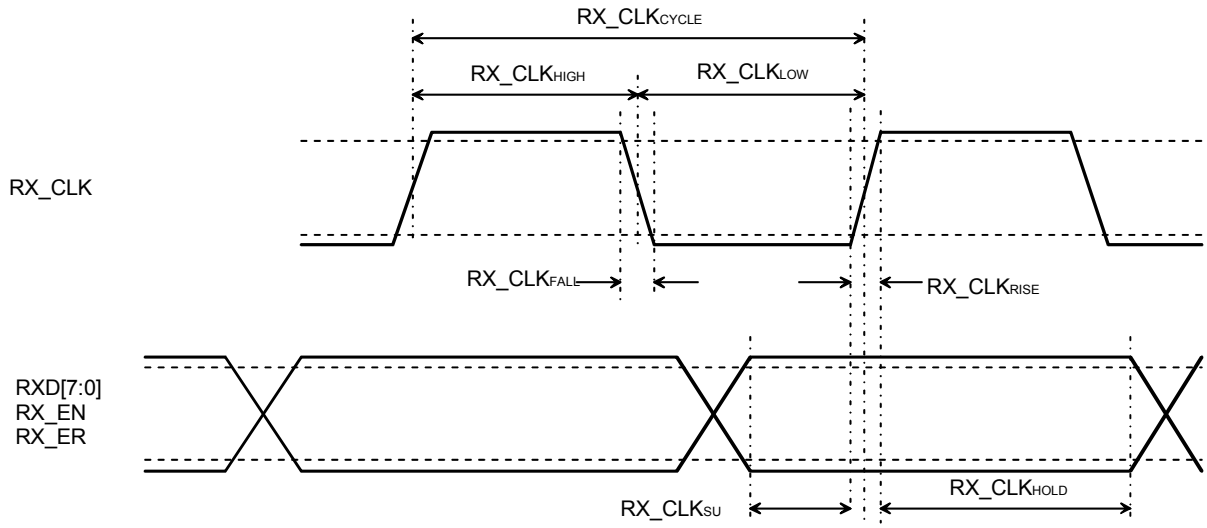


Figure 15. GMII 1000Base-T Receive Timing

Table 57. GMII 1000Base-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Cycle Time	RX_CLK_{CYCLE}	7.5	8.0	—	ns
RX_CLK High Time	RX_CLK_{HIGH}	2.5	—	—	ns
RX_CLK Low Time	RX_CLK_{LOW}	2.5	—	—	ns
RX_CLK Rise Time	RTX_CLK_{RISE}	—	—	1.0	ns
RX_CLK Fall Time	RX_CLK_{FALL}	—	—	1.0	ns
GMII Output Signal Setup Time to RX_CLK	RX_CLK_{SU}	2.5	—	—	ns
GMII Output Signal Hold Time to RX_CLK	RX_CLK_{HOLD}	0.5	—	—	ns

Timing Specification (continued)

RGMII 1000Base-T Transmit Timing

Trace Delay

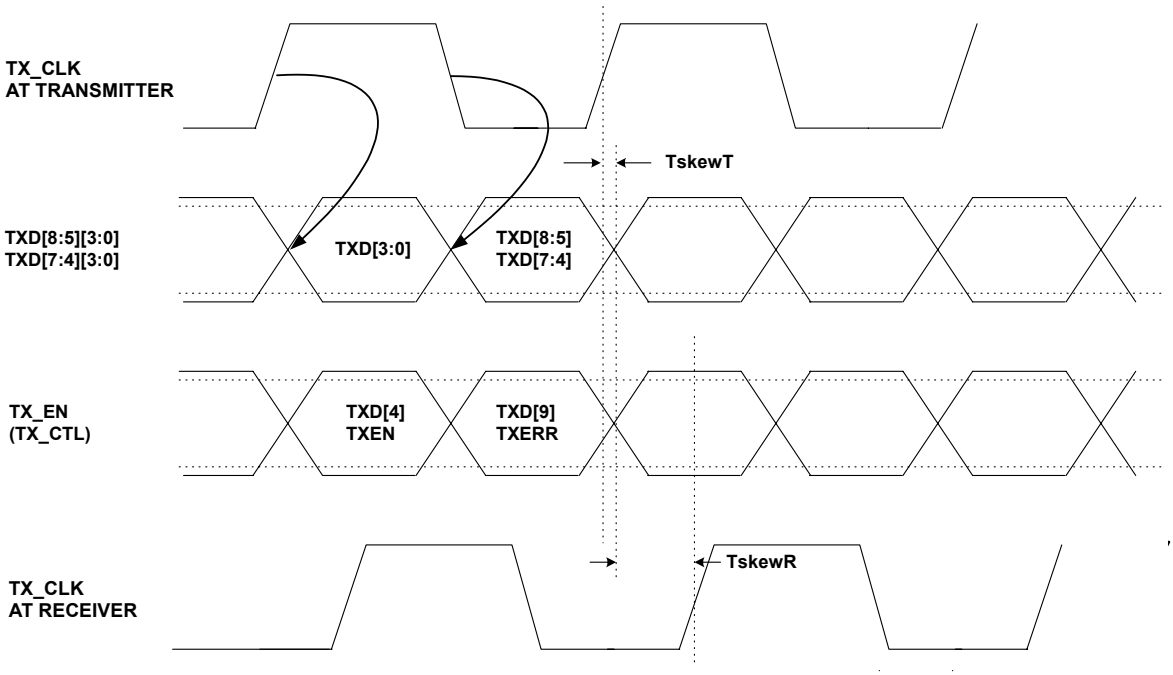


Figure 16. RGMII 1000Base-T Transmit Timing—Trace Delay

Table 58. RGMII 1000Base-T Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Output Skew (at transmitter)—Trace Delay[1]	TskewT	–500	0	500	ps
Data to Clock Input Skew (at receiver)—Trace Delay[1]	TskewR	1	1.8	2.6	ns
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns
Duty Cycle for Gigabit[3]	Duty_G	45	50	55	%
Duty Cycle for 10Base-T/100Base-TX[3]	Duty_T	40	50	60	%
Rise/Fall Time (20%—80%)	Tr/Tf	—	—	0.75	ns

1. This implies that PCB design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. To enable internal delay, see MII register 22 bits 2:0.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specification (continued)

Internal Delay

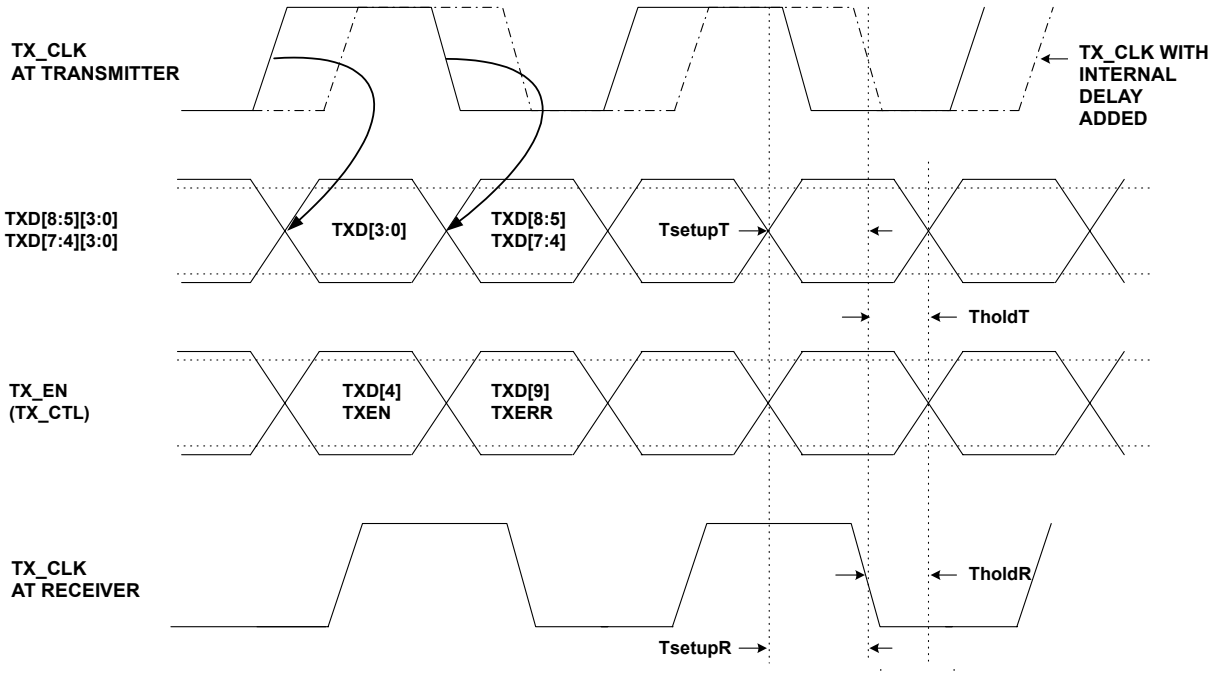


Figure 17. RGMII 1000Base-T Transmit Timing—Internal Delay

Table 59. RGMII 1000Base-T Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Output Setup (at transmitter—integrated delay)[1]	TsetupT	1.2	2.0	—	ns
Clock to Data Output Hold (at transmitter—integrated delay)[1]	TholdT	1.2	2.0	—	ns
Data to Clock Input Setup (at receiver—integrated delay)[1]	TsetupR	1.0	2.0	—	ns
Data to Clock Input Setup (at receiver—integrated delay)[1]	TholdR	1.0	2.0	—	ns
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns
Duty Cycle for Gigabit[3]	Duty_G	45	50	55	%
Duty Cycle for 10Base-T/100Base-TX[3]	Duty_T	40	50	60	%
Rise/Fall Time (20%—80%)	Tr/Tf	—	—	0.75	ns

1. The PHY uses internal delay to compensate by delaying both incoming and outgoing clocks by ~2.0 ns.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specification (continued)

RGMII 1000Base-T Receive Timing

Trace Delay

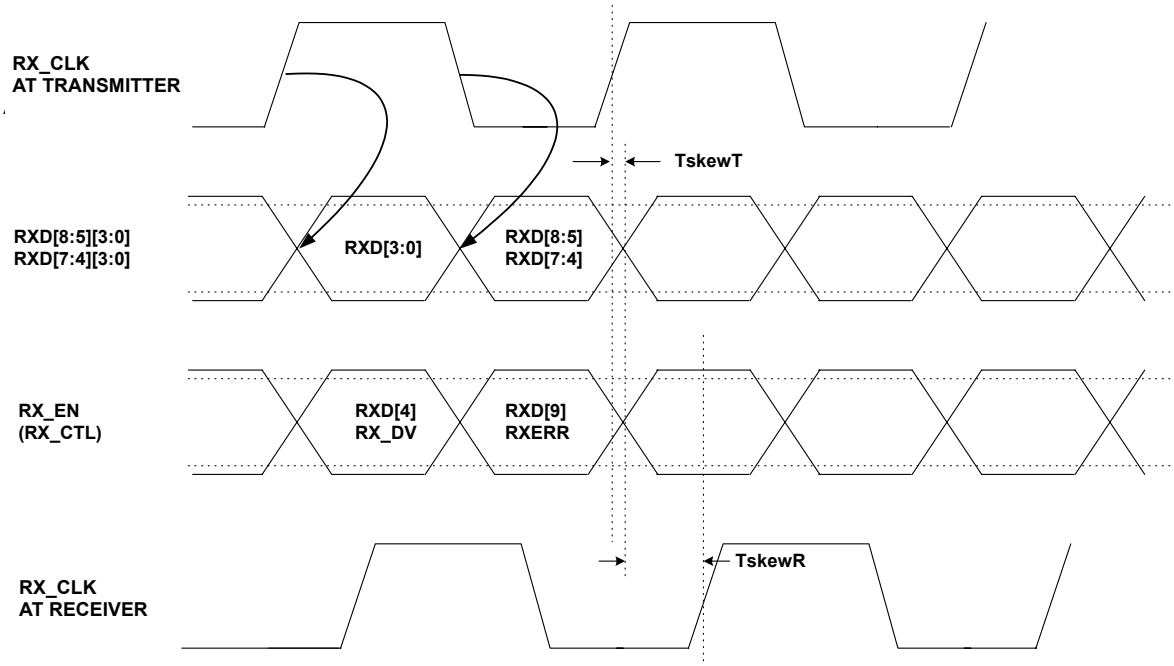


Figure 18. RGMII 1000Base-T Receive Timing—Trace Delay

Table 60. RGMII 1000Base-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Output Skew (at transmitter)—Trace Delay[1]	TskewT	–500	0	500	ps
Data to Clock Input Skew (at receiver)—Trace Delay[1]	TskewR	1	1.8	2.6	ns
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns
Duty Cycle for Gigabit[3]	Duty_G	45	50	55	%
Duty Cycle for 10Base-T/100Base-TX[3]	Duty_T	40	50	60	%
Rise/Fall Time (20%—80%)	Tr/Tf	—	—	0.75	ns

1. This implies that PCB design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. To enable internal delay, see MII register 22 bits 2:0.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specification (continued)

Internal Delay

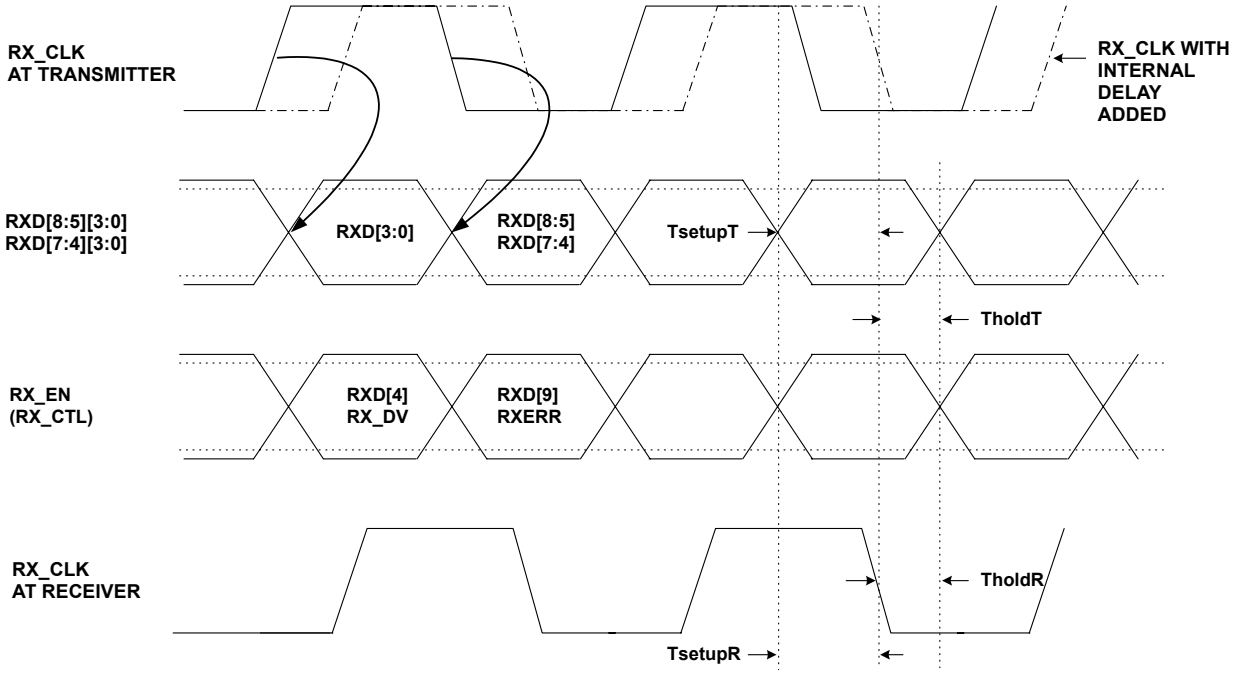


Figure 19. RGMII 1000Base-T Receive Timing—Internal Delay

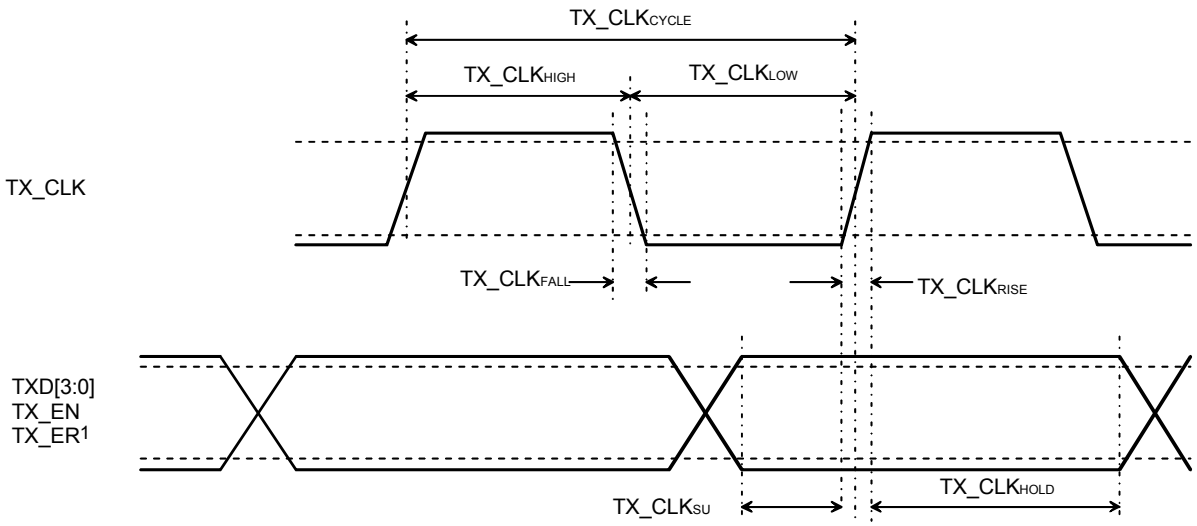
Table 61. RGMII 1000Base-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Output Setup (at transmitter—integrated delay)[1]	TsetupT	1.2	2.0	—	ns
Clock to Data Output Hold (at transmitter—integrated delay)[1]	TholdT	1.2	2.0	—	ns
Data to Clock Input Setup (at receiver—integrated delay)[1]	TsetupR	1.0	2.0	—	ns
Data to Clock Input Setup (at receiver—integrated delay)[1]	TholdR	1.0	2.0	—	ns
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns
Duty Cycle for Gigabit[3]	Duty_G	45	50	55	%
Duty Cycle for 10Base-T/100Base-TX[3]	Duty_T	40	50	60	%
Rise/Fall Time (20%—80%)	Tr/Tf	—	—	0.75	ns

1. The PHY uses internal delay to compensate by delaying both incoming and outgoing clocks by ~2.0 ns.
2. For 10Base-T and 100Base-TX, Tcyc scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
3. Duty cycle may be shrunk/stretched during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Timing Specification (continued)

MII 100Base-TX Transmit Timing



1. TX_ER is not available on the 68-pin MLCC.

Figure 20. MII 100Base-TX Transmit Timing

Table 62. MII 100Base-TX Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK Cycle Time	TX_CLKCYCLE	—	40	—	ns
TX_CLK High Time	TX_CLKHIGH	—	20	—	ns
TX_CLK Low Time	TX_CLKLOW	—	20	—	ns
TX_CLK Rise Time	TX_CLKRISE	—	—	5	ns
TX_CLK Fall Time	TX_CLKFALL	—	—	5	ns
MII Input Signal Setup Time to TX_CLK	TX_CLKSU	15	—	—	ns
MII Input Signal Hold Time to TX_CLK	TX_CLKHOLD	0	—	—	ns

Timing Specification (continued)

MII 100Base-TX Receive Timing

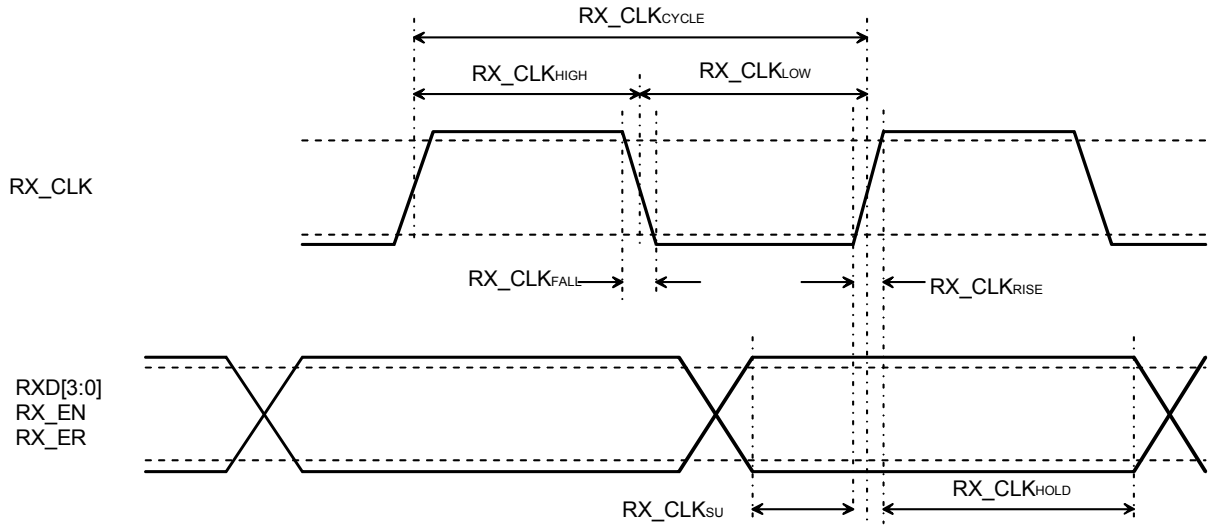


Figure 21. MII 100Base-TX Receive Timing

Table 63. MII 100Base-TX Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Cycle Time	RX_CLK_{CYCLE}	—	40	—	ns
RX_CLK High Time	RX_CLK_{HIGH}	—	20	—	ns
RX_CLK Low Time	RX_CLK_{LOW}	—	20	—	ns
RX_CLK Rise Time	RTX_CLK_{RISE}	—	1	—	ns
RX_CLK Fall Time	RX_CLK_{FALL}	—	1	—	ns
MII Output Signal Setup Time to RX_CLK	RX_CLK_{SU}	10	—	—	ns
MII Output Signal Hold Time to RX_CLK	RX_CLK_{HOLD}	10	—	—	ns

Timing Specification (continued)

MII 10Base-T Transmit Timing

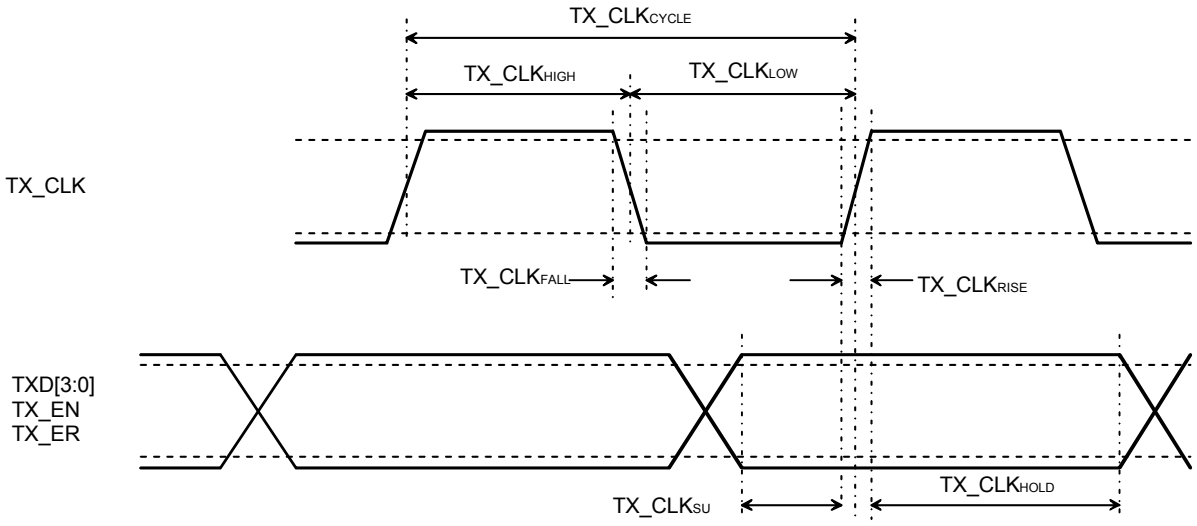


Figure 22. MII 10Base-T Transmit Timing

Table 64. MII 10Base-T Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK Cycle Time	TX_CLK_{CYCLE}	—	400	—	ns
TX_CLK High Time	TX_CLK_{HIGH}	—	200	—	ns
TX_CLK Low Time	TX_CLK_{LOW}	—	200	—	ns
TX_CLK Rise Time	TX_CLK_{RISE}	—	1	—	ns
TX_CLK Fall Time	TX_CLK_{FALL}	—	1	—	ns
MII Input Signal Setup Time to TX_CLK	TX_CLK_{SU}	15	—	—	ns
MII Input Signal Hold Time to TX_CLK	TX_CLK_{HOLD}	10	—	—	ns

Timing Specification (continued)

MII 10Base-T Receive Timing

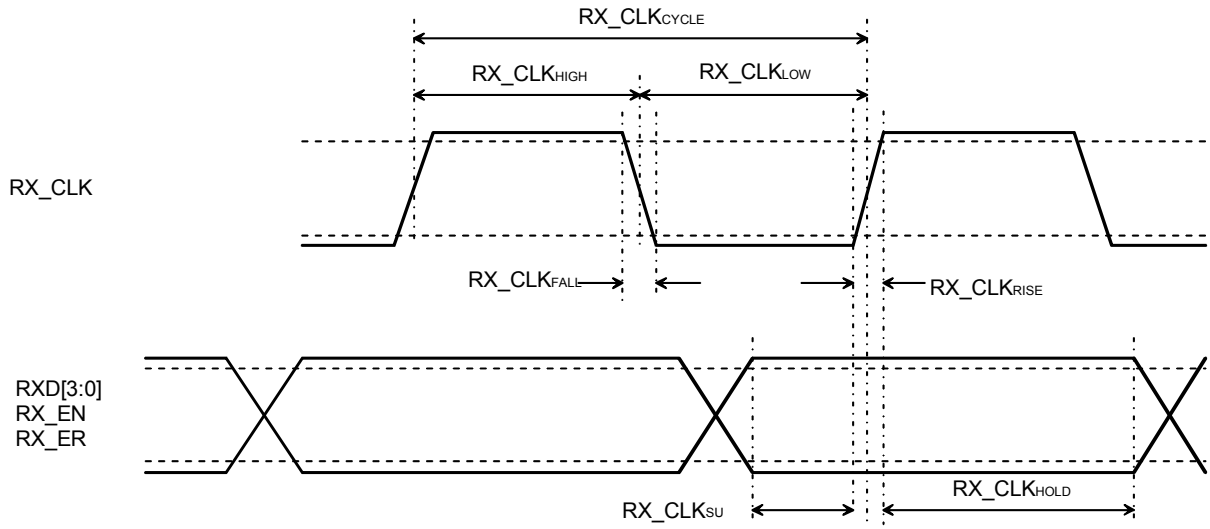


Figure 23. MII 10Base-T Receive Timing

Table 65. MII 10Base-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK Cycle Time	RX_CLKCYCLE	—	400	—	ns
RX_CLK High Time	RX_CLKHIGH	—	200	—	ns
RX_CLK Low Time	RX_CLKLOW	—	200	—	ns
RX_CLK Rise Time	RTX_CLKRISE	—	1	—	ns
RX_CLK Fall Time	RX_CLKFALL	—	1	—	ns
MII Output Signal Setup Time to RX_CLK	RX_CLKSU	10	—	—	ns
MII Output Signal Hold Time to RX_CLK	RX_CLKHOLD	10	—	—	ns

Timing Specification (continued)

Serial Management Interface Timing

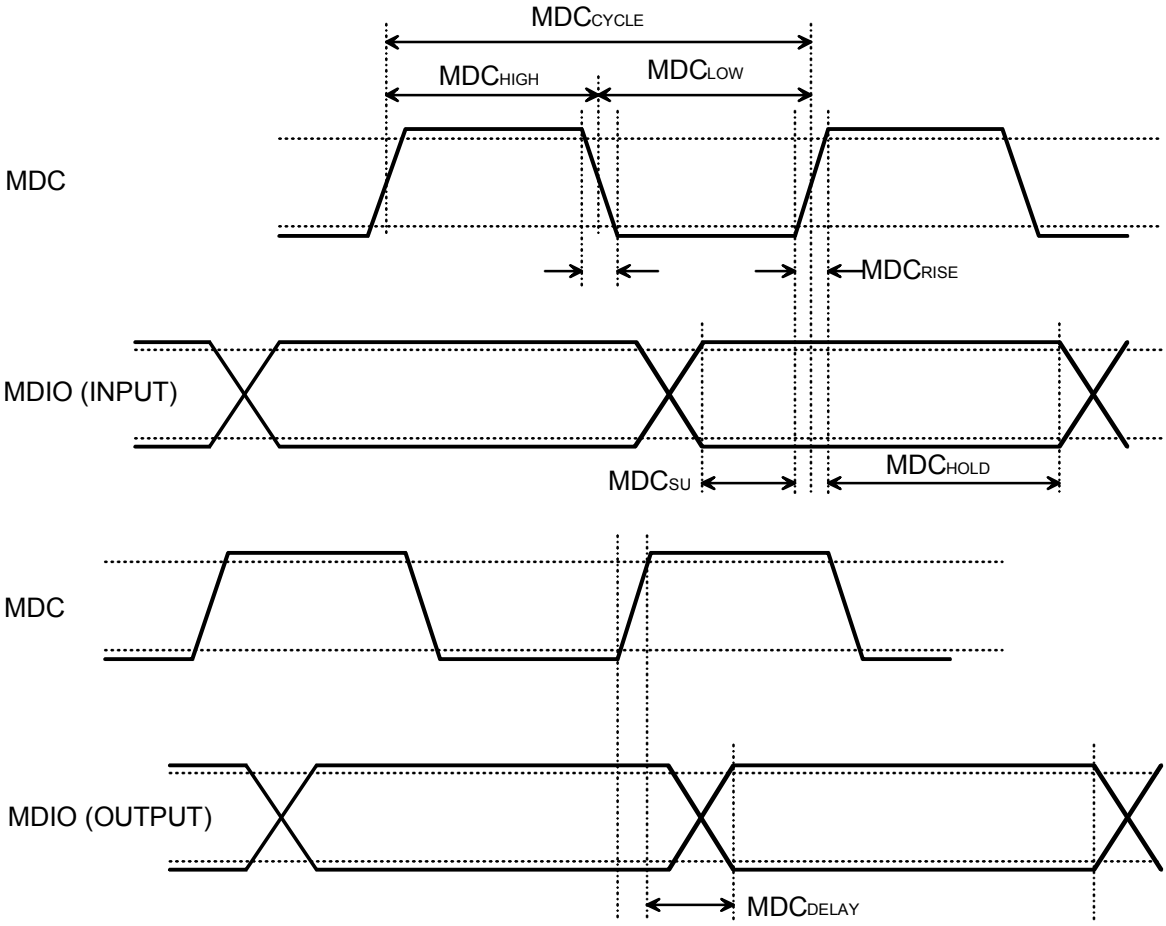


Figure 24. Serial Management Interface Timing

Table 66. Serial Management Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
MDC Cycle Time	MDCCYCLE	100	—	—	ns
MDC High Time	MDCHIGH	40	—	—	ns
MDC Low Time	MDCLOW	40	—	—	ns
MDC Rise Time	MDCRISE	—	—	5	ns
MDC Fall Time	MDCFALL	—	—	5	ns
MDIO Signal Setup Time to MDC	MDCSU	10	—	—	ns
MDIO Signal Hold Time to MDC	MDCHOLD	10	—	—	ns
MDIO Delay Time from MDC	MDCDELAY	—	—	80	ns

Timing Specification (continued)

Reset Timing

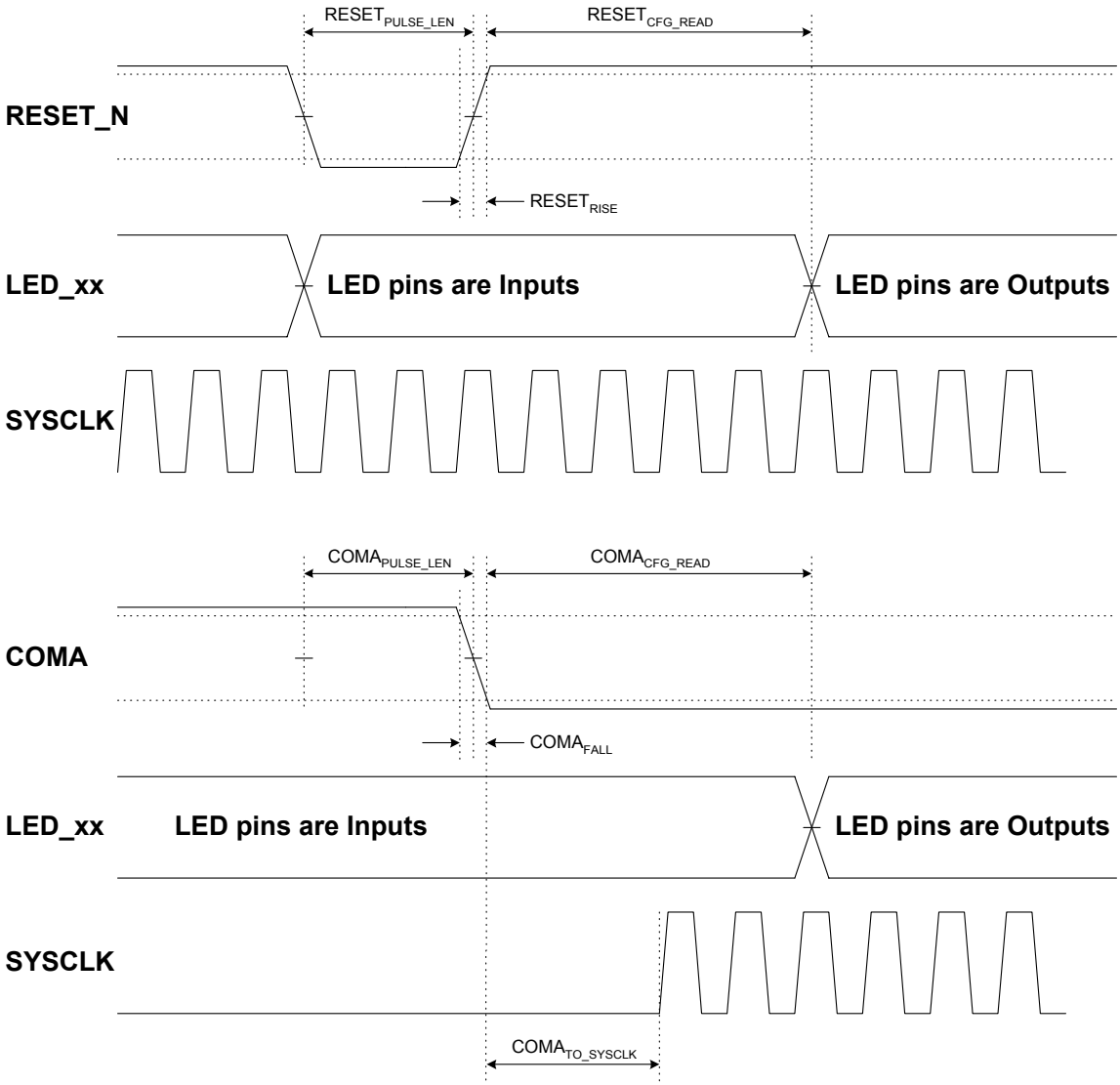


Figure 25. Reset Timing

Table 67. Reset Timing

Parameter	Symbol	Min	Typ	Max	Unit
RESET_N Pulse Length	$RESET_{PULSE\_LEN}$	1.0	—	—	µs
RESET_N Rise Time	$RESET_{RISE}$	—	1.0	—	ns
RESET_N Deassertion to Configuration Read	$RESET_{CFG\_READ}$	—	—	5.0	ms
COMA Pulse Length	$COMA_{PULSE\_LEN}$	1.0	—	—	µs
COMA Fall Time	$COMA_{FALL}$	—	1.0	—	ns
COMA Deassertion to SYS_CLK Valid	$COMA_{TO\_SYSCLK}$	—	1.0	—	ns
COMA Deassertion to Configuration Read	$COMA_{CFG\_READ}$	—	—	5.0	ms

Timing Specification (continued)

Clock Timing

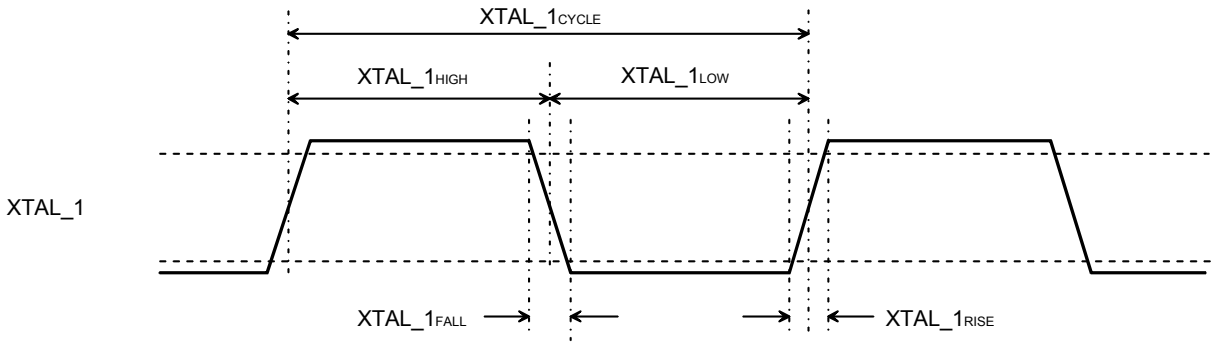


Figure 26. Clock Timing

Table 68. Clock Timing

Parameter	Symbol	Min	Typ	Max	Unit
XTAL_1 Cycle Time	XTAL_1CYCLE	39.998	40	40.002	ns
XTAL_1 High Time	XTAL_1HIGH	15	20	25	ns
XTAL_1 Low Time	XTAL_1LOW	15	20	25	ns
XTAL_1 Rise Time	XTAL_1RISE	—	—	3	ns
XTAL_1 Fall Time	XTAL_1FALL	—	—	3	ns
XTAL_1 Input Clock Jitter (RMS)	—	—	—	20	ps
XTAL_1 Input Clock Frequency	—	—	25	—	MHz
XTAL_1 Input Clock Accuracy	—	—	—	50	ppm

Timing Specification (continued)

JTAG Timing

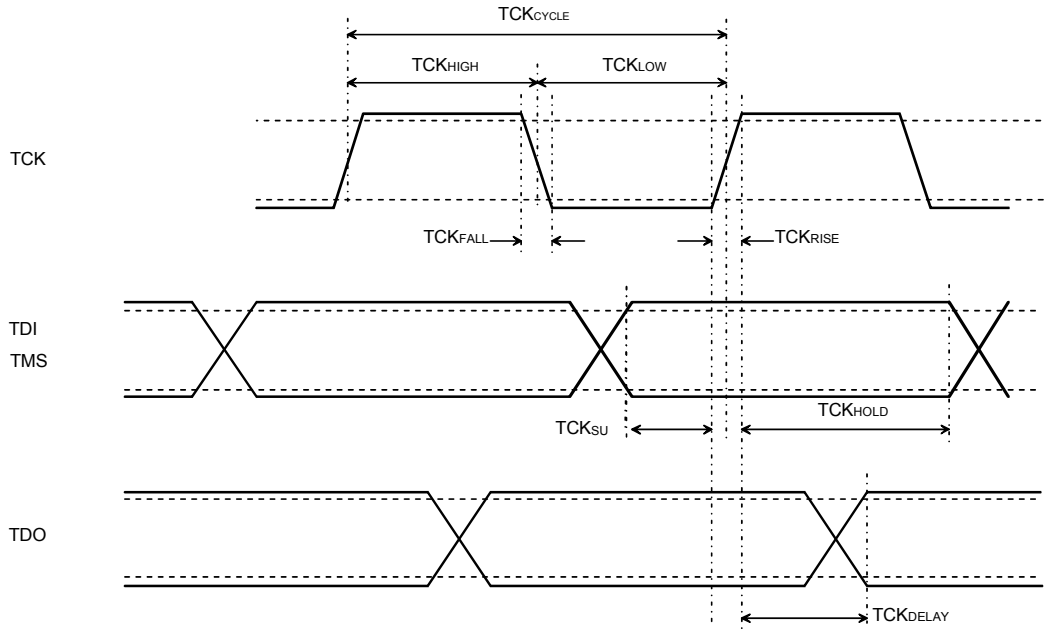
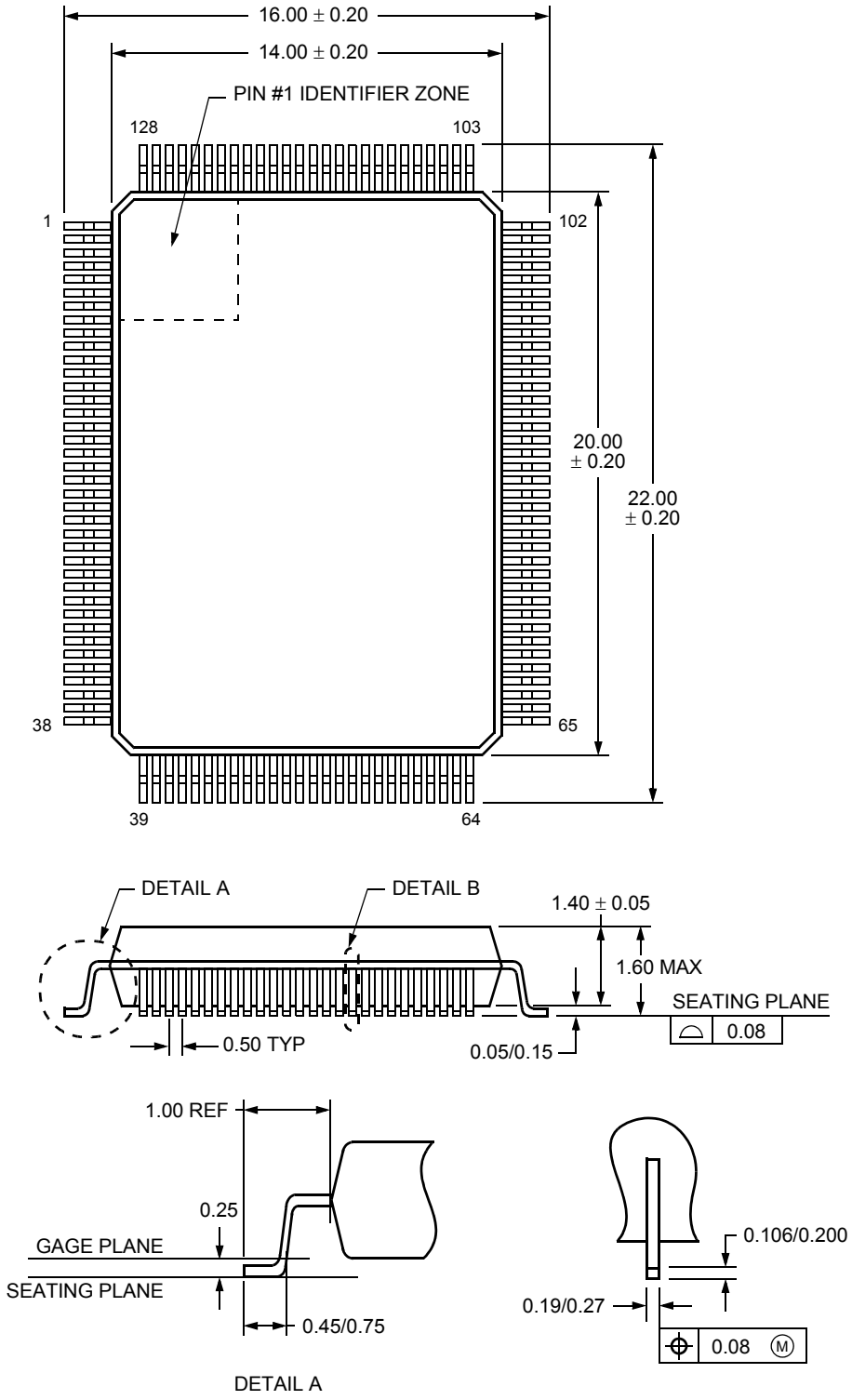


Figure 27. JTAG Timing

Table 69. JTAG Timing

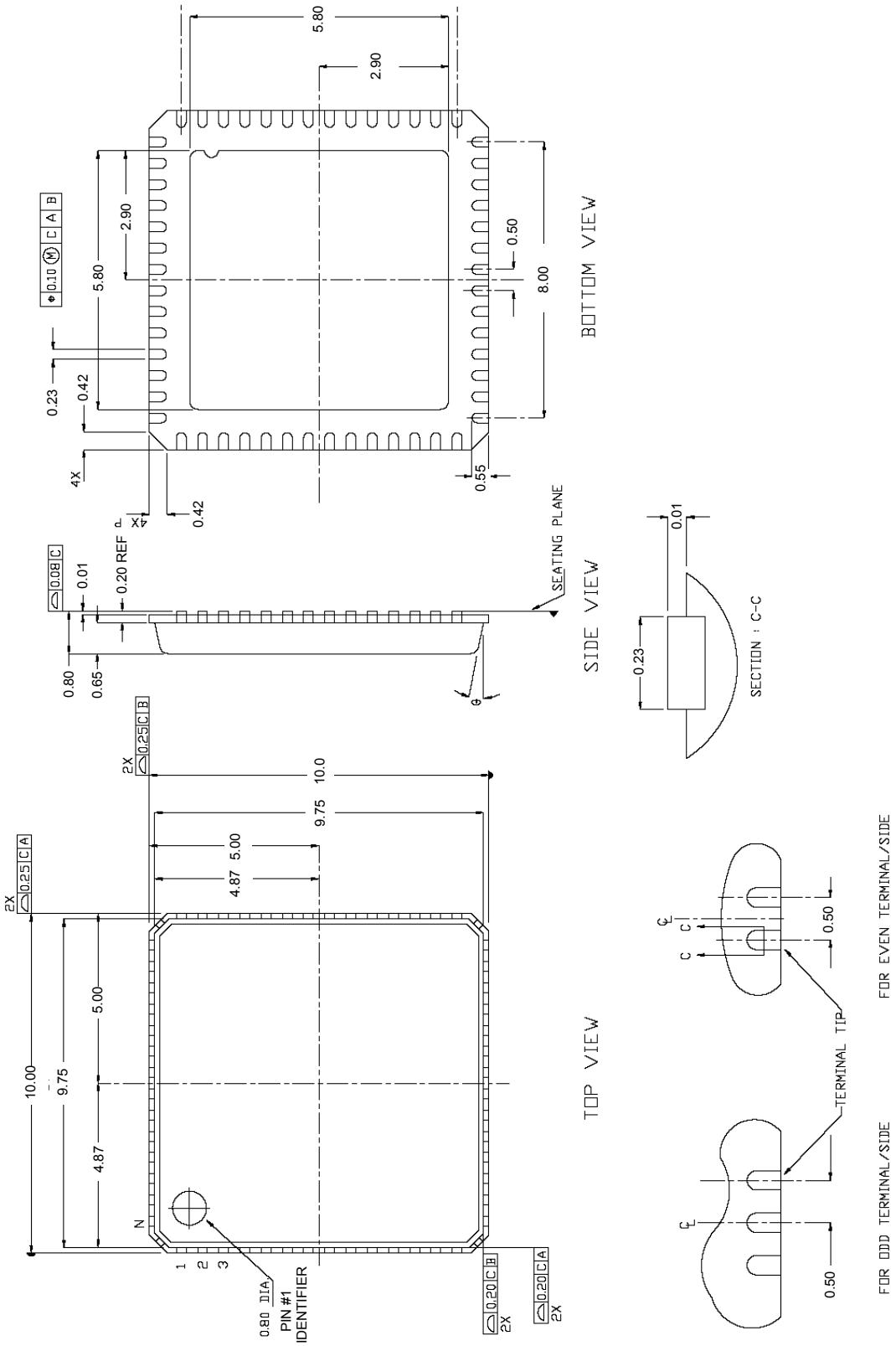
Parameter	Symbol	Min	Typ	Max	Unit
TCK Cycle Time	TCK_{CYCLE}	20	—	—	ns
TCK High Time	TCK_{HIGH}	10	—	—	ns
TCK Low Time	TCK_{LOW}	10	—	—	ns
TCK Rise Time	TCK_{RISE}	—	1	—	ns
TCK Fall Time	TCK_{FALL}	—	1	—	ns
TDI, TMS Setup Time to TCK	TCK_{SU}	2.7	—	—	ns
TDI, TMS Hold Time to TCK	TCK_{HOLD}	0.8	—	—	ns
TDO Delay Time from TCK	TCK_{DELAY}	—	—	8.1	ns

Package Diagram, 128-Pin TQFP



Package Diagram, 68-Pin MLCC (Dimensions are in millimeters.)

Note: Package outlines are unofficial and for reference only.



Ordering Information

Table 70. Chip Set Names and Part Numbers

Device	Description	Package	Part Number	Comcode
ET1011	Ethernet Transceiver	128-pin TQFP	ET1011-128T	7000497740
ET1011	Ethernet Transceiver	68-pin MLCC	ET1011-68M-D	700066380

Related Product Documentation

Table 71. Related Product Documentation

Device	Description	Document Type	Document Number
ET1010	Gigabit Ethernet Transceiver	Data Sheet	DS04-017GPHY
ET4101	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	Data Sheet	TBD
ET1081	Gigabit Ethernet Octal PHY	Data Sheet	DS04-056GPHY
ET4101	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	Product Brief	PB04-039GWSC
ET4100	Single-Chip 28 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	Product Brief	PB04-049GWSC
ET4000	Single-Chip 28 x 1 Gbit/s Layer 2+ Ethernet Switch	Product Brief	PB04-047GWSC
ET4001	Single-Chip 48 x 1 Gbit/s Layer 2+ Ethernet Switch	Product Brief	PB04-048GWSC

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