

**New Product**

**M64893AFP/AGP**

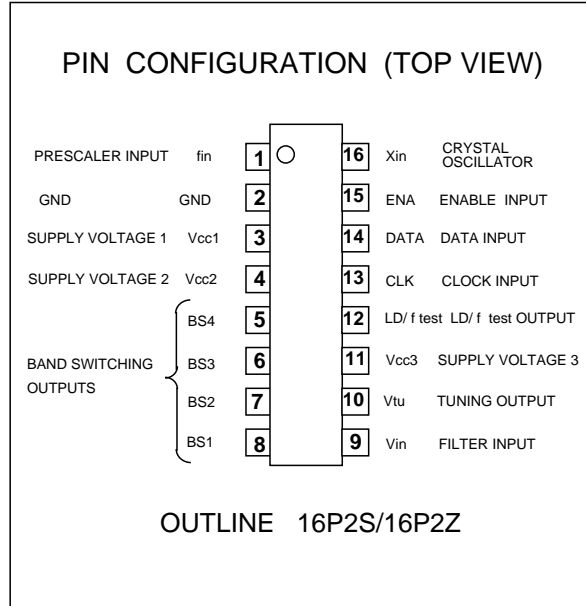
**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR**

**Description**

The M64893AFP/AGP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using Bip process. It contains the prescaler with operating up to 1.3GHz, 4 band drivers and Op.Amp for direct tuning.

**Features**

- 4 integrated PNP band drivers  
( $I_o=40mA, V_{sat}=0.2V$  typ@ $V_{cc1}$  to 13.2V)
- Built-in Op.Amp for direct tuning voltage output (33V)
- Low power dissipation ( $I_{cc}=20mA, V_{cc1}=5V$ )
- Built-in prescaler with input amplifier ( $F_{max}=1.3GHz$ )
- PLL lock/unlock status display output (Built-in pull up resistor)
- X'tal 4MHz is used to realize 1 type of tuning steps (Division ratio 1/640)
- Serial data input (3 wire bus)
- Built-in Power on reset system
- Small Package(16SOP/16SSOP)



16P2S



16P2Z

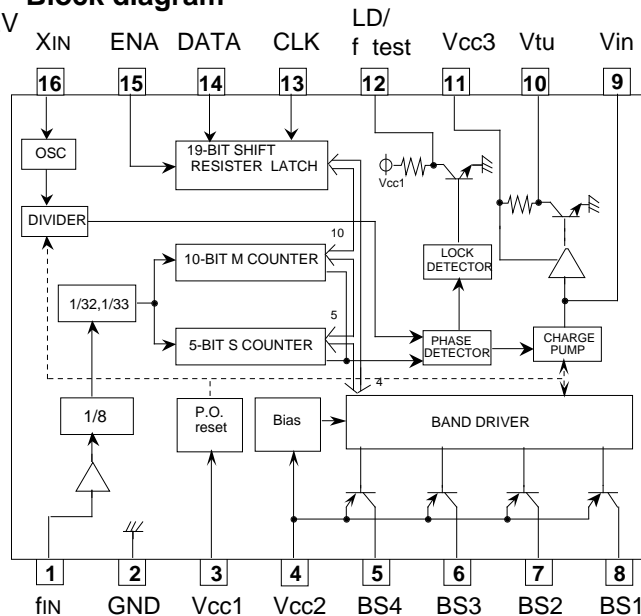
**Application**

TV,VCR tuners

**Recommended operating condition**

- Supply voltage range ●  $V_{cc1}=4.5$  to  $5.5V$   
 $V_{cc2}=V_{cc1}$  to  $13.2V$   
 $V_{cc3}=28$  to  $35V$
- Rated supply voltage ●  $V_{cc1}=5.0V$   
 $V_{cc2}=12V$   
 $V_{cc3}=33V$

**Block diagram**



**Function**

- 1/32, 1/33 dual-modulus prescaler
- 4MHz crystal oscillator, reference divider
- Programmable divider (10-bit M counter, 5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op. Amp for direct tuning

# M64893AFP/AGP

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### Pin description

Symbol	Pin No.	Pin name	Function
f in	1	Prescaler input	Input for the VCO frequency.
GND	2	GND	Ground to 0V.
Vcc1	3	Power supply voltage 1	Power supply voltage terminal. 5.0 ±0.5V
Vcc2	4	Power supply voltage 2	Power supply for band switching, Vcc1 to 13.2V
BS4 BS3 BS2 BS1	5 6 7 8	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
Vin	9	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output ( f 1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
Vtu	10	Tuning output	This supplies the tuning voltage.
Vcc3	11	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
LD/ f test	12	Lock detect/ Test port	When 19 bit data is input, lock detector is output. When 27 bit data is input, lock detector is output, the programmable freq. Divider output and reference freq. Output is selected by the test mode.
CLOCK	13	Clock input	Data is read into the shift register when the clock signal falls.
DATA	14	Data input	Input for band SW and programmable freq. divider set up.
ENABLE	15	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the 19th pulse of the clock signal falls.
X in	16	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

# M64893AFP/AGP

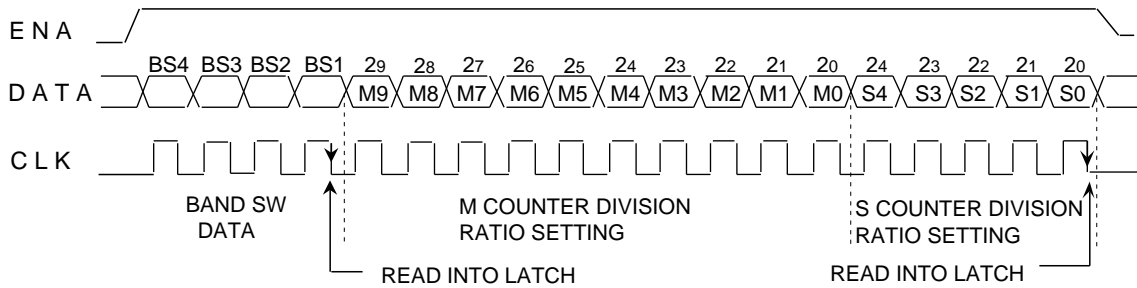
## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### Method of setting data

The frequency demultiplying ratio uses 15bits. Setting up the band switching output uses 4bits. The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal. The program counter data is read into the latch by the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 19th pulse of the enable signal, only the band SW data is updated and other data is ignored.

The data is latched at the 19th pulse of the clock signal. At this time, 1/640 frequency division ratio is used. Clock signals after the above are invalid.



### How to set the dividing ratio of the programmable divider

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32M + S)$$

M : 10 bit main counter division  
S : 5 bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

$$\begin{matrix} 32 & M & 1023 \\ 0 & S & 31 \end{matrix}$$

Therefore, the range of division N is 8,192 to 262,136.

The tuning frequency  $f_{VCO}$  is given in the following equations.

$$\begin{aligned} f_{VCO} &= f_{REF} \times N \\ &= 6.25 \times 8 \times (32M + S) \\ &= 50.0 \times (32M + S) \quad [\text{kHz}] \end{aligned}$$

But, the tuning frequency range is 51.2MHz to 1300MHz from the maximum prescaler operating frequency.

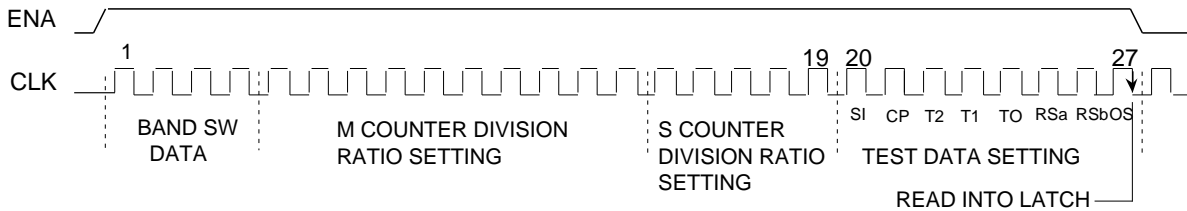
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### Test mode data set up method

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27 bit data



(2) Test Mode Bit Set Up

- X :Random, 0 or 1.normal "0"
- CP :Set up the charge pump current value
- T0, T1,&T2 :Set up test modes
- RSa, Rsa :Set up for the reference Frequency division ratio
- OS :Set up the tuning amplifier
- S I :1 Only (It is prohibit to "0 ")

### Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70 uA	Test
1	270 uA	Normal

### Setting up for the test mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	fREF	Test mode
1	0	1	High impedance	f1/N	Test mode

# M64893AFP/AGP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

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### Set up for the reference Frequency division ratio

RSa	RSb	Division ratio
1	1	1/ 512
0	1	1/ 1024
X	0	1/ 640

### Set up the tuning amplifier

OS	Tuning voltage out put	Mode
0	ON	Normal
1	OFF	Test

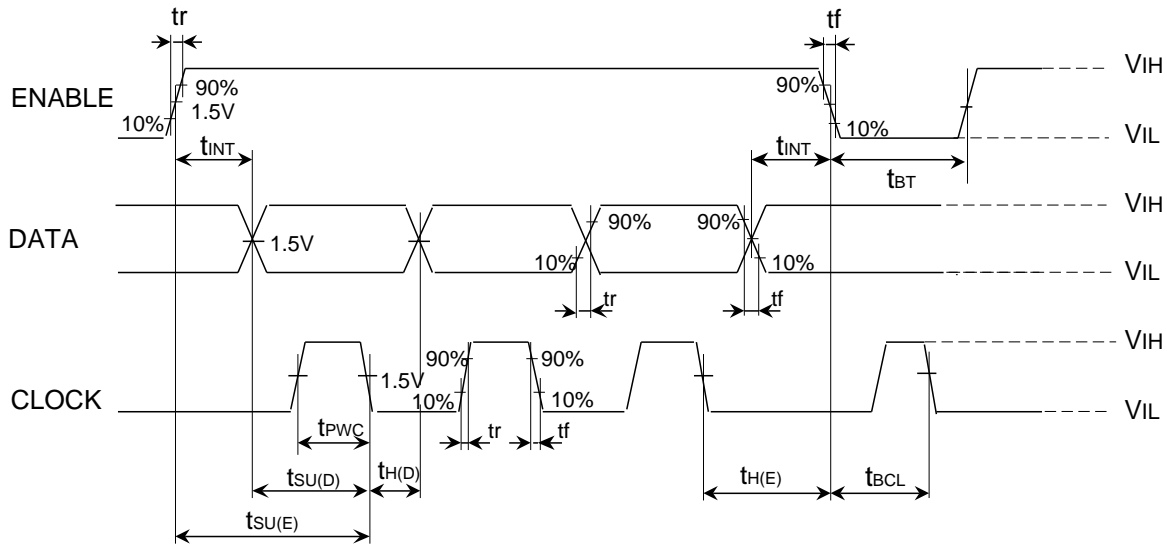
### Power on reset operation (Initial state the power is turned ON)

BS4 to BS1 : OFF  
 Charge pump : High impedance  
 Tuning amplifier : OFF  
 Charge pump current : 270uA  
 Frequency division ratio : 1/640  
 Lock detect : H

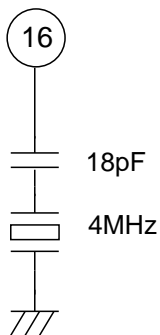
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## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### Timing diagram



### Crystal oscillator connection diagram



Crystal oscillator characteristics  
 Actual resistance : less than 3 0 0  
 Load capacitance : 2 0 p F

# M64893AFP/AGP

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### Absolute maximum ratings (Ta=-20°C to +75°C unless otherwise noted)

Parameter	Symbols	Max.ratings	Units	Conditions
Supply voltage 1	Vcc1	6.0	V	Pin3
Supply voltage 2	Vcc2	14.4	V	Pin4
Supply voltage 3	Vcc3	36.0	V	Pin11
Input voltage	VI	6.0	V	Not to exceed Vcc1
Output voltage	Vo	6.0	V	LD output
Voltage applied when the band output is OFF	VBSOFF	14.4	V	
Band output current	IBSON	50.0	mA	per 1 band output circuit
ON the time when the band output is ON	tBSON	10	sec	50mA per 1 band output circuit 3circuits are on at same time,
Power dissipation	Pd	470	mW	Ta= +75°C
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

### Recommended operating conditions (Ta=-20°C to +75°C unless otherwise noted)

Parameter	Symbol	Ratings	Units	Conditions
Supply voltage 1	Vcc1	4.5 to 5.5	V	Pin3
Supply voltage 2	Vcc2	Vcc1 to 13.2	V	Pin4
Supply voltage 3	Vcc3	28 to 35	V	Pin11
Operating frequency (1)	fopr1	4.0	MHz	Crystal oscillation circuit
Operating frequency (2)	fopr2	80 to 1,300	MHz	
Band output current 5 to 8	IBDL	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

# M64893AFP/AGP

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

**Electrical characteristics** (Ta=-20°C to +75°C unless otherwise noted)  
Vcc1=5.0V, Vcc=12V, Vcc3=33V

Parameters	Symbol	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
Input terminals							
"H"input voltage	V <sub>IH</sub>	13 to 15		3.0	-	V <sub>cc1</sub> +0.3	V
"L"input voltage	V <sub>IL</sub>	13 to 15		-	-	1.5	V
"H"input current	I <sub>IH</sub>	13 to 15	V <sub>cc1</sub> =5.5V, V <sub>i</sub> =4.0V	-	-	10	μA
"L"input current	I <sub>IL</sub>	13,15	V <sub>cc1</sub> =5.5V, V <sub>i</sub> =0.4V	-	-6	-10	μA
"L"input current	I <sub>IL</sub>	14	V <sub>cc1</sub> =5.5V, V <sub>i</sub> =0.4V	-	-18	-30	μA
Lock output							
"H"output voltage	V <sub>OH</sub>	12	V <sub>cc1</sub> =5.5V	5.0	-	-	V
"L"output voltage	V <sub>OL</sub>	12	V <sub>cc1</sub> =5.5V	-	0.3	0.5	V
Band SW							
output voltage	V <sub>BS</sub>	5 to 8	V <sub>cc2</sub> =12V I <sub>o</sub> =-40mA	11.6	11.8	-	V
Leak current	I <sub>oIK2</sub>	5 to 8	V <sub>cc2</sub> =12V Band SW is OFF	-	-	-10	μA
Tuning output							
output voltage "H"	V <sub>toH</sub>	10	V <sub>cc3</sub> =33V	32.5	-	-	V
output voltage "L"	V <sub>toL</sub>	10	V <sub>cc3</sub> =33V	-	0.2	0.4	V
Charge pump							
"H" output current	I <sub>CPH</sub>	9	V <sub>cc1</sub> =5.0V V <sub>o</sub> =1V	-	±270	±370	μA
"L" output current	I <sub>CPL</sub>	9	V <sub>cc1</sub> =5.0V V <sub>o</sub> =1V	-	±70	±110	μA
Leak current	I <sub>cpLK</sub>	9	V <sub>cc1</sub> =5.0V V <sub>o</sub> =2.5V	-	-	±50	nA
Supply current 1	I <sub>cc1</sub>	3	V <sub>cc1</sub> =5.5V	-	20	30	mA
Supply current 2							
4 circuits OFF	I <sub>cc2A</sub>	4	V <sub>cc2</sub> =12V	-	-	0.3	mA
1 circuits ON, Output open	I <sub>cc2B</sub>	4	V <sub>cc2</sub> =12V	-	6.0	8.0	mA
Output current 40mA	I <sub>cc2C</sub>	4	V <sub>cc2</sub> =12V I <sub>o</sub> =-40mA	-	46.0	48.0	mA
Supply current 3	I <sub>cc3</sub>	11	V <sub>cc3</sub> =33V Output ON	-	3.0	4.0	mA

The typical values are at V<sub>cc1</sub>=5V, V<sub>cc2</sub>=12V, V<sub>cc3</sub>=33V, Ta=+25°C



# M64893AFP/AGP

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### Switching characteristics (Ta=-20°C to +75°C unless otherwise noted)

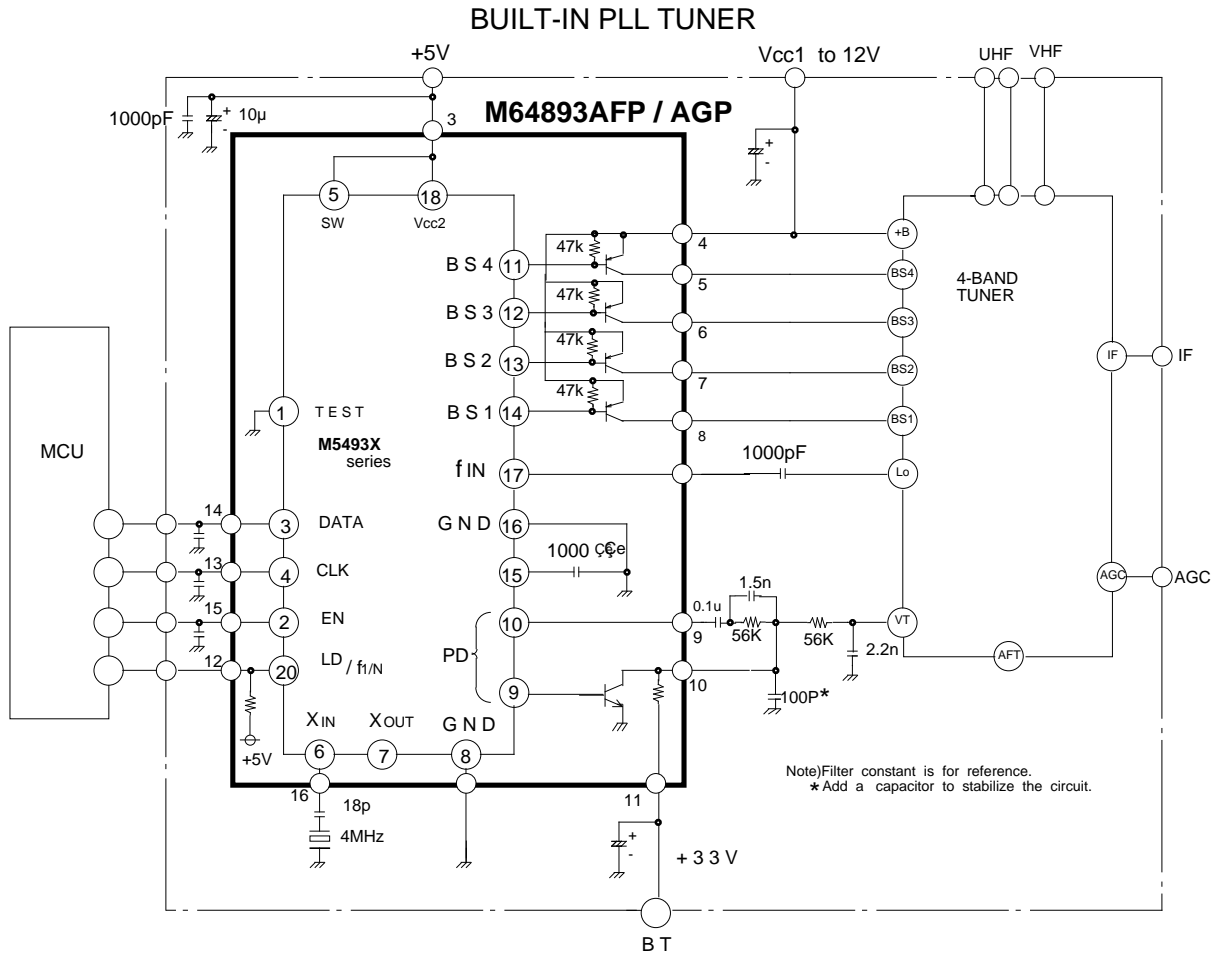
Vcc1=5.0V, Vcc2=12V, Vcc3=33V

Parameter	Symbol	Test pin	Test conditions	Limits			Unit used
				Min.	Typ	Max	
Prescaler operating frequency	f opr2	1	Vcc1=4.5 to 5.5V Vin=Vinmin to Vinmax	80	-	1300	MHz
Operating input voltage	V in	1	Vcc1=4.5 80 to 100MHz	- 24	-	4	dBm
			to 5.5V 100 to 200MHz	- 27	-	4	
			200 to 800MHz	- 30	-	4	
			800 to 1000MHz	- 27	-	4	
			1000 to 1300MHz	- 18	-	4	
Clock pulse width	t PWC	13	Vcc1=4.5 to 5.5V	1	-	-	us
Data setup time	t SU(D)	14	Vcc1=4.5 to 5.5V	2	-	-	us
Data hold time	t H(D)	14	Vcc1=4.5 to 5.5V	1	-	-	us
Enable setup time	t SU(E)	15	Vcc1=4.5 to 5.5V	3	-	-	us
Enable hold time	t H(E)	15	Vcc1=4.5 to 5.5V	3	-	-	us
Enable data interval time	t INT	15,14	Vcc1=4.5 to 5.5V	1	-	-	us
Rise time	t r	13,14,15	Vcc1=4.5 to 5.5V	-	-	1	us
Fall time	t f	13,14,15	Vcc1=4.5 to 5.5V	-	-	1	us
Next enable prohibit time	t BT	15	Vcc1=4.5 to 5.5V	5	-	-	us
Next clock prohibit time	t BCL	13,15	Vcc1=4.5 to 5.5V	5	-	-	us

# M64893AFP/AGP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

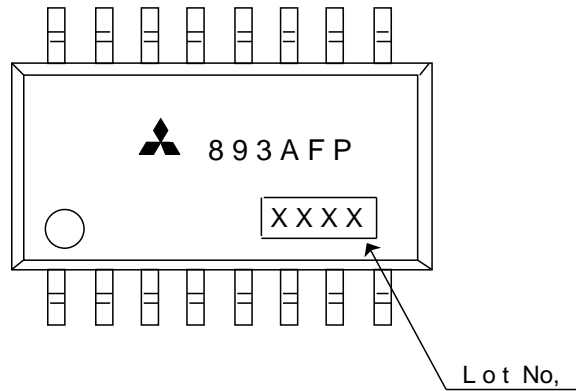
## Application example



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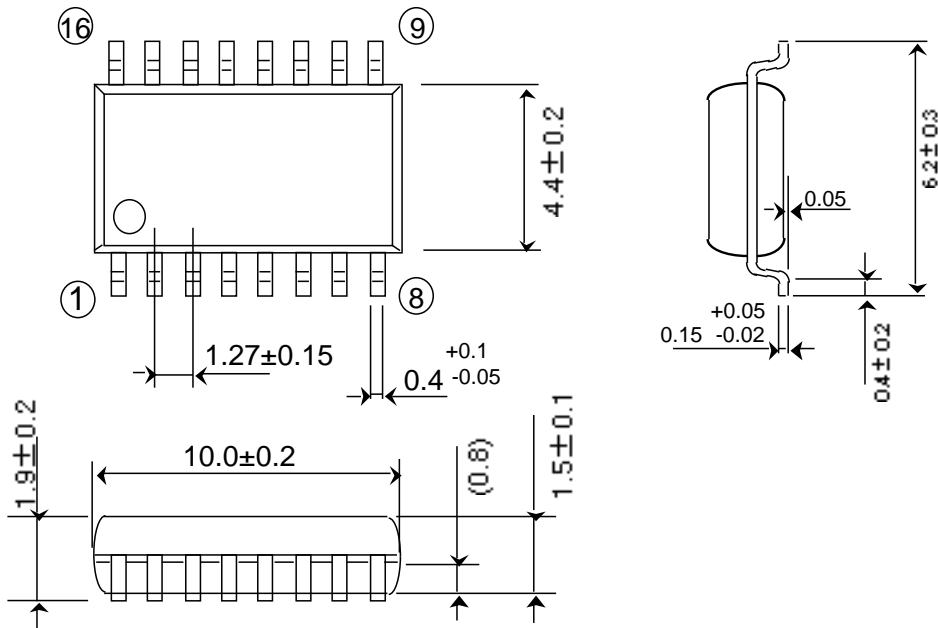
SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

## Marking DWG (M64893AFP)



## External appearance

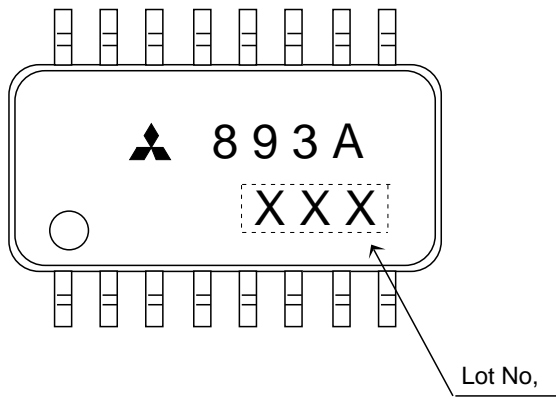
16P2S type <16pin plastic mold SOP> Unit:mm



# M64893AFP/AGP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

Marking DWG ( M 6 4 8 9 3 A G P )



## External appearance

16P2Z type <16pin plastic mold SSOP> Unit:mm

