Enhanced Sensorless BLDC Motor Controller

GENERAL DESCRIPTION

The ML4420 motor controller provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect Sensors to indicate rotor position. It senses the back EMF of the motor windings (no neutral required) to determine the proper commutation phase sequence using PLL techniques. The ML4420 uses a patented Back-EMF sensing technique which will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing circuitry.

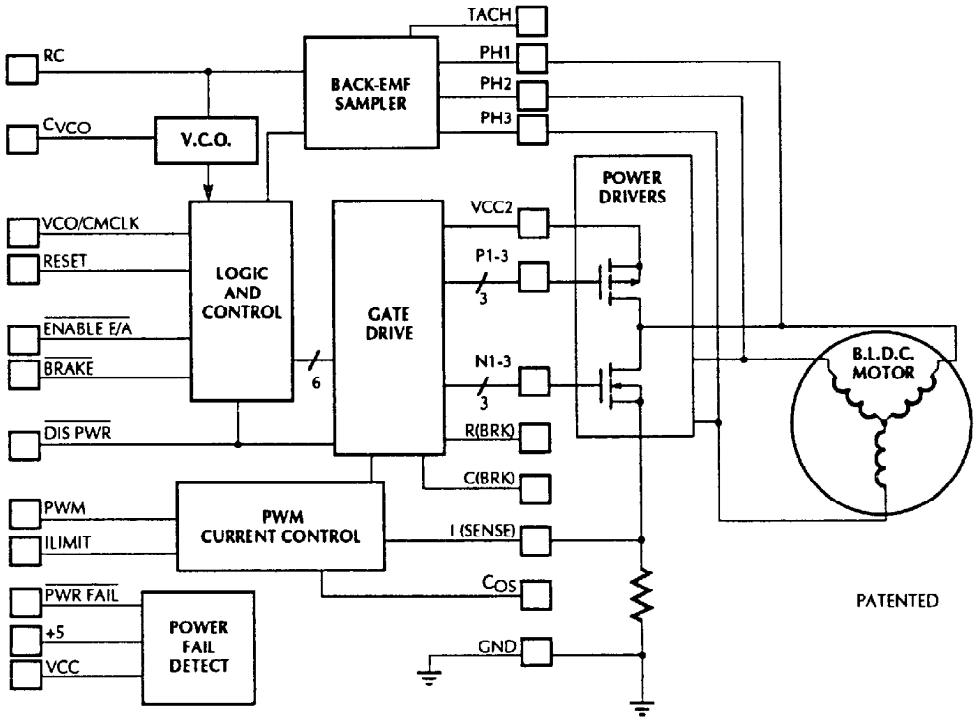
The ML4420 controls the motor current with a constant off-time PWM or with a microprocessor controlled constant frequency PWM input. The velocity loop can be controlled with an external microprocessor or through an analog feedback loop. An accurate, jitter-free, VCO output is provided, equal to the commutation frequency of the motor. The ML4420 modulates the gates of external N-channel power MOSFETs to regulate the motor current and directly drives the P-channel MOSFETs. The ML4420 supports enhancements like a blanker circuit to prevent false retriggering of the one shot during a motor current spike and circuitry to ensure that there is no shoot through in any state.

The start-up algorithm consists of measuring a fixed VCO frequency and externally ramping the commutation clock until it is equal to the VCO frequency. The timing of the start-up sequencing is determined by the microprocessor thus allowing the optimization for a wide range of motors and inertial loads.

FEATURES

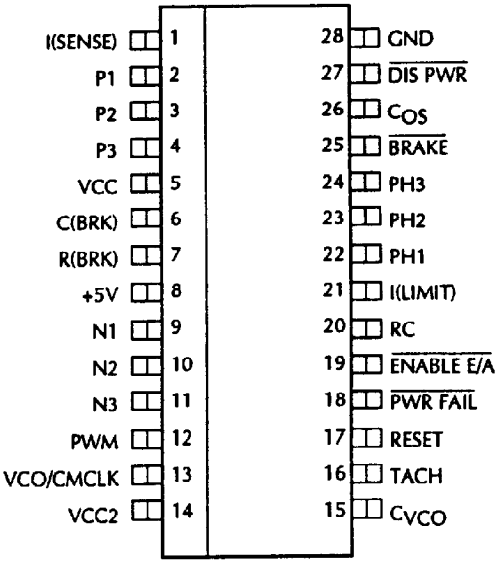
- Less than 200mW power dissipation
- Patented Back-EMF commutation technique provides jitterless torque for minimum "spin-up" time
- PWM motor current control
- Microprocessor based start-up algorithm allows for optimized start-up sequencing, speed control and support for variable motor loads
- Back-EMF comparator output senses motor rotation after power fail for fast re-lock after brownout
- Onboard power fail detect monitor
- Onboard motor braking circuit allows 'life' braking on command
- Drives external N-ch & P-ch FETs
- Enhanced version of the ML4410 & ML4411

BLOCK DIAGRAM



PIN CONFIGURATION

ML4420
28-Pin SOIC (S28W)



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	I(SENSE)	Motor current sense input
2	P1	Drives the external P-Channel transistor driving motor PH1
3	P2	Drives the external P-Channel transistor driving motor PH2
4	P3	Drives the external P-Channel transistor driving motor PH3
5	VCC	12V power supply. Terminal which is sensed for power fail
6	C(BRK)	Capacitor which stores energy to charge N-Channel MOSFETs for braking with power off
7	R(BRK)	External resistor to C(BRK) to drive NMOS during braking
8	+5V	5V power supply input
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	PWM	TTL input of PMW signal
13	VCO/CMCLK	Logic Output from VCO serves as an input pin for the commutation clock used in start-up sequencing
14	VCC2	12V power and power for the braking function
15	C_{VCO}	Timing capacitor for VCO
16	TACH	Logic Output from TACH comparator serves as an input pin for the commutation clock used in start-up sequencing
17	RESET	Input which holds the VCO off and sets the IC to the RESET condition (refer table 1)
18	$\overline{\text{PWR FAIL}}$	A "0" output indicates 5V or 12V is under-voltage. This is an open collector output with a 4.5kΩ pull-up to +5V
19	$\overline{\text{ENABLE E/A}}$	A "0" logic input enables the error amplifier and closes the Back-EMF feedback loop (refer table 1)
20	RC	VCO loop filter components
21	I(LIMIT)	Sets the threshold for the PWM comparator
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit
26	C_{OS}	Timing capacitor to GND and resistor to +5V, for fixed off-time PWM current control
27	$\overline{\text{DIS PWR}}$	A logic 0 on this pin turns off the N and P outputs and causes the TACH comparator output to appear on TACH OUT
28	GND	Signal and Power Ground

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 5, 14) 14V
Output Current (pins 2, 3, 4, 9,10,11) ..... ±150mA
Logic Inputs (pins 14, 17, 18, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Voltage +12V (pin 14) ..... 12V ± 10%
+5V (pin 8) ..... 5V ± 10%
I Control Voltage Range (pins 13, 21) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section					
Frequency vs. V_{PIN20}	$1V \le V_{PIN20} \le 10V$		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	Reset mode	70	140	210	Hz
Sampling Amplifier (note 1)					
V_{RC}	State R	400	500	600	mV
I_{RC}	State A, V_{PH2} = 4V	30	50	70	µA
	State A, V_{PH2} = 6V	–13	2	13	µA
	State A, V_{PH2} = 8V	–30	–50	–70	µA
Motor Current Control Section					
I(SENSE) Gain	V_{PIN21} = 2.5V	4.5	5	5.5	V/V
One Shot off time		5	10	15	µS
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–500	–350	–200	µA
Braking Circuit					
Brake Active Threshold		1.0	1.4	1.8	V
PIN 25 Bias Current	V_{PIN25} = 0V		0.3	1	µA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = Operating Temperature Range, VCC = VCC2 = 12V, R_{SENSE} = 1Ω, C_{VCO} = 0.01µF, C_{OS} = 0.001µF, R_{OS} = 10kΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Outputs I(LIMIT) = 2.5V					
I_P low	V_P = 2V	0.5		1.2	mA
V_P high	I_P = –10µA	VCC2 – 1V			V
P3 Comparator Threshold		VCC2 – 3.6V		VCC2 – 2.4V	V
V_N high	V_{PIN1} = 0V	VCC – 3.2	10	VCC – 1.2	V
V_N low	I_N = 1mA		0.2	0.7	V
LOGIC low (V_{OL})	I_{OUT} = 0.4mA			0.5	V
VCO/TACH V_{OH}	I_{OUT} = 100µA	2.4			V
POWER FAIL V_{OH}	I_{OUT} = 10µA	V_{PIN8} – 0.2	V_{PIN8} – 0.1	V_{PIN8}	V
Supply Currents (N and P outputs open)					
5V Current			8	25	mA
VCC Current			1	1.5	mA
VCC2 Current			8	16	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

SUMMARY OF ENHANCEMENTS IN ML4420 OVER THE ML4411

1. Lower power dissipation, 200mW versus 450mW in the ML4411.
2. Accurate and customized start-up by using commutation clock provided by the microprocessor instead of relying on I_{RAMP} as in the ML4411.
3. True braking function which is biased by TOB, to allow braking block to work under a power loss situation.
4. ML4420 adds hysteresis into braking comparator to accelerate the transition as soon as the (Vth) threshold is reached.
5. ML4420 adds comparator to prevent the PMOS from coming "ON" when the braking is active.
6. ML4420 adds active pull-up to the P output to replace the resistor pull-up in ML4411.
7. ML4420 enhances pull-down capability to the N output to prevent injected shoot through (only 3 mA in the ML4411).
8. ML4420 adds comparator to prevent P3 N3 shoot through during reset to state A transition.
9. The one-shot accuracy in the ML4420 is improved over the ML4411's.
10. ML4420 adds a blanker circuit to one-shot to prevent it from false triggering which occurrs when large starting currents cause noise coupling to the chip.
11. Directly controls speed through external PWM input.

FUNCTIONAL DESCRIPTION

The ML4420 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, Integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either constant frequency or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4420 is designed to drive external power transistors (N-channel sinking transistors and P-Channel sourcing transistors) directly.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal, phased-locked to the commutation frequency of the monitor.

BACK-EMF SENSING AND COMMUTATOR

The ML4420 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2 below) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early commutation causes pin 20 to discharge. Analog speed control loops can use Pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 5kΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC.

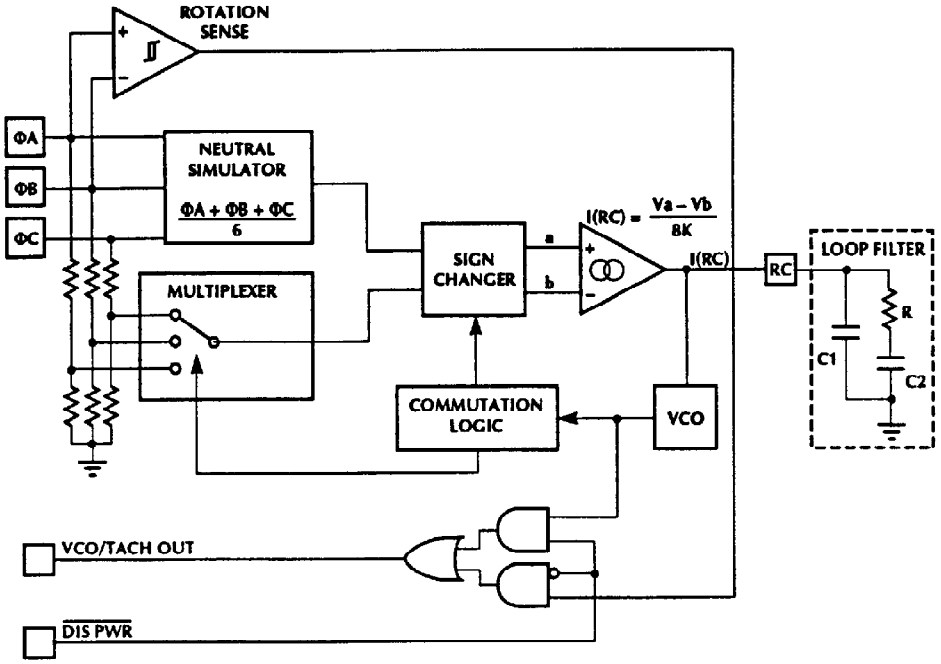


Figure 1. Back-EMF sensing block diagram

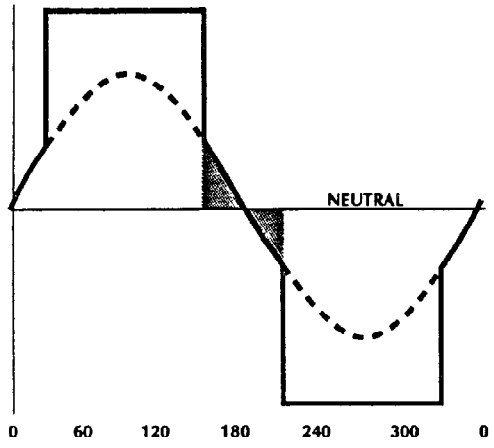


Figure 2. Typical motor phase waveform with Back-EMF superimposed (Ideal Commutation)

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per Minute.

The minimum VCO gain derived from the specification table (using the minimum F_{VCO} at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 9.5V, then

$$C_{VCO} = \frac{9.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{460}{POLES \times RPM} \mu F$$

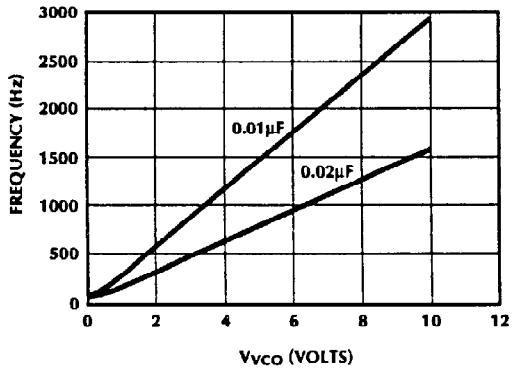


Figure 3. VCO Output Frequency vs. V_{VCO} (pin 20)

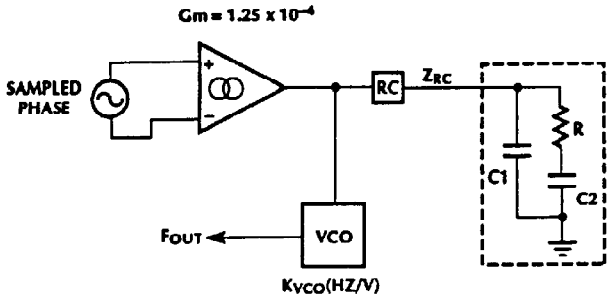


Figure 4. Back EMF Phase Lock Loop Components

Figure 4 above shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C_1, and C_2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s}\frac{(s+\omega_{LEAD})}{(s+\omega_{LAG})}$$

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{RC_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{RC_1C_2}$$

Requiring the loop to settle in 20 PLL cycles with a spread of 10 between $\omega_{LEAD} = 10 \times \omega_{LAG}$ produces the following calculations for R, C_1, and C_2:

$$C_1 \approx \frac{4.66 \times 10^{-9}}{C_{VCO} \times F_{VCO}^{\ 2}}$$

$$C_2 = 9 \times C_1$$

$$R = \frac{12.54}{C_2 \times F_{VCO}}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained. The following steps are a typical procedure for starting a motor which is at rest. It is possible to determine if the motor is running by polling the VCO/TACH OUT pin with power disabled (Pin 27 = low).

STEP 1 The IC is held in reset state until the platters are steady by setting pin 17 and pin 19 to a '1', with full power applied to the winding (see figure 5). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state. Pin 20 is held at 0.5V internally. Microprocessor needs to measure VCO frequency by setting pin 27 to a '1' and then store it.

STEP 2 Setting pin 17 to a '0' and pin 19 to a '1' holds the IC in a ramping state. Microprocessor sends starting commutation clock to pin 16 which is an input pin in this state. This clock frequency is gradually increasing until it reaches the VCO frequency previously stored in Step 1.

STEP 3 As soon as commutation clock reaches the VCO frequency of Step 1, pin 19 is switched to "0" while pin 17 remains '0'. Now the PLL is closed and the VCO is locked to the Back EMF. Pin 16 becomes an output pin. Thus the commutation clock from the microprocessor should be held in tri-state.

Table 1 Commutation, Braking and PLL States

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

STATE	ENABLE E/A	RESET	PIN20 (RC)	VCO	COMMUTATOR
RESET	1	1	0.5V	RUNNING PER V_{PIN20}	IN RESET STATE
RAMP	1	0	0.5V	PRESET	CLOCKED FROM COMMUTATION CLOCK
RUN	0	0	DRIVEN BY PLL	RUNNING PER V_{PIN20}	SEQUENCED BY VCO
BRAKE	0	1	X	X	X

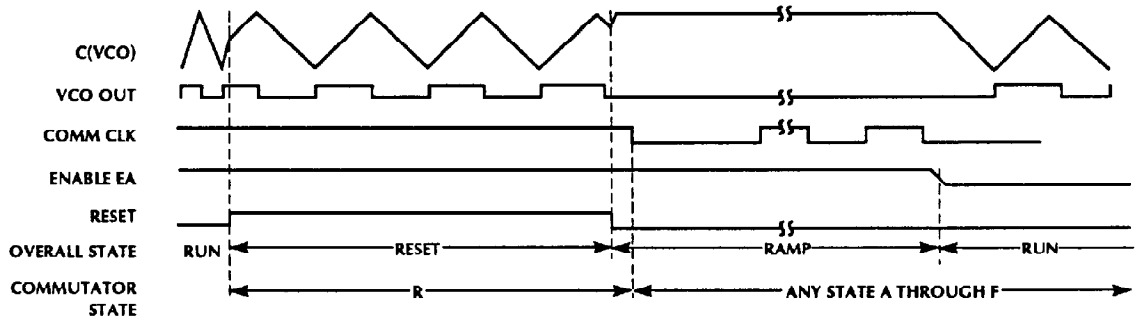


Figure 5. Start up sequencing (from stop)

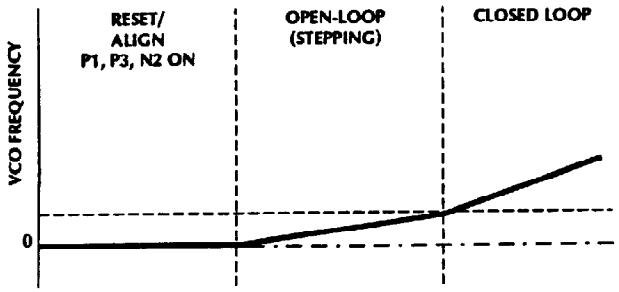


Figure 6. Typical Start-up Sequence

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

TABLE 2. START-UP SEQUENCE

STEP	PIN 17	PIN 19	PIN 21	I(LIMIT) I(CMD)
1	1	1	FIXED	I_{MAX}
2	0	1	FIXED	I_{MAX}
3	0	0	0	I_{MAX}

PWM CURRENT CONTROL

To facilitate speed control, the ML4420 has a PWM input pin to receive a constant frequency PWM signal generated from an external speed control loop.

The ML4420 also includes a current mode constant off-time PWM circuit. When motor current builds to the threshold set on I(LIMIT) input (pin 21), a one-shot is fired whose timing is set by C_{OS} and R_{OS} where

$$t_{OFF} = 1.3 \times R_{OS} \times C_{OS}$$

The I(SENSE) input pin should be kept below 1V. If I(SENSE) goes above 1V, a bias current of about –300µA will flow out of pin 1 and the N outputs will be inhibited. Bringing I(SENSE) below 0.7V returns the bias current to its normal level For this reason, the noise filter resistor on the I(SENSE) pin (1kΩ on Figure 8) should be less than 1.5kΩ.

The noise filter time constant should be great enough to filter the leading edge current spike when the N-FETs turn on but small enough to avoid excessive phase shift in the I(SENSE) signal.

OUTPUT DRIVERS

The motor's source drivers (P1 thru P3) are NPN emitter followers. N3 is inhibited until P3 is within 3V (typ) of VCC2. Drivers N1 through N3 are totem-pole outputs capable of sinking 10mA. Switching noise in the external MOSFETs is reduced by an internal 4KΩ resistor in series with the sourcing NPN to form an RC time constant with the N-Channel gate capacitance.

BRAKING

As shown in Figure 7 the braking circuit pulls the N-channel MOSFET Gates high when the BRAKE pin falls below a 2 x Vbe threshold (Vth). After a power failure, C(DLY) is discharged slowly through R(DLY) providing a delay for retract to occur before the braking circuit is activated. The P-channel MOSFETs are turned off well before braking occurs. As soon as the Vth threshold is reached, the braking comparator with hysteresis will accelerate the transition and tri-state the N-channel buffer (B1, refer figure 7) before C(BRK) dump charges into the N-channel Gates. This is to ensure that no charge from C(BRK) is lost through the pull-down transistors in B1, (figure 7). The C(BRK) will continue charging the N-channel Gates, to ensure braking, even when VCC2 (motor BEMF rectified through the MOSFET body diode), drops due to the braking process. An external signal could be used to brake the motor. To accomplish this set pin 17 = '1', pin 19 = '0'. This will pull pin 26 below the threshold to activate the braking circuit.

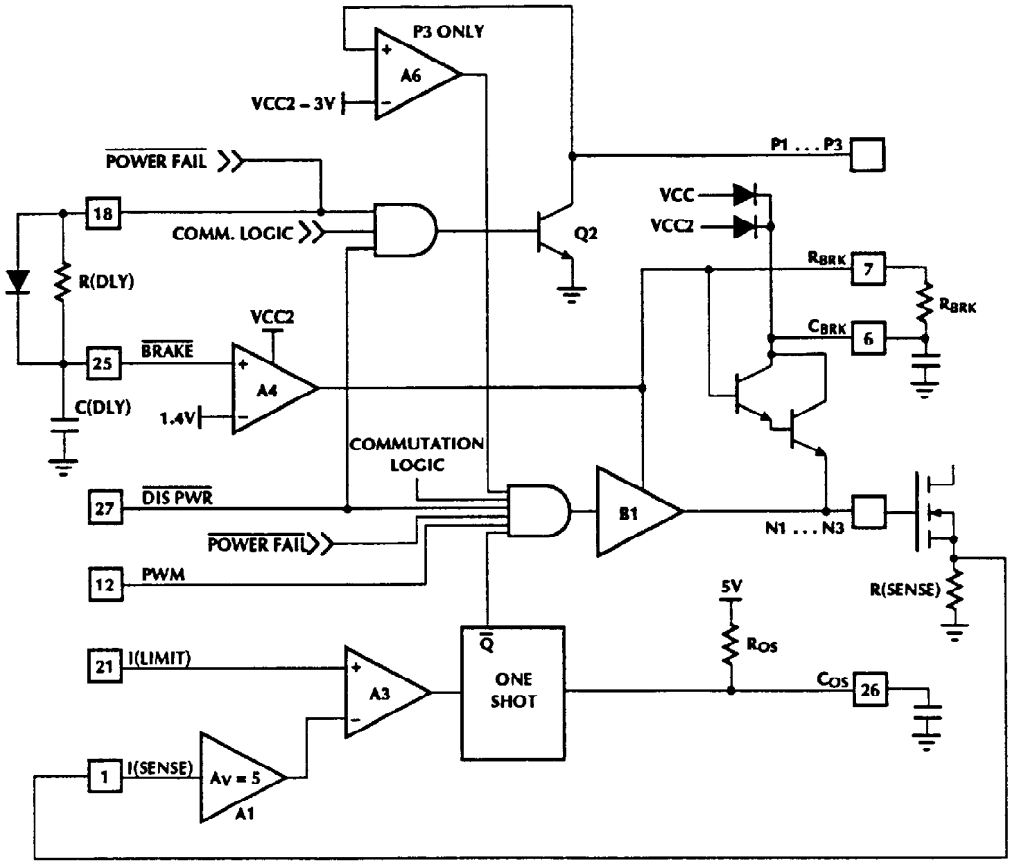


Figure 7. PWM Current Control, Gate Drive and Braking Circuits

APPLICATIONS

Figure 8 shows a typical application of the ML4420 in a hard disk drive spindle control. The timing needed to start the motor in most applications would be generated by a microcontroller.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting the duty cycle of PWM signal sending into PWM pin.
2. Using analog circuitry for speed control. (Fig. 9)

OUTPUT STAGE HINTS

In the circuit in Figure 8, Q1, Q2 and Q3 are IRFR9024 or equivalent. Q4, Q5 and Q6 are IRFR024 or equivalent. New MOSFET packaging technology such as the Little Foot® series may decrease the PC board space. These packages, however have much lower thermal inertia and dissipation capabilities than the larger packages, and care should be taken not to exceed their rated current and junction temperature.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross conduction is the condition where an N-FET and P-FET in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see Figure 10):

1. When transitioning from mode 0 to mode A (see table 1) P3 goes from on to off at the same time N3 goes from off to on. If P3 turns off slowly and N3 turns on quickly, cross conduction may occur. This condition has been prevented inside the IC on the ML4420 through the addition of comparator A6 on the P3 output (Fig. 7).

2. When the MOSFET in the same phase switches on gate current flows due to capacative coupling of current through the MOSFET's drain to gate capacitance. This could cause the MOSFET that was off to be turned on.

3. In condition 2 above, the P-channel MOSFET is pulled up inside the ML4420 by a NPN follower with base pulled up to VCC2 via 16KΩ. If the current through Cdgp is greater than the Vth_{PMOS}/16KΩ/Beta NPN, when the N-FET turns ON, the P-FET could be turned ON simultaneously, causing cross-conduction. The same mechanism can be applied to N-FET when P-FET is turned ON. The ML4420 is designed to take care of both the cases through slow turn-on, fast turn-off schemes ie P-FET Gate is pulled down by an 800µA current source and the N-FET Gate is charged up by an emitter follower in series with 4KΩ.

Figure 10 shows the output stages and the potential causes of cross-conduction. The diode D1 shown, may be needed for high power applications to limit the negative current pulled (through Cdgn) out of the substrate diode in the ML4420 when P-FET turns off.

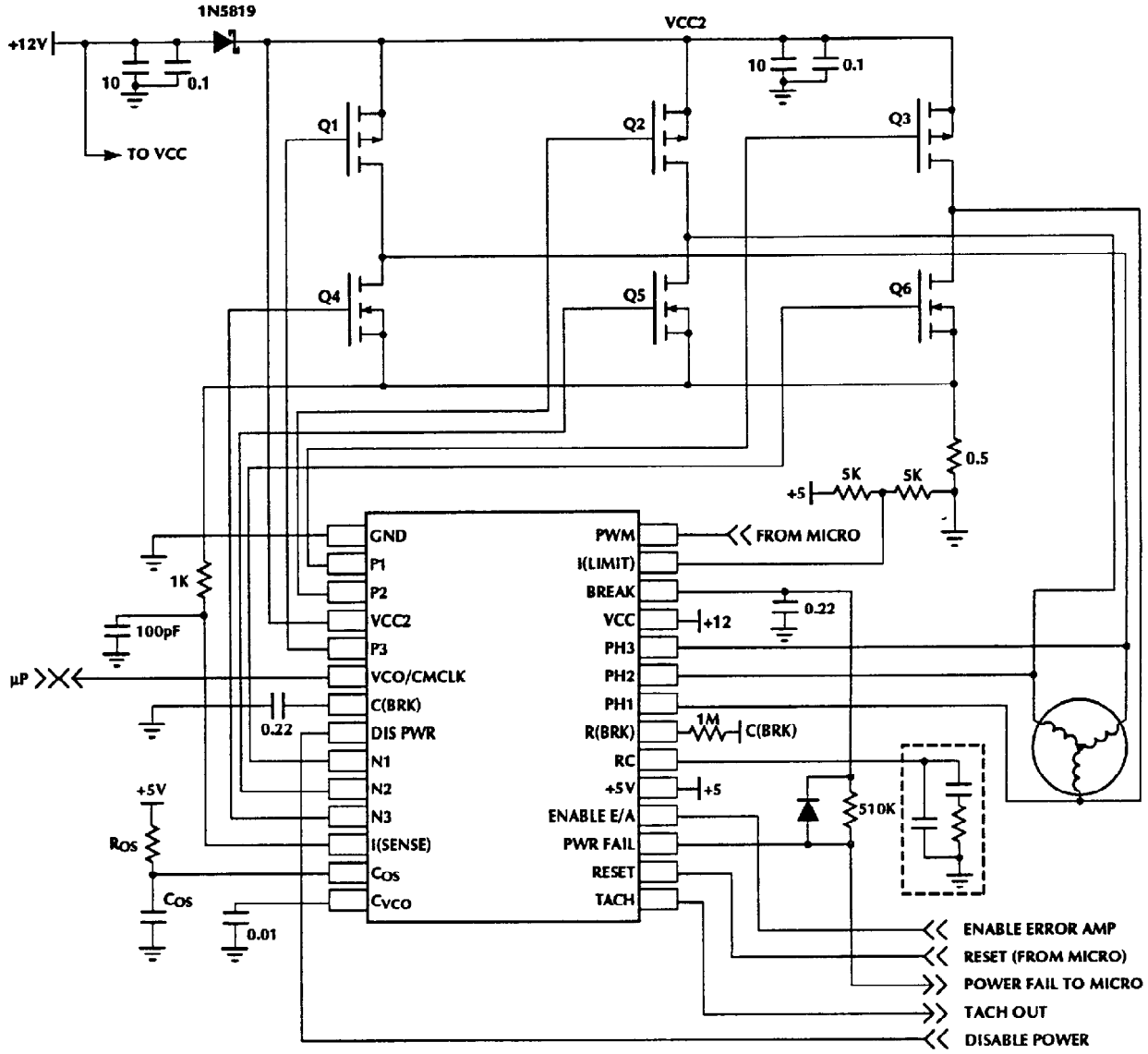


Figure 8. ML4420 Typical Application

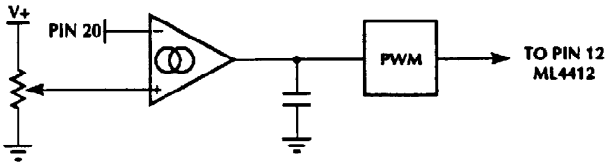


Figure 9. Voltage Controller PWM Generator

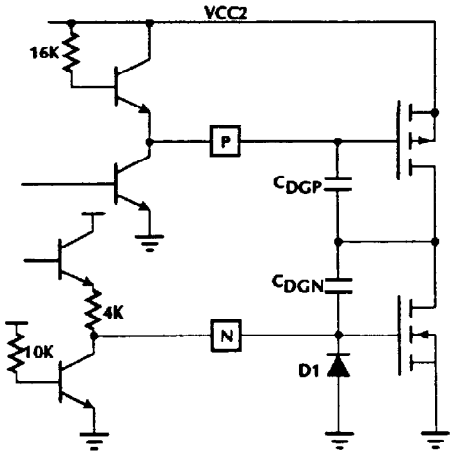


Figure 10. Causes of Cross-conduction

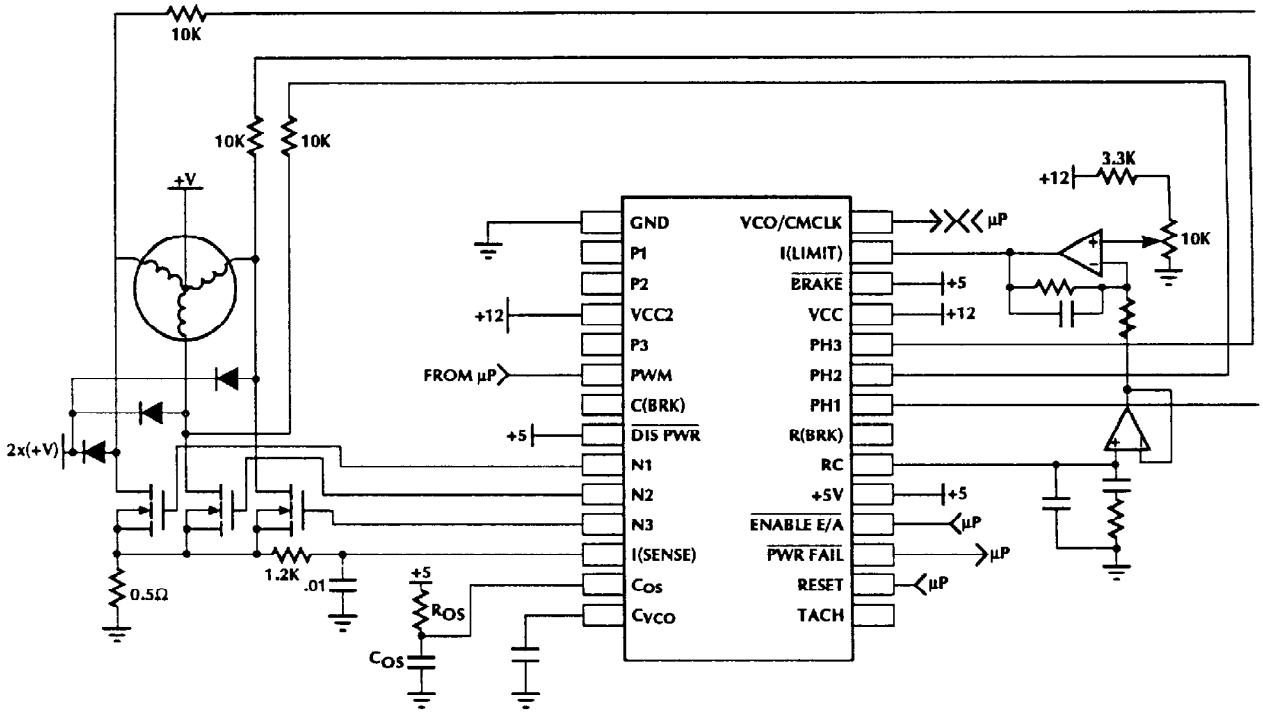


Figure 11. ML4420 Unipolar Drive Application

UNIPOLAR OPERATION

Unipolar mode offers the potential advantage of lower motor drive cost by only requiring the use of 3 transistors to drive the motor. The ML4420 will operate in unipolar mode (Figure 11) provided the following precautions are taken:

1. The IC supplies should not exceed 12V + 10%.
2. The phase pins on the IC should not exceed the supply voltage.

In unipolar operation, the motor's windings must be allowed to drive freely to:

$$V_{\Phi(MAX)} = V_{SUPPLY\ (MAX)} + V_{EMF\ (MAX)}$$

Therefore, there can be no diodes to clamp the inductive energy to V_{SUPPLY}. This energy must be clamped, however, to avoid an over-voltage condition on the MOSFETs and other components. Typically, a V(CLAMP) voltage is created to provide the clamping voltage. The inductive energy may either be dissipated (Figure 12) or alternately efficiently regenerated back to the system supply (Figure 13).

The circuit in Figure 11 is designed to minimize the external components necessary, at some compromise to performance. The 3 resistors from the motor phase windings to the PH inputs work with the ML4420's 5KΩ internal resistance to ground to divide the motor's phase voltage down, providing input signals that do not exceed 12V. This circuit uses analog speed regulation. The "one shot" circuitry to time the reset is replaced by a diode and RC delay from the rising edge or the $\overline{\text{POWERFAIL}}$ signal. The error amplifier is left enabled continuously since at low speeds its current contribution is negligible. The current injected into the loop filter must be greater than the leakage current from the phase detector amplifier for the motor to start reliably.

HIGHER VOLTAGE MOTOR DRIVE

To drive a higher voltage motor, the same precautions regarding ML4420 voltage limitations as were outlined for Unipolar drive above should be followed. Figures 14–16 provide several methods of translating the ML4420's P outputs to drive a higher voltage.

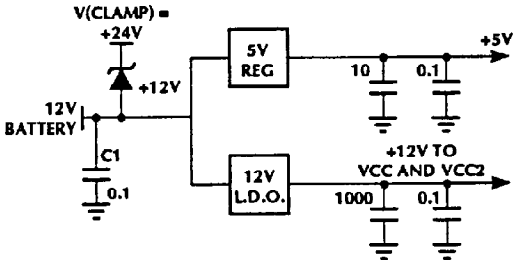


Figure 12. Dissipative Clamping Technique

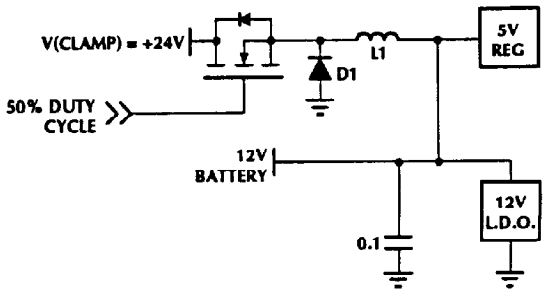


Figure 13. Non-Dissipative Clamping Technique

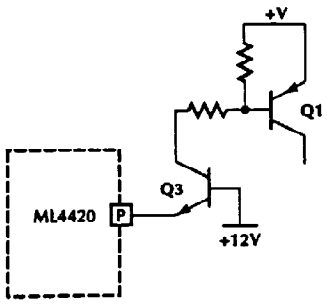


Figure 14. High Voltage Translation using PNP Power Transistor

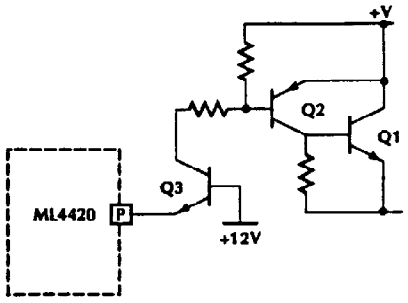


Figure 15. High Voltage Translation using "Composite" PNP Power Transistor

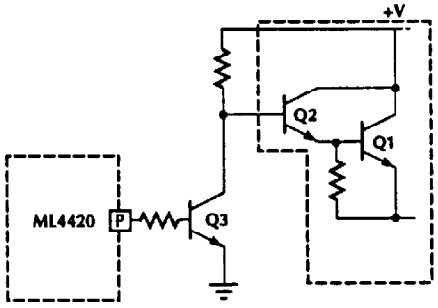


Figure 16. High Voltage Translation with NPN Darlington

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4420CS	0°C to +70°C	28-PIN SOIC (S28W)

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