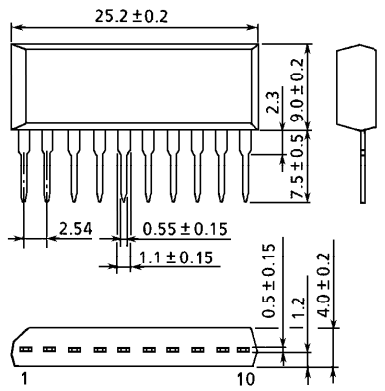
TOSHIBA POWER MOS FET MODULE SILICON N & P CHANNEL MOS TYPE (L^2-π-MOS V 4 IN 1)

MP4212

HIGH POWER HIGH SPEED SWITCHING APPLICATIONS
H - SWITCH DRIVER

INDUSTRIAL APPLICATIONS

Unit in mm



1, 10 SOURCE
2, 4, 6, 8 GATE
3, 5, 7, 9 DRAIN

(PIN 1 AND PIN 10 ARE DISCONNECTED INTERNALLY)

JEDEC	—
EIAJ	—
TOSHIBA	2-25A1C

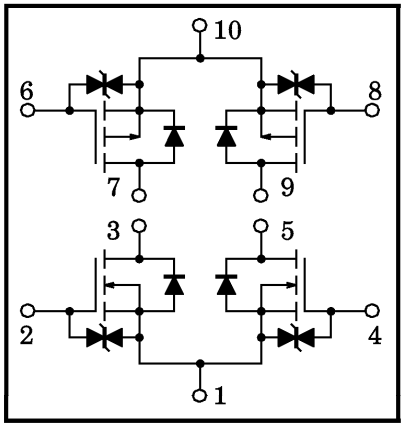
Weight : 2.1 g (typ.)

- 4 V Gate Drive
- Small Package by Full Molding (SIP 10 Pin)
- High Drain Power Dissipation (4 Devices Operation)
  : P_T = 4 W (Ta = 25°C)
- Low Drain-Source ON Resistance
  : $R_{DS\,(ON)}$ = 120 mΩ (typ.) (N-ch)
  160 mΩ (typ.) (P-ch)
- High Forward Transfer Admittance
  : $|Y_{fs}|$ = 5.0 S (typ.) (Nch)
  4.0 S (typ.) (Pch)
- Low Leakage Current : I_{GSS} = ±10 μA (max.) (V_{GS} = ±16 V)
  I_{DSS} = 100 μA (max.) (V_{DS} = 60 V)
- Enhancement-Mode : V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING Nch	RATING Pch	UNIT
Drain-Source Voltage		V_{DSS}	60	−60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ)		V_{DGR}	60	−60	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D	5	−5	A
	Pulse	I_{DP}	20	−20	
Drain Power Dissipation (1 Device Operation, Ta = 25°C)		P_D	2.0		W
Drain Power Dissipation (4 Devices Operation, Ta = 25°C)		P_{DT}	4.0		W
Single Pulse Avalanche Energy*		E_{AS}	129	273	mJ
Avalanche Current		I_{AR}	5	−5	A
Repetitive Avalanche Energy**	1 Device Operation	E_{AR}	0.2		mJ
	4 Devices Operation	E_{ART}	0.4		
Channel Temperature		T_{ch}	150		°C
Storage Temperature Range		T_{stg}	−55~150		°C

ARRAY CONFIGURATION



Note ;

* Avalanche energy (single pulse) applied condition
Nch : V_{DD} = 25 V, Starting T_{ch} = 25°C, L = 7 mH, R_G = 25 Ω, I_{AR} = 5 A
Pch : V_{DD} = −25 V, Starting T_{ch} = 25°C, L = 14.84 mH, R_G = 25 Ω, I_{AR} = −5 A

** Repetitive rating ; Pulse Width Limited by maximum channel temperature.

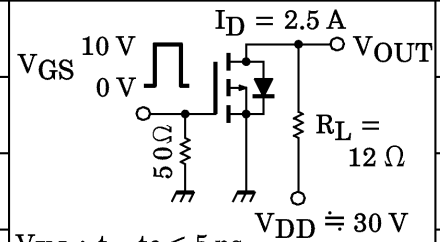
This transistor is an electrostatic sensitive device. Please handle with caution.

000707EAA2

THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, Ta = 25°C)	$\Sigma R_{th\ (ch\text{-}a)}$	31.2	°C / W
Maximum Lead Temperature for Soldering Purposes (3.2 mm from Case for t = 10 s)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Nch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS} = \pm 16$ V, $V_{DS} = 0$ V	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS} = 60$ V, $V_{GS} = 0$ V	—	—	100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\ DSS}$	$I_D = 10$ mA, $V_{GS} = 0$ V	60	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS} = 10$ V, $I_D = 1$ mA	0.8	—	2.0	V
Drain-Source ON Resistance		$R_{DS\ (ON)}$	$V_{GS} = 4$ V, $I_D = 2.5$ A	—	0.21	0.32	Ω
			$V_{GS} = 10$ V, $I_D = 2.5$ A	—	0.12	0.16	
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS} = 10$ V, $I_D = 2.5$ A	3.0	5.0	—	S
Input Capacitance		C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1 MHz	—	370	—	pF
Reverse Transfer Capacitance		C_{rss}		—	60	—	
Output Capacitance		C_{oss}		—	180	—	
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f < 5$ ns, Duty ≦ 1%, $t_w = 10$ μs	—	18	—	ns
	Turn-on Time	t_{on}		—	25	—	
	Fall Time	t_f		—	55	—	
	Turn-off Time	t_{off}		—	170	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$V_{DD} \fallingdotseq 48$ V, $V_{GS} = 10$ V, $I_D = 5$ A	—	12	—	nC
Gate-Source Charge		Q_{gs}		—	8	—	
Gate-Drain (“Miller”) Charge		Q_{gd}		—	4	—	

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I_{DR}	—	—	—	5	A
Pulse Drain Reverse Current	I_{DRP}	—	—	—	20	A
Diode Foward Voltage	V_{DSF}	$I_{DR} = 5$ A, $V_{GS} = 0$ V	—	—	−1.7	V
Reverse Recovery Time	t_{rr}	$I_{DR} = 5$ A, $V_{GS} = 0$ V	—	70	—	ns
Reverse Recovery Charge	Q_{rr}	$dI_{DR} / dt = 50$ A / μs	—	0.1	—	μC

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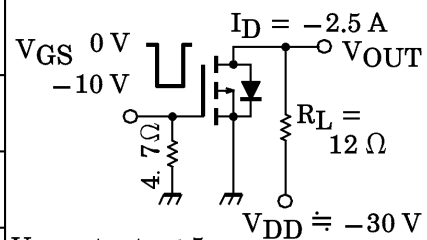
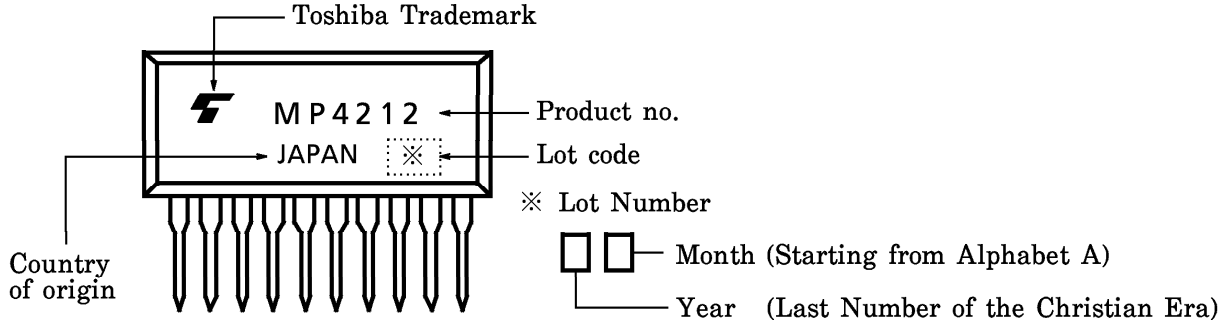
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Pch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS} = \pm 16$ V, $V_{DS} = 0$ V	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS} = -60$ V, $V_{GS} = 0$ V	—	—	−100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	$I_D = -10$ mA, $V_{GS} = 0$ V	−60	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS} = -10$ V, $I_D = -1$ mA	−0.8	—	−2.0	V
Drain-Source ON Resistance		$R_{DS\,(ON)}$	$V_{GS} = -4$ V, $I_D = -2.5$ A	—	0.24	0.28	Ω
			$V_{GS} = -10$ V, $I_D = -2.5$ A	—	0.16	0.19	
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS} = -10$ V, $I_D = -2.5$ A	2.0	4.0	—	S
Input Capacitance		C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1 MHz	—	630	—	pF
Reverse Transfer Capacitance		C_{rss}		—	95	—	
Output Capacitance		C_{oss}		—	290	—	
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f < 5$ ns Duty ≦ 1%, $t_w = 10$ μs	—	25	—	ns
	Turn-on Time	t_{on}		—	45	—	
	Fall Time	t_f		—	55	—	
	Turn-off Time	t_{off}		—	200	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$V_{DD} \fallingdotseq -48$ V, $V_{GS} = -10$ V, $I_D = -5$ A	—	22	—	nC
Gate-Source Charge		Q_{gs}		—	16	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	6	—	

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)

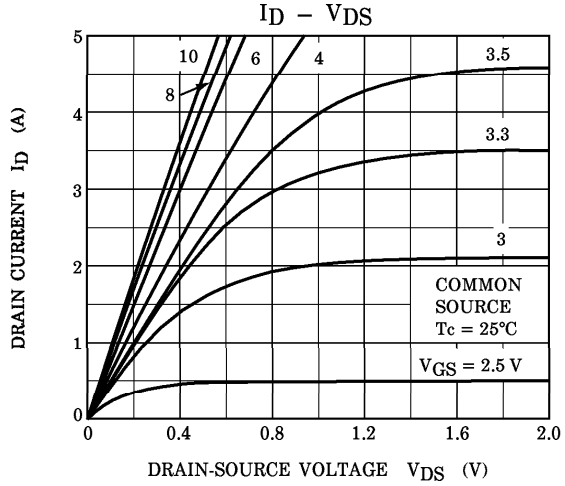
	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I_{DR}	—	—	—	−5	A
Pulse Drain Reverse Current	I_{DRP}	—	—	—	−20	A
Diode Foward Voltage	V_{DSF}	$I_{DR} = -5$ A, $V_{GS} = 0$ V	—	—	1.7	V
Reverse Recovery Time	t_{rr}	$I_{DR} = -5$ A, $V_{GS} = 0$ V	—	80	—	ns
Reverse Recovery Charge	Q_{rr}	$dI_{DR}/dt = 50$ A/μs	—	0.1	—	μC

MARKING

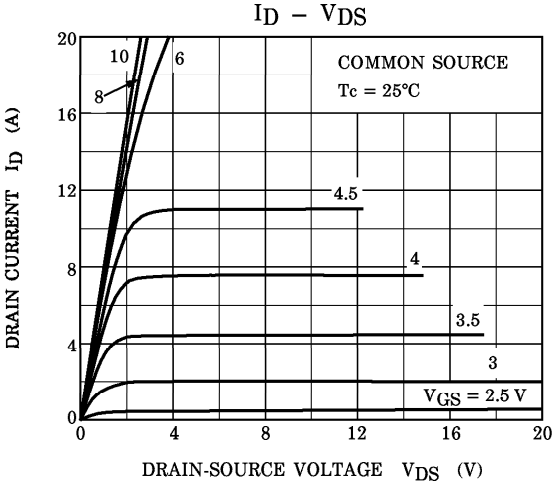


Nch MOS FET

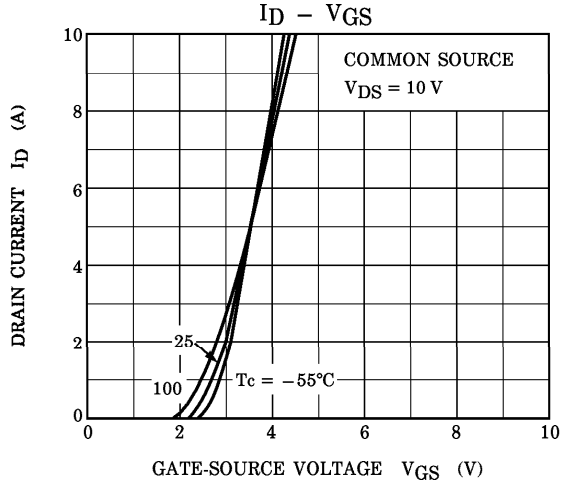
$I_D - V_{DS}$



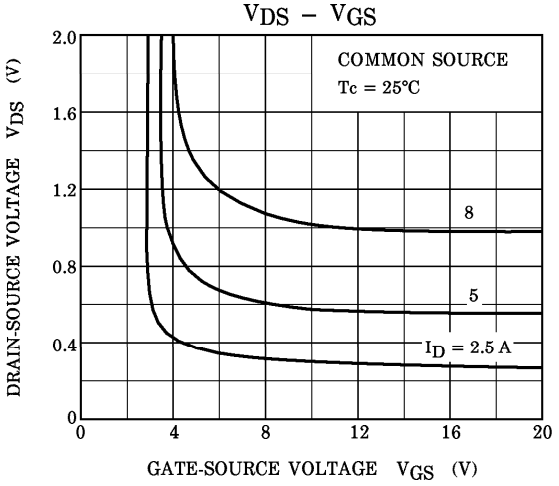
$I_D - V_{DS}$



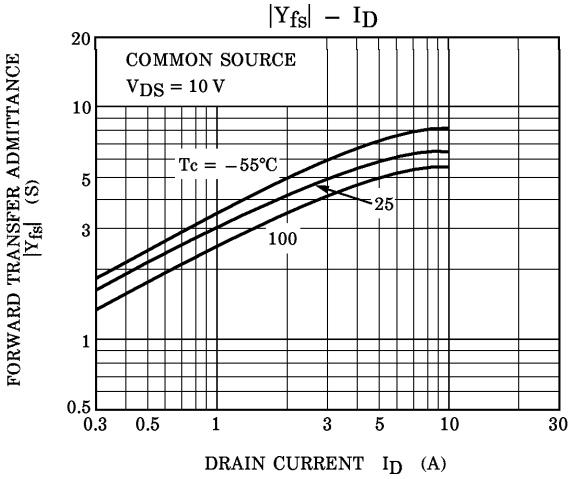
$I_D - V_{GS}$



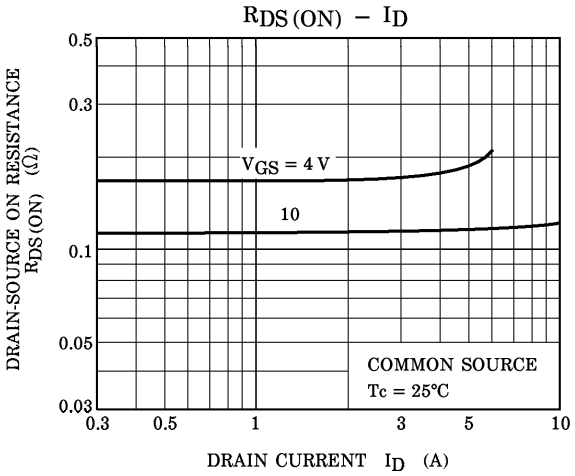
$V_{DS} - V_{GS}$



$|Y_{fs}| - I_D$

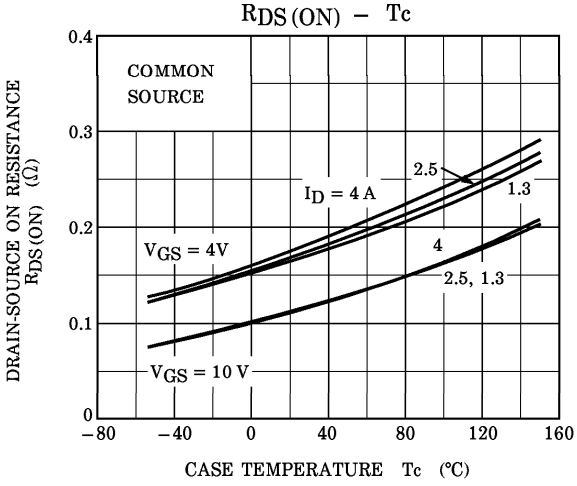


$R_{DS\,(ON)} - I_D$

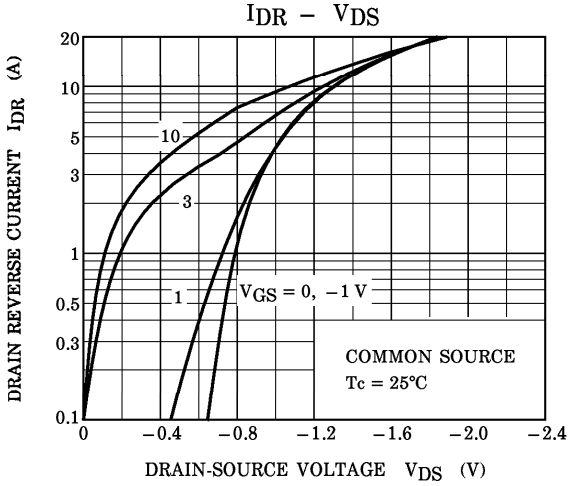


Nch MOS FET

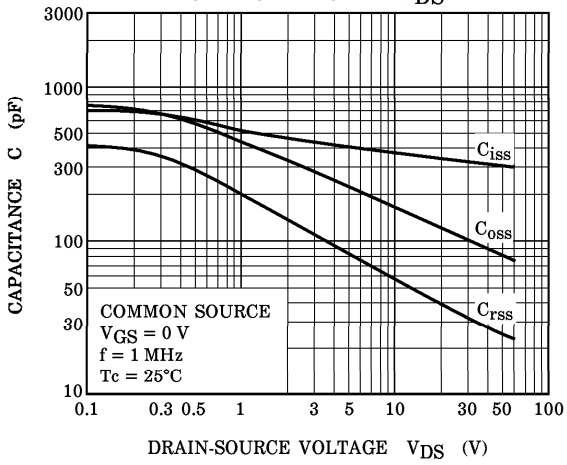
$R_{DS(ON)}$ – Tc



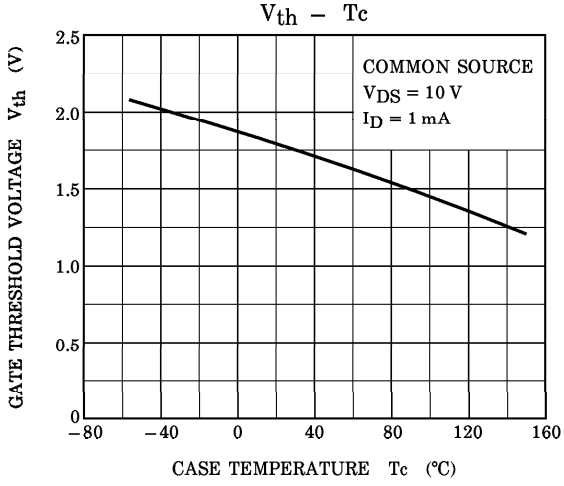
I_{DR} – V_{DS}



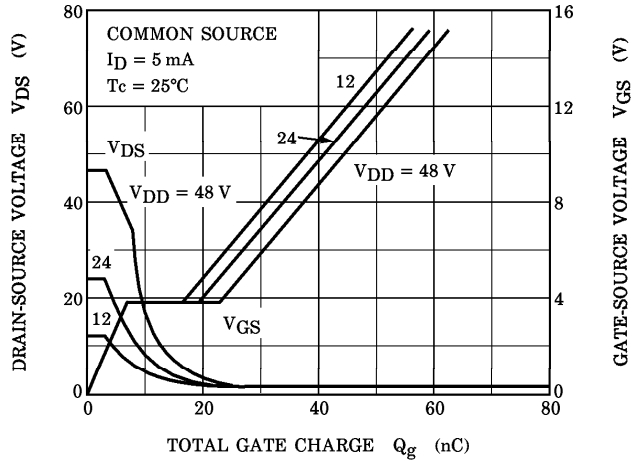
CAPACITANCE – V_{DS}



V_{th} – Tc

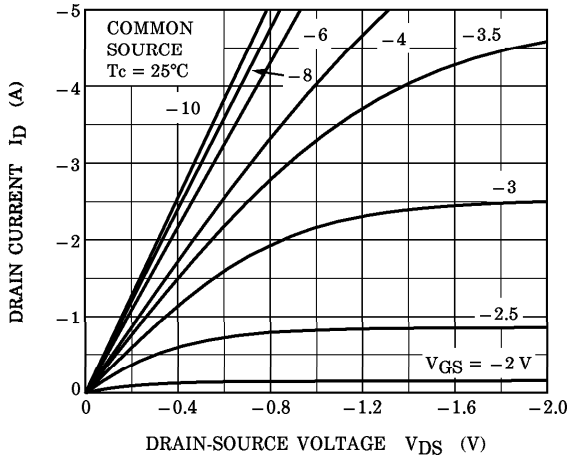


DYNAMIC INPUT / OUTPUT CHARACTERISTICS

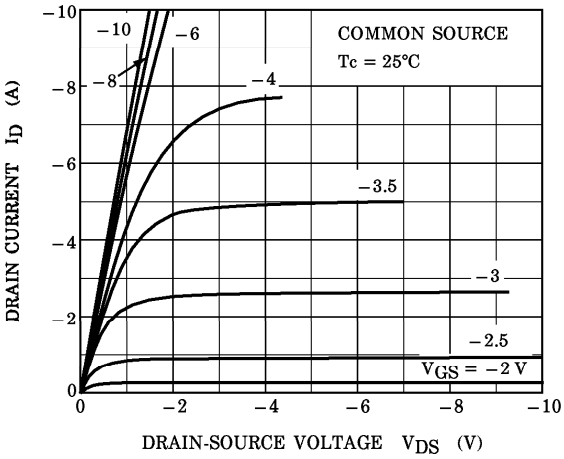


Pch MOS FET

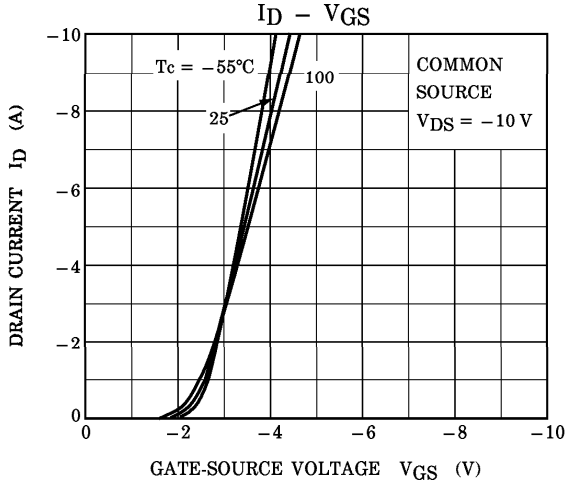
$I_D - V_{DS}$



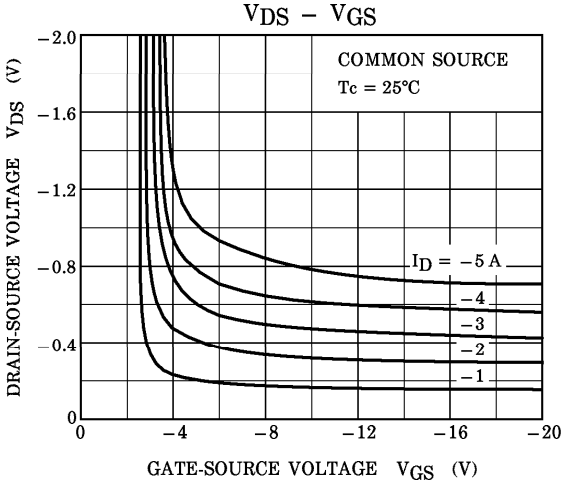
$I_D - V_{DS}$



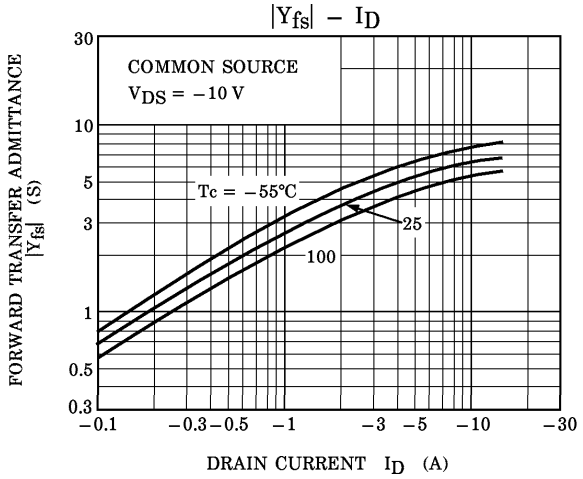
$I_D - V_{GS}$



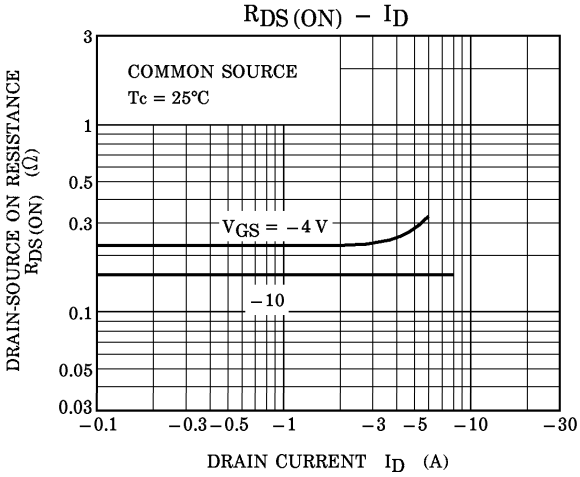
$V_{DS} - V_{GS}$



$|Y_{fs}| - I_D$

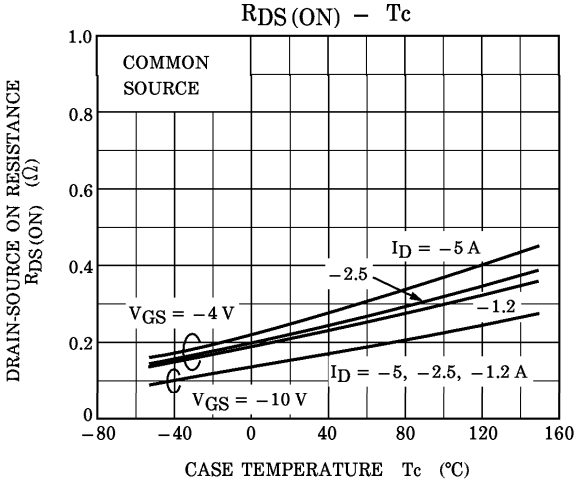


$R_{DS(ON)} - I_D$

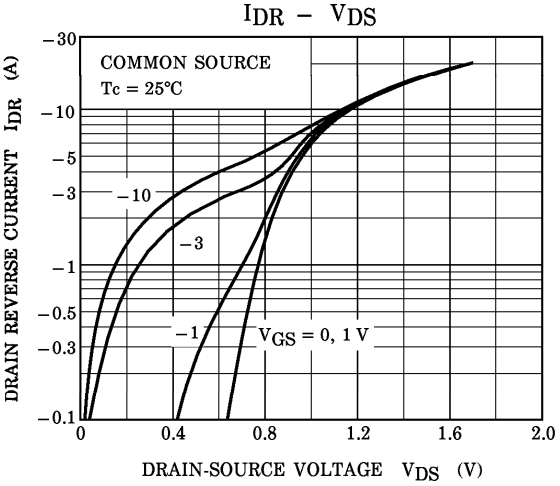


Pch MOS FET

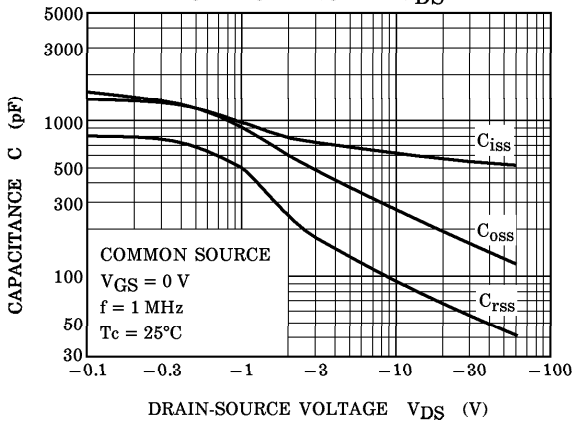
$R_{DS(ON)}$ – Tc



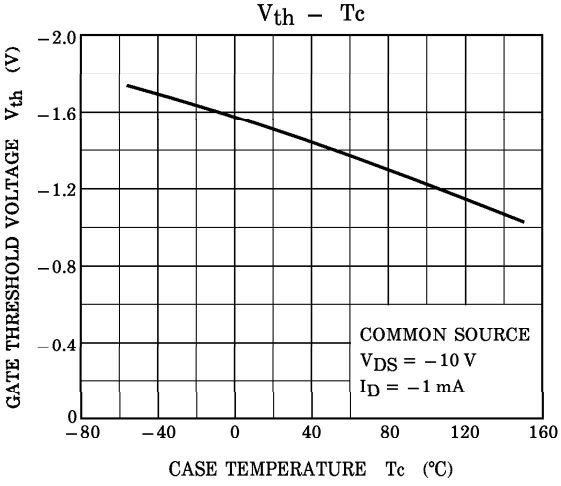
I_{DR} – V_{DS}



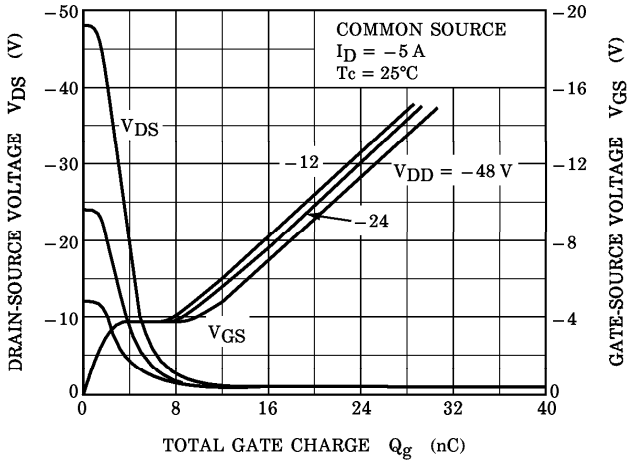
CAPACITANCE – V_{DS}



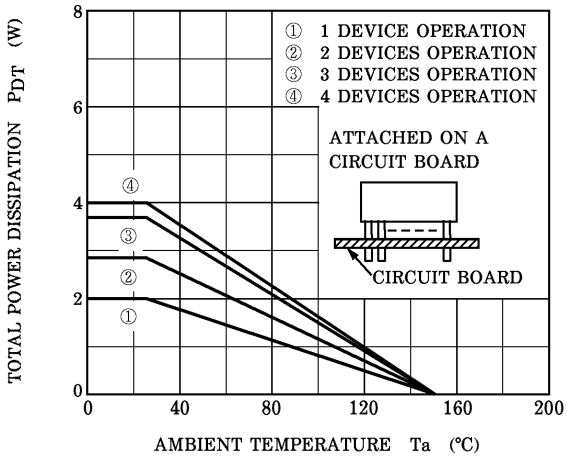
V_{th} – Tc



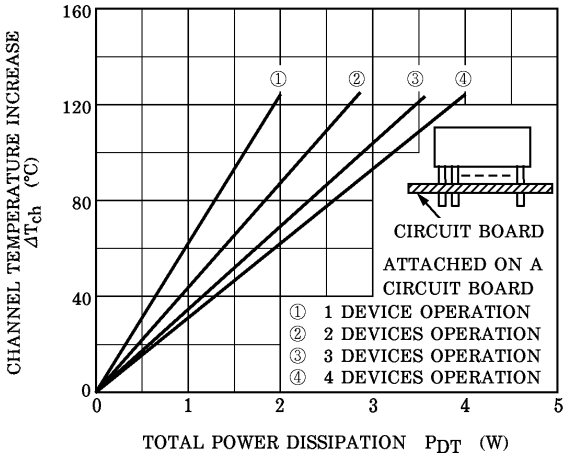
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



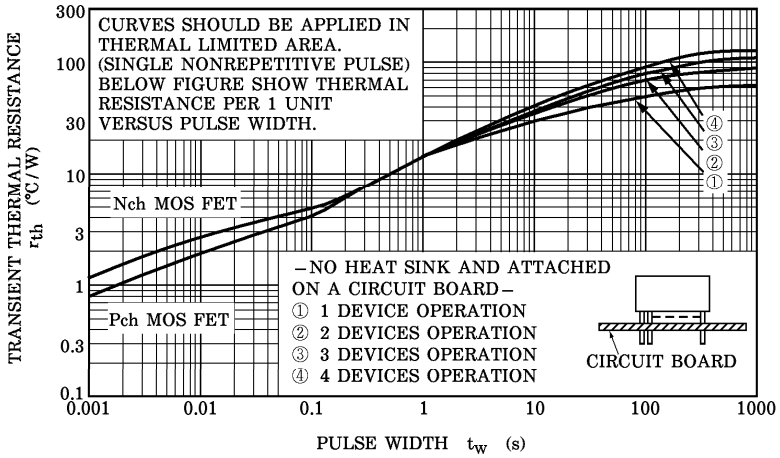
P_{DT} – Ta



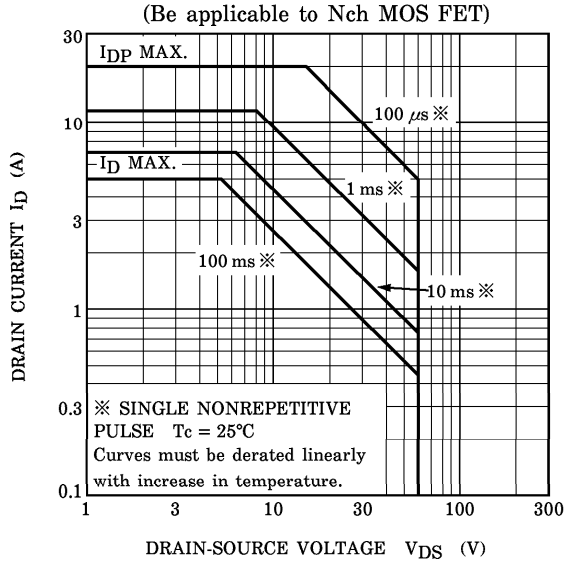
ΔT_{ch} – P_{DT}



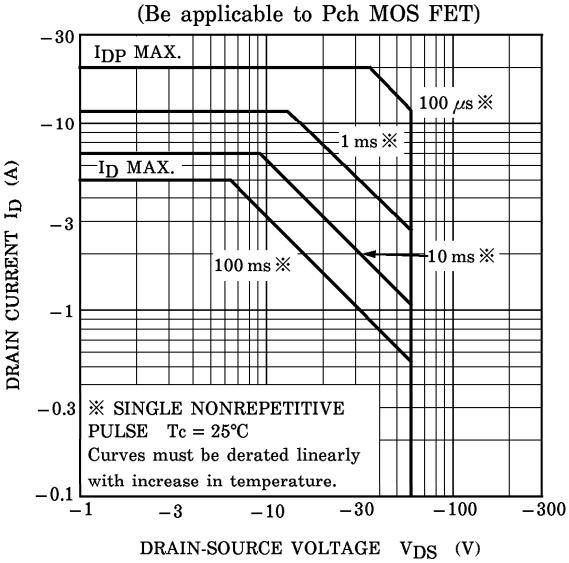
r_{th} – t_w



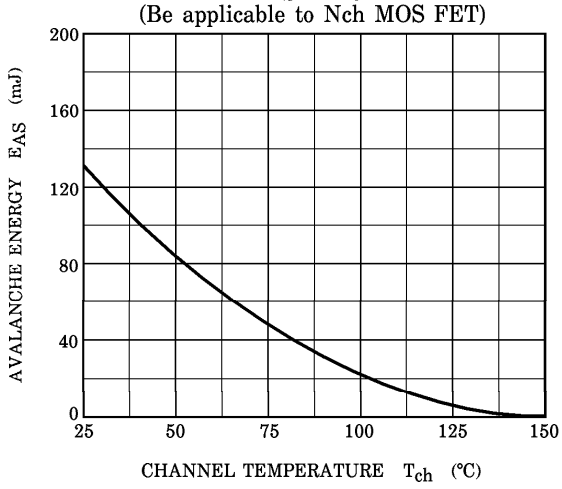
SAFE OPERATING AREA
(Be applicable to Nch MOS FET)



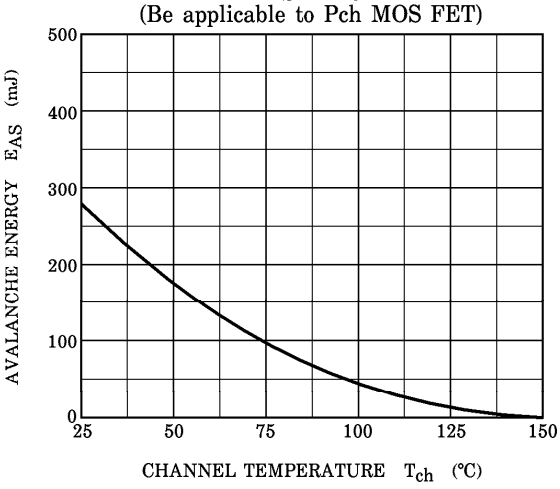
SAFE OPERATING AREA
(Be applicable to Pch MOS FET)

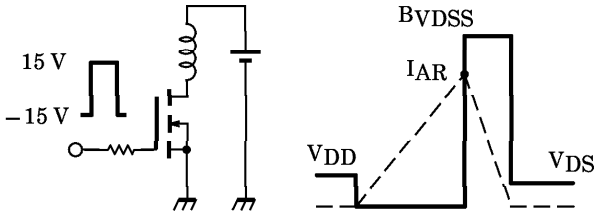


E_{AS} – T_{ch}
(Be applicable to Nch MOS FET)



E_{AS} – T_{ch}
(Be applicable to Pch MOS FET)

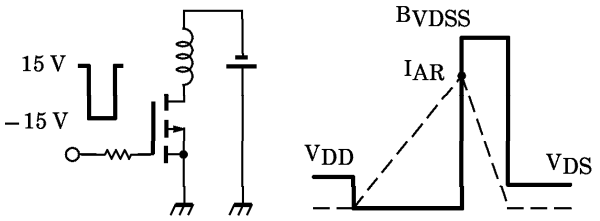




TEST CIRCUIT TEST WAVE FORM

Peak I_{AR} = 5 A, R_G = 25Ω
V_{DD} = 25 V, L = 7 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$



TEST CIRCUIT TEST WAVE FORM

Peak I_{AR} = −5 A, R_G = 25 Ω
V_{DD} = −25 V, L = 14.84 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$