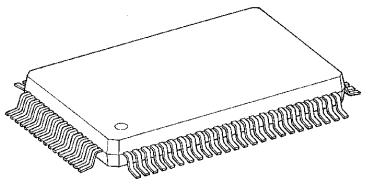
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A46F

PAL NOISE REDUCTION IC

TC90A46F is a noise reduction IC for PAL.
Used together with TC90A36F (field double-speed conversion), the device realizes a noise reduction (NR) function.
As input data, the Y and C signals processed by TC90A36F are used.
The input Y and C signals are digitally processed and their noise is reduced (YNR, CNR).
As memory, general-purpose memory (4M bit EDO) is used.



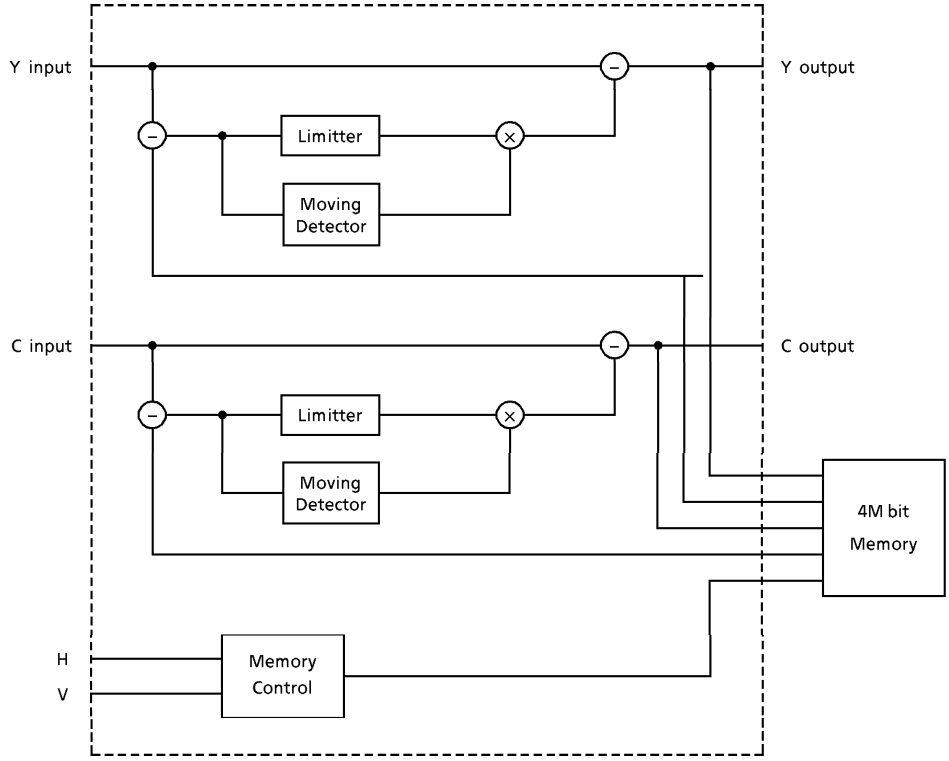
QFP80-P-1420-0.80A

Weight : 1.6 g (Typ.)

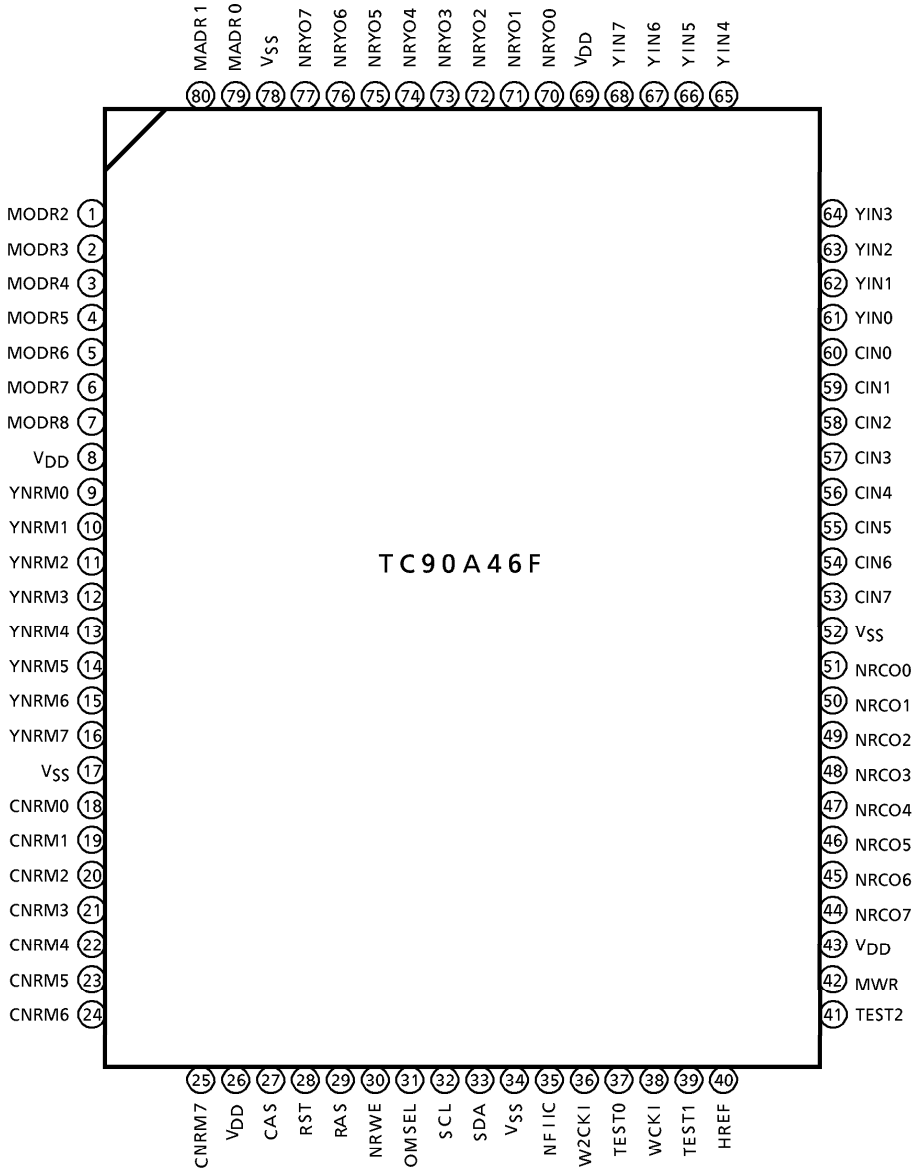
FEATURES

- Realizes PAL noise reduction in combination with TC90A36F.
- Noise reduce processing between Y and C frames using 4M bit memory.
- Motion detector circuit built in.
- EDO memory controller built in.
- Variable NR level
- Y / C digital interface
- Interface with microcontroller using I^2C bus
- 5 V single power supply

BLOCK DIAGRAM



PIN CONNECTION



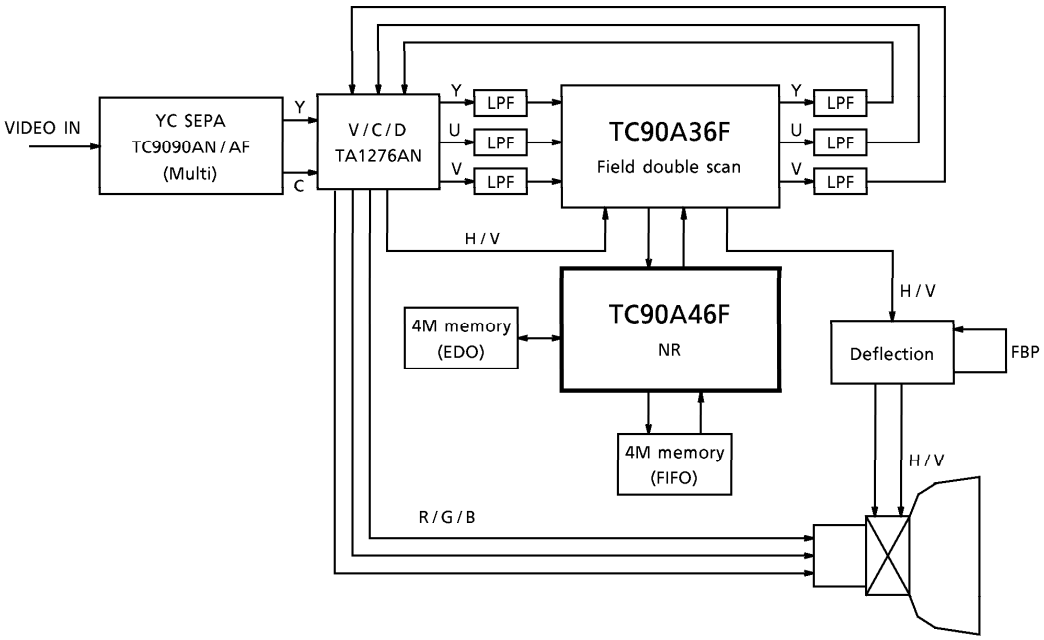
PIN FUNCTION

Pin List (80 pin FP)

PIN No.	PIN NAME	I / O	FUNCTION
1	MADR2	O	Memory address output
2	MADR3	O	Memory address output
3	MADR4	O	Memory address output
4	MADR5	O	Memory address output
5	MADR6	O	Memory address output
6	MADR7	O	Memory address output
7	MADR8	O	Memory address output (MSB)
8	V_{DD}		Digital V_{DD} (±5%)
9	YNRM0	I / O	Y signal memory input / output (LSB)
10	YNRM1	I / O	Y signal memory input / output
11	YNRM2	I / O	Y signal memory input / output
12	YNRM3	I / O	Y signal memory input / output
13	YNRM4	I / O	Y signal memory input / output
14	YNRM5	I / O	Y signal memory input / output
15	YNRM6	I / O	Y signal memory input / output
16	YNRM7	I / O	Y signal memory input / output (MSB)
17	V_{SS}		Digital V_{SS}
18	CNRM0	I / O	C signal memory input / output (LSB)
19	CNRM1	I / O	C signal memory input / output
20	CNRM2	I / O	C signal memory input / output
21	CNRM3	I / O	C signal memory input / output
22	CNRM4	I / O	C signal memory input / output
23	CNRM5	I / O	C signal memory input / output
24	CNRM6	I / O	C signal memory input / output
25	CNRM7	I / O	C signal memory input / output (MSB)
26	V_{DD}		Digital V_{DD} (±5%)
27	CAS	O	CAS signal
28	RST	I	System reset signal
29	RAS	O	RAS signal
30	NRWE	O	Memory write enable
31	OMSEL	I	Test pin
32	SCL	I	I^2C bus clock input
33	SDA	I / O	I^2C bus data input / output
34	V_{SS}		Digital V_{SS}
35	NFIIC	I	I^2C bus noise filter switch
36	W2CKI	I	Double clock input
37	TEST0	I	Test pin
38	WCKI	I	Clock input
39	TEST1	I	Test pin
40	HREF	I	Horizontal reference input

PIN No.	NAME	I / O	FUNCTION
41	TEST2	I	Test pin
42	MWR	I	Frame reset signal input
43	V_{DD}		Digital V_{DD} (±5%)
44	NRCO7	O	C signal output (MSB)
45	NRCO6	O	C signal output
46	NRCO5	O	C signal output
47	NRCO4	O	C signal output
48	NRCO3	O	C signal output
49	NRCO2	O	C signal output
50	NRCO1	O	C signal output
51	NRCO0	O	C signal output (LSB)
52	V_{SS}		Digital V_{SS}
53	CIN7	I	C signal input (MSB)
54	CIN6	I	C signal input
55	CIN5	I	C signal input
56	CIN4	I	C signal input
57	CIN3	I	C signal input
58	CIN2	I	C signal input
59	CIN1	I	C signal input
60	CIN0	I	C signal input (LSB)
61	YIN7	I	Y signal input (MSB)
62	YIN6	I	Y signal input
63	YIN5	I	Y signal input
64	YIN4	I	Y signal input
65	YIN3	I	Y signal input
66	YIN2	I	Y signal input
67	YIN1	I	Y signal input
68	YIN0	I	Y signal input (LSB)
69	V_{DD}		Digital V_{DD} (±5%)
70	NRYO7	O	Y signal output (MSB)
71	NRYO6	O	Y signal output
72	NRYO5	O	Y signal output
73	NRYO4	O	Y signal output
74	NRYO3	O	Y signal output
75	NRYO2	O	Y signal output
76	NRYO1	O	Y signal output
77	NRYO0	O	Y signal output (LSB)
78	V_{SS}		Digital V_{SS}
79	MADR0	O	Memory address output (LSB)
80	MADR1	O	Memory address output

NR SYSTEM

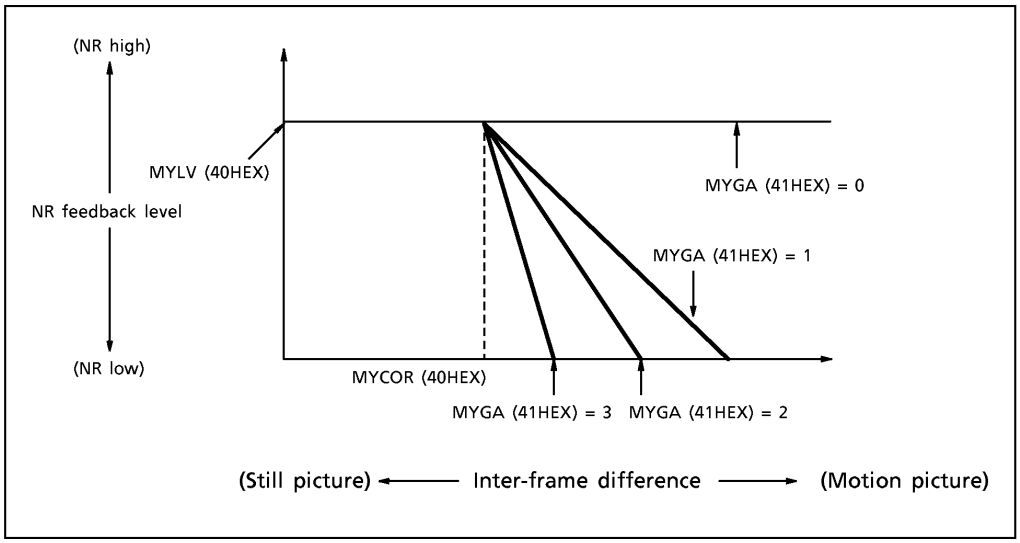

VIDEO IN
YC SEPA
TC9090AN / AF
(Multi)
Y
C
V / C / D
TA1276AN
Y
U
V
LPF
LPF
LPF
TC90A36F
Field double scan
Y
U
V
LPF
LPF
LPF
H / V
TC90A46F
NR
4M memory
(EDO)
4M memory
(FIFO)
H / V
Deflection
FBP
H / V
R / G / B

I²C BUS REGISTERS

SUB ADDRESS	15	14	13	12	11	10	9	8	7
40HEX	ONMVF	YSTD	YSTD	MYST	MYLV3	MYLV2	MYLV1	MYLV0	

6	5	4	3	2	1	0
		MYCO4	MYCO3	MYCO2	MYCO1	MYCO0

ONMVF (1) Y motion detect horizontal filter 0 : off 1 : on
YSTDP (1) Y PAL detection (1 : on)
YSTDN (1) Y NTSC detection (1 : on)
MYSTD (1) Y forced standard mode (1 : on)
MYLV (4) Y NR level
MYCOR (5) Y motion detect sensitivity Offset



SUB ADDRESS	15	14	13	12	11	10	9	8	7
41HEX	YEGL3	YEGL2	YEGL1	YEGL0	YEDON		MYGA1	MYGA0	FBL

6	5	4	3	2	1	0
YLTL6	YLTL5	YLTL4	YLTL3	YLTL2	YLTL1	YLTL0

YEGL Y motion detect horizontal edge detect level
YEGON Y motion detect horizontal edge detect control on / off (1 : on)
MYGA Y motion detect sensitivity Gradient
FBNLC Y motion detect non-linear control (normally set to 0)
YLTL Y feedback limit value

SUB ADDRESS	15	14	13	12	11	10	9	8	7
42HEX		CSTDP	CSTDN	MCSTD	MCLV3	MCLV2	MCLV1	MCLV0	

6	5	4	3	2	1	0
		MCCO4	MCCO3	MCCO2	MCCO1	MCCO0

CSTDP C PAL detection (1 : on)
CSTDN C NTSC detection (1 : on)
MCSTD C forced standard mode (1 : on)
MCLV C NR level
MCCOR C motion detect sensitivity Offset

SUB ADDRESS	15	14	13	12	11	10	9	8	7
43HEX							MCGA1	MCGA0	

6	5	4	3	2	1	0
CLTL6	CLTL5	CLTL4	CLTL3	CLTL2	CLTL1	CLTL0

MCGA C motion detect sensitivity Gradient
CLTL C feedback limit value

SUB ADDRESS	15	14	13	12	11	10	9	8	7
44HEX	NVWS8	NVWS7	NVWS6	NVWS5	NVWS4	NVWS3	NVWS2	NVWS1	NVWS0

6	5	4	3	2	1	0
NHWS6	NHWS5	NHWS4	NHWS3	NHWS2	NHWS1	NHWS0

NVWST NR vertical start phase
NHWST NR horizontal start phase

SUB ADDRESS	15	14	13	12	11	10	9	8	7
45HEX	NVWE8	NVWE7	NVWE6	NVWE5	NVWE4	NVWE3	NVWE1	NVWE2	NVWE0

6	5	4	3	2	1	0
NHWE6	NHWE5	NHWE4	NHWE3	NHWE2	NHWE1	NHWE0

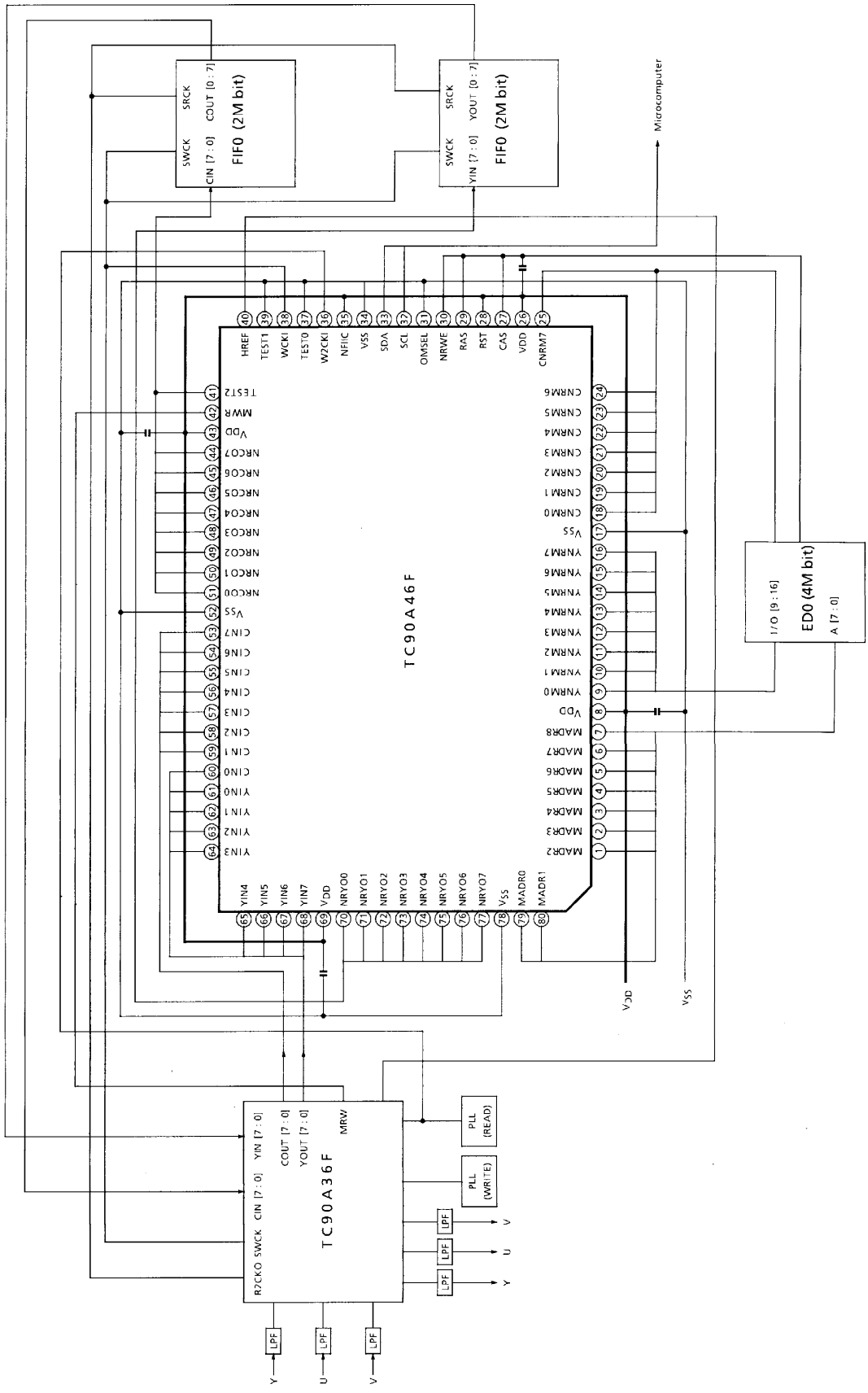
NVWST NR vertical end phase
NVWST NR horizontal end phase

SUB ADDRESS	15	14	13	12	11	10	9	8	7
46HEX	YCLT3	YCLT2	YCLT1	YCLT0			YNGA1	YNGA0	

6	5	4	3	2	1	0
		YNCO	YNCL3	YNCL2	YNCL1	YNCL0

YCLT Motion-linked Y coring level limit
YNGA Motion-linked Y coring gain
YNCON Motion-linked Y coring on / off (1 : on)
YNCL Motion-linked Y coring offset (must match MYLV)

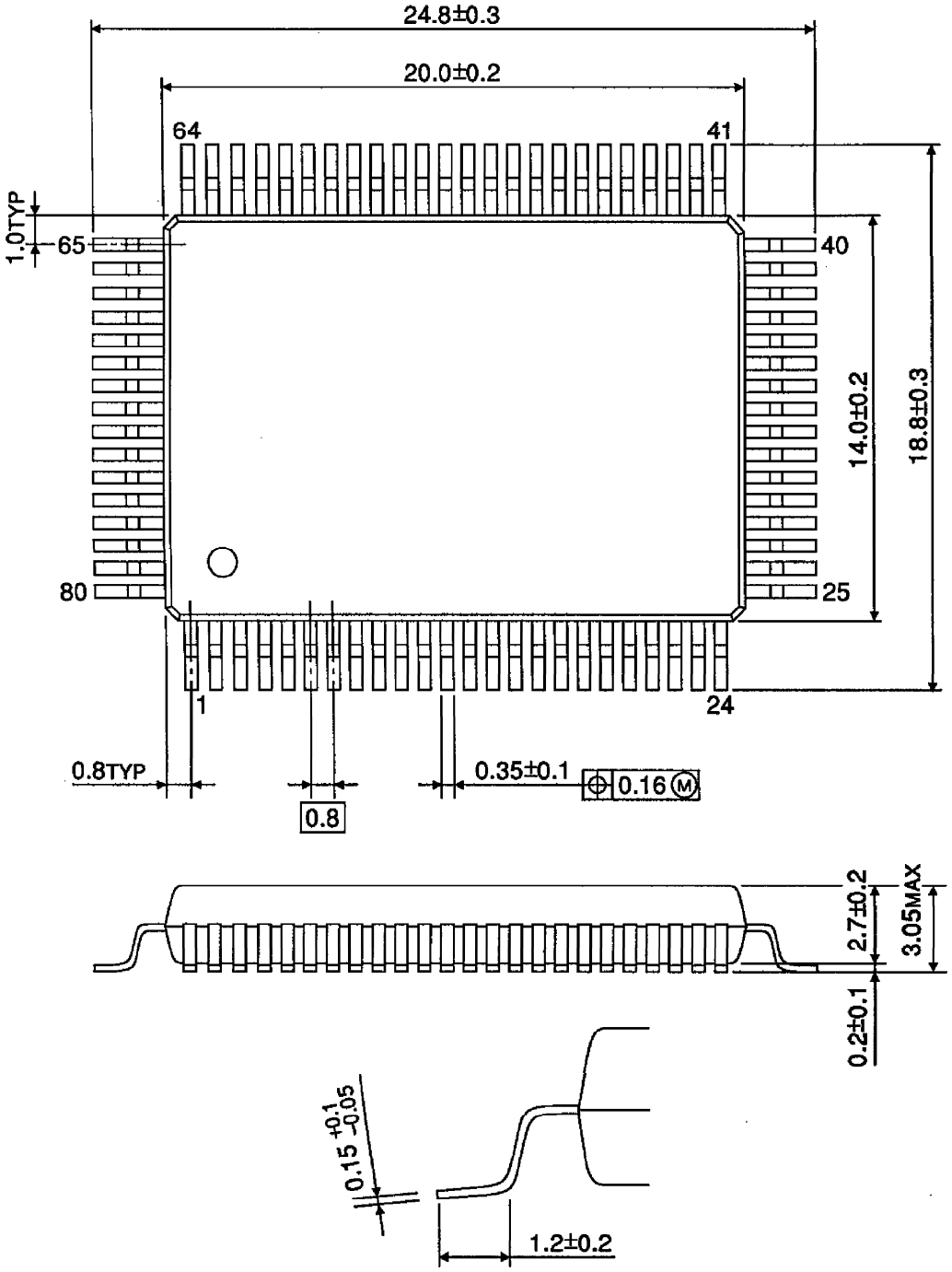
APPLICATION CIRCUIT



TC90A46F-9

PACKAGE DIMENSIONS

QFP80-P-1420-0.80A Unit : mm



Weight : 1.6g (Typ.)