CMOS 8-Bit Microcomputer

TMP87CH48U / DF

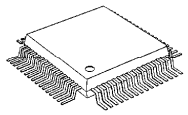
TMP87CH48 is a low power, high-speed and high-performance 8-bit single chip microcomputer, including large capacity ROM/RAM, input/output ports, a multiple timer counter, serial interfaces (UART, I2C-bus, and SIO), four 12-bit PWM outputs, a 10-bit A/D converter and two oscillators.

Part No.	ROM	RAM	Package	OTP
TMP87CH48U	16 Kbytes	512 bytes	P-LQFP64-1010-0.50	TMP87PH48U
TMP87CH48DF			P-QFP64-1414-0.80A	TMP87PH48DF

Features

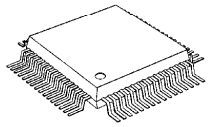
- ◆ 8-bit single chip microcomputer TLCS-870 series
- ◆ Minimum instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- ◆ 412 basic machine instructions: 129 types
- ◆ 15 interrupt sources (External: 6, Internal: 9)
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject.
  - High-speed task switching by register bank changeover
- ◆ Input/output ports (56 pins)
  - High current output: 8 pins (typ.20 mA), LED direct drive
- ◆ 16-bit timer counters: 2 channels
  - Timer, Event counter, PPG (Programmable Pulse Generator) output, Pulse width measurement, External trigger timer, Window modes
- ◆ 8-bit timer counters: 2 channels
  - Timer, Event counter, Capture (Pulse width/duty measurement) PWM (Changeable pulse width) output, PDO (ProgrammableDivider Output)
- ◆ Time base timer (Interrupt frequency: 1 to 16384 Hz)
- ◆ Divider output functions (Frequency: 1 to 8 kHz)
- ◆ Watchdog timer
  - Interrupt/Reset output (programmable)
- ◆ D/A conversion (changeable pulse width) output
  - 12-bit resolution: 4 channels
- ◆ UART: 1 channel (parity·framing·overrun error detection)
- ◆ Serial bus interface (SBI-ver. B)
  1 channel (I2C bus or clock synchronous SIO)
- ◆ 10-bit successive approximation type A/D converter
  - Analog input: 16 channels
  - Conversion time: 24.5 μs or 98 μs (at 8 MHz)

P-LQFP64-1010-0.50



TMP87CH48U
TMP87PH48U

P-QFP64-1414-0.80A



TMP87CH48DF
TMP87PH48DF

980910EBP1

◆ Clock oscillation circuit: Two circuits
- Single/Dual clock modes (Initial mode is always set to a single clock mode.)

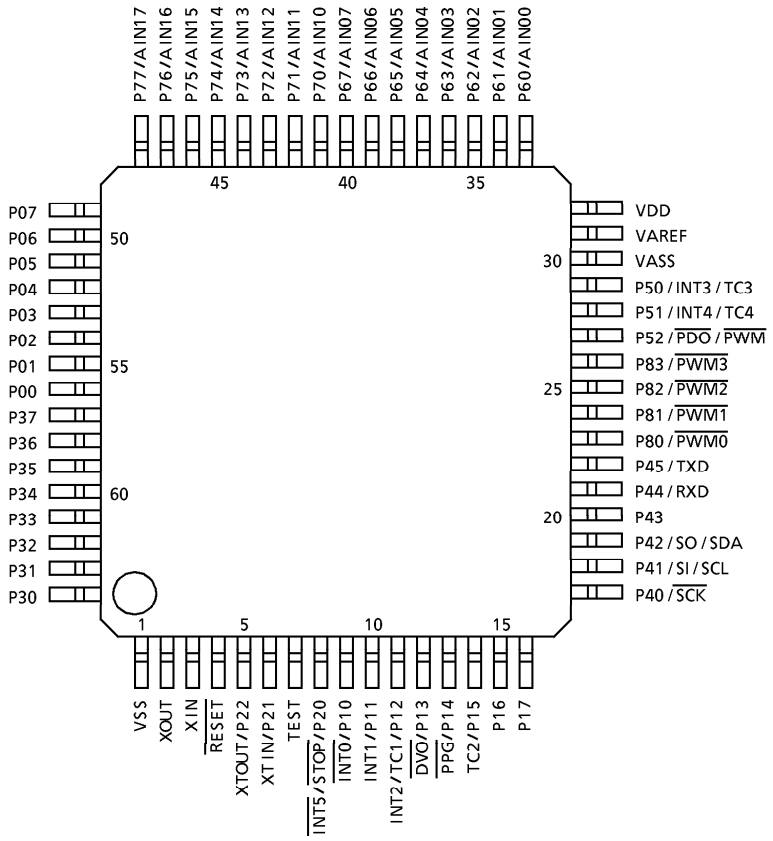
◆ Low consumption power (Five modes)
- STOP mode: Oscillation stop (Battery/Capacitor back-up). Port output hold/high-impedance.
- SLOW mode: Low consumption power operation by low-frequency clock
- IDEL1 mode: CPU stops, and only peripheral hardware operates using high-frequency clock. Release by interrupts (CPU restarts).
- IDEL2 mode: CPU stops, and only peripheral hardware operates using high or low-frequency clock). Release by interrupts.
- SLEEP mode: CPU stops, and only peripheral hardware operates using low-frequency clock. Release by interrupts.

◆ Operation voltage: 2.7 to 5.5 V at 4.2 MHz / 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz

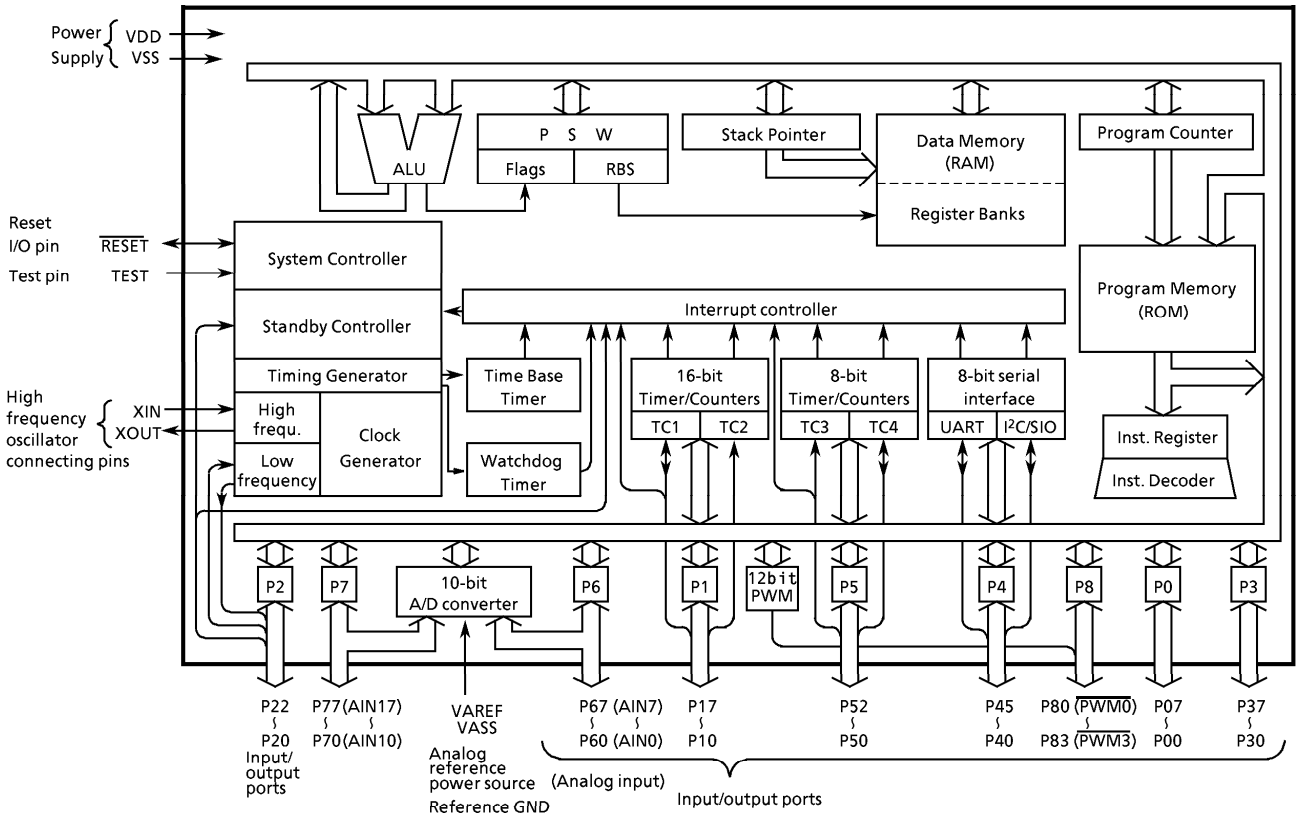
◆ Emulation pod: BM87CH48U0A

Pin Assignments (Top View)

P-LQFP64-1010-0.50
P-QFP64-1414-0.80A



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
P07 to P00	I/O	8-bit programmable input/output port (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as an external interrupt input or a timer counter input, the latch must be set to input mode. When used as PPG output or a divider output, the output latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port. When used as an input port, an oscillator connecting pin, an external interrupt input or STOP mode release input of P20, the output latch must be set to "1".	Low frequency oscillator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P37 to P30	I/O	8-bit input/output port (high current output). When used as an input port, the output latch must be set to "1".	
P45 (TxD)	I/O (Output)	8-bit input/output port. When used as an input port, a serial interface pin, the output latch must be set to "1".	UART serial data output (send)
P44 (RxD)	I/O (Input)		UART serial data output (receive)
P43	I/O		
P42 (SO / SDA)	I/O (Output, I/O)		SIO serial data output or I^2C bus data input/output
P41 (SI / SCL)	I/O (Input, I/O)		SIO serial data output or I^2C bus clock input/output
P40 ($\overline{SCK}$)	I/O (I/O)		SIO serial clock input/output
	I/O		
P52 ($\overline{PWM}$ / $\overline{PDO}$)	I/O (Output)	3-bit input/output port. When used as an input port, PWM output, high-speed PWM output, a programmable divider output, an external interrupt input or timer counter input, the output latch must be set to "1".	8-bit PWM output or 8-bit programmable divider output
P51 (INT4 / TC4)	I/O (Input)		External interrupt input 4 or Timer counter 4 input
P50 (INT3 / TC3)			External interrupt input 3 or Timer counter 3 input
P67 (AIN7) to P60 (AIN0)	I/O	8-bit programmable input/output port (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as an analog input, the latch must be set to an analog input mode by P6CR and P7CR.)	A/D converter analog input
P77 (AIN17) to P70 (AIN10)			
P83 ($\overline{PWM3}$) to P80 ($\overline{PWM0}$)	I/O (Output)	4-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control. An input or an output is determined by setting P8CR.	DA conversion (PWM) output ($\overline{PWM3}$ to $\overline{PWM0}$)
XIN, XOUT	Input, Output	Oscillator connecting pins for high frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for outgoing test. Be externally tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		A/D conversion analog reference voltage, Reference GND.	

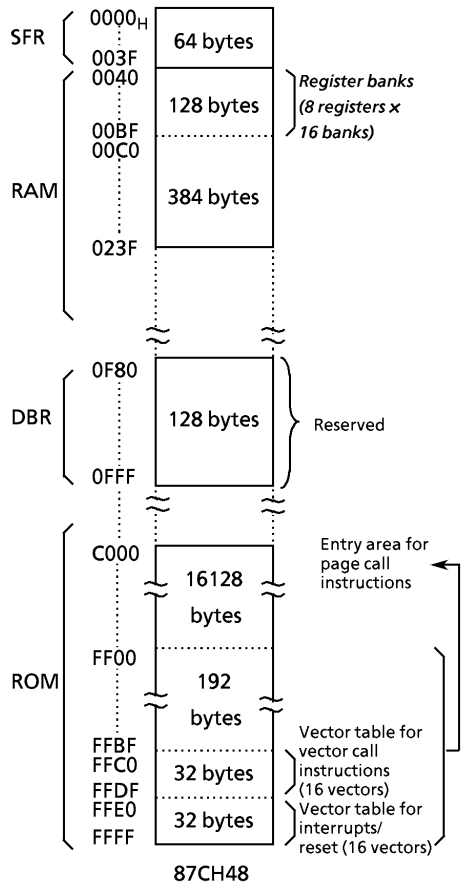
OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CH48. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.



Note :

ROM ; Read Only Memory includes :
Program memory

RAM ; Random Access Memory includes :
Data memory
Stack
General-purpose register banks

SFR ; Special Function Register includes :
I/O ports
Peripheral control registers
Peripheral status registers
System control registers
Interrupt control registers
Program Status Word

DBR ; Data Buffer Register includes :
SIO data buffer

Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	120	mA
	ΣI_{OUT2}	Port P3	120	
Power Dissipation	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	* V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs	VDD = 5.0 V	–	0.9	–	V
Input Current	I_{IN1}	TEST	VDD = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$	VDD = 5.0 V	100	220	450	kΩ
Output Leakage Current	I_{LO}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
		Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5/0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except for XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	mA
Output Low current	I_{OL3}	P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 8 MHz fs = 32.768 kHz	–	4.5	5.5	mA
Supply Current in IDLE 1, 2 modes				–	2.5	4.0	mA
Supply Current in NORMAL 1, 2 modes			V_{DD} = 3.0 V, V_{IN} = 2.8V/0.2V V_{IN} = 4.19 MHz fs = 32.768 kHz	–	1.75	3.0	mA
Supply Current in IDLE 1, 2 modes				–	1.25	2.0	mA
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz	–	20	30	μA
Supply Current in SLEEP mode				–	10	20	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C
Note 2: Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-upor pull-down) is contained.
Note 3: IDD except for I_{REF}.

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max			Unit
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	—	V_{DD}			V
	V_{ASS}		V_{SS}	—	1.5			
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}			V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	—	0.5	1.2			mA
Nonlinearity Error		V_{DD} = 5.0, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	—	—	1.0			LSB
Zero Point Error			—	—	± 1	± 3	± 2	
Full Scale Error			—	—	± 1	± 3	± 2	
Total Error			—	—	± 2	± 6	± 4	

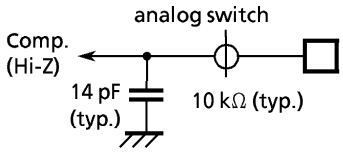
Note 1: $\triangle V_{AREF} = V_{AREF} - V_{ASS}$
ADCDR1 ; 8 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 256)
ADCDR2 ; 10 bit – A/D conversion result (1LSB = $\triangle V_{AREF}$ / 1024)
Note 2: Quantizing error is not contained in those errors.

A.C. Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	V_{DD}	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL 1, 2 mode	4.5 to 5.5V	0.5	–	10	μs
		In IDLE 1, 2 mode					
		In SLOW mode	2.7 to 5.5V	117.6	–	133.3	
		In SLEEP mode					
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	4.5 to 5.5V	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}						
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	2.7 to 5.5V	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}						
A/D Conversion Time	t_{ADC}	ADCCR bit 4 ; ACK = 0	–	–	49 tcy	–	ns
		ADCCR bit 4 ; ACK = 1	–	–	196 tcy	–	

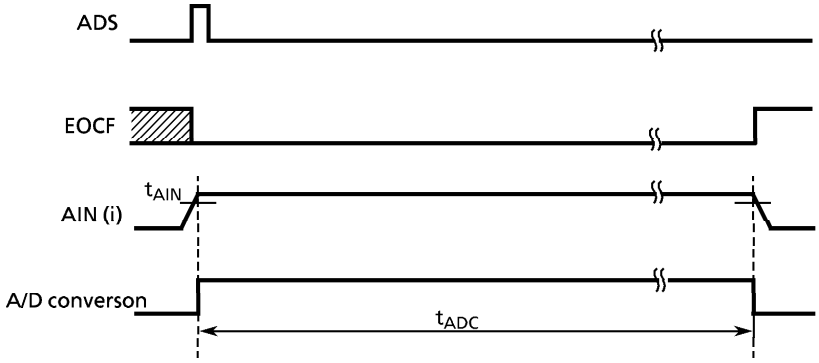
AIN (i) internal circuit



Note 1: V_{AIN} must be kept the voltage level during A/D conversion period (t_{ADC})

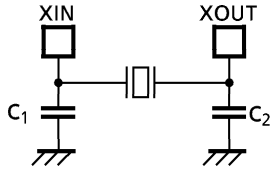
Note 2: i = 17 to 10, 07 to 00

Timing of A/D Conversion

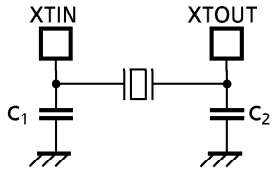


Recommended Oscillating Conditions (V_{SS} = 0 V, V_{DD} = 2.7 / 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C_1	C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	4.5 to 5.5V	KYOCERA KBR8.0M	30 pF	30 pF
		4 MHz	2.7 to 5.5V	KYOCERA KBR4.0MS		
				MURATA CSA4.00MG		
	Crystal Oscillator	8 MHz	4.5 to 5.5V	TOYOCOM 210B 8.0000	20 pF	20 pF
		4 MHz	2.7 to 5.5V	TOYOCOM 204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 to 5.5V	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.