TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95C061B

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-bit Microcontroller
TMP95C061BF

1. Outline and Device Characteristics

TMP95C061BF is high-speed advanced 16-bit microcontroller developed for controlling medium to large-scale equipment. TMP95C061BF is housed in an 100-pin mini flat package (QFP100-P-1414-0.50). TMP95C061BEF is housed in QFP100-P-2222-0.80A package.

Device characteristics are as follows:

(1) Original High speed 16-bit CPU (900/H CPU)
- TLCS-90/900 instruction mnemonic upward compatible.
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication / division and bit transfer / arithmetic instructions
- Micro DMA : 4 channels (640 ns / 2 bytes at 25 MHz)

(2) Minimum instruction execution time : 160 ns at 25 MHz

(3) Internal RAM : None
Internal ROM : None

(4) External memory expansion
- Can be expanded up to16 Mbytes (for both programs and data).
- AM8 / $\overline{16}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses. ··· Dynamic data bus sizing

(5) DRAM Controller

(6) 8-bit timer : 4 channels

(7) 16-bit timer : 2 channels

(8) Pattern generator : 4 bits, 2 channels

(9) Serial interface : 2 channels
(Only for channel 0, external clock can be used in UART mode.)
(10) 10-bit A/D converter : 4 channels
(11) Watchdog timer
(12) Chip select / wait controller : 4 blocks
(13) Interrupt functions
- 2 CPU interrupts ..... SWI instruction, and Illegal instruction
- 18 internal interrupts ... 7-level priority can be set.
- 6 external interrupts .... 7-level priority can be set.

(14) I/O ports
56 pins
(15) Standby function : 3 HALT modes (RUN, IDLE, STOP)

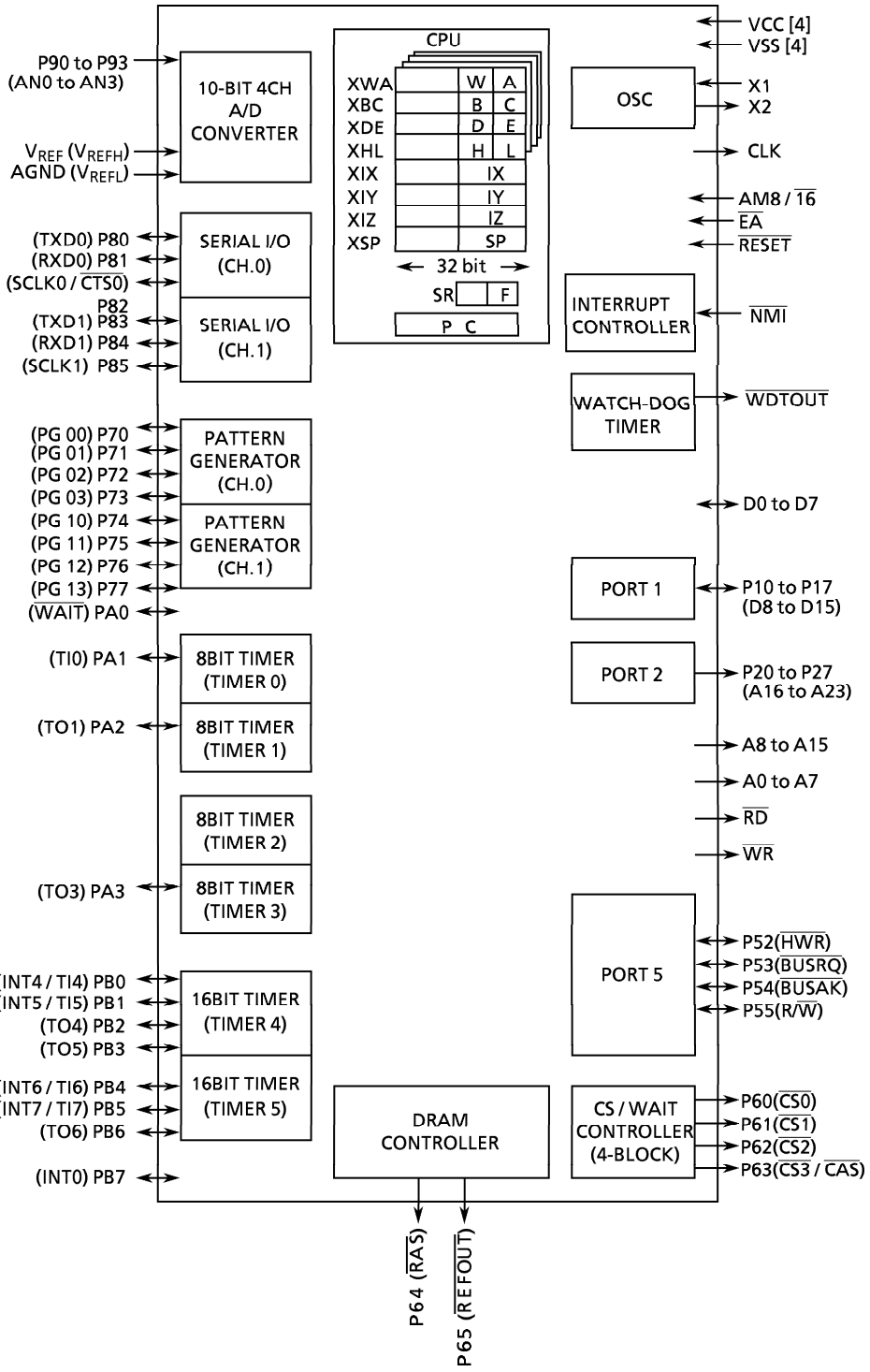


Figure 1 TMP95C061B Block Diagram

2. Pin Assignment and Functions

The assignment of input / output pins for TMP95C061B their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP95C061B.

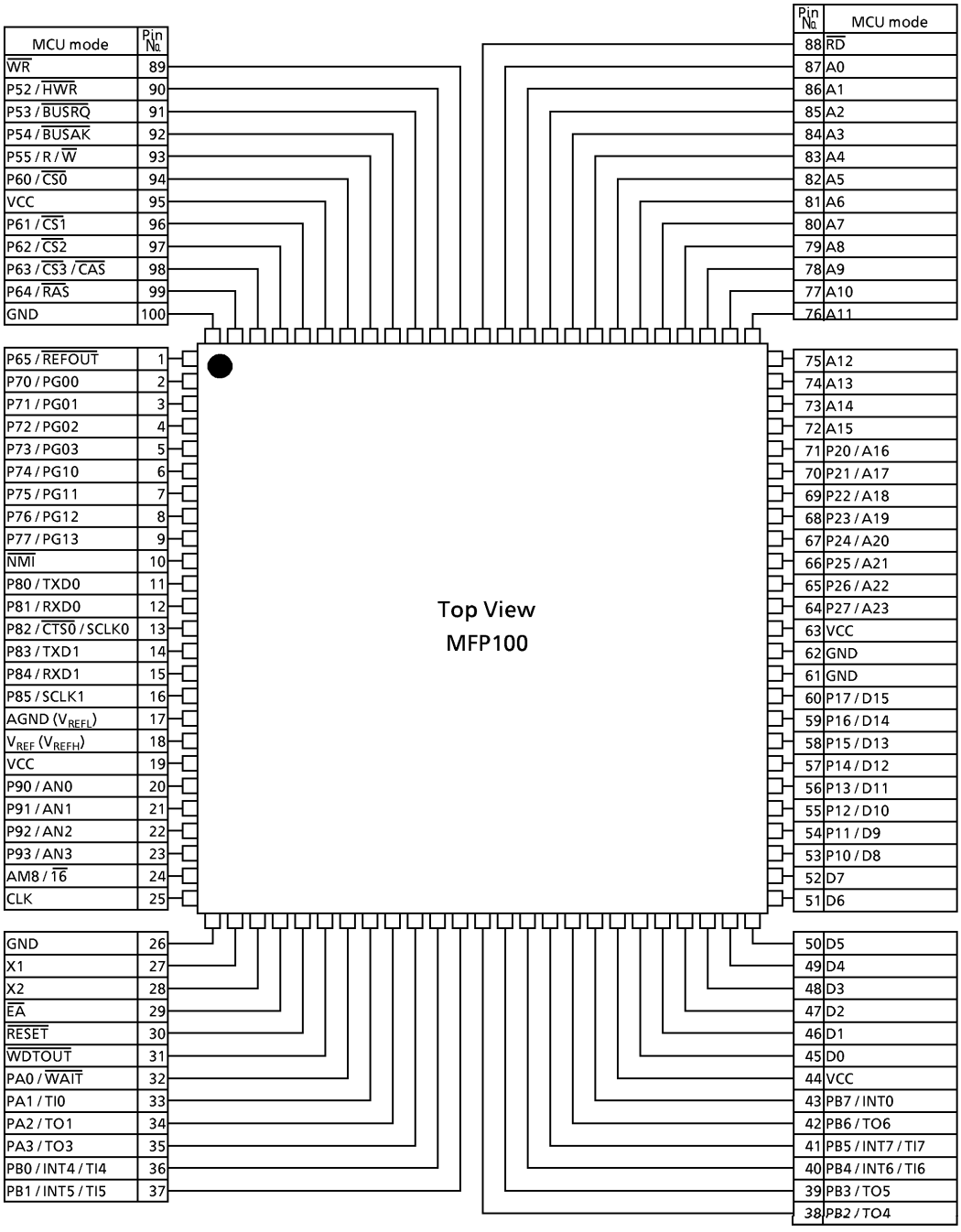


Figure 2.1 Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

The names of input / output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Table 2.2

Pin name	Number of pins	I/O	Functions
D0 to D7	8	I/O	Data : 0 to 7 for data bus
P10 to P17 D8 to D15	8	I/O I/O	Port 1 : I/O ports that allow I/O to be selected on a bit basls Data : 8 to 15 for data bus
P20 to P27 A16 to A23	8	Output Output	Port 2 : Output ports Address : 16 to 23 for address bus
A8 to A15	8	Output	Address : 8 to 15 for address bus
A0 to A7	8	Output	Address : 0 to 7 for address bus
$\overline{RD}$	1	Output	Read : Strobe signal for reading external memory
$\overline{WR}$	1	Output	Write : Strobe signal for writing data on pins D0 to 7
P52 $\overline{HWR}$	1	I/O Output	Port 52 : I/O port (with pull-up resistor) High Write : Strobe signal for writing data on pins D8 to 15
P53 $\overline{BUSRQ}$	1	I/O Input	Port 53 : I/O port (with pull-up resistor) Bus request : Signal used to request high impedance for D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$ to $\overline{CS3}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{REFOUT}$ (*) pins. (for external DMAC)
P54 $\overline{BUSAK}$	1	I/O Output	Port 54 : I/O port (with pull-up resistor) Bus Acknowledge : Signal indicating that D0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$ to $\overline{CS3}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{REFOUT}$ (*) pins are at high impedance after receiving $\overline{BUSRQ}$. (for external DMAC)
P55 R/$\overline{W}$	1	I/O Output	Port 55 : Output port (with pull-up resistor) Read/Write : 1 : indicates read or dummy cycle 0 : indicates write cycle
P60 $\overline{CS0}$	1	Output Output	Port 60 : Output port Chip Select 0 : Outputs 0 when address is within specified address area
P61 $\overline{CS1}$	1	Output Output	Port 61 : Output port Chip Select 1 : Output 0 when address is within specified address area

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

(*) $\overline{RAS}$, $\overline{CAS}$, and $\overline{REFOUT}$ are set to high impedance only when bus release mode is set using the DRAM controller. For details, see 3.7, Dynamic RAM (DRAM) Controller.

Pin name	Number of pins	I/O	Functions
P62 $\overline{CS2}$	1	Output Output	Port 62 : Output port Chip Select 2 : Outputs 0 if address is within specified address area
P63 $\overline{CS3}$ $\overline{CAS}$	1	Output Output Output	Port 63 : Output port Chip Select 3 : Outputs 0 if address is within specified address area Column address strobe : Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area
P64 $\overline{RAS}$	1	Output Output	Port 64 : Output port Low address strobe : Output $\overline{RAS}$ strobe for DRAM if address is within specified address area
P65 $\overline{REFOUT}$	1	Output Output	Port 65 : Output port Refresh Output : 0 : indicates priod of refresh cycle
P70 to P73 PG00 to PG03	4	I/O Output	Port 70 to 73 : I/O port that allow selection of I/O on a bit basis (with pull-up resister) Pattern generator Port : 00 to 03
P74 to P77 PG10 to PG13	4	I/O Output	Port 74 to 77 : I/O port that allow selection of I/O on a bit basis (with pull-up resister) Pattern generator Port : 10 to 13
P80 TXD0	1	I/O Output	Port 80 : I/O port (with pull-up resister) Serial send data 0
P81 RXD0	1	I/O Input	Port 81 : I/O port (with pull-up resister) Serial receive data 0
P82 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 82 : I/O port (with pull-up resister) Serial data send enable (clear to send) Serial Clock I/O 0
P83 TXD1	1	I/O Output	Port 83 : I/O port (with pull-up resister) Serial send data 1
P84 RXD1	1	I/O Input	Port 84 : I/O port (with pull-up resister) Serial receive data 1
P85 SCLK1	1	I/O I/O	Port 85 : I/O port (with pull-up resister) Serial clock I/O 1
P90 to P93 AN0 to AN3	4	Input Input	Port 9 : Input port Analog input : Input to A/D converter
PA0 $\overline{WAIT}$	1	I/O Input	Port A0 : I/O port (with pull-up resister) Wait : Pin used to request CPU us wait
PA1 TI0	1	I/O Input	Port A1 : I/O port (with pull-up resister) Timer input 0 : Timer 0 input
PA2 TO1	1	I/O Output	Port A2 : I/O port (with pull-up resister) Timer output 1 : Timer 0 or 1 output

Pin name	Number of pins	I/O	Functions
PA3 TO3	1	I/O Output	Port A3 : I/O port (with pull-up resistor) Timer output3 : Timer 2 or 3 output
PB0 TI4 INT4	1	I/O Input Input	Port B0 : I/O port (with pull-up resistor) Timer input 4 : Timer 4 count / capture trigger signal input Interrupt request pin 4 : Interrupt request pin with programmable rising / falling edge
PB1 TI5 INT5	1	I/O Input Input	Port 86 : I/O port (with pull-up resistor) Timer input 5 : Timer 4 count / capture trigger signal input Interrupt request pin 5 : Interrupt request pin with rising edge
PB2 TO4	1	I/O Output	Port B2 : I/O port (with pull-up resistor) Timer output4 : Timer4 output
PB3 TO5	1	I/O Output	Port B3 : I/O port (with pull-up resistor) Timer output5 : Timer4 output
PB4 TI6 INT6	1	I/O Input	Port B4 : I/O port (with pull-up resistor) Timer input 6 : Timer 5 count / capture trigger signal input Interrupt request pin 6 : Interrupt request pin with progmnable rising / fulling edge
PB5 TI7 INT7	1	I/O Input Input	Port B5 : I/O port (with pull-up resistor) Timer input 7 : Timer 5 count / capture trigger signal input Interrupt request pin 7 : Interrupt request pin with rising edge
PB6 TO6	1	I/O Output	Port B6 : I/O port (with pull-up resistor) Timer output6 : Timer5 output pin
PB7 INT0	1	I/O Input	Port B7 : I/O port (with pull-up resistor) Interrupt request pin 0 : Interrupt request pin with progmmable level / rising edge
V_{REF} (V_{REFH})	1	Input	Pin for refereme voltage input to A/D connecter
AGND (V_{REFL})	7	Input	Ground pin for A/D converter
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin : Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output : Outputs「external input clock X1 ÷ 4」clock. Pulled-up during reset.
$\overline{EA}$	1	Input	fixed GND
AM8/$\overline{16}$	1	Input	Address mode : Selects external Data Bus width "0" should be inputted with fixed 16 bit Bus width or 16 bit Bus interlorded with 8 bit Bus. "1" should be inputted with fixed 8 bit Bus width
$\overline{RESET}$	1	Input	Reset : Initializes LSI (with pull-up resister)
X1 / X2	2	I/O	Oscillator connecting pin
VCC	4		Power supply pin (+ 5 V) (All Vcc pins should be connected with the power supply pin.)
VSS	4		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note 1 : Pull-up resistor can be released from the pin by software.
Note 2 : Connect all VCC pins to power supply and all VSS pins to GND.

3. Operation

This section describes in blocks the functions and basic operations of TMP95C061B devices.

Check the 「7. Care Points and Restriction 」because of the Care Points etc are described.

3.1 CPU

TMP95C061B devices has a built-in high-performance 16-bit CPU (900/H CPU). (For CPU operation, see TLCS-900 CPU in the previous section).

This section describes CPU functions unique to TMP95C061B that are not described in the previous section.

3.1.1 Reset

To reset the TMP95C061B, the $\overline{\text{RESET}}$ input must be kept at 0 for at least 10 system clocks (10 states: 0.8 μs at 25 MHz) within an operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program Counter (PC) according to Reset Vector that is stored 0FFFF00H to 0FFFF02H.
  PC (7 : 0) ← stored data to 0FFFF00H
  PC (15 : 8) ← stored data to 0FFFF01H
  PC (23 : 16) ← stored data to 0FFFF02H
- Stack pointer (XSP) for system mode to 100H.
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- Sets the MAX bit of the status register (SR) to 1 (this sets maximum mode).
  (Note : This product does not support minimum mode. Do not use the MIN instruction.)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

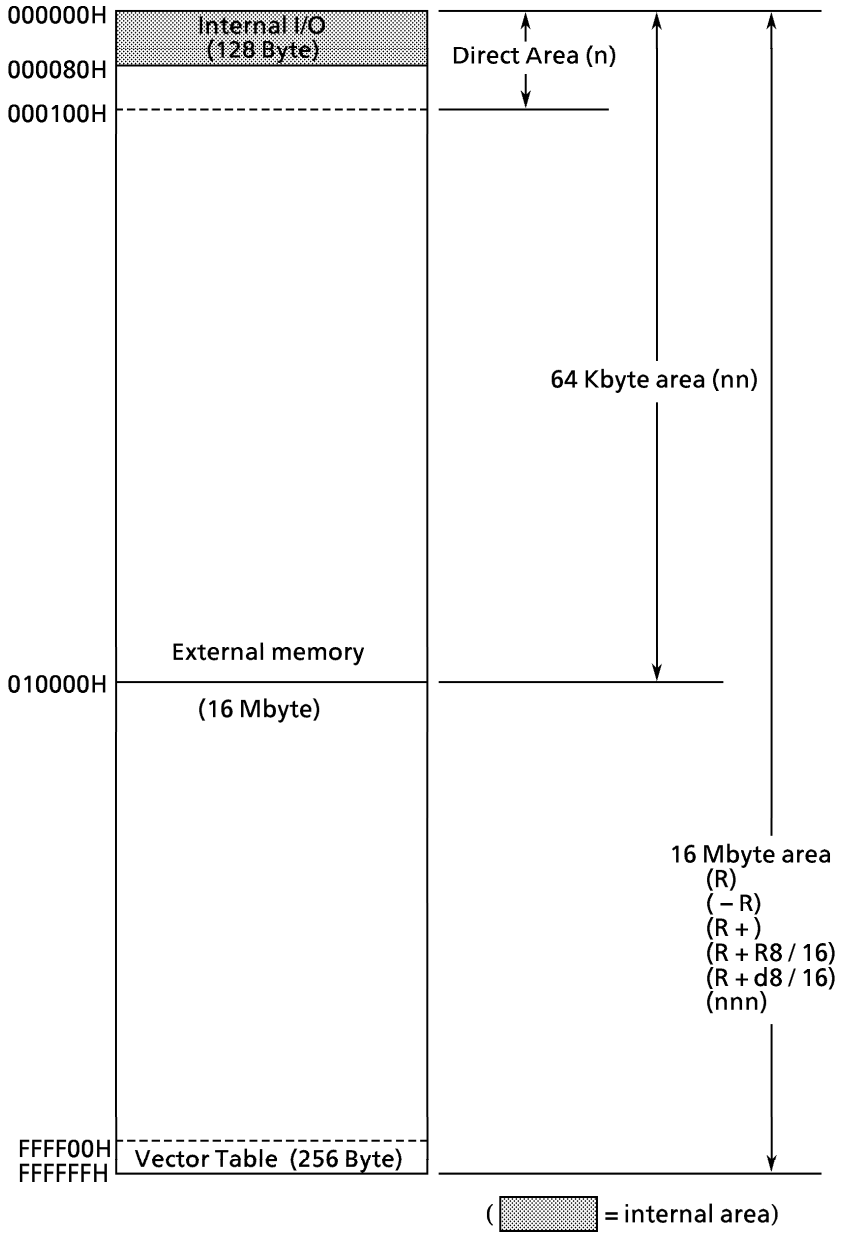
When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input / output port mode.
- Sets the $\overline{\text{WDTOUT}}$ pin to 0. (Watchdog timer is set to enable after reset.)
- Pulls up the CLK pin to 1.

3.2 Memory Map

Figure 3.2 shows a memory map of the TMP95C061B.



Note: After reset operation, Stack point (XSP) is set to 100H.

Figure 3.2 Memory Map

3.2.1 Operation at internal I/O area access

TMP95C061B uses 128 bytes of address space (0H to 7FH) as an internal I/O area. Internal I/O registers are mapped on this area.

Operation of the internal I/O area access is different from that of the other address area access about following two points.

(1) In the internal I/O area access, $\overline{RD}$, and $\overline{WR}$ ($\overline{HWR}$) strobe signals are nonactive and fixed to high level.

However, in PSRAM mode set by P5<RDE>register, $\overline{RD}$ strobe signal becomes active also in the internal I/O area access. (See 3.5.3 Port5 (P52 to P55).)

(2) In the internal I/O area access, the number of waits becomes zero or one depending on the internal state of the CPU. This wait can't be controlled by chip select / wait controller (see 3.6 Chip Select / Wait Controller, AM8/$\overline{16}$ pin). When the specified address area overlaps with the internal I/O area, the operation as the internal I/O area takes priority of the specified address area.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V cc	– 0.5 to 6.5	V
Input Voltage	V IN	– 0.5 to Vcc + 0.5	V
Output Current (total)	Σ IOL	120	mA
Output Current (total)	Σ IOH	– 120	mA
Power Dissipation (Ta = 70°C)	P D	600	mW
Soldering Temperature (10 s)	T SOLDER	260	°C
Storage Temperature	T STG	– 65 to 150	°C
Operation Temperature	T OPR	– 20 to 70	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC characteristics

Vcc = 5 V ± 10%, TA = – 20 to 70°C (8 to 25 MHz)

(Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) P5, P7, P8, P9, PA, PB RESET,NMI,INT0 (PB7) EA, AM8 / 16 X1	V IL V IL1 V IL2 V IL3 V IL4		– 0.3 – 0.3 – 0.3 – 0.3 – 0.3	0.8 0.3Vcc 0.25Vcc 0.3 0.2Vcc	V V V V V
Input High Voltage (D0 to 15) P5, P7, P8, P9, PA, PB RESET, NMI, INT0 (PB7) EA, AM8 / 16 X1	V IH V IH1 V IH2 V IH3 V IH4		2.2 0.7Vcc 0.75Vcc Vcc – 0.3 0.8Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V OL	I OL = 1.6 mA		0.45	V
Output High Voltage	V OH V OH1 V OH2	I OH = – 400 μA I OH = – 100 μA I OH = – 20 μA	2.4 0.75Vcc 0.9Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I DAR	V EXT = 1.5 V R EXT = 1.1 kΩ	– 1.0	– 3.5	mA
Input Leakage Current Output Leakage Current	I LI I LO	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 20 to 70°C) STOP (Ta = 0 to 50°C)	I cc	fc = 25 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	37 (Typ) 3.5 (Typ) 0.5 (Typ)	50 10 50 10	mA mA μA μA
Power Down Voltage (at STOP)	V STOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistance	R RST		50	150	kΩ
Pin Capacitance	C IO	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (PB7)	V TH		0.4	1.0 (Typ)	V
Pull Up Resistance	R K		50	150	kΩ

Note: I_{DAR} is guaranteed for total of up to 8 ports.

4.3 AC Electrical Characteristics

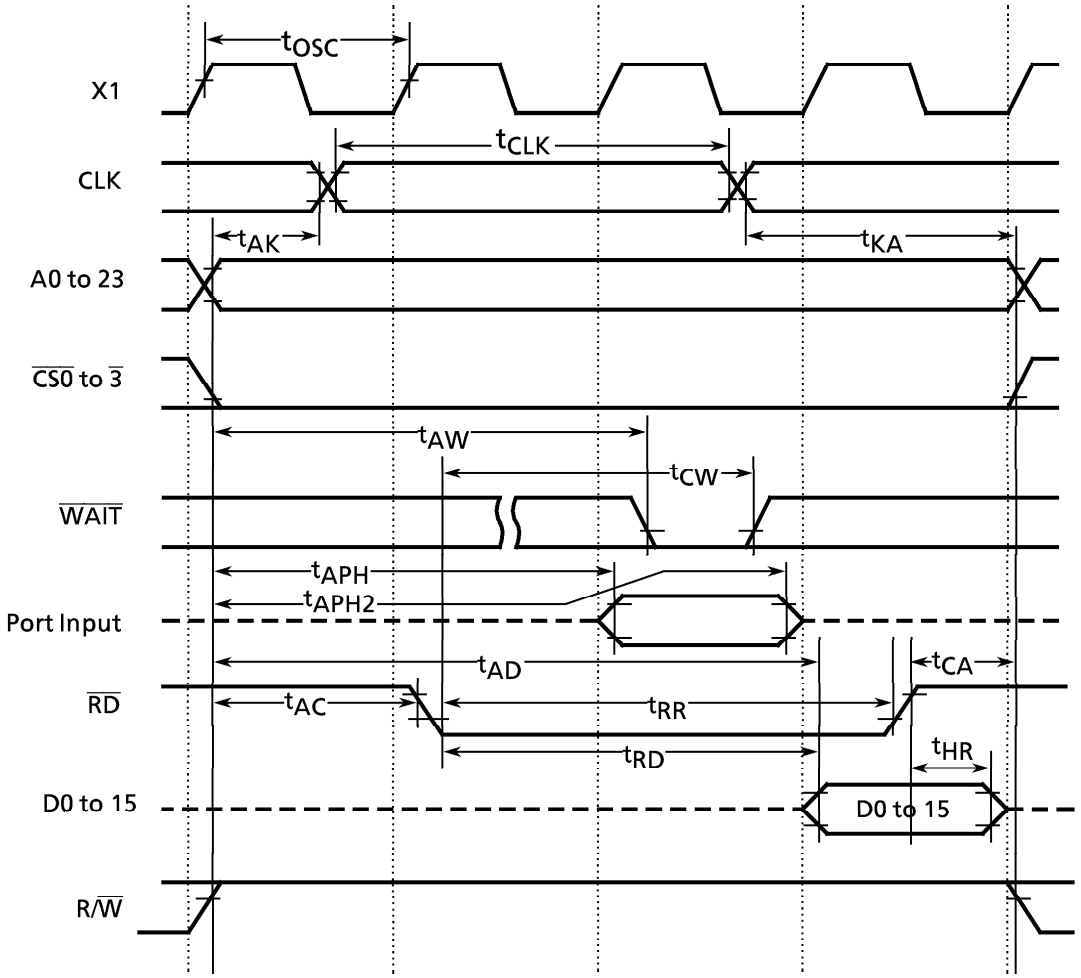
Vcc = 5 V ± 10%, TA = – 20 to 70°C
(8 MHz to 25 MHz)

No.	Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	40	125	50		40		ns
2	CLK width	t_{CLK}	2x – 40		60		40		ns
3	A0 to 23 Valid → CLK Hold	t_{AK}	0.5x – 20		5		0		ns
4	CLK Valid → A0 to 23 Hold	t_{KA}	1.5x – 60		5		0		ns
5	A0 to 23 Valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{AC}	1.0x – 20		30		20		ns
6	$\overline{RD}$ / $\overline{WR}$ rise → A0 to 23 Hold	t_{CA}	0.5x – 20		5		0		ns
7	A0 to 23 Valid → D0 to 15 input	t_{AD}		3.5x – 35		140		105	ns
8	$\overline{RD}$fall → D0 to 15 input	t_{RD}		2.5x – 40		85		60	ns
9	$\overline{RD}$ Low width	t_{RR}	2.5x – 40		85		60		ns
10	$\overline{RD}$rise → D0 to 15 Hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ Low width	t_{WW}	2.5x – 40		85		60		ns
12	D0 to 15 Valid → $\overline{WR}$rise	t_{DW}	2.0x – 40		60		40		ns
13	$\overline{WR}$ rise → D0 to 15 Hold	t_{WD}	0.5x – 10		15		10		ns
14	A0 to 23 Valid → $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AW}		3.5x – 90		85		50	ns
15	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ Hold (1 WAIT + n mode)	t_{CW}	2.5x + 0		125		100		ns
16	A0 to 23 Valid → PORT input	t_{APH}		2.5x – 90		35		10	ns
17	A0 to 23 Valid → PORT Hold	t_{APH2}	2.5x + 50		175		150		ns
18	$\overline{WR}$ rise → PORT Valid	t_{CP}		200		200		200	ns

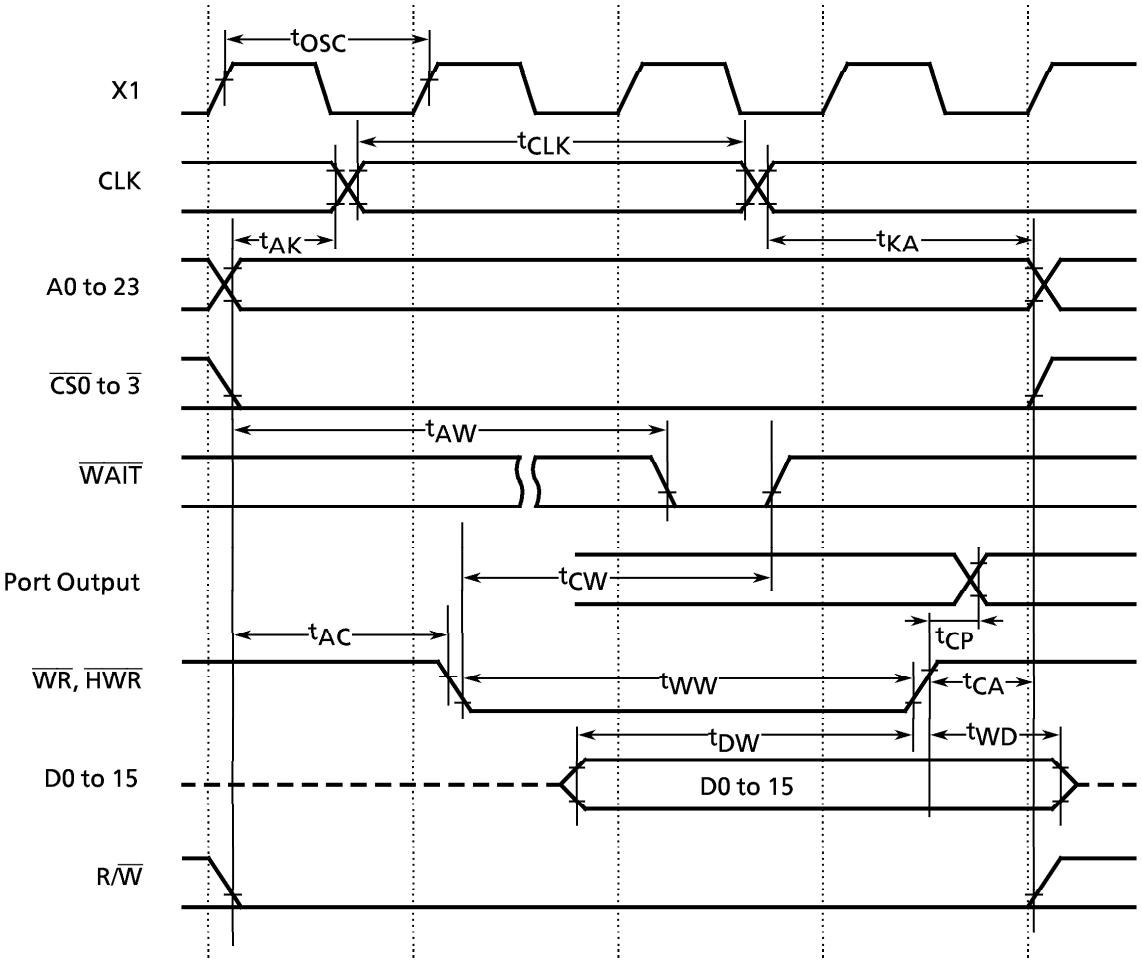
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However, D0 to D15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK, $\overline{CS0}$ to $\overline{CS3}$, CL = 100 pF)
- Input Level : High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 Vcc / Low 0.2 Vcc (exsept for D0 to D15)

(1) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to 3
tAW
tCW
WAIT
tAPH
tAPH2
Port Input
tAD
tCA
RD
tAC
tRR
tRD
tHR
D0 to 15
D0 to 15
R/W

(2) Write Cycle



4.4 DRAM Controller AC Electrical Characteristics

Vcc = 5 V ± 10%, TA = – 20 to 70°C
(8 MHz to 25 MHz)

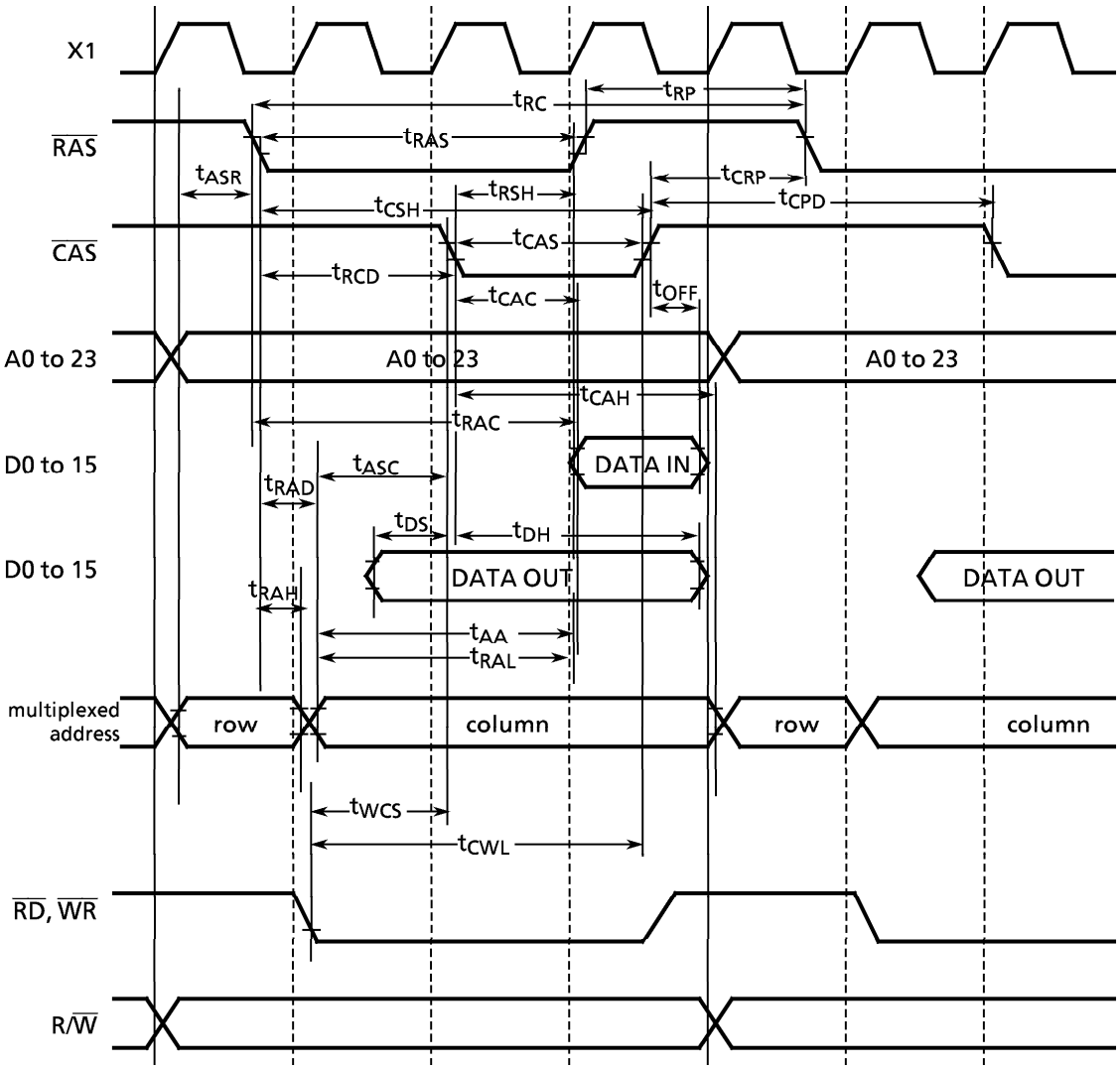
No.	Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	$\overline{RAS}$ cycle time	t_{RC}	4X		200		160		ns
2	$\overline{RAS}$ access time	t_{RAC}		3X-40		110		80	ns
3	$\overline{CAS}$ access time	t_{CAC}		1.5X-35		40		25	ns
4	column address access time	t_{AA}		2.5X-55		70		45	ns
5	Input data hold time	t_{OFF}	0		0		0		ns
6	$\overline{RAS}$ precharge time	t_{RP}	1.5X-10		65		50		ns
7	$\overline{RAS}$ low pulse width	t_{RAS}	2.5X-30		95		70		ns
8	$\overline{RAS}$ hold time	t_{RSH}	1X-15		35		25		ns
9	$\overline{CAS}$ hold time	t_{CSH}	3X-35		115		85		ns
10	$\overline{CAS}$ low pulse width	t_{CAS}	1.5X-15		65		45		ns
11	$\overline{RAS}$ – $\overline{CAS}$ delay time	t_{RCD}	1.5X-40	1.5X	35	75	20	60	ns
12	$\overline{RAS}$ column address delay time	t_{RAD}	0.5X-5	0.5X + 20	20	45	15	40	ns
13	$\overline{CAS}$ – $\overline{RAS}$ precharge time	t_{CRP}	1X-35		15		5		ns
14	$\overline{CAS}$ precharge time	t_{CPD}	2.5X-35		90		65		ns
15	Low address setup time	t_{ASR}	0.5X-15		10		5		ns
16	Low address hold time	t_{RAH}	0.5X-5		20		15		ns
17	Column address setup time	t_{ASC}	1X-25		25		15		ns
18	Column address hold time	t_{CAH}	2X-35		65		45		ns
19	Column address $\overline{RAS}$ read time	t_{RAL}	2X-30		70		50		ns
20	Write command $\overline{CAS}$ read time	t_{CWL}	2.5X-35		90		65		ns
21	Data output setup time	t_{DS}	0.5X-15		10		5		ns
22	Data output hold time	t_{DH}	2X-35		65		45		ns
23	Write command setup time	t_{WCS}	1X-30		20		10		ns
24	$\overline{CAS}$ hold time	t_{CHR}*1	2X-50		50		30		ns
25	$\overline{RAS}$ precharge $\overline{CAS}$ active time	t_{RPC}*	1.5X-30		45		30		ns
26	$\overline{CAS}$ setup time	t_{CSR}*	0.5X-10		15		10		ns
27	$\overline{RAS}$ precharge time	t_{RPS}*2	4X-20		180		140		ns
28	$\overline{CAS}$ hold time	t_{CHS}*2	0		0		0		ns
29	refresh setup time	t_{CFL}*	1X-5		45		35		ns
30	refresh hold time	t_{CFH}*	1X-10		40		30		ns

*1 $\overline{CAS}$ before $\overline{RAS}$ interval refresh mode
*2 $\overline{CAS}$ before $\overline{RAS}$ self-refresh mode
* Both refresh modes

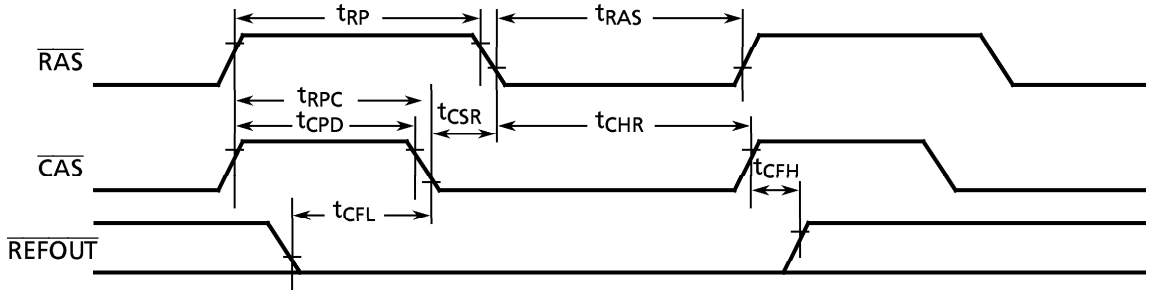
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However CL = 100pF for D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$)
- Input Level : High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 Vcc / Low 0.2 Vcc (Except for D0 to D15)

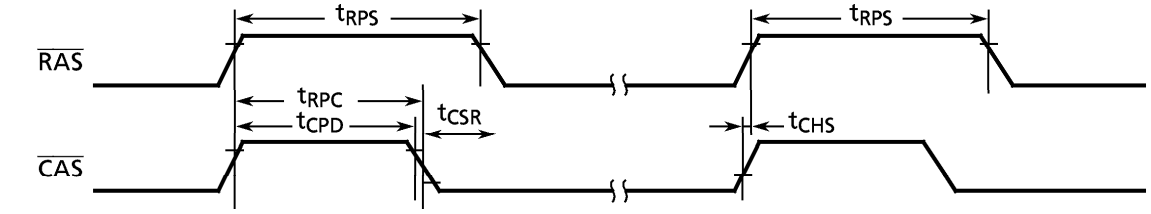
(1) Read/Write Access Cycle



(2) $\overline{CAS}$ before $\overline{RAS}$ interval refresh cycle



(3) $\overline{CAS}$ bifore $\overline{RAS}$ self-refresh cycle



4.5 A/D Conversion Characteristics

Vcc = 5V ± 10%, TA = – 20 to 70°C (8 to 25 MHz)

Parameter		Symbol	Min	Typ.	Max	Unit
Analog reference voltage		V_{REF} (V_{REFH})	Vcc – 1.5		Vcc	V
Analog reference voltage		A_{GND} (V_{REFL})	Vss		Vss	
Analog input voltage range		V_{AIN}	Vss		Vcc	
Anlog current for analog reference voltage		I_{REF}		0.5	1.5	mA
4 ≦ fc ≦ 16 MHz	slow mode	Error (Quantize error of ± 0.5 LSB not included)		± 1.5	± 4.0	LSB
	fast mode			± 3.0	± 6.0	
16 < fc ≦ 25 MHz	slow mode			± 1.5	± 4.0	
	fast mode			± 4.0	± 8.0	

4.6 Serial Channel Timing

(1) SCLK Input Mode (I/O Interface Mode)

Vcc = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16X		0.8		0.64		μs
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 − 5X − 50		100		70		ns
SCLK rising edge→ Output Data hold	t_{OHS}	5X − 100		150		100		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 5X − 100		450		340	ns

(2) SCLK Output Mode (I/O Interface Mode)

Vcc = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16X	8192X	0.8	409.6	0.64	327.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} − 2X − 150		550		410		ns
SCLK rising edge→ Output Data hold	t_{OHS}	2X − 80		20		0		ns
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} − 2X − 150		550		410	ns

(3) SCLK0 Input Mode (UART Mode)

Vcc = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4X + 20		220		180		ns
SCLK Low level Pulse width	t_{SCYL}	2X + 5		105		85		ns
SCLK High level Pulse width	t_{SCYH}	2X + 5		105		85		ns

4.7 Timer / Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Vcc = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

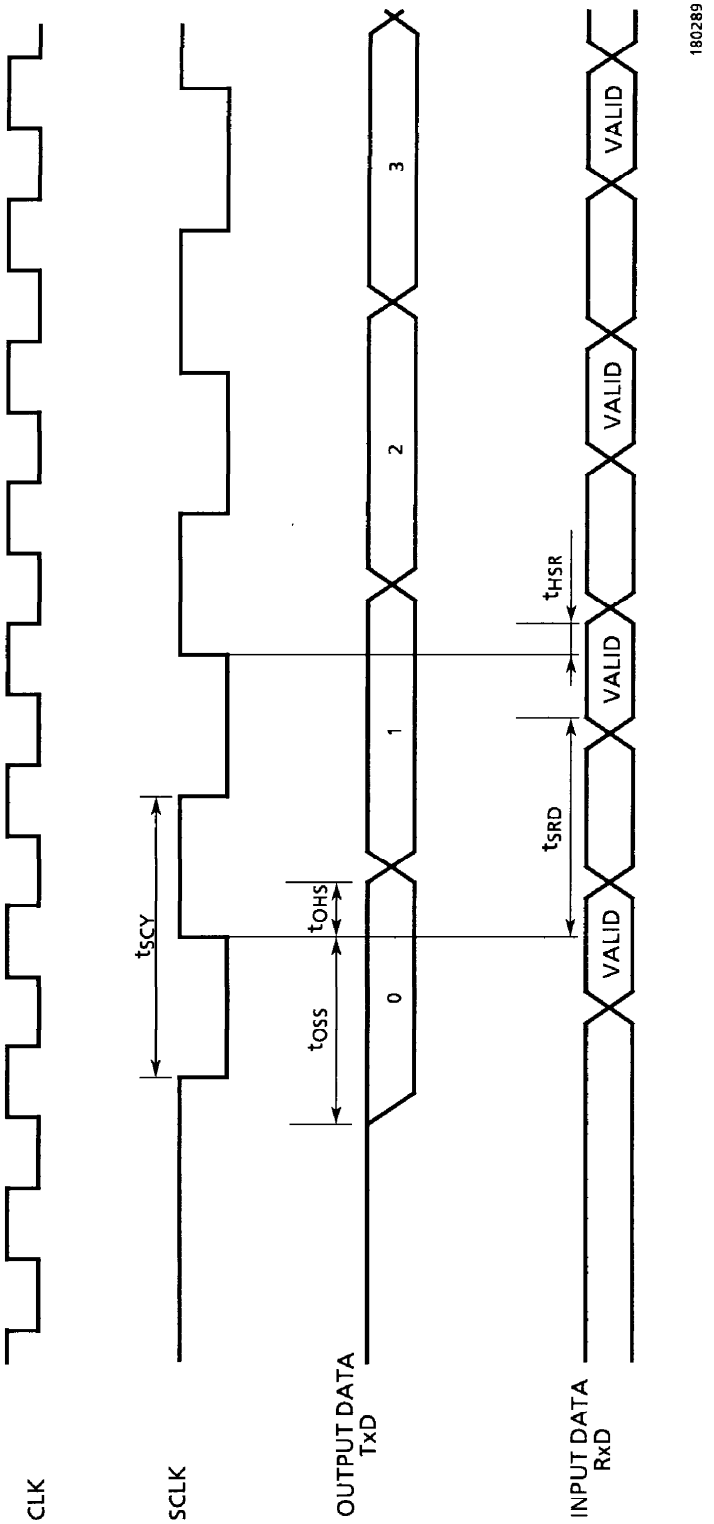
Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		500		420		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		240		200		ns
High level clock Pulse width	t_{VCKH}	4X + 40		240		200		ns

4.8 Interrupt Operation

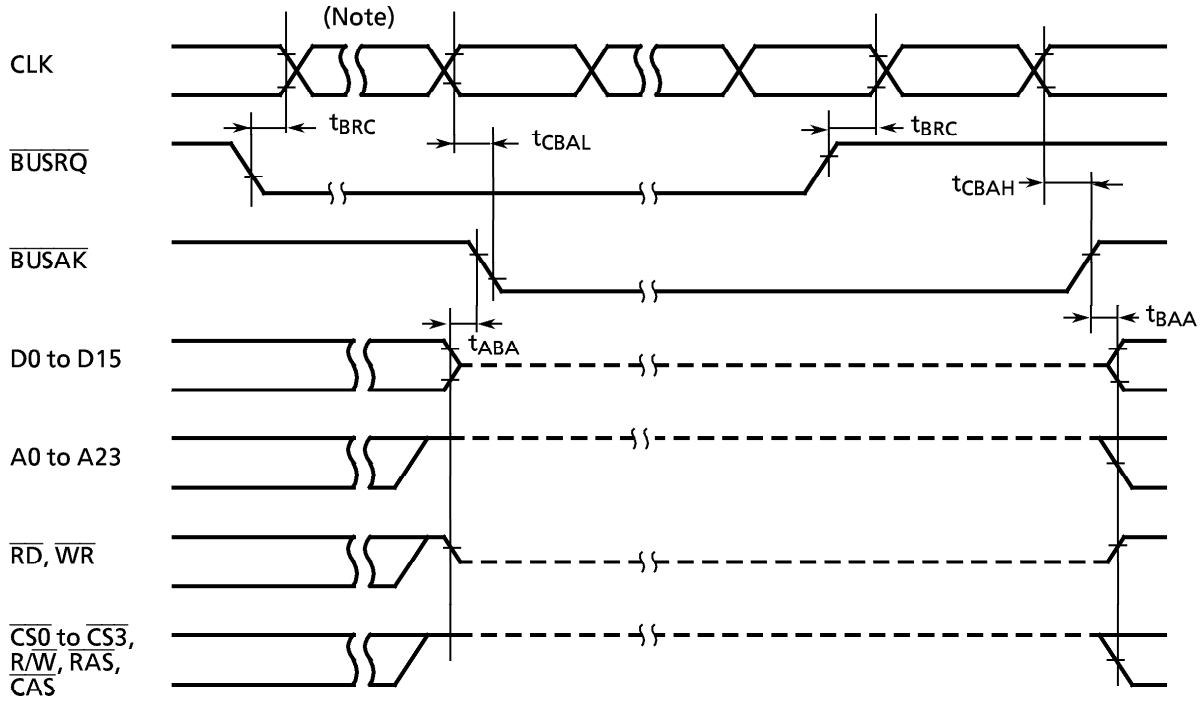
Vcc = 5 V ± 10%, TA = − 20 to 70°C (8 to 25 MHz)

Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level Pulse width	t_{INTAL}	4X		200		160		ns
$\overline{NMI}$, INT0 High level Pulse width	t_{INTAH}	4X		200		160		ns
INT4 to INT7 Low level Pulse width	t_{INTBL}	8X + 100		500		420		ns
INT4 to INT7 High level Pulse width	t_{INTBH}	8X + 100		500		420		ns

4.9 Timing Chart for I/O Interface Mode



4.10 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSQR}$ set-up time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ falling edge	t_{CBAL}		2.0x + 120		220		200	ns
CLK→ $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5x + 40		65		60	ns
Floating time to $\overline{BUSAK}$ fall	t_{ABA}	0	80	0	80	0	80	ns
Floating time to $\overline{BUSAK}$ rise	t_{BAA}	0	80	0	80	0	80	ns

Note : The bus will be released after the WAIT request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "wait" cycle.

4.11 Typical Characteristics

V_{CC} = 5V, Ta = 25°C, unless otherwise noted.

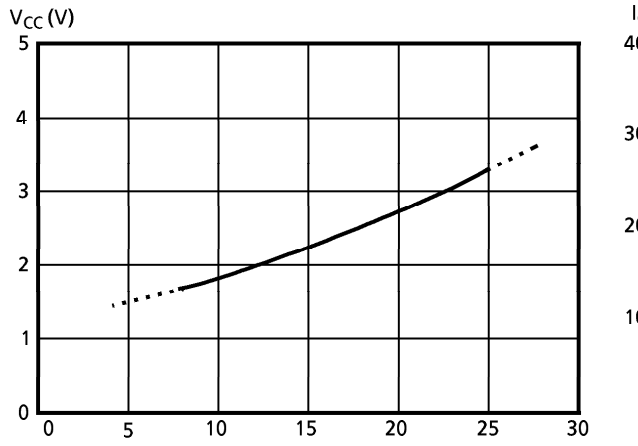


Figure 4.1 V_{CC} – f_{OSC} TYPICAL CURVE

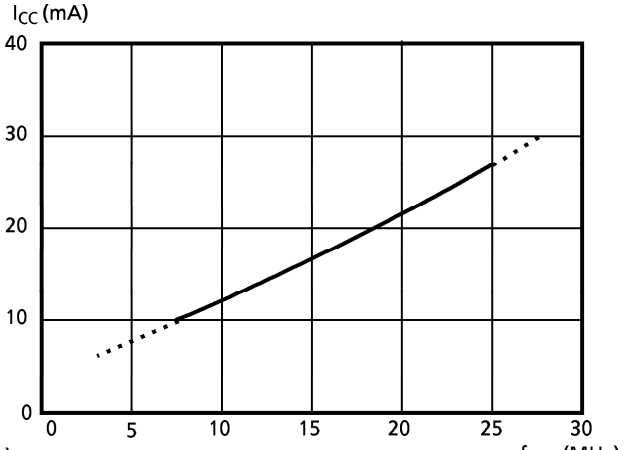


Figure 4.2 I_{CC} – f_{OSC} TYPICAL CURVE

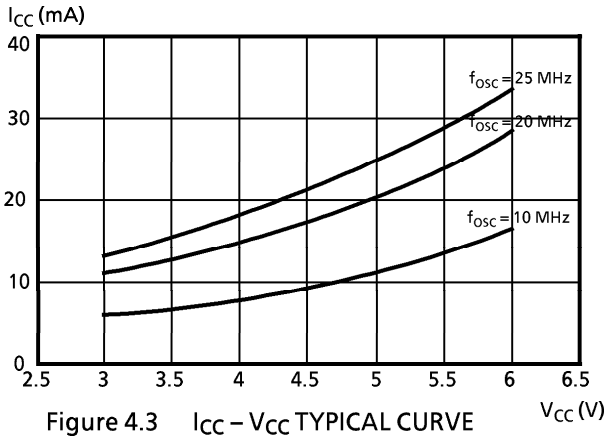


Figure 4.3 I_{CC} – V_{CC} TYPICAL CURVE

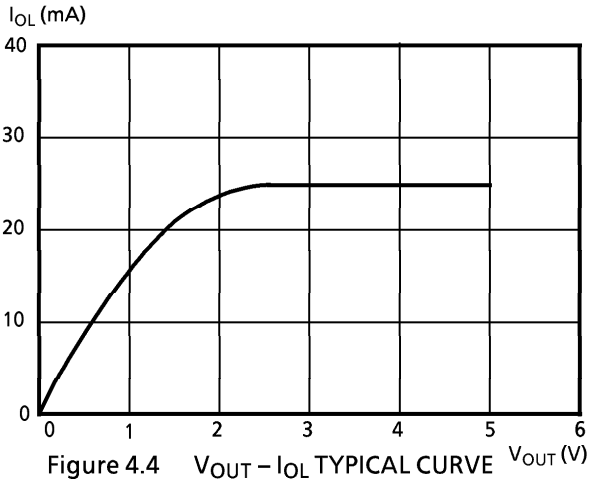


Figure 4.4 V_{OUT} – I_{OL} TYPICAL CURVE

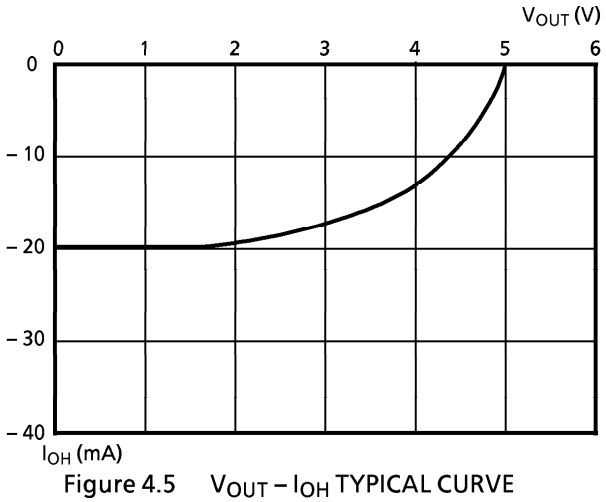


Figure 4.5 V_{OUT} – I_{OH} TYPICAL CURVE