NEC

Preliminary User's Manual

V850ES/KG2

32-Bit Single-Chip Microcontrollers

Hardware

μPD70F3731
μPD70F3732

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[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Ordering information
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PREFACE

Readers This manual is intended for users who wish to understand the functions of the V850ES/KG2 and design application systems using the V850ES/KG2.

Purpose This manual is intended to give users an understanding of the hardware functions of the V850ES/KG2 shown in the **Organization** below.

Organization This manual is divided into two parts: Hardware (this manual) and Architecture (**V850ES Architecture User's Manual**).

Hardware	Architecture
• Pin functions	• Data types
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications (target)	• Pipeline operation

How to Read This Manual It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To find the details of a register where the name is known
→ Refer to **APPENDIX B REGISTER INDEX**.

To understand the details of an instruction function
→ Refer to the **V850ES Architecture User's Manual**.

Register format
→ The name of the bit whose number is in angle brackets (<>) in the figure of the register format of each register is defined as a reserved word in the device file.

To understand the overall functions of the V850ES/KG2
→ Read this manual according to the **CONTENTS**.

To know the electrical specifications of the V850ES/KG2
→ Refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS (TARGET)**.

The "yyy bit of the xxx register" is described as the "xxx.yyy bit" in this manual. Note with caution that even if "xxx.yyy" is described as is in a program, however, the compiler/assembler cannot recognize it correctly.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: $\overline{xxx}$ (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on the bottom

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numeric representation: Binary ... xxxx or xxxxB
Decimal ... xxxx
Hexadecimal ... xxxxH

Prefix indicating power of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1,024$
M (mega): $2^{20} = 1,024^2$
G (giga): $2^{30} = 1,024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/KG2

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/KG2 Hardware User's Manual	This manual

Documents related to development tools (user's manuals)

Document Name		Document No.
CA850 Ver. 3.00 C Compiler Package	Operation	U17293E
	C Language	U17291E
	Assembly Language	U17292E
	Link Directives	U17294E
PM+ Ver. 6.00 Project Manager		U17178E
ID850QB Ver. 3.10 Integrated Debugger	Operation	U17435E
SM850 Ver. 2.50 System Simulator	Operation	U16218E
SM850 Ver. 2.00 or Later System Simulator	External Part User Open Interface Specification	U14873E
RX850 Ver. 3.20 or Later Real-Time OS	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro Ver. 3.20 Real-Time OS	Basics	U13773E
	Installation	U17421E
	Technical	U13772E
	Task Debugger	U17422E
AZ850 Ver. 3.30 System Performance Analyzer		U17423E
PG-FP4 Flash Memory Programmer		U15260E

CONTENTS

CHAPTER 1 INTRODUCTION

1.1 V850ES/Kx2 Product Lineup

Product Name		V850ES/KE2	V850ES/KF2		V850ES/KG2		V850ES/KJ2	
Number of pins		64 pins	80 pins		100 pins		144 pins	
Internal memory (KB)	Flash memory	128	128	256	128	256	128	256
	RAM	4	6	12	6	16	6	16
Supply voltage		2.7 to 5.5 V						
Minimum instruction execution time		50 ns @20 MHz						
Clock	X1 input	2 to 10 MHz						
	Subclock	32.768 kHz						
Port	CMOS input	8	8		8		16	
	CMOS I/O	41 (4)[Note]	57 (6)[Note]		72 (8)[Note]		106 (12)[Note]	
	N-ch open-drain I/O	2	2		4		6	
Timer	16-bit (TMP)	1 ch	1 ch		1 ch		1 ch	
	16-bit (TM0)	1 ch	2 ch		4 ch		6 ch	
	8-bit (TM5)	2 ch	2 ch		2 ch		2 ch	
	8-bit (TMH)	2 ch	2 ch		2 ch		2 ch	
	Interval timer	1 ch	1 ch		1 ch		1 ch	
	Watch	1 ch	1 ch		1 ch		1 ch	
	WDT1	1 ch	1 ch		1 ch		1 ch	
	WDT2	1 ch	1 ch		1 ch		1 ch	
RTO		6 bits × 1 ch	6 bits × 1 ch		6 bits × 1 ch		6 bits × 2 ch	
Serial interface	CSI	2 ch	2 ch		2 ch		3 ch	
	Automatic transmit/ receive 3-wire CSI	–	1 ch		2 ch		2 ch	
	UART	2 ch	2 ch		3 ch		3 ch	
	I^2C	1 ch	1 ch		1 ch		2 ch	
External bus	Address space	–	128 KB		3 MB		15 MB	
	Address bus	–	16 bits		22 bits		24 bits	
	Mode	–	Multiplex only		Multiplex/separate			
DMA controller		–	–		4 ch		4 ch	
10-bit A/D converter		8 ch	8 ch		8 ch		16 ch	
8-bit D/A converter		–	–		2 ch		2 ch	
Interrupt	External	9	9		9		9	
	Internal	26	29		41		47	
Key return input		8 ch	8 ch		8 ch		8 ch	
Reset	$\overline{\text{RESET}}$ pin	Provided						
	WDT1	Provided						
	WDT2	Provided						
Regulator		None	Provided					
Standby function		HALT/IDLE/STOP/sub-IDLE mode						
Operating ambient temperature		TA = −40 to +85°C						

Note Figures in parentheses indicate the number of pins for which the N-ch open-drain output can be selected.

1.2 Features

- Minimum instruction execution time: 50 ns (operation at main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32 registers
- CPU features: Signed multiplication (16 × 16 → 32): 1 to 2 clocks
  (Instructions without creating register hazards can be continuously executed in parallel)
  Saturated operations (overflow and underflow detection functions are included)
  32-bit shift instruction: 1 clock
  Bit manipulation instructions
  Load/store instructions with long/short format
- Memory space: 64 MB of linear address space
  Memory block division function: 2 MB, 2 MB (Total of 2 blocks)
  - Internal memory
    μPD70F3732 (flash memory: 256 KB/RAM: 16 KB)
    μPD70F3731 (flash memory: 128 KB/RAM: 6 KB)
  - External bus interface
    Separate bus/multiplex bus output selectable
    8-/16-bit data bus sizing function
    Wait function
    - Programmable wait function
    - External wait function

    Idle state function
    Bus hold function
- Interrupts and exceptions
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 47 sources
  Software exceptions: 32 sources
  Exception trap: 1 source
- I/O lines: Total: 84
- Key interrupt function
- Timer function
  16-bit timer/event counter P: 1 channel
  16-bit timer/event counter 0: 4 channels
  8-bit timer/event counter 5: 2 channels
  8-bit timer H: 2 channels
  8-bit interval timer BRG: 1 channel
  Watch timer/interval timer: 1 channel
  Watchdog timers
  Watchdog timer 1 (also usable as oscillation stabilization timer): 1 channel
  Watchdog timer 2: 1 channel

- Serial interface

Asynchronous serial interface (UART):	3 channels
3-wire serial I/O (CSI0):	2 channels
3-wire serial I/O (with automatic transmit/receive function) (CSIA):	2 channels
I^2C bus interface (I^2C):	1 channel

- A/D converter: 10-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- DMA controller: 4 channels
- Real-time output port: 6 bits × 1 channel
- Standby functions: HALT/IDLE/STOP modes, subclock/sub-IDLE modes
- Clock generator

  Main clock oscillation (f_X)/subclock oscillation (f_{XT})
  CPU clock (f_{CPU}) 7 steps (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, f_{XT})
  Clock-through mode/PLL mode selectable

- Reset
  - Reset by $\overline{\text{RESET}}$ pin
  - Reset by overflow of watchdog timer 1 (WDTRES1)
  - Reset by overflow of watchdog timer 2 (WDTRES2)

- Package: 100-pin plastic LQFP (fine pitch) (14 × 14)
  100-pin plastic QFP (14 × 20)

1.3 Applications

- Home audio, car audio
- AV equipment
- PC peripheral devices (keyboards, etc.)
- Household appliances
  - Outdoor units of air conditioners
  - Microwave ovens, rice cookers
- Industrial devices
  - Pumps
  - Vending machines
  - FA

1.4 Ordering Information

Part Number	Package
μPD70F3731GC-8EA-A	100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3732GC-8EA-A	100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3731GF-JBT-A	100-pin plastic QFP (14 × 20)
μPD70F3732GF-JBT-A	100-pin plastic QFP (14 × 20)

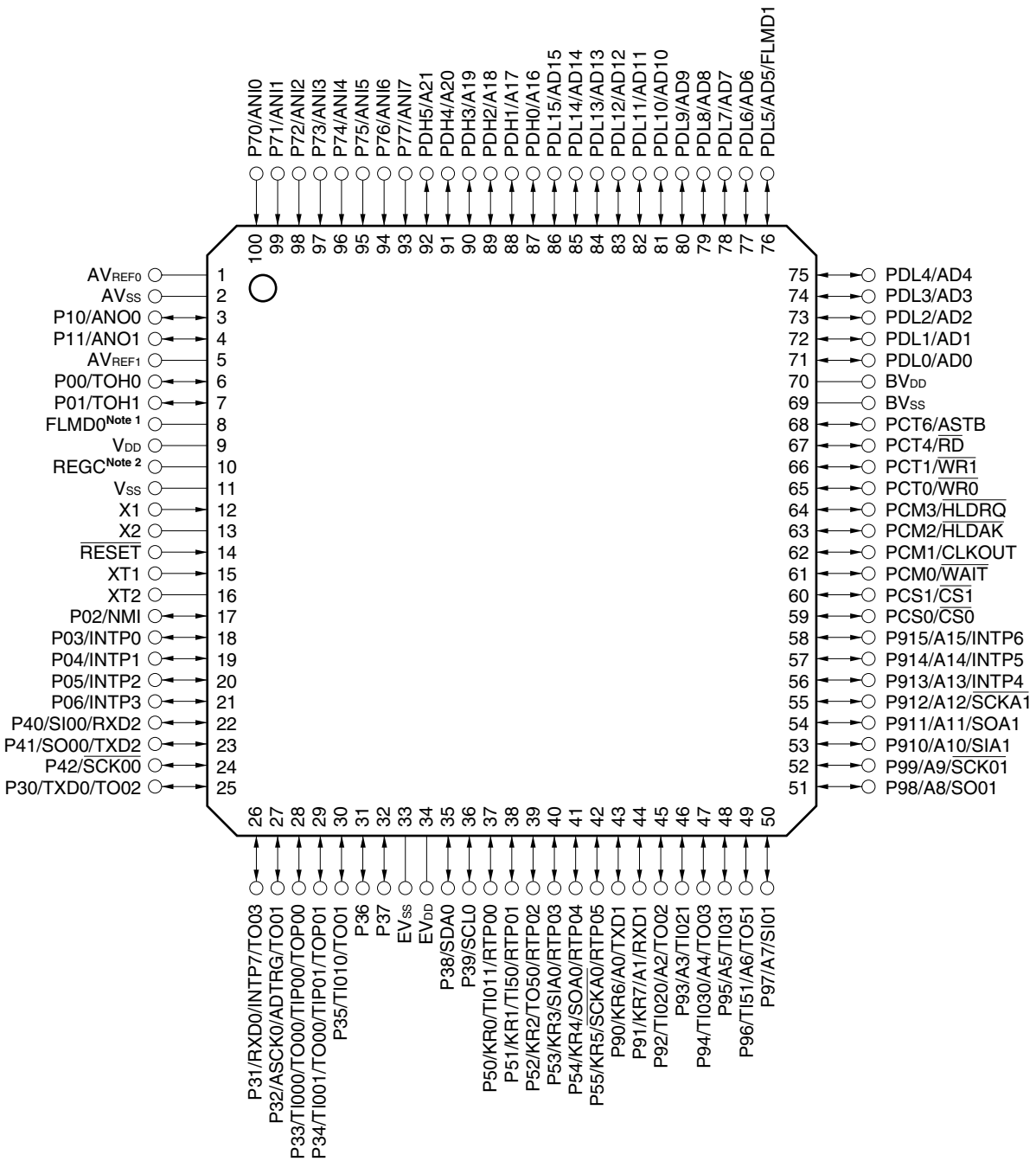
Remark Products with -A at the end of the part number are lead-free products.

1.5 Pin Configuration (Top View)

100-pin plastic LQFP (fine pitch) (14 × 14)

μPD70F3731GC-8EA-A

μPD70F3732GC-8EA-A



Notes 1. Connect to V_{SS} in normal operation mode.

2. When using a regulator, connect the REGC pin to V_{SS} via a 10 μF capacitor. When not using a regulator, connect the REGC pin directly to V_{DD}.

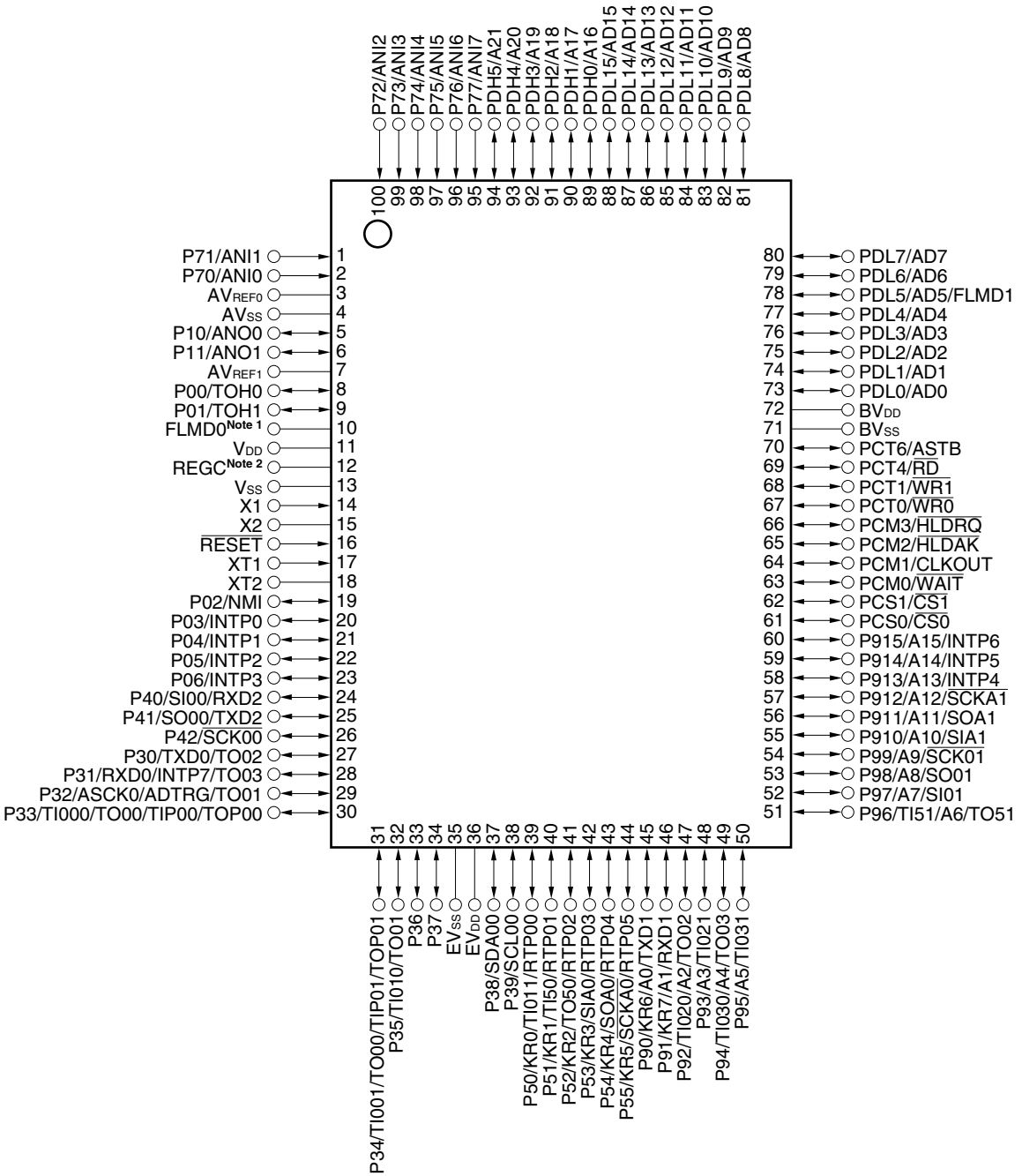
Caution Make EV_{DD} the same potential as V_{DD}.

BV_{DD} can be used when $V_{DD} = EV_{DD} \geq BV_{DD}$.

100-pin plastic QFP (14 × 20)

μPD70F3731GF-JBT-A

μPD70F3732GF-JBT-A



Notes 1. Connect to VSS in normal operation mode.

2. When using a regulator, connect the REGC pin to VSS via a 10 μF capacitor. When not using a regulator, connect the REGC pin directly to VDD.

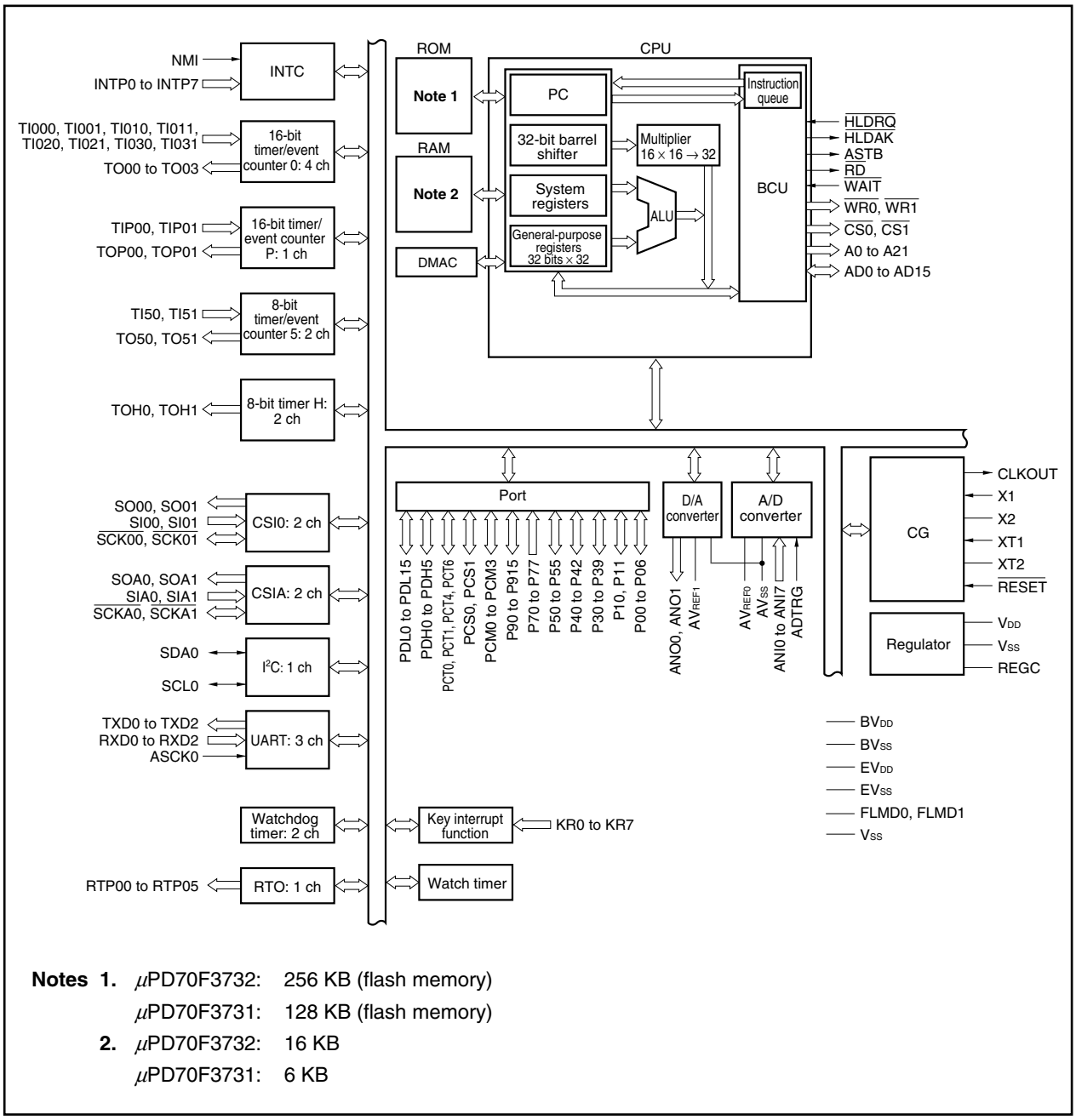
Caution Make EVDD the same potential as VDD.
BVDD can be used when VDD = EVDD ≥ BVDD.

Pin identification

A0 to A21:	Address bus	PDL0 to PDL15:	Port DL
AD0 to AD15:	Address/data bus	$\overline{RD}$:	Read strobe
ADTRG:	A/D trigger input	REGC:	Regulator control
ANI0 to ANI7:	Analog input	$\overline{RESET}$:	Reset
ANO0, ANO1:	Analog output	RTP00 to RTP05:	Real-time output port
ASCK0:	Asynchronous serial clock	RXD0 to RXD2:	Receive data
ASTB:	Address strobe	$\overline{SCK00}$, $\overline{SCK01}$,	
AV_{REF0}, AV_{REF1}:	Analog reference voltage	$\overline{SCKA0}$, $\overline{SCKA1}$:	Serial clock
AV_{SS}:	Ground for analog	SCL0:	Serial clock
BV_{DD}:	Power supply for bus interface	SDA0:	Serial data
BV_{SS}:	Ground for bus interface	SI00, SI01,	
CLKOUT:	Clock output	SIA0, SIA1:	Serial input
$\overline{CS0}$, $\overline{CS1}$:	Chip select	SO00, SO01,	
EV_{DD}:	Power supply for port	SOA0, SOA1:	Serial output
EV_{SS}:	Ground for port	TI000, TI001,	
FLMD0, FLMD1	Flash programming mode	TI010, TI011,	
$\overline{HLDAK}$:	Hold acknowledge	TI020, TI021,	
$\overline{HLDRQ}$:	Hold request	TI030, TI031,	
INTP0 to INTP7:	External interrupt input	TI50, TI51,	
KR0 to KR7:	Key return	TIP00, TIP01:	Timer input
NMI:	Non-maskable interrupt request	TO00 to TO03,	
P00 to P06:	Port 0	TO50, TO51,	
P10, P11:	Port 1	TOH0, TOH1,	
P30 to P39:	Port 3	TOP00, TOP01:	Timer output
P40 to P42:	Port 4	TXD0 to TXD2:	Transmit data
P50 to P55:	Port 5	V_{DD}:	Power supply
P70 to P77:	Port 7	V_{SS}:	Ground
P90 to P915:	Port 9	$\overline{WAIT}$:	Wait
PCM0 to PCM3:	Port CM	$\overline{WR0}$:	Lower byte write strobe
PCS0, PCS1:	Port CS	$\overline{WR1}$:	Upper byte write strobe
PCT0, PCT1		X1, X2:	Crystal for main clock
PCT4, PCT6:	Port CT	XT1, XT2:	Crystal for subclock
PDH0 to PDH5:	Port DH		

1.6 Function Block Configuration

(1) Internal block diagram



Notes 1. μPD70F3732: 256 KB (flash memory)
μPD70F3731: 128 KB (flash memory)
2. μPD70F3732: 16 KB
μPD70F3731: 6 KB

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other types of instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU.

When an instruction is fetched from external memory area and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an internal instruction queue.

(c) ROM

This consists of a 256 KB or 128 KB flash memory mapped to the address spaces from 0000000H to 003FFFFH or 0000000H to 001FFFFH, respectively.

ROM can be accessed by the CPU in one clock cycle during instruction fetch.

(d) RAM

This consists of a 16 KB or 6 KB RAM mapped to the address spaces from 3FFB000H to 3FFEFFFH or 3FFD800H to 3FFEFFFH.

RAM can be accessed by the CPU in one clock cycle during data access.

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP7) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed.

(f) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively.

There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 4.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(g) Timer/counter

Four 16-bit timer/event counter 0 channels, one 16-bit timer/event counter P channel, and two 8-bit timer/event counter 5 channels are incorporated, enabling measurement of pulse intervals and frequency as well as programmable pulse output.

Two 8-bit timer/event counter 5 channels can be connected in cascade to configure a 16-bit timer.

Two 8-bit timer H channels enabling programmable pulse output are provided on chip.

(h) Watch timer

This timer counts the reference time (0.5 seconds) for counting the clock from the subclock (32.768 kHz) or f_{BRG} (32.768 kHz) from the clock generator. At the same time, the watch timer can be used as an interval timer.

(i) Watchdog timer

Two watchdog timer channels are provided on chip to detect program loops and system abnormalities. Watchdog timer 1 can be used as an interval timer. When used as a watchdog timer, it generates a non-maskable interrupt request signal (INTWDT1) or system reset signal (WDTRES1) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request signal (INTWDTM1) after an overflow occurs.

Watchdog timer 2 operates by default following reset release.

It generates a non-maskable interrupt request signal (INTWDT2) or system reset signal (WDTRES2) after an overflow occurs.

(j) Serial interface (SIO)

The V850ES/KG2 includes four kinds of serial interfaces: an asynchronous serial interface (UARTn), a clocked serial interface (CSI0m), a clocked serial interface with an automatic transmit/receive function (CSIAm), and an I^2C bus interface (I^2C0), and can simultaneously use up to seven channels.

For UARTn, data is transferred via the TXDn and RXDn pins.

For CSI0m, data is transferred via the SO0m, SI0m, and $\overline{SCK0m}$ pins.

For CSIAm, data is transferred via the SOAm, SIAm, and $\overline{SCKAm}$ pins.

For I^2C0, data is transferred via the SDA0 and SCL0 pins.

Remark n = 0 to 2
m = 0, 1

(k) A/D converter

This high-speed, high-resolution 10-bit A/D converter includes 8 analog input pins. Conversion is performed using the successive approximation method.

(l) D/A converter

Two 8-bit resolution D/A converter channels are included on chip. The D/A converter uses the R-2R ladder method.

(m) DMA controller

A 4-channel DMA controller is provided on chip. This controller transfers data between the internal RAM, on-chip peripheral I/O devices, and external memory in response to interrupt requests sent by on-chip peripheral I/O.

(n) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins.

(o) Real-time output function

This function transfers 6-bit data set beforehand to output latches upon occurrence of a timer compare register match signal.

A 1-channel 6-bit data real-time output function is provided on chip.

(p) Ports

As shown below, the following ports have general-purpose port functions and control pin functions.

Port	I/O	Alternate Function
P0	7-bit I/O	NMI, external interrupt, timer output
P1	2-bit I/O	D/A converter analog output
P3	10-bit I/O	Serial interface, timer I/O, external interrupt, A/D converter trigger
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Serial interface, timer I/O, key interrupt function, real-time output function
P7	8-bit input	A/D converter analog input
P9	16-bit I/O	External address bus, serial interface, timer I/O, external interrupt, key interrupt function
PCM	4-bit I/O	External bus control signal
PCS	2-bit I/O	Chip select output
PCT	4-bit I/O	External bus control signal
PDH	6-bit I/O	External address bus
PDL	16-bit I/O	External address/data bus

1.7 Overview of Functions

Part Number		μPD70F3732	μPD70F3731
Internal memory	ROM	256 KB (single-power flash memory)	128 KB (single-power flash memory)
	High-speed RAM	16 KB	6 KB
Buffer RAM		64 bytes	
Memory space	Logical space	64 MB	
	External memory area	3 MB	
External bus interface		Address bus: 22 bits Data bus: 8/16 bits Multiplex bus mode/separate bus mode	
General-purpose registers		32 bits × 32 registers	
Main clock (oscillation frequency)		Ceramic/crystal/external clock	
		When PLL not used: 2 to 10 MHz (2.7 to 5.5 V)	
	When PLL used	REGC pin connected directly to V_{DD}: 2 to 5 MHz (4.5 to 5.5 V), 2 MHz (2.7 to 5.5 V)	
		10 μF capacitor connected to REGC pin: 2 MHz (4.0 to 5.5 V)	
Subclock (oscillation frequency)		Crystal/external clock (32.768 kHz)	
Minimum instruction execution time		50 ns (When main clock operated at (f_{XX}) = 20 MHz)	
DSP function		32 × 32 = 64: 200 to 250 ns (at 20 MHz) 32 × 32 + 32 = 32: 300 ns (at 20 MHz) 16 × 16 = 32: 50 to 100 ns (at 20 MHz) 16 × 16 + 32 = 32: 150 ns (at 20 MHz)	
I/O ports		84 • Input: 8 • I/O: 76 (among these, N-ch open-drain output selectable: 8, fixed to N-ch open-drain output: 4)	
Timer		16-bit timer/event counter P: 1 channel 16-bit timer/event counter 0: 4 channels 8-bit timer/event counter 5: 2 channels (16-bit timer/event counter: usable as 1 channel) 8-bit timer H: 2 channels Watchdog timer: 2 channels Watch timer: 1 channel 8-bit interval timer: 1 channel	
Real-time output port		4 bits × 1, 2 bits × 1, or 6 bits × 1	
A/D converter		10-bit resolution × 8 channels	
D/A converter		8-bit resolution × 2 channels	
Serial interface		CSI: 1 channel CSI/UART: 1 channel CSIA (with automatic transmit/receive function): 2 channels UART: 2 channels I^2C bus: 1 channel Dedicated baud rate generator: 3 channels	
Interrupt sources		External: 9 (9)[Note], internal: 41	
Power save function		STOP/IDLE/HALT/sub-IDLE mode	
Operating supply voltage		4.5 to 5.5 V (at 20 MHz)/2.7 to 5.5 V (at 10 MHz)	
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)	

Note The figure in parentheses indicates the number of external interrupts that can release STOP mode.

CHAPTER 2 PIN FUNCTIONS

The names and functions of the pins of the V850ES/KG2 are described below, divided into port pins and non-port pins.

The pin I/O buffer power supplies are divided into three systems; AV_{REF0}/AV_{REF1}, BV_{DD}, and EV_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Ports CM, CS, CT, DH, DL
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 5, 9

2.1 List of Pin Functions

(1) Port pins

(1/3)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
P00	6	8	I/O	Yes	Port 0 I/O port Input/output can be specified in 1-bit units.	TOH0
P01	7	9				TOH1
P02	17	19				NMI
P03	18	20				INTP0
P04	19	21				INTP1
P05	20	22				INTP2
P06	21	23				INTP3
P10	3	5	I/O	Yes	Port 1 I/O port Input/output can be specified in 1-bit units.	ANO0
P11	4	6				ANO1
P30	25	27	I/O	Yes	Port 3 I/O port Input/output can be specified in 1-bit units. P36 to P39 are fixed to N-ch open-drain output.	TXD0/TO02
P31	26	28				RXD0/INTP7/TO03
P32	27	29				ASCK0/ADTRG/TO01
P33	28	30				TI000/TO00/TIP00/TOP00
P34	29	31				TI001/TO00/TIP01/TOP01
P35	30	32				TI010/TO01
P36	31	33		No		–
P37	32	34				–
P38	35	37				SDA0
P39	36	38				SCL0

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(2/3)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
P40	22	24	I/O	Yes	Port 4 I/O port Input/output can be specified in 1-bit units. P41 and P42 can be specified as N-ch open-drain output in 1-bit units.	SI00/RXD2
P41	23	25				SO00/TXD2
P42	24	26				$\overline{\text{SCK00}}$
P50	37	39	I/O	Yes	Port 5 I/O port Input/output can be specified in 1-bit units. P54 and P55 can be specified as N-ch open-drain output in 1-bit units.	TI011/RTP00/KR0
P51	38	40				TI50/RTP01/KR1
P52	39	41				TO50/RTP02/KR2
P53	40	42				SIA0/RTP03/KR3
P54	41	43				SOA0/RTP04/KR4
P55	42	44				$\overline{\text{SCKA0}}$/RTP05/KR5
P70	100	2	Input	No	Port 7 Input port	ANI0
P71	99	1				ANI1
P72	98	100				ANI2
P73	97	99				ANI3
P74	96	98				ANI4
P75	95	97				ANI5
P76	94	96				ANI6
P77	93	95				ANI7
P90	43	45	I/O	Yes	Port 9 I/O port Input/output can be specified in 1-bit units. P98, P99, P911, and P912 can be specified as N-ch open-drain output in 1-bit units.	A0/TXD1/KR6
P91	44	46				A1/RXD1/KR7
P92	45	47				A2/TI020/TO02
P93	46	48				A3/TI021
P94	47	49				A4/TI030/TO03
P95	48	50				A5/TI031
P96	49	51				A6/TI51/TO51
P97	50	52				A7/SI01
P98	51	53				A8/SO01
P99	52	54				A9/$\overline{\text{SCK01}}$
P910	53	55				A10/SIA1
P911	54	56				A11/SOA1
P912	55	57				A12/$\overline{\text{SCKA1}}$
P913	56	58				A13/INTP4
P914	57	59				A14/INTP5
P915	58	60				A15/INTP6

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(3/3)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
PCM0	61	63	I/O	Yes	Port CM I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1	62	64				CLKOUT
PCM2	63	65				$\overline{\text{HLDAK}}$
PCM3	64	66				$\overline{\text{HLDRQ}}$
PCS0	59	61	I/O	Yes	Port CS I/O port Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$
PCS1	60	62				$\overline{\text{CS1}}$
PCT0	65	67	I/O	Yes	Port CT I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WR0}}$
PCT1	66	68				$\overline{\text{WR1}}$
PCT4	67	69				$\overline{\text{RD}}$
PCT6	68	70				ASTB
PDH0	87	89	I/O	Yes	Port DH I/O port Input/output can be specified in 1-bit units.	A16
PDH1	88	90				A17
PDH2	89	91				A18
PDH3	90	92				A19
PDH4	91	93				A20
PDH5	92	94				A21
PDL0	71	73	I/O	Yes	Port DL I/O port Input/output can be specified in 1-bit units.	AD0
PDL1	72	74				AD1
PDL2	73	75				AD2
PDL3	74	76				AD3
PDL4	75	77				AD4
PDL5	76	78				AD5/FLMD1
PDL6	77	79				AD6
PDL7	78	80				AD7
PDL8	79	81				AD8
PDL9	80	82				AD9
PDL10	81	83				AD10
PDL11	82	84				AD11
PDL12	83	85				AD12
PDL13	84	86				AD13
PDL14	85	87				AD14
PDL15	86	88				AD15

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(2) Non-port pins

(1/5)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
A0	43	45	Output	Yes	Address bus for external memory (when using a separate bus)	P90/TXD1/KR6
A1	44	46				P91/RXD1/KR7
A2	45	47				P92/TI020/TO02
A3	46	48				P93/TI021
A4	47	49				P94/TI030/TO03
A5	48	50				P95/TI031
A6	49	51				P96/TI51/TO51
A7	50	52				P97/SI01
A8	51	53				P98/SO01
A9	52	54				P99/$\overline{\text{SCK01}}$
A10	53	55				P910/SIA1
A11	54	56				P911/SOA1
A12	55	57				P912/$\overline{\text{SCKA1}}$
A13	56	58				P913/INTP4
A14	57	59				P914/INTP5
A15	58	60				P915/INTP6
A16	87	89	Output	Yes	Address bus for external memory	PDH0
A17	88	90				PDH1
A18	89	91				PDH2
A19	90	92				PDH3
A20	91	93				PDH4
A21	92	94				PDH5
AD0	71	73	I/O	Yes	Address/data bus for external memory	PDL0
AD1	72	74				PDL1
AD2	73	75				PDL2
AD3	74	76				PDL3
AD4	75	77				PDL4
AD5	76	78				PDL5/FLMD1
AD6	77	79				PDL6
AD7	78	80				PDL7
AD8	79	81				PDL8
AD9	80	82				PDL9
AD10	81	83				PDL10
AD11	82	84				PDL11
AD12	83	85				PDL12
AD13	84	86				PDL13
AD14	85	87				PDL14
AD15	86	88				PDL15

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

GF: 100-pin plastic QFP (14 × 20)

(2/5)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
ADTRG	27	29	Input	Yes	A/D converter external trigger input	P32/ASCK0/TO01
ANI0	100	2	Input	No	Analog voltage input for A/D converter	P70
ANI1	99	1				P71
ANI2	98	100				P72
ANI3	97	99				P73
ANI4	96	98				P74
ANI5	95	97				P75
ANI6	94	96				P76
ANI7	93	95				P77
ANO0	3	5	Output	Yes	Analog voltage output for D/A converter	P10
ANO1	4	6				P11
ASCK0	27	29	Input	Yes	UART0 serial clock input	P32/ADTRG/TO01
ASTB	68	70	Output	Yes	Address strobe signal output for external memory	PCT6
AV_{REF0}	1	3	–	–	Reference voltage for A/D converter and positive power supply for alternate-function ports	–
AV_{REF1}	5	7	–	–	Reference voltage for D/A converter and positive power supply for alternate-function ports	–
AV_{SS}	2	4	–	–	Ground potential for A/D and D/A converters and alternate-function ports	–
BV_{DD}	70	72	–	–	Positive power supply for bus interface and alternate-function ports	–
BV_{SS}	69	73	–	–	Ground potential for bus interface and alternate-function ports	–
CLKOUT	62	64	Output	Yes	Internal system clock output	PCM1
$\overline{CS0}$	59	61	Output	Yes	Chip select output	PCS0
$\overline{CS1}$	60	62				PCS1
EV_{DD}	34	36	–	–	Positive power supply for external	–
EV_{SS}	33	35	–	–	Ground potential for external	–
FLMD0	8	10	Input	No	Flash programming mode setting pin	–
FLMD1	76	78		Yes		PDL5/AD5
$\overline{HLDAK}$	63	65	Output	Yes	Bus hold acknowledge output	PCM2
$\overline{HLDRQ}$	64	66	Input	Yes	Bus hold request input	PCM3

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(3/5)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
INTP0	18	20	Input	Yes	External interrupt request input (maskable, analog noise elimination)	P03
INTP1	19	21				P04
INTP2	20	22				P05
INTP3	21	23			External interrupt request input (maskable, digital + analog noise elimination)	P06
INTP4	56	58			External interrupt request input (maskable, analog noise elimination)	P913/A13
INTP5	57	59				P914/A14
INTP6	58	60				P915/A15
INTP7	26	28				P31/RXD0/TO03
KR0	37	39	Input	Yes	Key return input	P50/TI011/RTP00
KR1	38	40				P51/TI50/RTP01
KR2	39	41				P52/TO50/RTP02
KR3	40	42				P53/SIA0/RTP03
KR4	41	43				P54/SOA0/RTP04
KR5	42	44				P55/$\overline{\text{SCKA0}}$/RTP05
KR6	43	45				P90/A0/TXD1
KR7	44	46				P91/A1/RXD1
NMI	17	19	Input	Yes	External interrupt input (non-maskable, analog noise elimination)	P02
$\overline{\text{RD}}$	67	69	Output	Yes	Read strobe signal output for external memory	PCT4
REGC	10	12	–	–	Connecting capacitor for regulator output stabilization	–
$\overline{\text{RESET}}$	14	16	Input	–	System reset input	–
RTP00	37	39	Output	Yes	Real-time output port	P50/TI011/KR0
RTP01	38	40				P51/TI50/KR1
RTP02	39	41				P52/TO50/KR2
RTP03	40	42				P53/SIA0/KR3
RTP04	41	43				P54/SOA0/KR4
RTP05	42	44				P55/$\overline{\text{SCKA0}}$/KR5
RXD0	26	28	Input	Yes	Serial receive data input for UART0	P31/INTP7/TO03
RXD1	44	46			Serial receive data input for UART1	P91/A1/KR7
RXD2	22	25			Serial receive data input for UART2	P40/SI00
$\overline{\text{SCK00}}$	24	26	I/O	Yes	Serial clock I/O for CSI00, CSI01, CSIA0, CSIA1 N-ch open-drain output can be specified in 1-bit units.	P42
$\overline{\text{SCK01}}$	52	54				P99/A9
$\overline{\text{SCKA0}}$	42	44				P55/RTP05/KR5
$\overline{\text{SCKA1}}$	55	57				P912/A12

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(4/5)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
SCL0	36	38	I/O	No	Serial clock I/O for I^2C0 Fixed to N-ch open-drain output	P39
SDA0	35	37	I/O	No	Serial transmit/receive data I/O for I^2C0 Fixed to N-ch open-drain output	P38
SI00	22	24	Input	Yes	Serial receive data input for CSI00	P40/RXD2
SI01	50	52			Serial receive data input for CSI01	P97/A7
SIA0	40	42			Serial receive data input for CSIA0	P53/RTP03/KR3
SIA1	53	55			Serial receive data input for CSIA1	P910/A10
SO00	23	25	Output	Yes	Serial transmit data output for CSI00, CSI01, CSIA0, CSIA1 N-ch open-drain output can be specified in 1-bit units.	P41/TXD2
SO01	51	53				P98/A8
SOA0	41	43				P54/RTP04/KR4
SOA1	54	56				P911/A11
TI000	28	30	Input	Yes	Capture trigger input/external event input for TM00	P33/TO00/TIP00/TOP00
TI001	29	31			Capture trigger input for TM00	P34/TO00/TIP01/TOP01
TI010	30	32			Capture trigger input/external event input for TM01	P35/TO01
TI011	37	39			Capture trigger input for TM01	P50/RTP00/KR0
TI020	45	47			Capture trigger input/external event input for TM02	P92/A2/TO02
TI021	46	48			Capture trigger input for TM02	P93/A3
TI030	47	49			Capture trigger input/external event input for TM03	P94/A4/TO03
TI031	48	50			Capture trigger input for TM03	P95/A5
TI50	38	40			External event input for TM50	P51/RTP01/KR1
TI51	49	51			External event input for TM51	P96/A6/TO51
TIP00	28	30			Capture trigger input/external event input for TMP0	P33/TI000/TO00/TOP00
TIP01	29	31			Capture trigger input for TMP0	P34/TI001/TO00/TOP01

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(5/5)

Pin Name	Pin No.		I/O	Pull-up Resistor	Function	Alternate Function
	GC	GF				
TO00	28	30	Output	Yes	Timer output for TM00	P33/TI000/TIP00/TOP00
	29	31				P34/TI001/TIP01/TOP01
TO01	27	29			Timer output for TM01	P32/ASCK0/ADTRG
	30	32				P35/TI010
TO02	25	27			Timer output for TM02	P30/TXD0
	45	47				P92/A2/TI020
TO03	26	28			Timer output for TM03	P31/RXD0/INTP7
	47	49				P94/A4/TI030
TO50	39	41			Timer output for TM50	P52/RTP02/KR2
TO51	49	51			Timer output for TM51	P96/A6/TI51
TOH0	6	8			Timer output for TMH0	P00
TOH1	7	9			Timer output for TMH1	P01
TOP00	28	30			Timer output for TMP0	P33/TI000/TO00/TIP00
TOP01	29	31				P34/TI001/TO00/TIP01
TXD0	25	27	Output	Yes	Serial transmit data output for UART0	P30/TO02
TXD1	43	45			Serial transmit data output for UART1	P90/A0/KR6
TXD2	23	25			Serial transmit data output for UART2	P41/SO00
V_{DD}	9	11	–	–	Positive power supply pin for internal	–
V_{SS}	11	13	–	–	Ground potential for internal	–
$\overline{WAIT}$	61	63	Input	Yes	External wait input	PCM0
$\overline{WR0}$	65	67	Output	Yes	Write strobe for external memory (lower 8 bits)	PCT0
$\overline{WR1}$	66	68			Write strobe for external memory (higher 8 bits)	PCT1
X1	12	14	Input	No	Connecting resonator for main clock	–
X2	13	15	–	No		–
XT1	15	17	Input	No	Connecting resonator for subclock	–
XT2	16	18	–	No		–

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

2.2 Pin Status

The address bus becomes undefined during accesses to the internal RAM and ROM. The data bus goes into the high-impedance state without data output. The external bus control signal becomes inactive.

During peripheral I/O access, the address bus outputs the addresses of the on-chip peripheral I/Os that are accessed. The data bus goes into the high-impedance state without data output. The external bus control signal becomes inactive.

Table 2-2. Pin Operation Status in Operation Modes

Operating Status / Pin	Reset[Note 1]	HALT Mode	IDLE Mode/ STOP Mode	Idle State[Note 2]	Bus Hold
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	**Note 3**	Hi-Z	Held	Hi-Z
A0 to A15 (P90 to P915)	Hi-Z	Undefined[Note 4]	Hi-Z	Held	Hi-Z
A16 to A21 (PDH0 to PDH5)	Hi-Z	Undefined	Hi-Z	Held	Hi-Z
$\overline{\text{WAIT}}$ (PCM0)	Hi-Z	–	–	–	–
CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$ (PCS0, PCS1)	Hi-Z	H	H	Held	Hi-Z
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$ (PCT0, PCT1)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{RD}}$ (PCT4)	Hi-Z	H	H	H	Hi-Z
ASTB (PCT6)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{HLDAK}}$ (PCM2)	Hi-Z	Operating	H	H	L
$\overline{\text{HLDRQ}}$ (PCM3)	Hi-Z	Operating	–	–	Operating

Notes 1. Since the bus control pin is also used as a port pin, it is initialized to the port mode (input) after reset.

2. The pin statuses in the idle state inserted after the T3 state in the multiplex bus mode and after the T2 state in the separate bus mode are listed.

3. In separate bus mode: Hi-Z
In multiplex bus mode: Undefined

4. Only in separate bus mode

Remark Hi-Z: High impedance
H: High-level output
L: Low-level output
–: Input without sampling (input acknowledgment not possible)

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

(1/2)

Pin	Alternate Function	Pin No.		I/O Circuit Type	Recommended Connection
		GC	GF		
P00	TOH0	6	8	5-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P01	TOH1	7	9		
P02	NMI	17	19	5-W	
P03 to P06	INTP0 to INTP3	18 to 21	20 to 23		
P10	ANO0	3	5	12-B	Input: Independently connect to AV_{REF1} or AV_{SS} via a resistor. Output: Leave open.
P11	ANO1	4	6		
P30	TXD0/TO02	25	27	5-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P31	RXD0/INTP7/TO03	26	28	5-W	
P32	ASCK0/ADTRG/TO01	27	29		
P33	TI000/TO00/TIP00/TOP00	28	30		
P34	TI001/TO00/TIP01/TOP01	29	31		
P35	TI010/TO01	30	32		
P36, P37	–	31, 32	33, 34	13-AB	
P38	SDA0	35	37	13-AD	
P39	SCL0	36	38		
P40	SI00/RXD2	22	24	5-W	
P41	SO00/TXD2	23	25	10-E	
P42	$\overline{\text{SCK00}}$	24	26	10-F	
P50	TI011/RTP00/KR0	37	39	8-A	
P51	TI50/RTP01/KR1	38	40		
P52	TO50/RTP02/KR2	39	41		
P53	SIA0/RTP03/KR3	40	42		
P54	SOA0/RTP04/KR4	41	43	10-A	
P55	$\overline{\text{SCKA0}}$/RTP05/KR5	42	44		
P70 to P77	ANI0 to ANI7	100 to 93	2, 1, 100 to 95	9-C	Connect to AV_{REF0} or AV_{SS}.
P90	A0/TXD1/KR6	43	45	8-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P91	A1/RXD1/KR7	44	46		
P92	A2/TI020/TO02	45	47		
P93	A3/TI021	46	48	5-W	
P94	A4/TI030/TO03	47	49	8-A	
P95	A5/TI031	48	50	5-W	
P96	A6/TI51/TO51	49	51	8-A	
P97	A7/SI01	50	52	5-W	
P98	A8/SO01	51	53	10-E	

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(2/2)

Pin	Alternate Function	Pin No.		I/O Circuit Type	Recommended Connection
		GC	GF		
P99	A9/$\overline{SCK01}$	52	54	10-F	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P910	A10/SIA1	53	55	5-W	
P911	A11/SOA1	54	56	10-E	
P912	A12/$\overline{SCKA1}$	55	57	10-F	
P913 to P915	A13/INTP4 to A15/INTP6	56 to 58	58 to 60	5-W	
PCM0	$\overline{WAIT}$	61	63	5-A	Input: Independently connect to BV_{DD} or BV_{SS} via a resistor. Output: Leave open.
PCM1	CLKOUT	62	64		
PCM2	$\overline{HLDAK}$	63	65		
PCM3	$\overline{HLDRQ}$	64	66		
PCS0, PCS1	$\overline{CS0}$, $\overline{CS1}$	59, 60	61, 62	5-A	
PCT0	$\overline{WR0}$	65	67	5-A	
PCT1	$\overline{WR1}$	66	68		
PCT4	$\overline{RD}$	67	69		
PCT6	ASTB	68	70		
PDL0 to PDL4	AD0 to AD4	71 to 75	73 to 77	5-A	
PDL5	AD5/FLMD1	76	78		
PDL6 to PDL15	AD6 to AD15	77 to 86	79 to 88		
PDH0 to PDH5	A16 to A21	87 to 92	89 to 94	5-A	
AV_{REF0}	–	1	3	–	Directly connect to V_{DD}.
AV_{REF1}	–	5	7	–	Directly connect to V_{DD}.
AV_{SS}	–	2	4	–	–
BV_{DD}	–	70	72	–	–
BV_{SS}	–	69	71	–	–
EV_{DD}	–	34	36	–	–
EV_{SS}	–	33	35	–	–
$\overline{RESET}$	–	14	16	2	–
FLMD0	–	8	10	–	Directly connect to EV_{SS} or V_{SS} or pull down with a 10 kΩ resistor.
V_{DD}	–	9	11	–	–
V_{SS}	–	11	13	–	–
X1	–	12	14	–	–
X2	–	13	15	–	–
XT1	–	15	17	16	Directly connect to V_{SS}[Note].
XT2	–	16	18	16	Leave open.

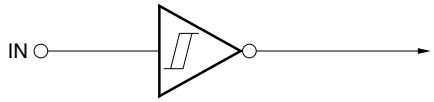
Note Be sure to set the PSMR.XTSTP bit to 1 when this pin is not used.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

2.4 Pin I/O Circuits

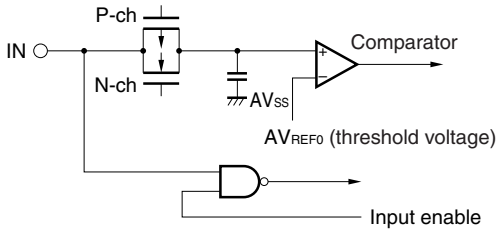
(1/2)

Type 2

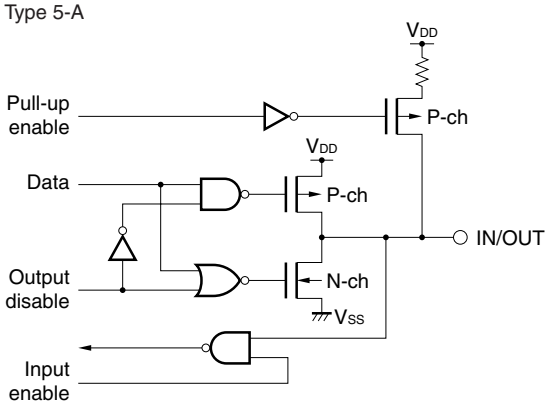


Schmitt-triggered input with hysteresis characteristics

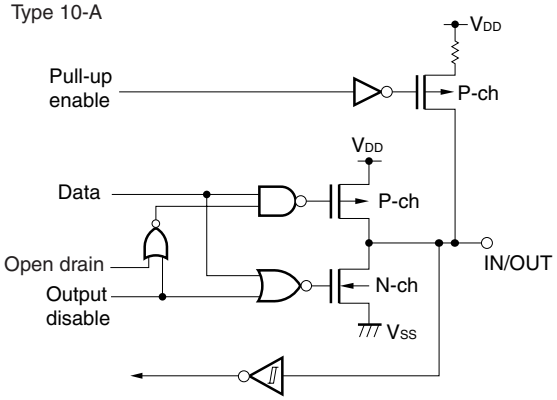
Type 9-C



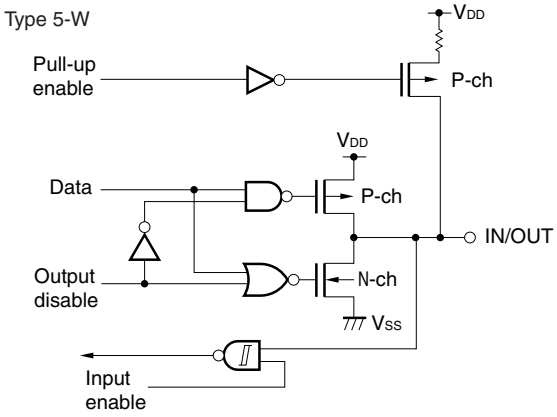
Type 5-A



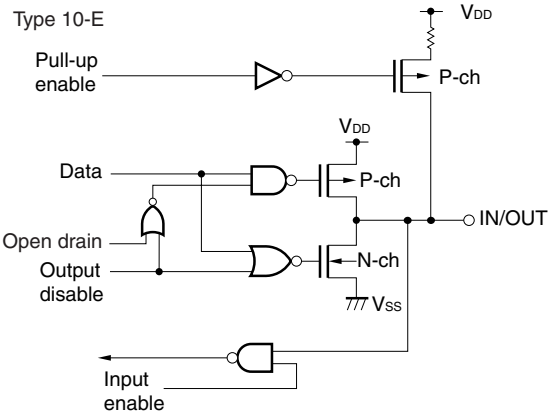
Type 10-A



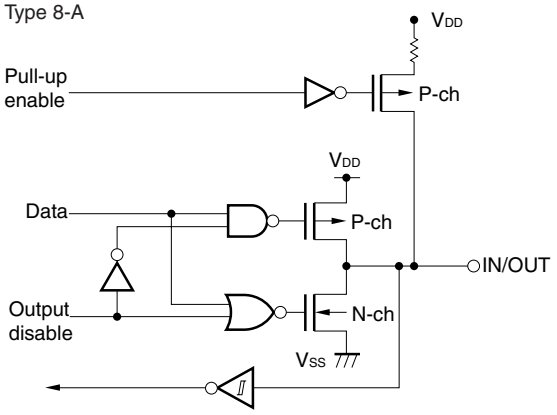
Type 5-W



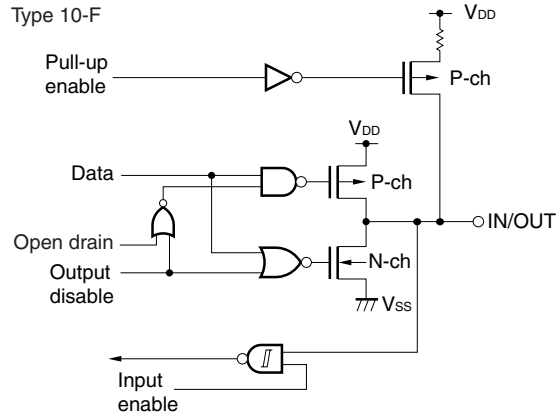
Type 10-E



Type 8-A

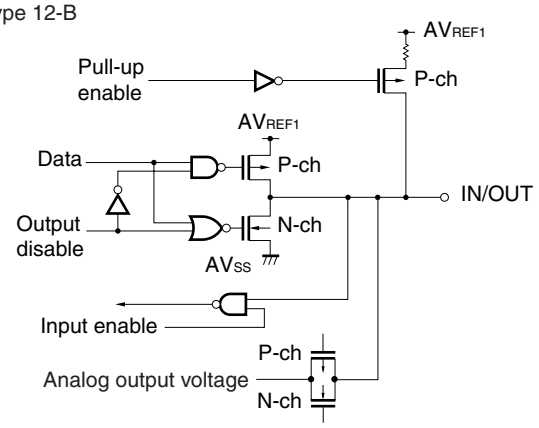


Type 10-F

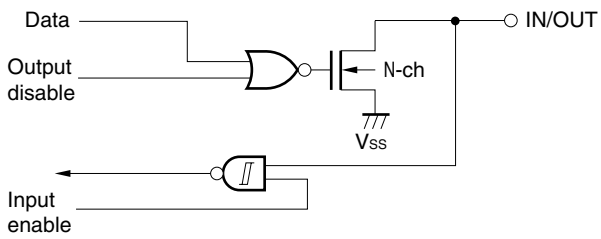


(2/2)

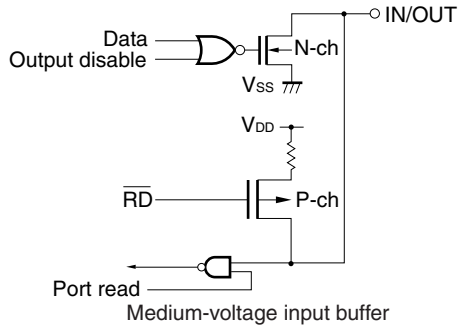
Type 12-B



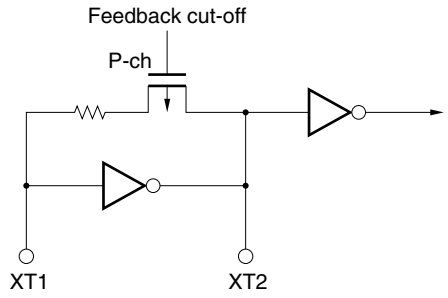
Type 13-AD



Type 13-AB



Type 16



Remark Read V_{DD} as EV_{DD} or BV_{DD}. Also, read V_{SS} as EV_{SS} or BV_{SS}.

CHAPTER 3 CPU FUNCTIONS

The CPU of the V850ES/KG2 is based on the RISC architecture and executes most instructions in one clock cycle by using 5-stage pipeline control.

3.1 Features

- Number of instructions: 83
- Minimum instruction execution time: 50.0 ns (@ 20 MHz operation: 4.5 to 5.5 V, REGC = V_{DD})
  62.5 ns (@ 16 MHz operation: 4.0 to 5.5 V, REGC = 10 μF)
  100 ns (@ 10 MHz operation: 2.7 to 5.5 V, REGC = V_{DD})
- Memory space Program (physical address) space: 64 MB linear
  Data (logical address) space: 4 GB linear
  - Memory block division function: 2 MB, 2 MB, 4 MB, 8 MB/Total of 4 blocks
- General-purpose registers: 32 bits × 32
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- 32-bit shift instruction: 1 clock
- Load/store instruction with long/short format
- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

3.2 CPU Register Set

The CPU registers of the V850ES/KG2 can be classified into two categories: a general-purpose program register set and a dedicated system register set. All the registers have 32-bit width.

For details, refer to the **V850ES Architecture User's Manual**.

(1) Program register set

31		0
r0	(Zero register)	
r1	(Assembler-reserved register)	
r2		
r3	(Stack pointer (SP))	
r4	(Global pointer (GP))	
r5	(Text pointer (TP))	
r6		
r7		
r8		
r9		
r10		
r11		
r12		
r13		
r14		
r15		
r16		
r17		
r18		
r19		
r20		
r21		
r22		
r23		
r24		
r25		
r26		
r27		
r28		
r29		
r30	(Element pointer (EP))	
r31	(Link pointer (LP))	

31		0
PC	(Program counter)	

(2) System register set

31		0
EIPC	(Interrupt status saving register)	
EIPSW	(Interrupt status saving register)	
FEPC	(NMI status saving register)	
FEPSW	(NMI status saving register)	
ECR	(Interrupt source register)	
PSW	(Program status word)	
CTPC	(CALLT execution status saving register)	
CTPSW	(CALLT execution status saving register)	
DBPC	(Exception/debug trap status saving register)	
DBPSW	(Exception/debug trap status saving register)	
CTBP	(CALLT base pointer)	

3.2.1 Program register set

The program register set includes general-purpose registers and a program counter.

(1) General-purpose registers (r0 to r31)

Thirty-two general-purpose registers, r0 to r31, are available. All of these registers can be used as a data variable or address variable.

However, r0 and r30 are implicitly used by instructions and care must be exercised when using these registers. r0 always holds 0 and is used for operations that use 0 and offset 0 addressing. r30 is used as a base pointer when performing memory access with the SLD and SST instructions.

Also, r1, r3 to r5, and r31 are implicitly used by the assembler and C compiler. Therefore, before using these registers, their contents must be saved so that they are not lost, and they must be restored to the registers after the registers have been used. There are cases when r2 is used by the real-time OS. If r2 is not used by the real-time OS, r2 can be used as a variable register.

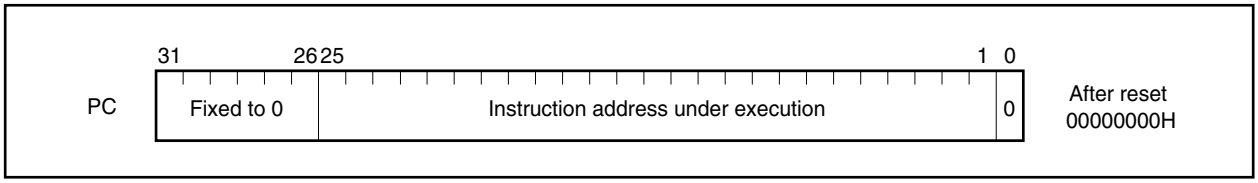
Table 3-1. Program Registers

Name	Usage	Operation
r0	Zero register	Always holds 0
r1	Assembler-reserved register	Working register for generating 32-bit immediate
r2	Address/data variable register (when r2 is not used by the real-time OS to be used)	
r3	Stack pointer	Used to generate stack frame when function is called
r4	Global pointer	Used to access global variable in data area
r5	Text pointer	Register to indicate the start of the text area (area for placing program code)
r6 to r29	Address/data variable register	
r30	Element pointer	Base pointer when memory is accessed
r31	Link pointer	Used by compiler when calling function
PC	Program counter	Holds instruction address during program execution

(2) Program counter (PC)

This register holds the address of the instruction under execution. The lower 26 bits of this register are valid, and bits 31 to 26 are fixed to 0. If a carry occurs from bit 25 to bit 26, it is ignored.

Bit 0 is fixed to 0, and branching to an odd address cannot be performed.



3.2.2 System register set

System registers control the status of the CPU and hold interrupt information.

Read from and write to system registers are performed by setting the system register numbers shown below with the system register load/store instructions (LDSR, STSR instructions).

Table 3-2. System Register Numbers

System Register No.	System Register Name	Operand Specification Enabled	
		LDSR Instruction	STSR Instruction
0	Interrupt status saving register (EIPC)[Note 1]	Yes	Yes
1	Interrupt status saving register (EIPSW)[Note 1]	Yes	Yes
2	NMI status saving register (FEPC)[Note 1]	Yes	Yes
3	NMI status saving register (FEPSW)[Note 1]	Yes	Yes
4	Interrupt source register (ECR)	No	Yes
5	Program status word (PSW)	Yes	Yes
6 to 15	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No
16	CALLT execution status saving register (CTPC)	Yes	Yes
17	CALLT execution status saving register (CTPSW)	Yes	Yes
18	Exception/debug trap status saving register (DBPC)	Yes[Note 2]	Yes[Note 2]
19	Exception/debug trap status saving register (DBPSW)	Yes[Note 2]	Yes[Note 2]
20	CALLT base pointer (CTBP)	Yes	Yes
21 to 31	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No

Notes 1. Since only one set of these registers is available, the contents of this register must be saved by the program when multiple interrupt servicing is enabled.

2. These registers can be accessed only during the interval between the execution of the DBTRAP instruction or illegal opcode and the DBRET instruction.

Caution Even if bit 0 of EIPC, FEPC, or CTPC is set (1) by the LDSR instruction, bit 0 is ignored during return with the RETI instruction following interrupt servicing (because bit 0 of PC is fixed to 0). When setting a value to EIPC, FEPC, and CTPC, set an even number (bit 0 = 0).

(1) Interrupt status saving registers (EIPC, EIPSW)

There are two interrupt status saving registers, EIPC and EIPSW.

Upon occurrence of a software exception or a maskable interrupt, the contents of the program counter (PC) are saved to EIPC and the contents of the program status word (PSW) are saved to EIPSW (upon occurrence of a non-maskable interrupt (NMI), the contents are saved to the NMI status saving registers (FEPC, FEPSW)).

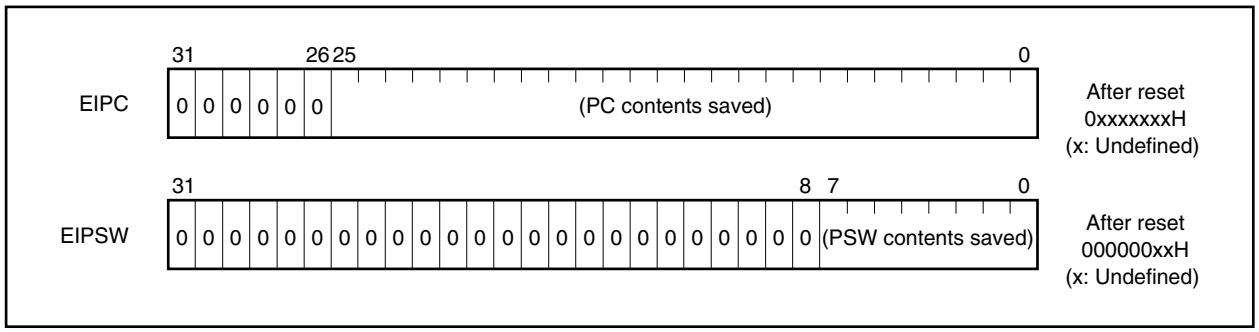
The address of the next instruction following the instruction executed when a software exception or maskable interrupt occurs is saved to EIPC, except for some instructions (refer to **21.9 Period in Which Interrupts Are Not Acknowledged by CPU**).

The current PSW contents are saved to EIPSW.

Since there is only one set of interrupt status saving registers, the contents of these registers must be saved by the program when multiple interrupt servicing is enabled.

Bits 31 to 26 of EIPC and bits 31 to 8 of EIPSW are reserved (fixed to 0) for future function expansion.

When the RETI instruction is executed, the values in EIPC and EIPSW are restored to the PC and PSW, respectively.



(2) NMI status saving registers (FEPC, FEPSW)

There are two NMI status saving registers, FEPC and FEPSW.

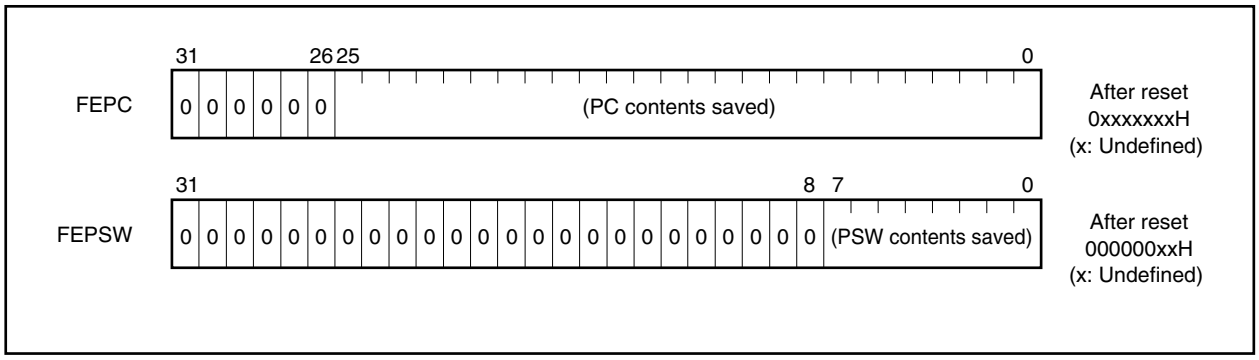
Upon occurrence of a non-maskable interrupt (NMI), the contents of the program counter (PC) are saved to FEPC and the contents of the program status word (PSW) are saved to FEPSW.

The address of the next instruction following the instruction executed when a non-maskable interrupt occurs is saved to FEPC, except for some instructions.

The current PSW contents are saved to FEPSW.

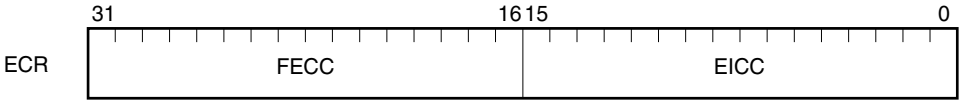
Since there is only one set of NMI status saving registers, the contents of these registers must be saved by the program when multiple interrupt servicing is performed.

Bits 31 to 26 of FEPC and bits 31 to 8 of FEPSW are reserved (fixed to 0) for future function expansion.



(3) Interrupt source register (ECR)

Upon occurrence of an interrupt or an exception, the interrupt source register (ECR) holds the source of an interrupt or an exception. The value held by ECR is the exception code coded for each interrupt source. This register is a read-only register, and thus data cannot be written to it using the LDSR instruction.



Bit position	Bit name	Description
31 to 16	FECC	Non-maskable interrupt (NMI) exception code
15 to 0	EICC	Exception, maskable interrupt exception code

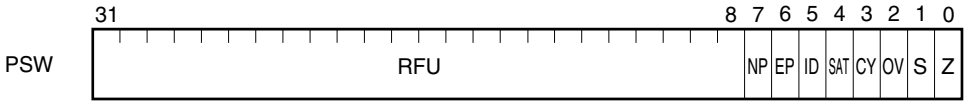
(4) Program status word (PSW)

The program status word (PSW) is a collection of flags that indicate the program status (instruction execution result) and the CPU status.

When the contents of this register are changed using the LDSR instruction, the new contents become valid immediately following completion of LDSR instruction execution. Interrupt request acknowledgment is held pending while a write to the PSW is being executed by the LDSR instruction.

Bits 31 to 8 are reserved (fixed to 0) for future function expansion.

(1/2)



Bit position	Flag name	Description
31 to 8	RFU	Reserved field. Fixed to 0.
7	NP	Indicates that non-maskable interrupt (NMI) servicing is in progress. This flag is set to 1 when an NMI request is acknowledged, and disables multiple interrupts. 0: NMI servicing not in progress 1: NMI servicing in progress
6	EP	Indicates that exception processing is in progress. This flag is set to 1 when an exception occurs. Moreover, interrupt requests can be acknowledged even when this bit is set. 0: Exception processing not in progress 1: Exception processing in progress
5	ID	Indicates whether maskable interrupt request acknowledgment is enabled. 0: Interrupt enabled 1: Interrupt disabled
4	SAT[Note]	Indicates that the result of executing a saturated operation instruction has overflowed and that the calculation result is saturated. Since this is a cumulative flag, it is set to 1 when the result of a saturated operation instruction becomes saturated, and it is not cleared to 0 even if the operation results of successive instructions do not become saturated. This flag is neither set nor cleared when arithmetic operation instructions are executed. 0: Not saturated 1: Saturated
3	CY	Indicates whether carry or borrow occurred as the result of an operation. 0: No carry or borrow occurred 1: Carry or borrow occurred
2	OV[Note]	Indicates whether overflow occurred during an operation. 0: No overflow occurred 1: Overflow occurred.
1	S[Note]	Indicates whether the result of an operation is negative. 0: Operation result is positive or 0. 1: Operation result is negative.
0	Z	Indicates whether operation result is 0. 0: Operation result is not 0. 1: Operation result is 0.

Remark **Note** is explained on the following page.

(2/2)

Note During saturated operation, the saturated operation results are determined by the contents of the OV flag and S flag. The SAT flag is set (to 1) only when the OV flag is set (to 1) during saturated operation.

Operation result status	Flag status			Saturated operation result
	SAT	OV	S	
Maximum positive value exceeded	1	1	0	7FFFFFFFH
Maximum negative value exceeded	1	1	1	80000000H
Positive (maximum value not exceeded)	Holds value before operation	0	0	Actual operation result
Negative (maximum value not exceeded)			1	

(5) CALLT execution status saving registers (CTPC, CTPSW)

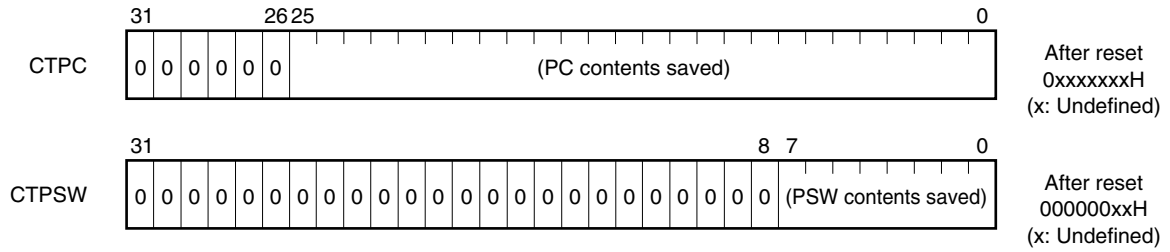
There are two CALLT execution status saving registers, CTPC and CTPSW.

When the CALLT instruction is executed, the contents of the program counter (PC) are saved to CTPC, and the program status word (PSW) contents are saved to CTPSW.

The contents saved to CTPC consist of the address of the next instruction after the CALLT instruction.

The current PSW contents are saved to CTPSW.

Bits 31 to 26 of CTPC and bits 31 to 8 of CTPSW are reserved (fixed to 0) for future function expansion.



(6) Exception/debug trap status saving registers (DBPC, DBPSW)

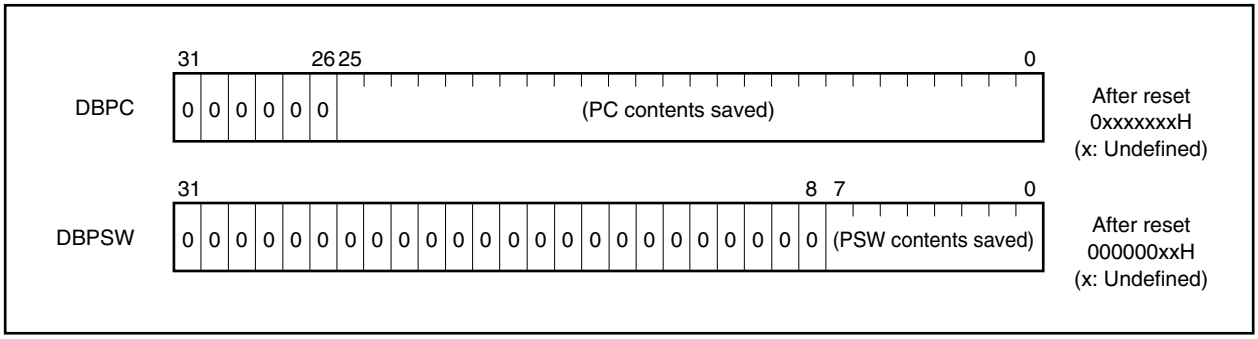
There are two exception/debug trap status saving registers, DBPC and DBPSW.

Upon occurrence of an exception trap or debug trap, the contents of the program counter (PC) are saved to DBPC, and the program status word (PSW) contents are saved to DBPSW.

The contents saved to DBPC consist of the address of the next instruction after the instruction executed when an exception trap or debug trap occurs.

The current PSW contents are saved to DBPSW.

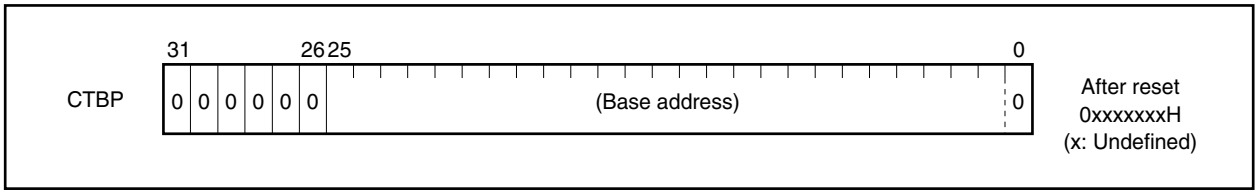
Bits 31 to 26 of DBPC and bits 31 to 8 of DBPSW are reserved (fixed to 0) for future function expansion.



(7) CALLT base pointer (CTBP)

The CALLT base pointer (CTBP) is used to specify table addresses and generate target addresses (bit 0 is fixed to 0).

Bits 31 to 26 are reserved (fixed to 0) for future function expansion.



3.3 Operating Modes

The V850ES/KG2 has the following operating modes.

(1) Normal operating mode

After the system has been released from the reset state, the pins related to the bus interface are set to the port mode, execution branches to the reset entry address of the internal ROM, and instruction processing is started.

(2) Flash memory programming mode

When this mode is specified, the internal flash memory can be programmed by using a flash programmer.

(a) Specifying operating mode

The operating mode is specified according to the status (input level) of the FLMD0 and FLMD1 pins.

In the normal operating mode, input a low level to the FLMD0 pin during the reset period.

A high level is input to the FLMD0 pin by the flash programmer in the flash memory programming mode if a flash programmer is connected. In the self-programming mode, input a high level to this pin from an external circuit.

Fix the specification of these pins in the application system and do not change the setting of these pins during operation.

FLMD0	FLMD1	Operating Mode
L	×	Normal operating mode
H	L	Flash memory programming mode
H	H	Setting prohibited

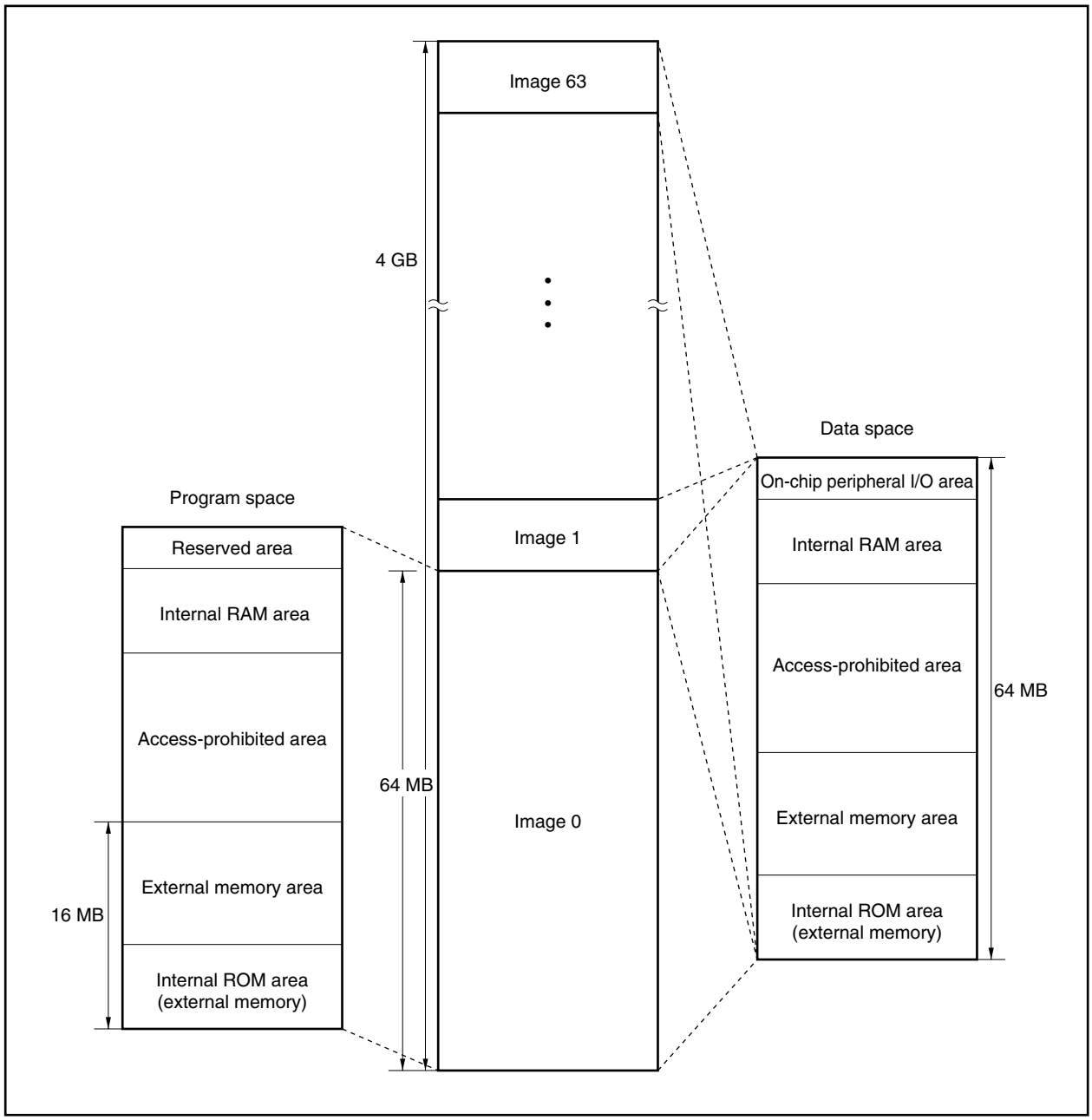
Remark H: High level
L: Low level
×: don't care

3.4 Address Space

3.4.1 CPU address space

For instruction addressing, up to a combined total of 16 MB of external memory area and internal ROM area, plus an internal RAM area, are supported in a linear address space (program space) of up to 64 MB. For operand addressing (data access), up to 4 GB of a linear address space (data space) is supported. The 4 GB address space, however, is viewed as 64 images of a 64 MB physical address space. This means that the same 64 MB physical address space is accessed regardless of the value of bits 31 to 26.

Figure 3-1. Address Space Image



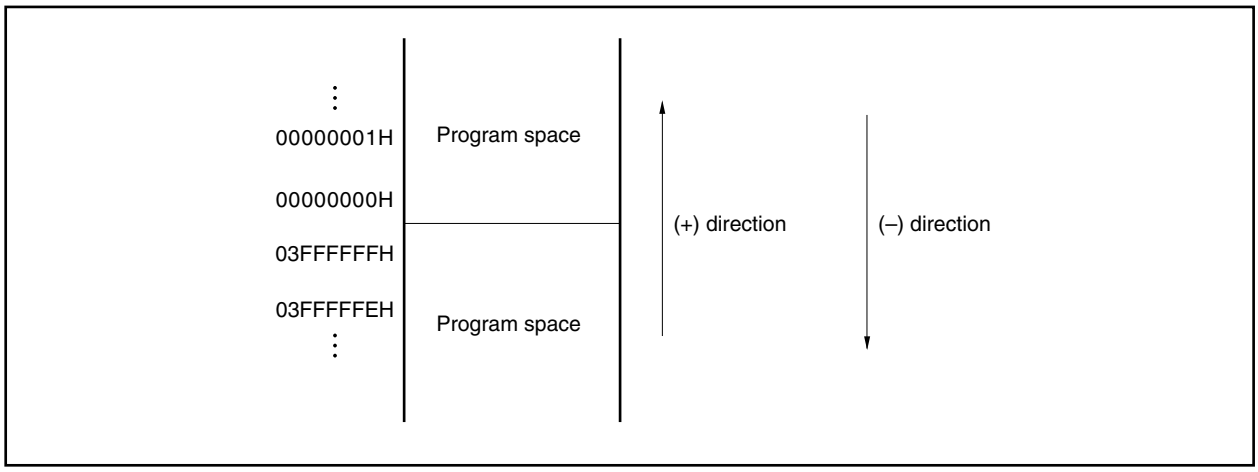
3.4.2 Wraparound of CPU address space

(1) Program space

Of the 32 bits of the program counter (PC), the higher 6 bits are fixed to 0 and only the lower 26 bits are valid. Even if a carry or borrow occurs from bit 25 to bit 26 as a result of branch address calculation, the higher 6 bits ignore this and remain 0.

Therefore, the lower-limit address of the program space, 00000000H, and the upper-limit address, 03FFFFFFH, are contiguous addresses, and the program space is wrapped around at the boundary of these addresses.

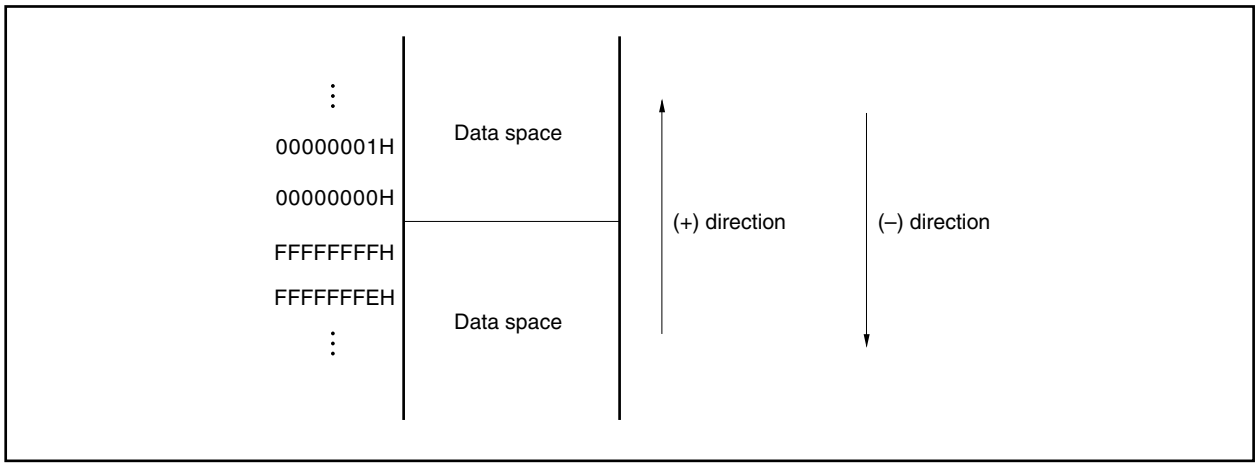
Caution No instructions can be fetched from the 4 KB area of 03FFF000H to 03FFFFFFH because this area is an on-chip peripheral I/O area. Therefore, do not execute any branch operation instructions in which the destination address will reside in any part of this area.



(2) Data space

The result of an operand address calculation that exceeds 32 bits is ignored.

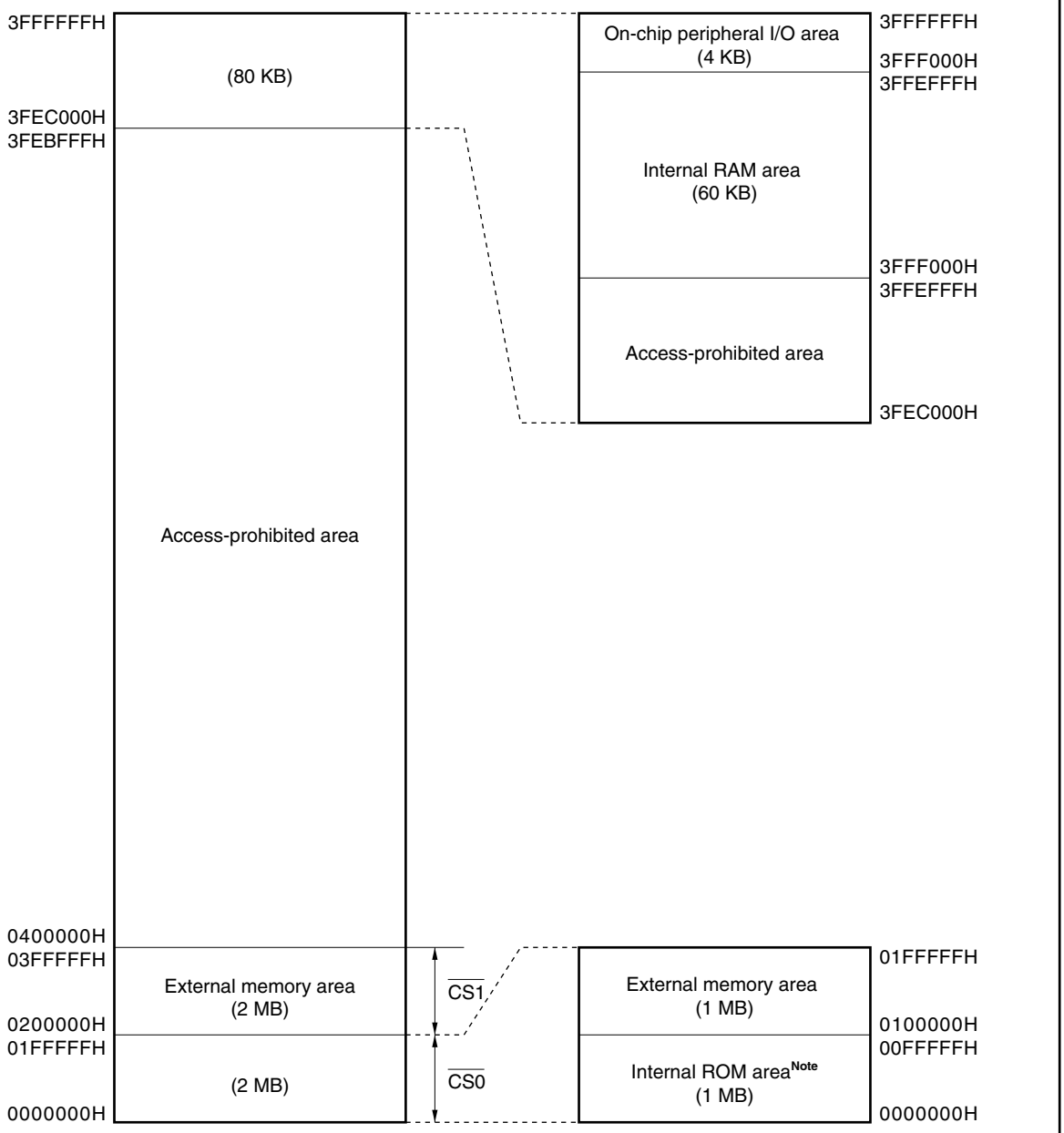
Therefore, the lower-limit address of the data space, address 00000000H, and the upper-limit address, FFFFFFFFH, are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



3.4.3 Memory map

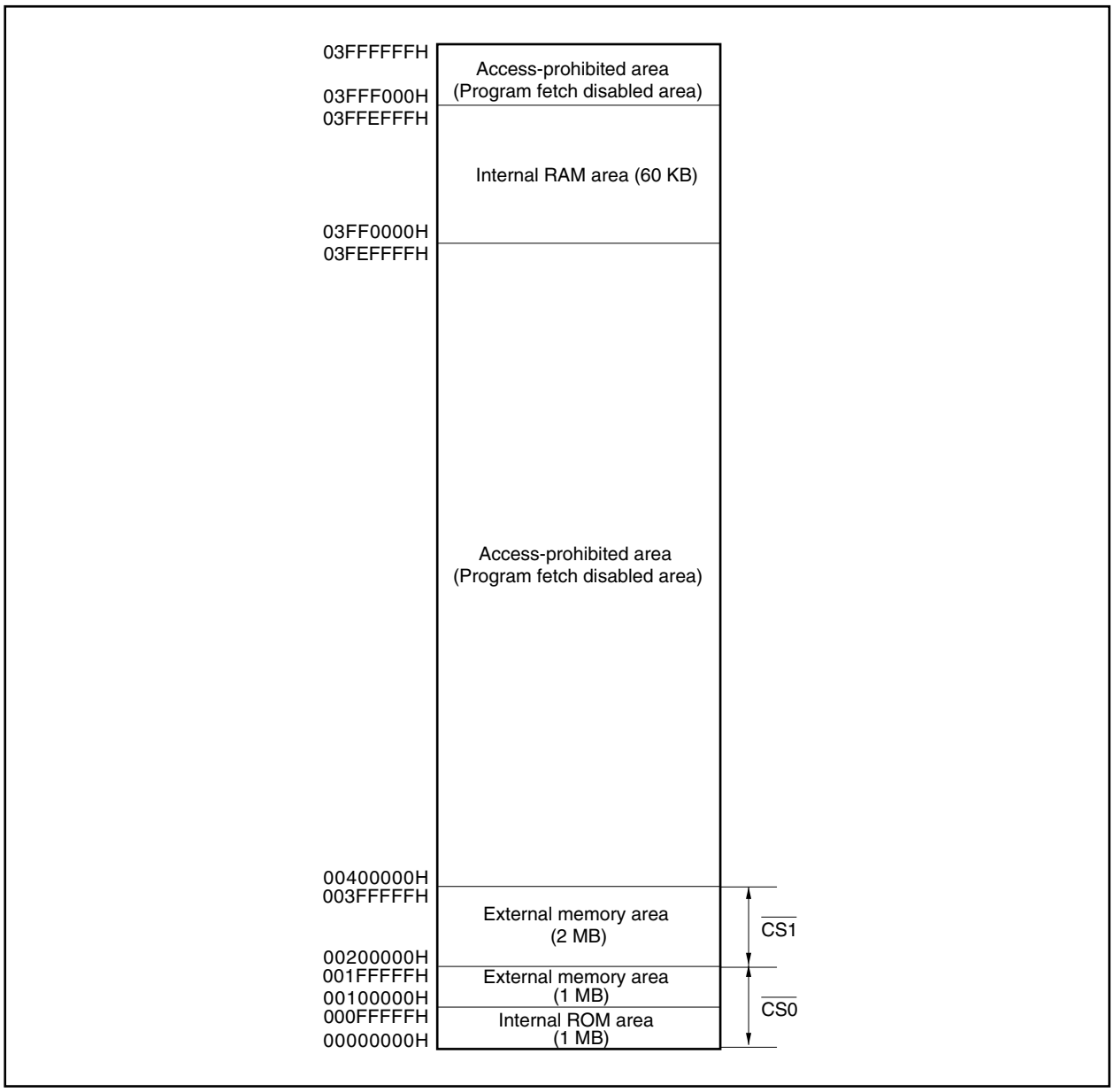
The V850ES/KG2 has reserved areas as shown below.

Figure 3-2. Data Memory Map (Physical Addresses)



Note Fetch access and read access to addresses 0000000H to 00FFFFFH is performed for the internal ROM area, but in the case of data write access, it is performed for an external memory area.

Figure 3-3. Program Memory Map



3.4.4 Areas

(1) Internal ROM area

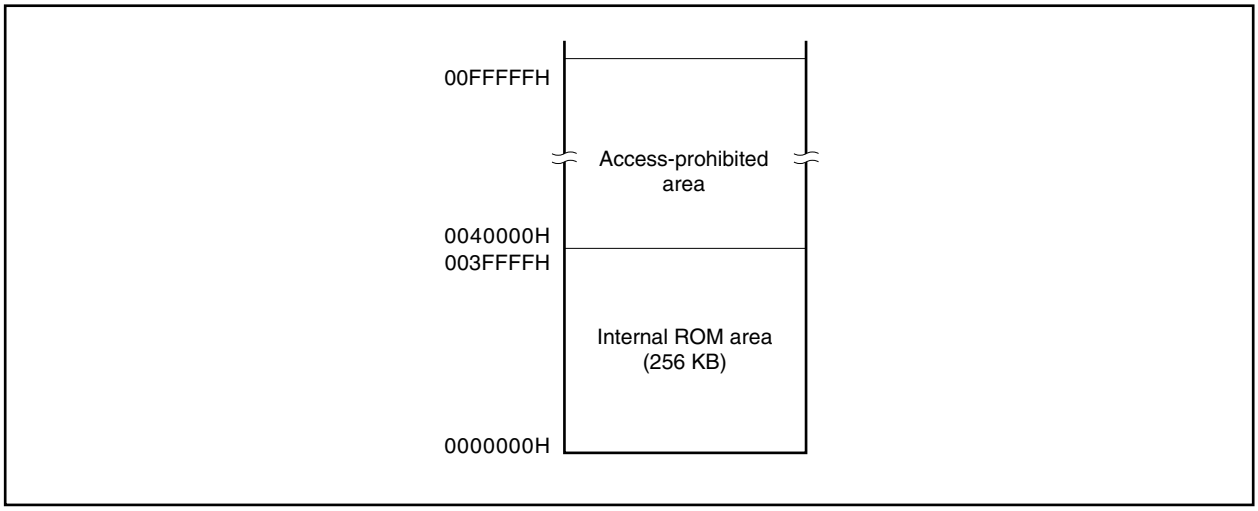
An area of 1 MB from 0000000H to 00FFFFFH is reserved for the internal ROM area.

(a) Internal ROM (256 KB)

A 256 KB area from 0000000H to 003FFFFH is provided in the following products.
Addresses 0040000H to 00FFFFFH are an access-prohibited area.

- μPD70F3732

Figure 3-4. Internal ROM Area (256 KB)

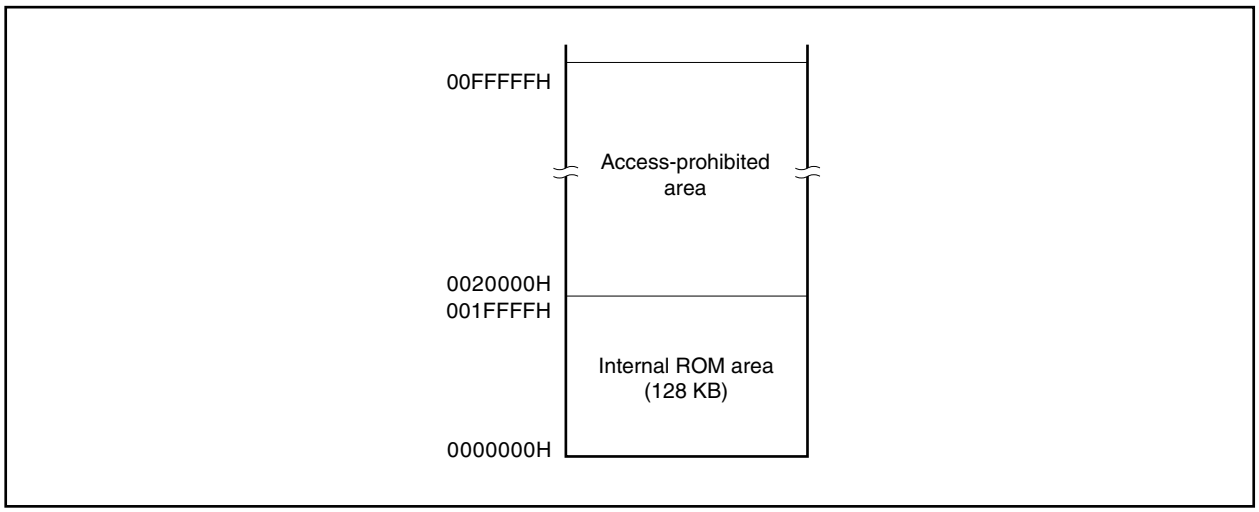


(b) Internal ROM (128 KB)

A 128 KB area from 0000000H to 001FFFFH is provided in the following products.
Addresses 0020000H to 00FFFFFH are an access-prohibited area.

- μPD70F3731

Figure 3-5. Internal ROM Area (128 KB)



(2) Internal RAM area

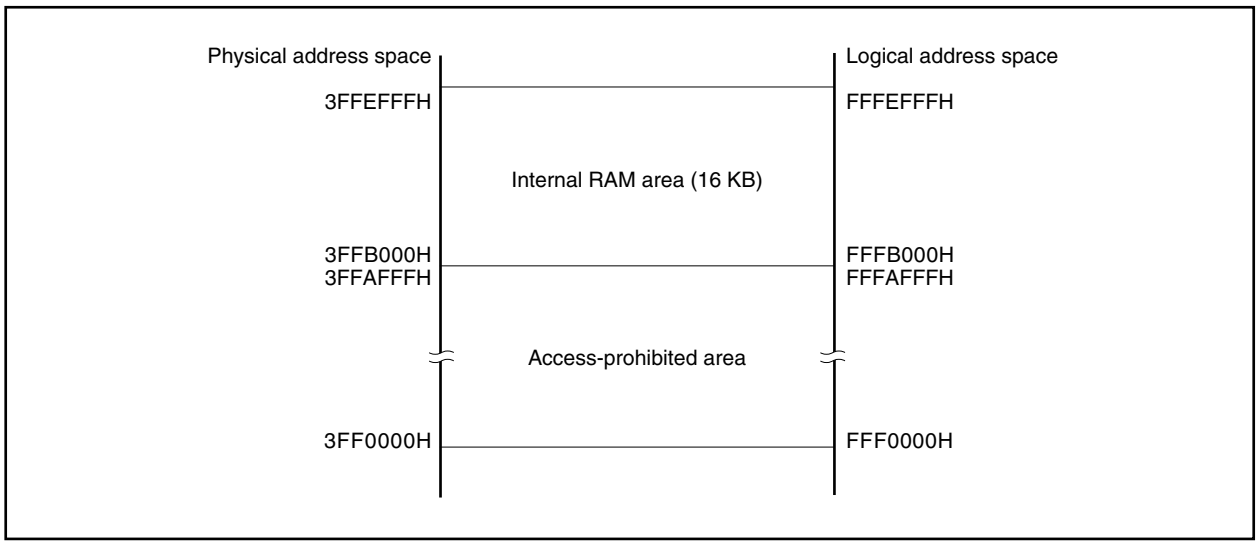
An area of 60 KB maximum from 3FF0000H to 3FFEFFFH is reserved for the internal RAM area.

(a) Internal RAM (16 KB)

A 16 KB area from 3FFB000H to 3FFEFFFH is provided as physical internal RAM.
Addresses 3FF0000H to 3FFAFFFH are an access-prohibited area.

- μPD70F3732

Figure 3-6. Internal RAM Area (16 KB)



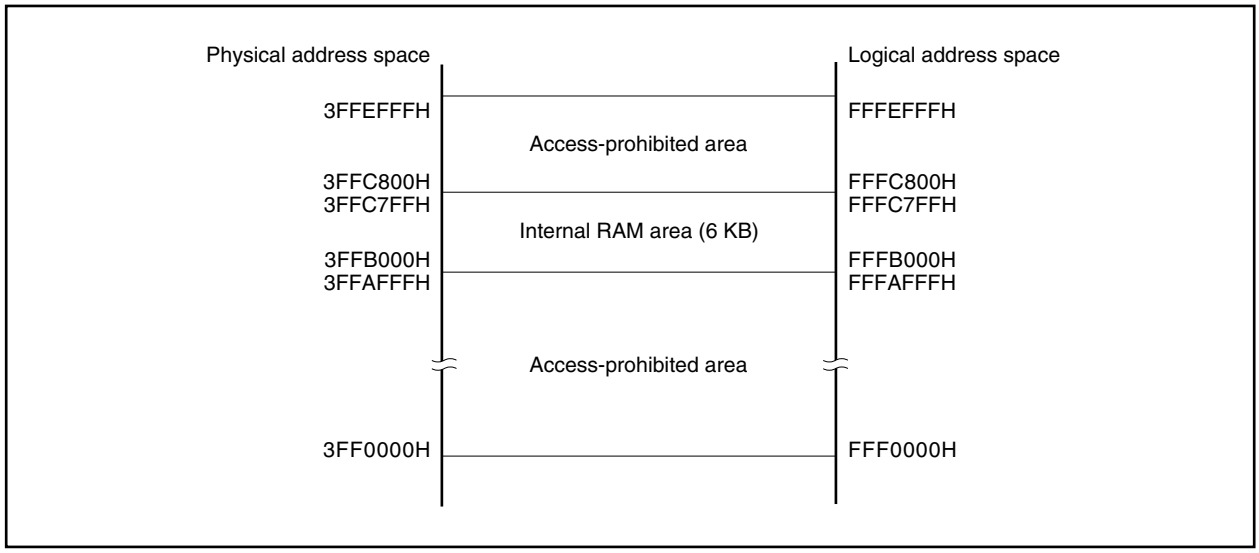
(b) Internal RAM (6 KB)

A 6 KB area from 3FFB000H to 3FFC7FFH is provided as physical internal RAM.

Addresses 3FF0000H to 3FFAFFFH and 3FFC800H to 3FFEFFFH are an access-prohibited area.

- μPD70F3731

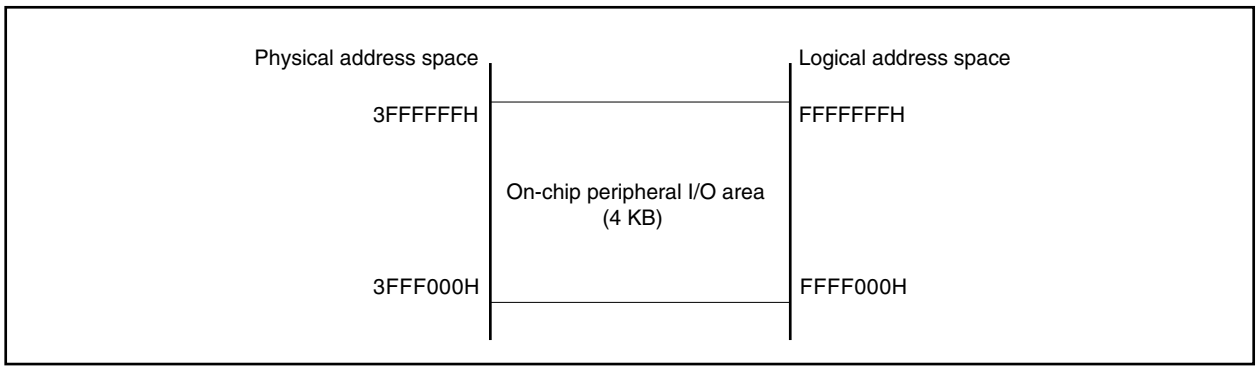
Figure 3-7. Internal RAM Area (6 KB)



(3) On-chip peripheral I/O area

A 4 KB area from 3FFF000H to 3FFFFFFH is reserved as the on-chip peripheral I/O area.

Figure 3-8. On-Chip Peripheral I/O Area



Peripheral I/O registers assigned with functions such as on-chip peripheral I/O operation mode specification and state monitoring are mapped to the on-chip peripheral I/O area. Program fetches are not allowed in this area.

Cautions 1. If word access of a register is attempted, halfword access to the word area is performed twice, first for the lower bits, then for the higher bits, ignoring the lower 2 address bits.

2. If a register that can be accessed in byte units is accessed in halfword units, the higher 8 bits become undefined if the access is a read operation. If a write access is performed, only the data in the lower 8 bits is written to the register.

3. Addresses that are not defined as registers are reserved for future expansion. If these addresses are accessed, the operation is undefined and not guaranteed.

(4) External memory area

3 MB (0100000H to 03FFFFH) are provided as the external memory area. For details, refer to **CHAPTER 5 BUS CONTROL FUNCTION**.

3.4.5 Recommended use of address space

The architecture of the V850ES/KG2 requires that a register that serves as a pointer be secured for address generation when operand data in the data space is accessed. The address stored in this pointer ±32 KB can be directly accessed by an instruction for operand data. Because the number of general-purpose registers that can be used as a pointer is limited, however, by keeping the performance from dropping during address calculation when a pointer value is changed, as many general-purpose registers as possible can be secured for variables, and the program size can be reduced.

(1) Program space

Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0, and only the lower 26 bits are valid. Regarding the program space, therefore, a 64 MB space of contiguous addresses starting from 00000000H unconditionally corresponds to the memory map.

To use the internal RAM area as the program space, access following addresses.

RAM Size	Access Address
6 KB	3FFB000H to 3FFC7FFH
16 KB	3FFB000H to 3FFEFFFH

(2) Data space

With the V850ES/KG2, it seems that there are sixty-four 64 MB address spaces on the 4 GB CPU address space. Therefore, the least significant bit (bit 25) of a 26-bit address is sign-extended to 32 bits and allocated as an address.

(a) Application example of wraparound

If R = r0 (zero register) is specified for the LD/ST disp16 [R] instruction, a range of addresses 00000000H ±32 KB can be addressed by sign-extended disp16. All the resources, including the internal hardware, can be addressed by one pointer.

The zero register (r0) is a register fixed to 0 by hardware, and practically eliminates the need for registers dedicated to pointers.

Example: μPD70F3732

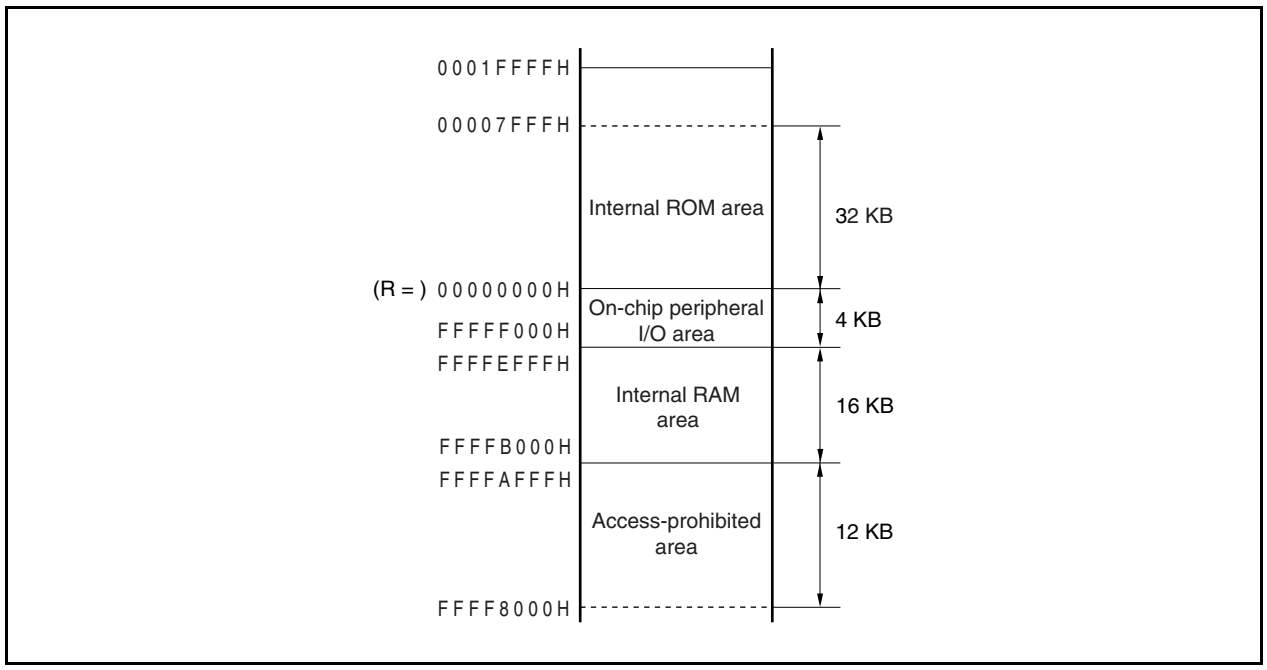
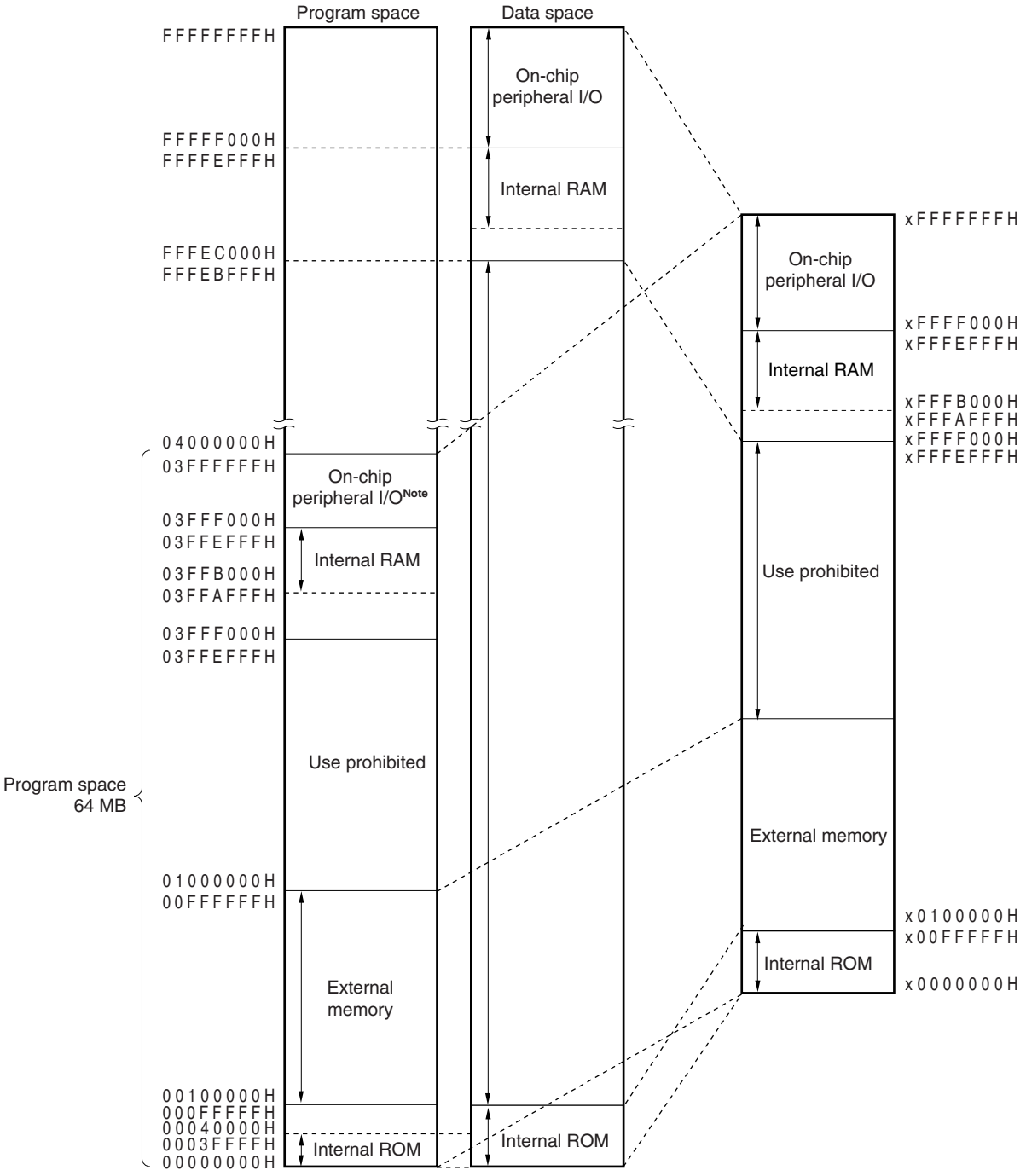


Figure 3-9. Recommended Memory Map



Note Access to this area is prohibited. To access the on-chip peripheral I/O in this area, specify addresses FFFF000H to FFFFFFFH.

Remarks 1. ↕ indicates the recommended area.

2. This figure is the recommended memory map of the μPD70F3732.

3.4.6 Peripheral I/O registers

(1/11)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF004H	Port DL register	PDL	R/W			√	0000H[Note]
FFFFF004H	Port DL register L	PDLL	R/W	√	√		00H[Note]
FFFFF005H	Port DL register H	PDLH	R/W	√	√		00H[Note]
FFFFF006H	Port DH register	PDH	R/W	√	√		00H[Note]
FFFFF008H	Port CS register	PCS	R/W	√	√		00H[Note]
FFFFF00AH	Port CT register	PCT	R/W	√	√		00H[Note]
FFFFF00CH	Port CM register	PCM	R/W	√	√		00H[Note]
FFFFF024H	Port DL mode register	PMDL	R/W			√	FFFFH
FFFFF024H	Port DL mode register L	PMDLL	R/W	√	√		FFH
FFFFF025H	Port DL mode register H	PMDLH	R/W	√	√		FFH
FFFFF026H	Port DH mode register	PMDH	R/W	√	√		FFH
FFFFF028H	Port CS mode register	PMCS	R/W	√	√		FFH
FFFFF02AH	Port CT mode register	PMCT	R/W	√	√		FFH
FFFFF02CH	Port CM mode register	PMCM	R/W	√	√		FFH
FFFFF044H	Port DL mode control register	PMCDL	R/W			√	0000H
FFFFF044H	Port DL mode control register L	PMCDLL	R/W	√	√		00H
FFFFF045H	Port DL mode control register H	PMCDLH	R/W	√	√		00H
FFFFF046H	Port DH mode control register	PMCDH	R/W	√	√		00H
FFFFF048H	Port CS mode control register	PMCCS	R/W	√	√		00H
FFFFF04AH	Port CT mode control register	PMCCT	R/W	√	√		00H
FFFFF04CH	Port CM mode control register	PMCCM	R/W	√	√		00H
FFFFF066H	Bus size configuration register	BSC	R/W			√	5555H
FFFFF06EH	System wait control register	VSWC	R/W	√	√		77H
FFFFF080H	DMA source address register 0L	DSA0L	R/W			√	Undefined
FFFFF082H	DMA source address register 0H	DSA0H	R/W			√	Undefined
FFFFF084H	DMA destination address register 0L	DDA0L	R/W			√	Undefined
FFFFF086H	DMA destination address register 0H	DDA0H	R/W			√	Undefined
FFFFF088H	DMA source address register 1L	DSA1L	R/W			√	Undefined
FFFFF08AH	DMA source address register 1H	DSA1H	R/W			√	Undefined
FFFFF08CH	DMA destination address register 1L	DDA1L	R/W			√	Undefined
FFFFF08EH	DMA destination address register 1H	DDA1H	R/W			√	Undefined
FFFFF090H	DMA source address register 2L	DSA2L	R/W			√	Undefined
FFFFF092H	DMA source address register 2H	DSA2H	R/W			√	Undefined
FFFFF094H	DMA destination address register 2L	DDA2L	R/W			√	Undefined
FFFFF096H	DMA destination address register 2H	DDA2H	R/W			√	Undefined
FFFFF098H	DMA source address register 3L	DSA3L	R/W			√	Undefined
FFFFF09AH	DMA source address register 3H	DSA3H	R/W			√	Undefined
FFFFF09CH	DMA destination address register 3L	DDA3L	R/W			√	Undefined
FFFFF09EH	DMA destination address register 3H	DDA3H	R/W			√	Undefined

Note The output latch is 00H or 0000H. When input, the pin status is read.

(2/11)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF0C0H	DMA byte count register 0	DBC0	R/W			√	Undefined
FFFFF0C2H	DMA byte count register 1	DBC1	R/W			√	Undefined
FFFFF0C4H	DMA byte count register 2	DBC2	R/W			√	Undefined
FFFFF0C6H	DMA byte count register 3	DBC3	R/W			√	Undefined
FFFFF0D0H	DMA addressing control register 0	DADC0	R/W			√	0000H
FFFFF0D2H	DMA addressing control register 1	DADC1	R/W			√	0000H
FFFFF0D4H	DMA addressing control register 2	DADC2	R/W			√	0000H
FFFFF0D6H	DMA addressing control register 3	DADC3	R/W			√	0000H
FFFFF0E0H	DMA channel control register 0	DCHC0	R/W	√	√		00H
FFFFF0E2H	DMA channel control register 1	DCHC1	R/W	√	√		00H
FFFFF0E4H	DMA channel control register 2	DCHC2	R/W	√	√		00H
FFFFF0E6H	DMA channel control register 3	DCHC3	R/W	√	√		00H
FFFFF100H	Interrupt mask register 0	IMR0	R/W			√	FFFFH
FFFFF100H	Interrupt mask register 0L	IMR0L	R/W	√	√		FFH
FFFFF101H	Interrupt mask register 0H	IMR0H	R/W	√	√		FFH
FFFFF102H	Interrupt mask register 1	IMR1	R/W			√	FFFFH
FFFFF102H	Interrupt mask register 1L	IMR1L	R/W	√	√		FFH
FFFFF103H	Interrupt mask register 1H	IMR1H	R/W	√	√		FFH
FFFFF104H	Interrupt mask register 2	IMR2	R/W			√	FFFFH
FFFFF104H	Interrupt mask register 2L	IMR2L	R/W	√	√		FFH
FFFFF105H	Interrupt mask register 2H	IMR2H	R/W	√	√		FFH
FFFFF106H	Interrupt mask register 3	IMR3	R/W			√	FFFFH
FFFFF106H	Interrupt mask register 3L	IMR3L	R/W	√	√		FFH
FFFFF107H	Interrupt mask register 3H	IMR3H	R/W	√	√		FFH
FFFFF110H	Interrupt control register	WDT1IC	R/W	√	√		47H
FFFFF112H	Interrupt control register	PIC0	R/W	√	√		47H
FFFFF114H	Interrupt control register	PIC1	R/W	√	√		47H
FFFFF116H	Interrupt control register	PIC2	R/W	√	√		47H
FFFFF118H	Interrupt control register	PIC3	R/W	√	√		47H
FFFFF11AH	Interrupt control register	PIC4	R/W	√	√		47H
FFFFF11CH	Interrupt control register	PIC5	R/W	√	√		47H
FFFFF11EH	Interrupt control register	PIC6	R/W	√	√		47H
FFFFF120H	Interrupt control register	TM0IC00	R/W	√	√		47H
FFFFF122H	Interrupt control register	TM0IC01	R/W	√	√		47H
FFFFF124H	Interrupt control register	TM0IC10	R/W	√	√		47H
FFFFF126H	Interrupt control register	TM0IC11	R/W	√	√		47H
FFFFF128H	Interrupt control register	TM5IC0	R/W	√	√		47H
FFFFF12AH	Interrupt control register	TM5IC1	R/W	√	√		47H
FFFFF12CH	Interrupt control register	CSI0IC0	R/W	√	√		47H
FFFFF12EH	Interrupt control register	CSI0IC1	R/W	√	√		47H
FFFFF130H	Interrupt control register	SREIC0	R/W	√	√		47H
FFFFF132H	Interrupt control register	SRIC0	R/W	√	√		47H

(3/11)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF134H	Interrupt control register	STIC0	R/W	√	√		47H
FFFFF136H	Interrupt control register	SREIC1	R/W	√	√		47H
FFFFF138H	Interrupt control register	SRIC1	R/W	√	√		47H
FFFFF13AH	Interrupt control register	STIC1	R/W	√	√		47H
FFFFF13CH	Interrupt control register	TMHIC0	R/W	√	√		47H
FFFFF13EH	Interrupt control register	TMHIC1	R/W	√	√		47H
FFFFF140H	Interrupt control register	CSIAIC0	R/W	√	√		47H
FFFFF142H	Interrupt control register	IICIC0	R/W	√	√		47H
FFFFF144H	Interrupt control register	ADIC	R/W	√	√		47H
FFFFF146H	Interrupt control register	KRIC	R/W	√	√		47H
FFFFF148H	Interrupt control register	WTIIC	R/W	√	√		47H
FFFFF14AH	Interrupt control register	WTIC	R/W	√	√		47H
FFFFF14CH	Interrupt control register	BRGIC	R/W	√	√		47H
FFFFF14EH	Interrupt control register	TM0IC20	R/W	√	√		47H
FFFFF150H	Interrupt control register	TM0IC21	R/W	√	√		47H
FFFFF152H	Interrupt control register	TM0IC30	R/W	√	√		47H
FFFFF154H	Interrupt control register	TM0IC31	R/W	√	√		47H
FFFFF156H	Interrupt control register	CSIAIC1	R/W	√	√		47H
FFFFF162H	Interrupt control register	SREIC2	R/W	√	√		47H
FFFFF164H	Interrupt control register	SRIC2	R/W	√	√		47H
FFFFF166H	Interrupt control register	STIC2	R/W	√	√		47H
FFFFF172H	Interrupt control register	PIC7	R/W	√	√		47H
FFFFF174H	Interrupt control register	TP0OVIC	R/W	√	√		47H
FFFFF176H	Interrupt control register	TP0CCIC0	R/W	√	√		47H
FFFFF178H	Interrupt control register	TP0CCIC1	R/W	√	√		47H
FFFFF17AH	Interrupt control register	DMAIC0	R/W	√	√		47H
FFFFF17CH	Interrupt control register	DMAIC1	R/W	√	√		47H
FFFFF17EH	Interrupt control register	DMAIC2	R/W	√	√		47H
FFFFF180H	Interrupt control register	DMAIC3	R/W	√	√		47H
FFFFF1FAH	In-service priority register	ISPR	R	√	√		00H
FFFFF1FCH	Command register	PRCMD	W		√		Undefined
FFFFF1FEH	Power save control register	PSC	R/W	√	√		00H
FFFFF200H	A/D converter mode register	ADM	R/W	√	√		00H
FFFFF201H	Analog input channel specification register	ADS	R/W	√	√		00H
FFFFF202H	Power fail comparison mode register	PFM	R/W	√	√		00H
FFFFF203H	Power fail comparison threshold register	PFT	R/W		√		00H
FFFFF204H	A/D conversion result register	ADCR	R			√	Undefined
FFFFF205H	A/D conversion result register H	ADCRH	R		√		Undefined
FFFFF280H	D/A conversion value setting register 0	DACS0	R/W		√		00H
FFFFF282H	D/A conversion value setting register 1	DACS1	R/W		√		00H
FFFFF284H	D/A converter mode register	DAM	R/W	√	√		00H

(4/11)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF300H	Key return mode register	KRM	R/W	√	√		00H
FFFFF30AH	Selector operation control register 1	SELCNT1	R/W	√	√		00H
FFFFF318H	Digital noise elimination control register	NFC	R/W	√	√		00H
FFFFF400H	Port 0 register	P0	R/W	√	√		00H[Note]
FFFFF402H	Port 1 register	P1	R/W	√	√		00H[Note]
FFFFF406H	Port 3 register	P3	R/W			√	0000H[Note]
FFFFF406H	Port 3 register L	P3L	R/W	√	√		00H[Note]
FFFFF407H	Port 3 register H	P3H	R/W	√	√		00H[Note]
FFFFF408H	Port 4 register	P4	R/W	√	√		00H[Note]
FFFFF40AH	Port 5 register	P5	R/W	√	√		00H[Note]
FFFFF40EH	Port 7 register	P7	R		√		Undefined
FFFFF412H	Port 9 register	P9	R/W			√	0000H[Note]
FFFFF412H	Port 9 register L	P9L	R/W	√	√		00H[Note]
FFFFF413H	Port 9 register H	P9H	R/W	√	√		00H[Note]
FFFFF420H	Port 0 mode register	PM0	R/W	√	√		FFH
FFFFF422H	Port 1 mode register	PM1	R/W	√	√		FFH
FFFFF426H	Port 3 mode register	PM3	R/W			√	FFFFH
FFFFF426H	Port 3 mode register L	PM3L	R/W	√	√		FFH
FFFFF427H	Port 3 mode register H	PM3H	R/W	√	√		FFH
FFFFF428H	Port 4 mode register	PM4	R/W	√	√		FFH
FFFFF42AH	Port 5 mode register	PM5	R/W	√	√		FFH
FFFFF432H	Port 9 mode register	PM9	R/W			√	FFFFH
FFFFF432H	Port 9 mode register L	PM9L	R/W	√	√		FFH
FFFFF433H	Port 9 mode register H	PM9H	R/W	√	√		FFH
FFFFF440H	Port 0 mode control register	PMC0	R/W	√	√		00H
FFFFF446H	Port 3 mode control register	PMC3	R/W			√	0000H
FFFFF446H	Port 3 mode control register L	PMC3L	R/W	√	√		00H
FFFFF447H	Port 3 mode control register H	PMC3H	R/W	√	√		00H
FFFFF448H	Port 4 mode control register	PMC4	R/W	√	√		00H
FFFFF44AH	Port 5 mode control register	PMC5	R/W	√	√		00H
FFFFF452H	Port 9 mode control register	PMC9	R/W			√	0000H
FFFFF452H	Port 9 mode control register L	PMC9L	R/W	√	√		00H
FFFFF453H	Port 9 mode control register H	PMC9H	R/W	√	√		00H
FFFFF466H	Port 3 function control register	PFC3	R/W	√	√		00H
FFFFF468H	Port 4 function control register	PFC4	R/W	√	√		00H
FFFFF46AH	Port 5 function control register	PFC5	R/W	√	√		00H
FFFFF472H	Port 9 function control register	PFC9	R/W			√	0000H
FFFFF472H	Port 9 function control register L	PFC9L	R/W	√	√		00H
FFFFF473H	Port 9 function control register H	PFC9H	R/W	√	√		00H
FFFFF484H	Data wait control register 0	DWC0	R/W			√	7777H
FFFFF488H	Address wait control register	AWC	R/W			√	FFFFH

Note The output latch is 00H or 0000H. When input, the pin status is read.

(5/11)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF48AH	Bus cycle control register	BCC	R/W			√	AAAAH
FFFFF580H	8-bit timer H mode register 0	TMHMD0	R/W	√	√		00H
FFFFF581H	8-bit timer H carrier control register 0	TMCYC0	R/W	√	√		00H
FFFFF582H	8-bit timer H compare register 00	CMP00	R/W		√		00H
FFFFF583H	8-bit timer H compare register 01	CMP01	R/W		√		00H
FFFFF590H	8-bit timer H mode register 1	TMHMD1	R/W	√	√		00H
FFFFF591H	8-bit timer H carrier control register 1	TMCYC1	R/W	√	√		00H
FFFFF592H	8-bit timer H compare register 10	CMP10	R/W		√		00H
FFFFF593H	8-bit timer H compare register 11	CMP11	R/W		√		00H
FFFFF5A0H	TMP0 control register 0	TP0CTL0	R/W	√	√		00H
FFFFF5A1H	TMP0 control register 1	TP0CTL1	R/W	√	√		00H
FFFFF5A2H	TMP0 I/O control register 0	TP0IOC0	R/W	√	√		00H
FFFFF5A3H	TMP0 I/O control register 1	TP0IOC1	R/W	√	√		00H
FFFFF5A4H	TMP0 I/O control register 2	TP0IOC2	R/W	√	√		00H
FFFFF5A5H	TMP0 option register 0	TP0OPT0	R/W	√	√		00H
FFFFF5A6H	TMP0 capture/compare register 0	TP0CCR0	R/W			√	0000H
FFFFF5A8H	TMP0 capture/compare register 1	TP0CCR1	R/W			√	0000H
FFFFF5AAH	TMP0 counter read buffer register	TP0CNT	R			√	0000H
FFFFF5C0H	16-bit timer counter 5	TM5	R			√	0000H
FFFFF5C0H	8-bit timer counter 50	TM50	R		√		00H
FFFFF5C1H	8-bit timer counter 51	TM51	R		√		00H
FFFFF5C2H	16-bit timer compare register 5	CR5	R/W			√	0000H
FFFFF5C2H	8-bit timer compare register 50	CR50	R/W		√		00H
FFFFF5C3H	8-bit timer compare register 51	CR51	R/W		√		00H
FFFFF5C4H	Timer clock selection register 5	TCL5	R/W			√	0000H
FFFFF5C4H	Timer clock selection register 50	TCL50	R/W		√		00H
FFFFF5C5H	Timer clock selection register 51	TCL51	R/W		√		00H
FFFFF5C6H	16-bit timer mode control register 5	TMC5	R/W			√	0000H
FFFFF5C6H	8-bit timer mode control register 50	TMC50	R/W	√	√		00H
FFFFF5C7H	8-bit timer mode control register 51	TMC51	R/W	√	√		00H
FFFFF600H	16-bit timer counter 00	TM00	R			√	0000H
FFFFF602H	16-bit timer capture/compare register 000	CR000	R/W			√	0000H
FFFFF604H	16-bit timer capture/compare register 001	CR001	R/W			√	0000H
FFFFF606H	16-bit timer mode control register 00	TMC00	R/W	√	√		00H
FFFFF607H	Prescaler mode register 00	PRM00	R/W	√	√		00H
FFFFF608H	Capture/compare control register 00	CRC00	R/W	√	√		00H
FFFFF609H	16-bit timer output control register 00	TOC00	R/W	√	√		00H
FFFFF610H	16-bit timer counter 01	TM01	R			√	0000H
FFFFF612H	16-bit timer capture/compare register 010	CR010	R/W			√	0000H
FFFFF614H	16-bit timer capture/compare register 011	CR011	R/W			√	0000H
FFFFF616H	16-bit timer mode control register 01	TMC01	R/W	√	√		00H
FFFFF617H	Prescaler mode register 01	PRM01	R/W	√	√		00H
FFFFF618H	Capture/compare control register 01	CRC01	R/W	√	√		00H

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF619H	16-bit timer output control register 01	TOC01	R/W	√	√		00H
FFFFF620H	16-bit timer counter 02	TM02	R			√	0000H
FFFFF622H	16-bit timer capture/compare register 020	CR020	R/W			√	0000H
FFFFF624H	16-bit timer capture/compare register 021	CR021	R/W			√	0000H
FFFFF626H	16-bit timer mode control register 02	TMC02	R/W	√	√		00H
FFFFF627H	Prescaler mode register 02	PRM02	R/W	√	√		00H
FFFFF628H	Capture/compare control register 02	CRC02	R/W	√	√		00H
FFFFF629H	16-bit timer output control register 02	TOC02	R/W	√	√		00H
FFFFF630H	16-bit timer counter 03	TM03	R			√	0000H
FFFFF632H	16-bit timer capture/compare register 030	CR030	R/W			√	0000H
FFFFF634H	16-bit timer capture/compare register 031	CR031	R/W			√	0000H
FFFFF636H	16-bit timer mode control register 03	TMC03	R/W	√	√		00H
FFFFF637H	Prescaler mode register 03	PRM03	R/W	√	√		00H
FFFFF638H	Capture/compare control register 03	CRC03	R/W	√	√		00H
FFFFF639H	16-bit timer output control register 03	TOC03	R/W	√	√		00H
FFFFF680H	Watch timer operation mode register	WTM	R/W	√	√		00H
FFFFF6C0H	Oscillation stabilization time selection register	OSTS	R/W		√		01H
FFFFF6C1H	Watchdog timer clock selection register	WDCS	R/W		√		00H
FFFFF6C2H	Watchdog timer mode register 1	WDTM1	R/W	√	√		00H
FFFFF6D0H	Watchdog timer mode register 2	WDTM2	R/W		√		67H
FFFFF6D1H	Watchdog timer enable register	WDTE	R/W		√		9AH
FFFFF6E0H	Real-time output buffer register L0	RTBL0	R/W	√	√		00H
FFFFF6E2H	Real-time output buffer register H0	RTBH0	R/W	√	√		00H
FFFFF6E4H	Real-time output port mode register 0	RTPM0	R/W	√	√		00H
FFFFF6E5H	Real-time output port control register 0	RTPC0	R/W	√	√		00H
FFFFF706H	Port 3 function control expansion register	PFCE3	R/W	√	√		00H
FFFFF802H	System status register	SYS	R/W	√	√		00H
FFFFF806H	PLL control register	PLLCTL	R/W	√	√		01H
FFFFF810H	DMA trigger factor register 0	DTFR0	R/W	√	√		00H
FFFFF812H	DMA trigger factor register 1	DTFR1	R/W	√	√		00H
FFFFF814H	DMA trigger factor register 2	DTFR2	R/W	√	√		00H
FFFFF816H	DMA trigger factor register 3	DTFR3	R/W	√	√		00H
FFFFF820H	Power save mode register	PSMR	R/W	√	√		00H
FFFFF828H	Processor clock control register	PCC	R/W	√	√		03H
FFFFF8B0H	Interval timer BRG mode register	PRSM	R/W		√		00H
FFFFF8B1H	Interval timer BRG compare register	PRSCM	R/W		√		00H
FFFFFA00H	Asynchronous serial interface mode register 0	ASIM0	R/W	√	√		01H
FFFFFA02H	Receive buffer register 0	RXB0	R		√		FFH
FFFFFA03H	Asynchronous serial interface status register 0	ASIS0	R		√		00H
FFFFFA04H	Transmit buffer register 0	TXB0	R/W		√		FFH
FFFFFA05H	Asynchronous serial interface transmit status register 0	ASIF0	R	√	√		00H
FFFFFA06H	Clock select register 0	CKSR0	R/W		√		00H

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFA07H	Baud rate generator control register 0	BRGC0	R/W		√		FFH
FFFFFA10H	Asynchronous serial interface mode register 1	ASIM1	R/W	√	√		01H
FFFFFA12H	Receive buffer register 1	RXB1	R		√		FFH
FFFFFA13H	Asynchronous serial interface status register 1	ASIS1	R		√		00H
FFFFFA14H	Transmit buffer register 1	TXB1	R/W		√		FFH
FFFFFA15H	Asynchronous serial interface transmit status register 1	ASIF1	R	√	√		00H
FFFFFA16H	Clock select register 1	CKSR1	R/W		√		00H
FFFFFA17H	Baud rate generator control register 1	BRGC1	R/W		√		FFH
FFFFFA20H	Asynchronous serial interface mode register 2	ASIM2	R/W	√	√		01H
FFFFFA22H	Receive buffer register 2	RXB2	R		√		FFH
FFFFFA23H	Asynchronous serial interface status register 2	ASIS2	R		√		00H
FFFFFA24H	Transmit buffer register 2	TXB2	R/W		√		FFH
FFFFFA25H	Asynchronous serial interface transmit status register 2	ASIF2	R	√	√		00H
FFFFFA26H	Clock select register 2	CKSR2	R/W		√		00H
FFFFFA27H	Baud rate generator control register 2	BRGC2	R/W		√		FFH
FFFFFB00H	TIP00 noise elimination control register	P0NFC	R/W	√	√		00H
FFFFFB04H	TIP01 noise elimination control register	P1NFC	R/W	√	√		00H
FFFFFC00H	External interrupt falling edge specification register 0	INTF0	R/W	√	√		00H
FFFFFC06H	External interrupt falling edge specification register 3	INTF3	R/W	√	√		00H
FFFFFC13H	External interrupt falling edge specification register 9H	INTF9H	R/W	√	√		00H
FFFFFC20H	External interrupt rising edge specification register 0	INTR0	R/W	√	√		00H
FFFFFC26H	External interrupt rising edge specification register 3	INTR3	R/W	√	√		00H
FFFFFC33H	External interrupt rising edge specification register 9H	INTR9H	R/W	√	√		00H
FFFFFC40H	Pull-up resistor option register 0	PU0	R/W	√	√		00H
FFFFFC42H	Pull-up resistor option register 1	PU1	R/W	√	√		00H
FFFFFC46H	Pull-up resistor option register 3	PU3	R/W	√	√		00H
FFFFFC48H	Pull-up resistor option register 4	PU4	R/W	√	√		00H
FFFFFC4AH	Pull-up resistor option register 5	PU5	R/W	√	√		00H
FFFFFC52H	Pull-up resistor option register 9	PU9	R/W			√	0000H
FFFFFC52H	Pull-up resistor option register 9L	PU9L	R/W	√	√		00H
FFFFFC53H	Pull-up resistor option register 9H	PU9H	R/W	√	√		00H
FFFFFC67H	Port 3 function register H	PF3H	R/W	√	√		00H
FFFFFC68H	Port 4 function register	PF4	R/W	√	√		00H
FFFFFC6AH	Port 5 function register	PF5	R/W	√	√		00H
FFFFFC73H	Port 9 function register H	PF9H	R/W	√	√		00H
FFFFFD00H	Clocked serial interface mode register 00	CSIM00	R/W	√	√		00H
FFFFFD01H	Clocked serial interface clock selection register 0	CSIC0	R/W	√	√		00H
FFFFFD02H	Clocked serial interface receive buffer register 0	SIRB0	R			√	0000H
FFFFFD02H	Clocked serial interface receive buffer register 0L	SIRB0L	R		√		00H
FFFFFD04H	Clocked serial interface transmit buffer register 0	SOTB0	R/W			√	0000H
FFFFFD04H	Clocked serial interface transmit buffer register 0L	SOTB0L	R/W		√		00H
FFFFFD06H	Clocked serial interface read-only receive buffer register 0	SIRBE0	R			√	0000H
FFFFFD06H	Clocked serial interface read-only receive buffer register 0L	SIRBE0L	R		√		00H

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFD08H	Clocked serial interface initial transmit buffer register 0	SOTBF0	R/W			√	0000H
FFFFFD08H	Clocked serial interface initial transmit buffer register 0L	SOTBF0L	R/W		√		00H
FFFFFD0AH	Serial I/O shift register 0	SIO00	R/W			√	00H
FFFFFD0AH	Serial I/O shift register 0L	SIO00L	R/W		√		0000H
FFFFFD10H	Clocked serial interface mode register 01	CSIM01	R/W	√	√		00H
FFFFFD11H	Clocked serial interface clock selection register 1	CSIC1	R/W	√	√		00H
FFFFFD12H	Clocked serial interface receive buffer register 1	SIRB1	R			√	0000H
FFFFFD12H	Clocked serial interface receive buffer register 1L	SIRB1L	R		√		00H
FFFFFD14H	Clocked serial interface transmit buffer register 1	SOTB1	R/W			√	0000H
FFFFFD14H	Clocked serial interface transmit buffer register 1L	SOTB1L	R/W		√		00H
FFFFFD16H	Clocked serial interface read-only receive buffer register 1	SIRBE1	R			√	0000H
FFFFFD16H	Clocked serial interface read-only receive buffer register 1L	SIRBE1L	R		√		00H
FFFFFD18H	Clocked serial interface initial transmit buffer register 1	SOTBF1	R/W			√	0000H
FFFFFD18H	Clocked serial interface initial transmit buffer register 1L	SOTBF1L	R/W		√		00H
FFFFFD1AH	Serial I/O shift register 1	SIO01	R/W			√	00H
FFFFFD1AH	Serial I/O shift register 1L	SIO01L	R/W		√		0000H
FFFFFD40H	Serial operation mode specification register 0	CSIMA0	R/W	√	√		00H
FFFFFD41H	Serial status register 0	CSIS0	R/W	√	√		00H
FFFFFD42H	Serial trigger register 0	CSIT0	R/W	√	√		00H
FFFFFD43H	Divisor selection register 0	BRGCA0	R/W		√		03H
FFFFFD44H	Automatic data transfer address point specification register 0	ADTP0	R/W		√		00H
FFFFFD45H	Automatic data transfer interval specification register 0	ADTI0	R/W	√	√		00H
FFFFFD46H	Serial I/O shift register A0	SIOA0	R/W		√		00H
FFFFFD47H	Automatic data transfer address count register 0	ADTC0	R		√		00H
FFFFFD50H	Serial operation mode specification register 1	CSIMA1	R/W	√	√		00H
FFFFFD51H	Serial status register 1	CSIS1	R/W	√	√		00H
FFFFFD52H	Serial trigger register 1	CSIT1	R/W	√	√		00H
FFFFFD53H	Divisor selection register 1	BRGCA1	R/W		√		03H
FFFFFD54H	Automatic data transfer address point specification register 1	ADTP1	R/W		√		00H
FFFFFD55H	Automatic data transfer interval specification register 1	ADTI1	R/W	√	√		00H
FFFFFD56H	Serial I/O shift register A1	SIOA1	R/W		√		00H
FFFFFD57H	Automatic data transfer address count register 1	ADTC1	R		√		00H
FFFFFD80H	IIC shift register 0	IIC0	R/W		√		00H
FFFFFD82H	IIC control register 0	IICC0	R/W	√	√		00H
FFFFFD83H	Slave address register 0	SVA0	R/W		√		00H
FFFFFD84H	IIC clock selection register 0	IICCL0	R/W	√	√		00H
FFFFFD85H	IIC function expansion register 0	IICX0	R/W	√	√		00H
FFFFFD86H	IIC status register 0	IICS0	R	√	√		00H
FFFFFD8AH	IIC flag register 0	IICF0	R/W	√	√		00H
FFFFFE00H	CSIA0 buffer RAM 0	CSIA0B0	R/W			√	Undefined
FFFFFE00H	CSIA0 buffer RAM 0L	CSIA0B0L	R/W		√		Undefined
FFFFFE01H	CSIA0 buffer RAM 0H	CSIA0B0H	R/W		√		Undefined

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFE02H	CSIA0 buffer RAM 1	CSIA0B1	R/W			√	Undefined
FFFFFE02H	CSIA0 buffer RAM 1L	CSIA0B1L	R/W		√		Undefined
FFFFFE03H	CSIA0 buffer RAM 1H	CSIA0B1H	R/W		√		Undefined
FFFFFE04H	CSIA0 buffer RAM 2	CSIA0B2	R/W			√	Undefined
FFFFFE04H	CSIA0 buffer RAM 2L	CSIA0B2L	R/W		√		Undefined
FFFFFE05H	CSIA0 buffer RAM 2H	CSIA0B2H	R/W		√		Undefined
FFFFFE06H	CSIA0 buffer RAM 3	CSIA0B3	R/W			√	Undefined
FFFFFE06H	CSIA0 buffer RAM 3L	CSIA0B3L	R/W		√		Undefined
FFFFFE07H	CSIA0 buffer RAM 3H	CSIA0B3H	R/W		√		Undefined
FFFFFE08H	CSIA0 buffer RAM 4	CSIA0B4	R/W			√	Undefined
FFFFFE08H	CSIA0 buffer RAM 4L	CSIA0B4L	R/W		√		Undefined
FFFFFE09H	CSIA0 buffer RAM 4H	CSIA0B4H	R/W		√		Undefined
FFFFFE0AH	CSIA0 buffer RAM 5	CSIA0B5	R/W			√	Undefined
FFFFFE0AH	CSIA0 buffer RAM 5L	CSIA0B5L	R/W		√		Undefined
FFFFFE0BH	CSIA0 buffer RAM 5H	CSIA0B5H	R/W		√		Undefined
FFFFFE0CH	CSIA0 buffer RAM 6	CSIA0B6	R/W			√	Undefined
FFFFFE0CH	CSIA0 buffer RAM 6L	CSIA0B6L	R/W		√		Undefined
FFFFFE0DH	CSIA0 buffer RAM 6H	CSIA0B6H	R/W		√		Undefined
FFFFFE0EH	CSIA0 buffer RAM 7	CSIA0B7	R/W			√	Undefined
FFFFFE0EH	CSIA0 buffer RAM 7L	CSIA0B7L	R/W		√		Undefined
FFFFFE0FH	CSIA0 buffer RAM 7H	CSIA0B7H	R/W		√		Undefined
FFFFFE10H	CSIA0 buffer RAM 8	CSIA0B8	R/W			√	Undefined
FFFFFE10H	CSIA0 buffer RAM 8L	CSIA0B8L	R/W		√		Undefined
FFFFFE11H	CSIA0 buffer RAM 8H	CSIA0B8H	R/W		√		Undefined
FFFFFE12H	CSIA0 buffer RAM 9	CSIA0B9	R/W			√	Undefined
FFFFFE12H	CSIA0 buffer RAM 9L	CSIA0B9L	R/W		√		Undefined
FFFFFE13H	CSIA0 buffer RAM 9H	CSIA0B9H	R/W		√		Undefined
FFFFFE14H	CSIA0 buffer RAM A	CSIA0BA	R/W			√	Undefined
FFFFFE14H	CSIA0 buffer RAM AL	CSIA0BAL	R/W		√		Undefined
FFFFFE15H	CSIA0 buffer RAM AH	CSIA0BAH	R/W		√		Undefined
FFFFFE16H	CSIA0 buffer RAM B	CSIA0BB	R/W			√	Undefined
FFFFFE16H	CSIA0 buffer RAM BL	CSIA0BBL	R/W		√		Undefined
FFFFFE17H	CSIA0 buffer RAM BH	CSIA0BBH	R/W		√		Undefined
FFFFFE18H	CSIA0 buffer RAM C	CSIA0BC	R/W			√	Undefined
FFFFFE18H	CSIA0 buffer RAM CL	CSIA0BCL	R/W		√		Undefined
FFFFFE19H	CSIA0 buffer RAM CH	CSIA0BCH	R/W		√		Undefined
FFFFFE1AH	CSIA0 buffer RAM D	CSIA0BD	R/W			√	Undefined
FFFFFE1AH	CSIA0 buffer RAM DL	CSIA0BDL	R/W		√		Undefined
FFFFFE1BH	CSIA0 buffer RAM DH	CSIA0BDH	R/W		√		Undefined
FFFFFE1CH	CSIA0 buffer RAM E	CSIA0BE	R/W			√	Undefined
FFFFFE1CH	CSIA0 buffer RAM EL	CSIA0BEL	R/W		√		Undefined
FFFFFE1DH	CSIA0 buffer RAM EH	CSIA0BEH	R/W		√		Undefined

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFE1EH	CSIA0 buffer RAM F	CSIA0BF	R/W			√	Undefined
FFFFFE1EH	CSIA0 buffer RAM FL	CSIA0BFL	R/W		√		Undefined
FFFFFE1FH	CSIA0 buffer RAM FH	CSIA0BFH	R/W		√		Undefined
FFFFFE20H	CSIA1 buffer RAM 0	CSIA1B0	R/W			√	Undefined
FFFFFE20H	CSIA1 buffer RAM 0L	CSIA1B0L	R/W		√		Undefined
FFFFFE21H	CSIA1 buffer RAM 0H	CSIA1B0H	R/W		√		Undefined
FFFFFE22H	CSIA1 buffer RAM 1	CSIA1B1	R/W			√	Undefined
FFFFFE22H	CSIA1 buffer RAM 1L	CSIA1B1L	R/W		√		Undefined
FFFFFE23H	CSIA1 buffer RAM 1H	CSIA1B1H	R/W		√		Undefined
FFFFFE24H	CSIA1 buffer RAM 2	CSIA1B2	R/W			√	Undefined
FFFFFE24H	CSIA1 buffer RAM 2L	CSIA1B2L	R/W		√		Undefined
FFFFFE25H	CSIA1 buffer RAM 2H	CSIA1B2H	R/W		√		Undefined
FFFFFE26H	CSIA1 buffer RAM 3	CSIA1B3	R/W			√	Undefined
FFFFFE26H	CSIA1 buffer RAM 3L	CSIA1B3L	R/W		√		Undefined
FFFFFE27H	CSIA1 buffer RAM 3H	CSIA1B3H	R/W		√		Undefined
FFFFFE28H	CSIA1 buffer RAM 4	CSIA1B4	R/W			√	Undefined
FFFFFE28H	CSIA1 buffer RAM 4L	CSIA1B4L	R/W		√		Undefined
FFFFFE29H	CSIA1 buffer RAM 4H	CSIA1B4H	R/W		√		Undefined
FFFFFE2AH	CSIA1 buffer RAM 5	CSIA1B5	R/W			√	Undefined
FFFFFE2AH	CSIA1 buffer RAM 5L	CSIA1B5L	R/W		√		Undefined
FFFFFE2BH	CSIA1 buffer RAM 5H	CSIA1B5H	R/W		√		Undefined
FFFFFE2CH	CSIA1 buffer RAM 6	CSIA1B6	R/W			√	Undefined
FFFFFE2CH	CSIA1 buffer RAM 6L	CSIA1B6L	R/W		√		Undefined
FFFFFE2DH	CSIA1 buffer RAM 6H	CSIA1B6H	R/W		√		Undefined
FFFFFE2EH	CSIA1 buffer RAM 7	CSIA1B7	R/W			√	Undefined
FFFFFE2EH	CSIA1 buffer RAM 7L	CSIA1B7L	R/W		√		Undefined
FFFFFE2FH	CSIA1 buffer RAM 7H	CSIA1B7H	R/W		√		Undefined
FFFFFE30H	CSIA1 buffer RAM 8	CSIA1B8	R/W			√	Undefined
FFFFFE30H	CSIA1 buffer RAM 8L	CSIA1B8L	R/W		√		Undefined
FFFFFE31H	CSIA1 buffer RAM 8H	CSIA1B8H	R/W		√		Undefined
FFFFFE32H	CSIA1 buffer RAM 9	CSIA1B9	R/W			√	Undefined
FFFFFE32H	CSIA1 buffer RAM 9L	CSIA1B9L	R/W		√		Undefined
FFFFFE33H	CSIA1 buffer RAM 9H	CSIA1B9H	R/W		√		Undefined
FFFFFE34H	CSIA1 buffer RAM A	CSIA1BA	R/W			√	Undefined
FFFFFE34H	CSIA1 buffer RAM AL	CSIA1BAL	R/W		√		Undefined
FFFFFE35H	CSIA1 buffer RAM AH	CSIA1BAH	R/W		√		Undefined
FFFFFE36H	CSIA1 buffer RAM B	CSIA1BB	R/W			√	Undefined
FFFFFE36H	CSIA1 buffer RAM BL	CSIA1BBL	R/W		√		Undefined
FFFFFE37H	CSIA1 buffer RAM BH	CSIA1BBH	R/W		√		Undefined
FFFFFE38H	CSIA1 buffer RAM C	CSIA1BC	R/W			√	Undefined
FFFFFE38H	CSIA1 buffer RAM CL	CSIA1BCL	R/W		√		Undefined
FFFFFE39H	CSIA1 buffer RAM CH	CSIA1BCH	R/W		√		Undefined

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFE3AH	CSIA1 buffer RAM D	CSIA1BD	R/W			√	Undefined
FFFFFE3AH	CSIA1 buffer RAM DL	CSIA1BDL	R/W		√		Undefined
FFFFFE3BH	CSIA1 buffer RAM DH	CSIA1BDH	R/W		√		Undefined
FFFFFE3CH	CSIA1 buffer RAM E	CSIA1BE	R/W			√	Undefined
FFFFFE3CH	CSIA1 buffer RAM EL	CSIA1BEL	R/W		√		Undefined
FFFFFE3DH	CSIA1 buffer RAM EH	CSIA1BEH	R/W		√		Undefined
FFFFFE3EH	CSIA1 buffer RAM F	CSIA1BF	R/W			√	Undefined
FFFFFE3EH	CSIA1 buffer RAM FL	CSIA1BFL	R/W		√		Undefined
FFFFFE3FH	CSIA1 buffer RAM FH	CSIA1BFH	R/W		√		Undefined
FFFFFF44H	Pull-up resistor option register DL	PUDL	R/W			√	0000H
FFFFFF44H	Pull-up resistor option register DLL	PUDLL	R/W	√	√		00H
FFFFFF45H	Pull-up resistor option register DLH	PUDLH	R/W	√	√		00H
FFFFFF46H	Pull-up resistor option register DH	PUDH	R/W	√	√		00H
FFFFFF48H	Pull-up resistor option register CS	PUCS	R/W	√	√		00H
FFFFFF4AH	Pull-up resistor option register CT	PUCT	R/W	√	√		00H
FFFFFF4CH	Pull-up resistor option register CM	PUCM	R/W	√	√		00H
FFFFFFBEH	External bus interface mode control register	EXIMC	R/W	√	√		00H

3.4.7 Special registers

Special registers are registers that prevent invalid data from being written when an inadvertent program loop occurs. The V850ES/KG2 has the following three special registers.

- Power save control register (PSC)
- Processor clock control register (PCC)
- Watchdog timer mode register (WDTM1)

Moreover, there is also the PRCMD register, which is a protection register for write operations to the special registers that prevents the application system from unexpectedly stopping due to an inadvertent program loop. Write access to the special registers is performed with a special sequence and illegal store operations are notified to the SYS register.

(1) Setting data to special registers

Setting data to a special register is done in the following sequence.

<1> Disable the DMA operation.
<2> Prepare the data to be set to the special register in a general-purpose register.
<3> Write the data prepared in step <2> to the PRCMD register.
<4> Write the setting data to the special register (using following instructions).
- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<5> to <9> Insert NOP instructions (5 instructions)[Note].
<10> Enable the DMA operation if DMA is necessary.

Note When switching to the IDLE mode or the STOP mode (PSC.STP bit = 1), 5 NOP instructions must be inserted immediately after switching is performed.

Caution To resume the DMA operation in the status before the DMA operation is disabled after a special sequence, the DCHCn register status must be stored before the DMA operation is disabled.
After the DCHCn register status is stored, the DCHCn.TCn bit must be checked before the DMA operation is resumed and the following processing must be executed according to the TCn bit status because the DMA transfer completion may occur before the DMA operation is disabled.

- **When the TCn bit is 0 (DMA transfer not completed), the contents of the DCHCn register stored before the DMA operation is disabled are written to the DCHCn register again.**
- **When the TCn bit is 1 (DMA transfer completed), the DMA transfer completion processing is executed.**

Remark n = 0 to 3

[Description Example] When using PSC register (standby mode setting)

```
     ST.B r11, PSMR[r0]   ; PSMR register setting (IDLE, STOP mode setting)
     LD.B DCHCn[r0], r12  ; (a) DMA transfer status stored
     ANDI 0xfe, r12, r13
<1>  ST.B r13, DCHCn[r0]  ; (b) DMA operation stopped Note 1
<2>  MOV 0x02, r10
<3>  ST.B r10, PRCMD[r0]  ; PRCMD register write
<4>  ST.B r10, PSC[r0]    ; PSC register setting
<5>  NOP Note 2           ; Dummy instruction
<6>  NOP Note 2           ; Dummy instruction
<7>  NOP Note 2           ; Dummy instruction
<8>  NOP Note 2           ; Dummy instruction
<9>  NOP Note 2           ; Dummy instruction
     TST1 7, DCHCn[r0]    ; Check whether DMA transfer is completed or not between (a) and (b)
                          ; (whether the DCHCn register status is updated or not)
     BNE next             ; If updated, DMA transfer completion processing (to next routine)
<10> ST.B r12, DCHCn[r0]  ; If not updated, return to the status of (a) (DMA transfer enable)
     (next instruction)
```

No special sequence is required to read special registers.

Notes 1. A bit manipulation instruction is not used so as to prevent the DMA transfer completion status flag (DCHCn.TCn bit) from being cleared to 0 via reading. The TCn bit cannot be cleared to 0 by writing 0.

2. When switching to the IDLE mode or the STOP mode (PSC.STP bit = 1), 5 NOP instructions must be inserted immediately after switching is performed.

Remark n = 0 to 3

Cautions 1. Interrupts are not acknowledged for the store instruction for the PRCMD register. This is because continuous execution of store instructions by the program in steps <3> and <4> above is assumed. If another instruction is placed between step <3> and <4>, the above sequence may not be realized when an interrupt is acknowledged for that instruction, which may cause malfunction.

2. The data written to the PRCMD register is dummy data, but use the same register as the general-purpose register used for setting data to the special register (step <4>) when writing to the PRCMD register (step <3>). The same applies to when using a general-purpose register for addressing.

(2) Command register (PRCMD)

The PRCMD register is an 8-bit register used to prevent data from being written to registers that may have a large influence on the system, possibly causing the application system to unexpectedly stop, when an inadvertent program loop occurs. Only the first write operation to the special register following the execution of a previously executed write operation to the PRCMD register, is valid.

As a result, register values can be overwritten only using a preset sequence, preventing invalid write operations.

This register can only be written in 8-bit units (if it is read, an undefined value is returned).

After reset: Undefined W Address: FFFFF1FCH

	7	6	5	4	3	2	1	0
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

(3) System status register (SYS)

This register is allocated with status flags showing the operating state of the entire system.

This register can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF802H

	7	6	5	4	3	2	1	<0>
SYS	0	0	0	0	0	0	0	PRERR

PRERR	Detection of protection error
0	Protection error has not occurred
1	Protection error has occurred

The operation conditions of the PRERR flag are described below.

(a) Set conditions (PRERR = 1)

(i) When a write operation to the special register takes place without write operation being performed to the PRCMD register (when step <3> is performed without performing step <2> as described in **3.4.7 (1) Setting data to special registers**).

(ii) When a write operation (including bit manipulation instruction) to an on-chip peripheral I/O register other than a special register is performed following write to the PRCMD register (when <3> in **3.4.7 (1) Setting data to special registers** is not a special register).

Remark Regarding the special registers other than the WDTM register (PCC and PSC registers), even if on-chip peripheral I/O register read (except bit manipulation instruction) (internal RAM access, etc.) is performed in between write to the PRCMD register and write to a special register, the PRERR flag is not set and setting data can be written to the special register.

(b) Clear conditions (PRERR = 0)

(i) When 0 is written to the PRERR flag

(ii) When system reset is performed

Cautions 1. If 0 is written to the PRERR bit of the SYS register that is not a special register immediately following write to the PRCMD register, the PRERR bit becomes 0 (write priority).

2. If data is written to the PRCMD register that is not a special register immediately following write to the PRCMD register, the PRERR bit becomes 1.

3.4.8 Cautions

(1) Waits on register access

Be sure to set the following register before using the V850ES/KG2.

- System wait control register (VSWC)

After setting the VSWC register, set the other registers as required.

When using an external bus, set the VSWC register and then set the various pins to the control mode by setting the port-related registers.

(a) System wait control register (VSWC)

The VSWC register controls the bus access wait time for the on-chip peripheral I/O registers.

Access to the on-chip peripheral I/O register lasts 3 clocks (during no wait), but in the V850ES/KG2, waits are required according to the internal system clock frequency. Set the values shown below to the VSWC register according to the internal system clock frequency that is used.

This register can be read or written in 8-bit units (Address: FFFFF06EH, After reset: 77H).

Operation Conditions	Internal System Clock Frequency (f_{CLK})	VSWC Register Setting	Number of Waits
4.5 V ≤ REGC = V_{DD} ≤ 5.5 V	32 kHz ≤ f_{CLK} < 16.6 MHz	00H	0 (no waits)
	16.6 MHz ≤ f_{CLK} ≤ 20 MHz	01H	1
4.0 V ≤ REGC = V_{DD} < 4.5 V	32 kHz ≤ f_{CLK} ≤ 16 MHz	00H	0 (no waits)
REGC = 10 μF, 4.0 V ≤ V_{DD} ≤ 5.5 V	32 kHz ≤ f_{CLK} < 8.3 MHz	00H	0 (no waits)
	8.3 MHz ≤ f_{CLK} ≤ 16 MHz	01H	1
2.7 V ≤ REGC = V_{DD} < 4.0 V	32 kHz ≤ f_{CLK} < 8.3 MHz	00H	0 (no waits)
	8.3 MHz ≤ f_{CLK} ≤ 10 MHz	01H	1

Remark f_X: Main clock oscillation frequency

(b) Access to special on-chip peripheral I/O register

This product has two types of internal system buses.

One type is for the CPU bus and the other is for the peripheral bus to interface with low-speed peripheral hardware.

Since the CPU bus clock and peripheral bus clock are asynchronous, if a conflict occurs during access between the CPU and peripheral hardware, illegal data may be passed unexpectedly. Therefore, when accessing peripheral hardware that may cause a conflict, the number of access cycles is changed so that the data is received/passed correctly in the CPU. As a result, the CPU does not shift to the next instruction processing and enters the wait status. When this wait status occurs, the number of execution clocks of the instruction is increased by the number of wait clocks.

Note this with caution when performing real-time processing.

When accessing a special on-chip peripheral I/O register, additional waits may be required further to the waits set by the VSWC register.

The access conditions at that time and the method to calculate the number of waits to be inserted (number of CPU clocks) are shown below.

Number of waits to be inserted = (2 + m) × k (clocks)

Number of accesses to specific on-chip peripheral I/O register = 3 + m + (2 + m) × k (clocks)

Peripheral Function	Register Name	Access	k
Watchdog timer 1 (WDT1)	WDTM1	Write	1 to 5
	<Calculation of number of waits[Note]> $k = \{(1/f_X) \times 2/((2 + m)/f_{CPU})\} + 1$ f_X: Main clock oscillation frequency		
Watchdog timer 2 (WDT2)	WDTM2	Write	3 (fixed)
16-bit timer/event counter P0 (TMP0)	TP0CCR0, TP0CCR1, TP0CNT	Read	1
	<Calculation of number of waits[Note]> $k = \{(1/f_{XX})/((2 + m)/f_{CPU})\} + 1$		
	TP0CCR0, TP0CCR1	Write	0 to 2
	<Calculation of number of waits[Note]> $k = \{(1/f_{XX}) \times 5/((2 + m)/f_{CPU})\}$ A wait occurs when performing continuous write to same register		
16-bit timer/event counters 00 to 03 (TM00 to TM03)	TMC00 to TMC03	Read-modify-write	1 (fixed) A wait occurs during write
Clocked serial interfaces 0 and 1 with automatic transmit/receive function (CSIA0, CSIA1)	CSIA0B0 to CSIA0BF, CSIA1B0 to CSIA1BF	Write	0 to 18 (when performing continuous write via write instruction)
	<Calculation of number of waits[Note]> $k = \{(1/f_{SCKA}) \times 5 - (4 + m)/f_{CPU})\}/\{((2 + m)/f_{CPU})\}$ However, 1 wait if $f_{CPU} = f_{XX}$ if the CSISn.CKSAn1 and CSISn.CKSAn0 bits are 00. f_{SCKA}: CSIA selection clock frequency		
	CSIA0B0 to CSIA0BF, CSIA1B0 to CSIA1BF	Write	0 to 20 (when conflict occurs between write instruction and write via receive operation)
	<Calculation of number of waits[Note]> $k = \{((1/f_{SCKA}) \times 5)/((2 + m)/f_{CPU})\}$ f_{SCKA}: CSIA selection clock frequency		
I^2C0	IICS0	Read	1 (fixed)
Asynchronous serial interfaces 0 to 2 (UART0 to UART2)	ASIS0 to ASIS2	Read	1 (fixed)
Real-time output function 0 (RTO0)	RTBL0, RTBH0	Write (when RTPC0.RTPOE0 bit = 0)	1
A/D converter	ADM, ADS, PFM, PFT	Write	1 or 2
	ADCR, ADCRH	Read	1 or 2
	<Calculation of number of waits[Note]> $\{(1/f_{XX}) \times 2/[(2 + m)/f_{CPU}]\} + 1$		

Note In the calculation of number of waits, the fractional part of its result must be multiplied by $(1/f_{CPU})$ and rounded down if $(1/f_{CPU})/(2 + m)$ or lower, and rounded up if $(1/f_{CPU})/(2 + m)$ is exceeded.

Cautions 1. If fetched from the internal ROM or internal RAM, the number of waits is as shown above. If fetched from the external memory, the number of waits may be decreased below these. The effect of the external memory access cycles varies depending on the wait settings and the like. However, the number of waits shown above is the maximum value, so no higher value is generated.

2. When the CPU operates on the subclock and no clock is input to the X1 pin, do not access a register in which a wait occurs. If a wait occurs, it can only be released by a reset.

Remarks 1. In the calculation for the number of waits:

f_{CPU}: CPU clock frequency

f_{XX}: Main clock frequency

m: Set value of bits 2 to 0 of the VSWC register

When the VSWC register = 00H: m = 0

When the VSWC register = 01H: m = 1

2. n = 0, 1

(2) Restriction on conflict between sld instruction and interrupt request

(a) Description

If a conflict occurs between the decode operation of an instruction in <2> immediately before the sld instruction following an instruction in <1> and an interrupt request before the instruction in <1> is complete, the execution result of the instruction in <1> may not be stored in a register.

Instruction <1>

- ld instruction: ld.b, ld.h, ld.w, ld.bu, ld.hu
- sld instruction: sld.b, sld.h, sld.w, sld.bu, sld.hu
- Multiplication instruction: mul, mulh, mulhi, mulu

Instruction <2>

mov reg1, reg2	not reg1, reg2	satsubr reg1, reg2	satsub reg1, reg2
satadd reg1, reg2	satadd imm5, reg2	or reg1, reg2	xor reg1, reg2
and reg1, reg2	tst reg1, reg2	subr reg1, reg2	sub reg1, reg2
add reg1, reg2	add imm5, reg2	cmp reg1, reg2	cmp imm5, reg2
mulh reg1, reg2	shr imm5, reg2	sar imm5, reg2	shl imm5, reg2

<Example>

<i> ld.w [r11], r10
•
•
•
<ii> mov r10, r28
<iii> sld.w 0x28, r10

If the decode operation of the mov instruction <ii> immediately before the sld instruction <iii> and an interrupt request conflict before execution of the ld instruction <i> is complete, the execution result of instruction <i> may not be stored in a register.

(b) Countermeasure

<1> When compiler (CA850) is used
Use CA850 Ver. 2.61 or later because generation of the corresponding instruction sequence can be automatically suppressed.
<2> Countermeasure by assembler

When executing the sld instruction immediately after instruction <ii>, avoid the above operation using either of the following methods.

- Insert a nop instruction immediately before the sld instruction.
- Do not use the same register as the sld instruction destination register in the above instruction <ii> executed immediately before the sld instruction.

CHAPTER 4 PORT FUNCTIONS

4.1 Features

- Input-only ports: 8 pins
- I/O ports: 76 pins
  - Fixed to N-ch open-drain output: 4 (medium: 2)
  - Switchable to N-ch open-drain output: 8
- Input/output can be specified in 1-bit units

4.2 Basic Port Configuration

The V850ES/KG2 incorporates a total of 84 I/O port pins consisting of ports 0, 1, 3 to 5, 7, 9, CM, CS, CT, DH, and DL (including 8 input-only port pins). The port configuration is shown below.

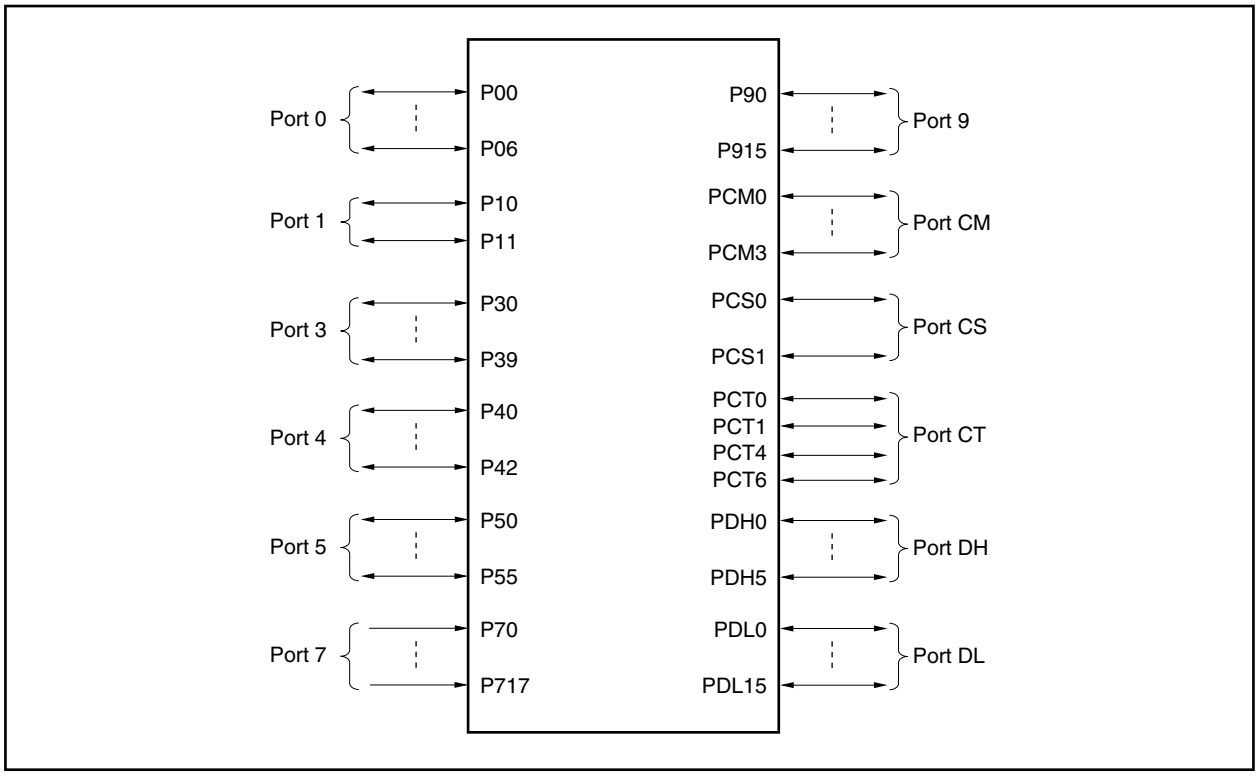


Table 4-1. Pin I/O Buffer Power Supplies of V850ES/KG2

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Ports CM, CS, CT, DH, DL
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 5, 9

4.3 Port Configuration

Table 4-2. Port Configuration

Item	Configuration
Control registers	Port n register (Pn: n = 0, 1, 3 to 5, 7, 9, CM, CS, CT, DL, DH) Port n mode register (PMn: n = 0, 1, 3 to 5, 9, CM, CS, CT, DL, DH) Port n mode control register (PMCn: n = 0, 3 to 5, 9, CM, CS, CT, DL, DH) Port n function control register (PFCn: n = 3 to 5, 9) Port n function register (PFn: n = 3 to 5, 9) Port 3 function control expansion register (PFCE3) Pull-up resistor option register (PUn: n = 0, 1, 3 to 5, 9, CM, CS, CT, DL, DH)
Ports	Input only: 8 I/O: 76
Pull-up resistors	Software control: 72

(1) Port n register (Pn)

Data I/O with external devices is performed by writing to and reading from the Pn register. The Pn register is configured of a port latch that retains the output data and a circuit that reads the pin status.

Each bit of the Pn register corresponds to one pin of port n and can be read or written in 1-bit units.

After reset: 00H[Note] (output latch) R/W

	7	6	5	7	3	2	1	0
Pn	Pn7	Pn6	Pn5	Pn4	Pn3	Pn2	Pn1	Pn0

Pnm	Control of output data (in output mode)
0	0 is output
1	1 is output

Note Input-only port pins are undefined.

Writing to and reading from the Pn register are executed as follows depending on the setting of each register.

Table 4-3. Reading to/Writing from Pn Register

Setting of PMCn Register	Setting of PMn Register	Writing to Pn Register	Reading from Pn Register
Port mode (PMCnm bit = 0)	Output mode (PMnm bit = 0)	Write to the output latch[Note]. The contents of the output latch are output from the pin.	The value of the output latch is read.
	Input mode (PMnm bit = 1)	Write to the output latch[Note]. The status of the pin is not affected.	The pin status is read.
Alternate-function mode (PMCnm bit = 1)	Output mode (PMnm bit = 0)	Write to the output latch[Note]. The status of the pin is not affected. The pin operates as an alternate-function pin.	• When alternate function is output The output status of the alternate function is read. • When alternate function is input The output latch value is read.
	Input mode (PMnm bit = 1)	Write to the output latch[Note]. The status of the pin is not affected. The pin operates as an alternate-function pin.	The pin status is read.

Note The value written to the output latch is retained until a new value is written to the output latch.

(2) Port n mode register (PMn)

PMn specifies the input mode/output mode of the port.

Each bit of the PMn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: FFH R/W

	7	6	5	4	3	2	1	0
PMn	PMn7	PMn6	PMn5	PMn4	PMn3	PMn2	PMn1	PMn0

PMnm	Control of I/O mode
0	Output mode
1	Input mode

(3) Port n mode control register (PMCn)

PMCn specifies the port mode/alternate function.

Each bit of the PMCn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PMCn	PMCn7	PMCn6	PMCn5	PMCn4	PMCn3	PMCn2	PMCn1	PMCn0

PMCnm	Specification of operation mode
0	Port mode
1	Alternate function mode

(4) Port n function control register (PFCn)

PFCn is a register that specifies the alternate function to be used when one pin has two or more alternate functions.

Each bit of the PFCn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCnm	Specification of alternate function
0	Alternate function 1
1	Alternate function 2

(5) Port n function control expansion register (PFCEn)

PFCEn is a register that specifies the alternate function to be used when one pin has three or more alternate functions.

Each bit of the PFCEn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCEn	PFCEn7	PFCEn6	PFCEn5	PFCEn4	PFCEn3	PFCEn2	PFCEn1	PFCEn0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCEnm	PFCnm	Specification of alternate function
0	0	Alternate function 1
0	1	Alternate function 2
1	0	Alternate function 3
1	1	Alternate function 4

(6) Port n function register (PFn)

PFn is a register that specifies normal output/N-ch open-drain output.

Each bit of the PFn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFn	PFn7	PFn6	PFn5	PFn4	PFn3	PFn2	PFn1	PFn0

PFnm[Note]	Control of normal output/N-ch open-drain output
0	Normal output (CMOS output)
1	N-ch open-drain output

Note The PFnm bit is valid only when the PMn.PMnm bit is 0 (output mode) regardless of the setting of the PMCn register. When the PMnm bit is 1 (input mode), the set value in the PFn register is invalid.

Example <1> When the value of the PFn register is valid
PFnm bit = 1 … N-ch open-drain output is specified.
PMnm bit = 0 … Output mode is specified.
PMCnm bit = 0 or 1

<2> When the value of the PFn register is invalid
PFnm bit = 0 … N-ch open-drain output is specified.
PMnm bit = 1 … Input mode is specified.
PMCnm bit = 0 or 1

(7) Pull-up resistor option register (PUn)

PUn is a register that specifies the connection of an on-chip pull-up resistor.

Each bit of the PUn register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

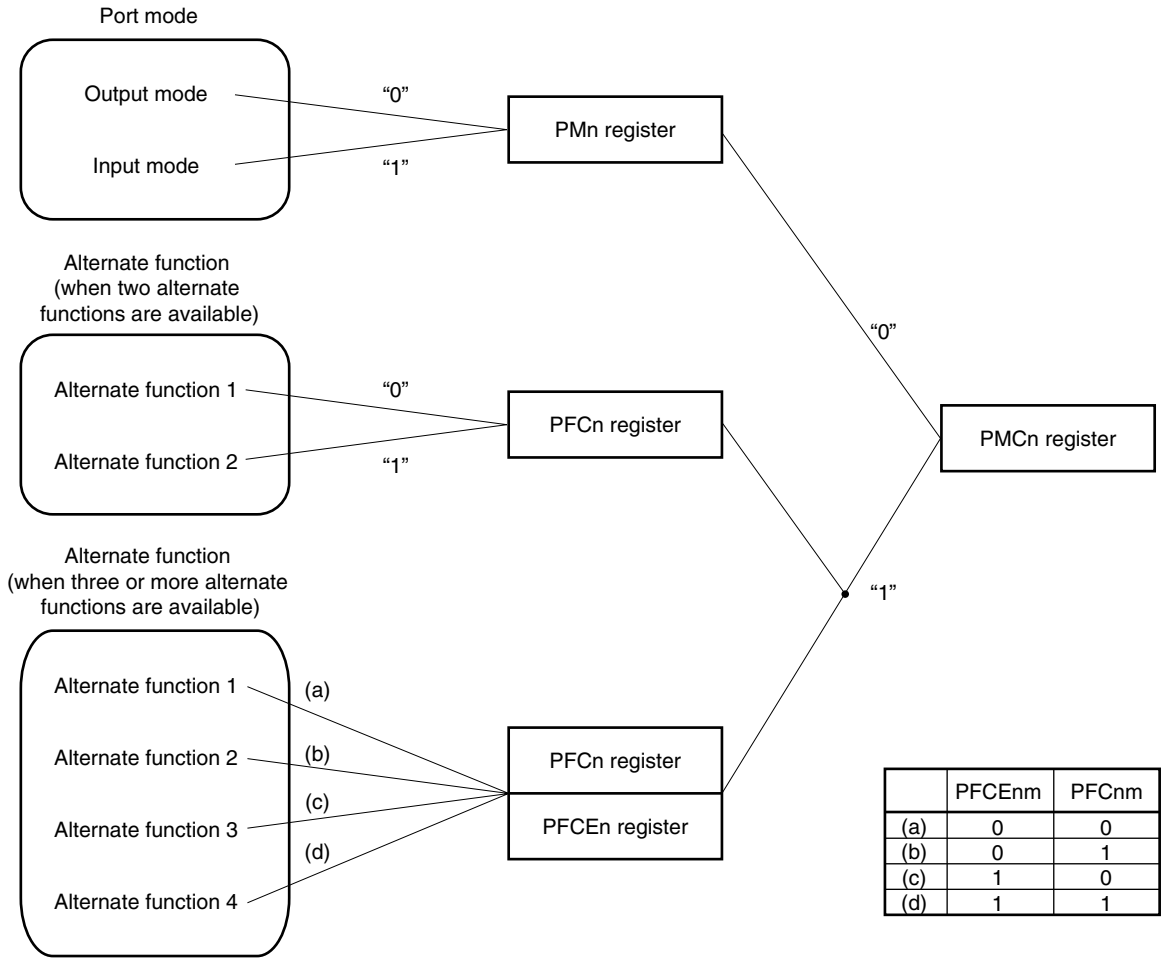
	7	6	5	4	3	2	1	0
PUn	PUn7	PUn6	PUn5	PUn4	PUn3	PUn2	PUn1	PUn0

PUnm	Control of on-chip pull-up resistor connection
0	Not connected
1	Connected

(8) Port settings

Set the ports as follows.

Figure 4-1. Register Settings and Pin Functions



	PFCEnm	PFCnm
(a)	0	0
(b)	0	1
(c)	1	0
(d)	1	1

Remark Switch to the alternate function using the following procedure.

<1> Set the PFCn and PFCEn registers.
<2> Set the PMCn register.
<3> Set the INTRn or INTFn register (to specify an external interrupt pin).

If the PMCn register is set first, an unintended function may be set while the PFCn and PFCEn registers are being set.

4.3.1 Port 0

Port 0 is a 7-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 0 includes the following alternate functions.

Table 4-4. Alternate-Function Pins of Port 0

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
6	8	P00	TOH0	Output	Yes	–	D0-U
7	9	P01	TOH1	Output			D0-U
17	19	P02	NMI	Input		Analog noise elimination	D1-SUIL
18	20	P03	INTP0	Input			D1-SUIL
19	21	P04	INTP1	Input			D1-SUIL
20	22	P05	INTP2	Input			D1-SUIL
21	23	P06	INTP3	Input		Analog/digital noise elimination	D1-SUIL

Note Software pull-up function

Caution P02 to P06 have hysteresis characteristics when the alternate function is input, but not in the port mode.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 0 register (P0)

After reset: 00H (output latch) R/W Address: FFFFF400H

	7	6	5	4	3	2	1	0
P0	0	P06	P05	P04	P03	P02	P01	P00

P0n	Control of output data (in output mode) (n = 0 to 6)
0	0 is output
1	1 is output

(2) Port 0 mode register (PM0)

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

PM0n	Control of I/O mode (n = 0 to 6)
0	Output mode
1	Input mode

(3) Port 0 mode control register (PMC0)

After reset: 00H R/W Address: FFFFF440H

	7	6	5	4	3	2	1	0
PMC0	0	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00

PMC06	Specification of P06 pin operation mode
0	I/O port
1	INTP3 input

PMC05	Specification of P05 pin operation mode
0	I/O port
1	INTP2 input

PMC04	Specification of P04 pin operation mode
0	I/O port
1	INTP1 input

PMC03	Specification of P03 pin operation mode
0	I/O port
1	INTP0 input

PMC02	Specification of P02 pin operation mode
0	I/O port
1	NMI input

PMC01	Specification of P01 pin operation mode
0	I/O port
1	TOH1 output

PMC00	Specification of P00 pin operation mode
0	I/O port
1	TOH0 output

(4) Pull-up resistor option register 0 (PU0)

After reset: 00H R/W Address: FFFFFC40H

	7	6	5	4	3	2	1	0
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00

PU0n	Control of on-chip pull-up resistor connection (n = 0 to 6)
0	Not connected
1	Connected

4.3.2 Port 1

Port 1 is a 2-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 1 includes the following alternate functions.

Table 4-5. Alternate-Function Pins of Port 1

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
3	5	P10	ANO0	Output	Yes	–	C-UA
4	6	P11	ANO1	Output			C-UA

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 1 register (P1)

After reset: 00H (output latch) R/W Address: FFFFF402H

	7	6	5	4	3	2	1	0
P1	0	0	0	0	0	0	P11	P10

P1n	Control of output data (in output mode) (n = 0, 1)
0	0 is output
1	1 is output

(2) Port 1 mode register (PM1)

Caution When used as the ANO0 and ANO1 pins, set PM1 = FFH all together.

After reset: FFH R/W Address: FFFFF422H

	7	6	5	4	3	2	1	0
PM1	1	1	1	1	1	1	PM11	PM10

PM1n	Control of I/O mode (n = 0, 1)
0	Output mode
1	Input mode

(3) Pull-up resistor option register 1 (PU1)

After reset: 00H R/W Address: FFFFFC42H

	7	6	5	4	3	2	1	0
PU1	0	0	0	0	0	0	PU11	PU10

PU1n	Control of on-chip pull-up resistor connection (n = 0, 1)
0	Not connected
1	Connected

4.3.3 Port 3

Port 3 is a 10-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 3 includes the following alternate functions.

Table 4-6. Alternate-Function Pins of Port 3

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
25	27	P30	TXD0/TO02	Output	Yes	–	E00-U
26	28	P31	RXD0/INTP7/TO03	I/O			E10-SUIHL
27	29	P32	ASCK0/ADTRG/TO01	I/O			E10-SUL
28	30	P33	TI000/TO00/TIP00/ TOP00	I/O			G1010-SUL
29	31	P34	TI001/TO00/TIP01/ TOP01	I/O			G1010-SUL
30	32	P35	TI010/TO01	I/O			E10-SUL
31	33	P36	–	–	No	N-ch open-drain output	C-N
32	34	P37	–	–			C-N
35	37	P38	SDA0	I/O			D2-SNFH
36	38	P39	SCL0	I/O			D2-SNFH

Note Software pull-up function

Caution P31 to P35, P38, and P39 have hysteresis characteristics when the alternate function is input, but not in the port mode.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 3 register (P3)

After reset: 00H (output latch) R/W Address: P3 FFFFF406H,
P3L FFFFF406H, P3H FFFFF407H

	15	14	13	12	11	10	9	8
P3 (P3H[Note])	0	0	0	0	0	0	P39	P38

	7	6	5	4	3	2	1	0
(P3L)	P37	P36	P35	P34	P33	P32	P31	P30

P3n	Control of output data (in output mode) (n = 0 to 9)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the P3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P3H register.

Remark The P3 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the P3 register are used as the P3H register and as the P3L register, respectively, this register can be read or written in 8-bit or 1-bit units.

(2) Port 3 mode register (PM3)

After reset: FFFFH R/W Address: PM3 FFFFF426H,
PM3L FFFFF426H, PM3H FFFFF427H

	15	14	13	12	11	10	9	8
PM3 (PM3H[Note])	1	1	1	1	1	1	PM39	PM38

	7	6	5	4	3	2	1	0
(PM3L)	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30

PM3n	Control of I/O mode (n = 0 to 9)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PM3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PM3H register.

Remark The PM3 register can be read or written in 16-bit units.
When the higher 8 bits and the lower 8 bits of the PM3 register are used as the PM3H register and as the PM3L register, respectively, this register can be read or written in 8-bit or 1-bit units.

(3) Port 3 mode control register (PMC3)

After reset: 0000H R/W Address: PMC3 FFFFF446H,
PMC3L FFFFF446H, PMC3H FFFFF447H

	15	14	13	12	11	10	9	8
PMC3 (PMC3H[Note])	0	0	0	0	0	0	PMC39	PMC38

	7	6	5	4	3	2	1	0
(PMC3L)	0	0	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

PMC39	Specification of P39 pin operation mode
0	I/O port
1	SCL0 I/O

PMC38	Specification of P38 pin operation mode
0	I/O port
1	SDA0 I/O

PMC35	Specification of P35 pin operation mode
0	I/O port
1	TI010 input/TO01 output

PMC34	Specification of P34 pin operation mode
0	I/O port
1	TI001 input/TO00 output/TIP01 input/TOP01 output

PMC33	Specification of P33 pin operation mode
0	I/O port
1	TI000 input/TO00 output/TIP00 input/TOP00 output

PMC32	Specification of P32 pin operation mode
0	I/O port
1	ASCK0 input/ADTRG input/TO01 output

PMC31	Specification of P31 pin operation mode
0	I/O port
1	RXD0 input/INTP7 input/TO03 output

PMC30	Specification of P30 pin operation mode
0	I/O port
1	TXD0 output/TO02 output

Note When reading from or writing to bits 8 to 15 of the PMC3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC3H register.

Remark The PMC3 register can be read or written in 16-bit units.
When the higher 8 bits and the lower 8 bits of the PMC3 register are used as the PMC3H register and as the PMC3L register, respectively, this register can be read or written in 8-bit or 1-bit units.

(4) Port 3 function register H (PF3H)

After reset: 00H R/W Address: FFFFFC67H

	7	6	5	4	3	2	1	0
PF3H	0	0	0	0	0	0	PF39	PF38

PF3n	Specification of normal port/alternate function (n = 8, 9)
0	When used as normal port (N-ch open-drain output)
1	When used as alternate-function (N-ch open-drain output)

Caution When using P38 and P39 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P3n bit = 1 → PF3n bit = 1 → PMC3n bit = 1

(5) Port 3 function control register (PFC3)

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	0	0	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30

Remark For details of specification of alternate-function pins, refer to **4.3.3 (7) Specifying alternate-function pins of port 3**.

(6) Port 3 function control expansion register (PFCE3)

After reset: 00H R/W Address: FFFFF706H

	7	6	5	4	3	2	1	0
PFCE3	0	0	0	PFCE34	PFCE33	0	0	0

Remark For details of specification of alternate-function pins, refer to **4.3.3 (7) Specifying alternate-function pins of port 3**.

(7) Specifying alternate-function pins of port 3

PFC35	Specification of Alternate-Function Pin of P35 Pin
0	TI010 input
1	TO01 output

PFCE34	PFC34	Specification of Alternate-Function Pin of P34 Pin
0	0	TI001 input
0	1	TO00 output
1	0	TIP01 input
1	1	TOP01 output

PFCE33	PFC33	Specification of Alternate-Function Pin of P33 Pin
0	0	TI000 input
0	1	TO00 output
1	0	TIP00 input
1	1	TOP00 output

PFC32	Specification of Alternate-Function Pin of P32 Pin
0	ASCK0/ADTRG[Note 1] input
1	TO01 output

PFC31	Specification of Alternate-Function Pin of P31 Pin
0	RXD0/INTP7[Note 2] input
1	TO03 output

PFC30	Specification of Alternate-Function Pin of P30 Pin
0	TXD0 output
1	TO02 output

Notes 1. The ASCK0 and ADTRG pins are alternate-function pins. When using the pin as the ASCK0 pin, disable the trigger input of the alternate-function ADTRG pin (clear the ADS.TRG bit to 0 or set the ADS.ADTMD bit to 1). When using the pin as the ADTRG pin, do not set the UART0 operation clock to external input (set the CKSR0.TPS03 to CKSR0.TPS00 bits to other than 1011).

2. The INTP7 and RXD0 pins are alternate-function pins. When using the pin as the RXD0 pin, disable edge detection of the alternate-function INTP7 pin (clear the INTF3.INTF31 and INTR3.INTR31 bits to 0). When using the pin as the INTP7 pin, stop the UART0 receive operation (clear the ASIM0.RXE0 bit to 0).

(8) Pull-up resistor option register 3 (PU3)

After reset: 00H R/W Address: FFFFFC46H

	7	6	5	4	3	2	1	0
PU3	0	0	PU35	PU34	PU33	PU32	PU31	PU30

PU3n	Control of on-chip pull-up resistor connection (n = 0 to 5)
0	Not connected
1	Connected

4.3.4 Port 4

Port 4 is a 3-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 4 includes the following alternate functions.

Table 4-7. Alternate-Function Pins of Port 4

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
22	24	P40	SI00/RXD2	Input	Yes	–	E11-SULH
23	25	P41	SO00/TXD2	Output		N-ch open-drain output can be selected.	E00-UF
24	26	P42	$\overline{SCK00}$	I/O			D2-SUFL

Note Software pull-up function

Caution P40 and P42 have hysteresis characteristics when the alternate function is input, but not in the port mode.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 4 register (P4)

After reset: 00H (output latch) R/W Address: FFFFF408H

	7	6	5	4	3	2	1	0
P4	0	0	0	0	0	P42	P41	P40

P4n	Control of output data (in output mode) (n = 0 to 2)
0	0 is output
1	1 is output

(2) Port 4 mode register (PM4)

After reset: FFH R/W Address: FFFFF428H

	7	6	5	4	3	2	1	0
PM4	1	1	1	1	1	PM42	PM41	PM40

PM4n	Control of I/O mode (n = 0 to 2)
0	Output mode
1	Input mode

(3) Port 4 mode control register (PMC4)

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	0	0	PMC42	PMC41	PMC40

PMC42	Specification of P42 pin operation mode
0	I/O port
1	$\overline{\text{SCK00}}$ I/O

PMC41	Specification of P41 pin operation mode
0	I/O port
1	SO00 output/TXD2 output

PMC40	Specification of P40 pin operation mode
0	I/O port
1	SI00 input/RXD2 input

(4) Port 4 function control register (PFC4)

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	0	0	0	0	0	0	PFC41	PFC40

PFC41	Specification of alternate-function pin of P41 pin
0	SO00 output
1	TXD2 output

PFC40	Specification of alternate-function pin of P40 pin
0	SI00 input
1	RXD2 input

(5) Port 4 function register (PF4)

After reset: 00H R/W Address: FFFFFC68H

	7	6	5	4	3	2	1	0
PF4	0	0	0	0	0	PF42	PF41	0

PF4n	Control of normal output/N-ch open-drain output (n = 1, 2)
0	Normal output
1	N-ch open-drain output

Caution When using P41 and P42 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P4n bit = 1 → PF4n bit = 1 → PMC4n bit = 1

(6) Pull-up resistor option register 4 (PU4)

After reset: 00H R/W Address: FFFFFC48H

	7	6	5	4	3	2	1	0
PU4	0	0	0	0	0	PU42	PU41	PU40

PU4n	Control of on-chip pull-up resistor connection (n = 0 to 2)
0	Not connected
1	Connected

4.3.5 Port 5

Port 5 is a 6-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 5 includes the following alternate functions.

Table 4-8. Alternate-Function Pins of Port 5

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
37	39	P50	TI011/RTP00/KR0	I/O	Yes	–	E10-SULT
38	40	P51	TI50/RTP01/KR1	I/O			E10-SULT
39	41	P52	TO50/RTP02/KR2	I/O			E00-SUT
40	42	P53	SIA0/RTP03/KR3	I/O			E10-SULT
41	43	P54	SOA0/RTP04/KR4	I/O		N-ch open-drain output can be selected.	E00-SUFT
42	44	P55	$\overline{\text{SCKA0}}$/RTP05/KR5	I/O			E20-SUFLT

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 5 register (P5)

After reset: 00H (output latch) R/W Address: FFFFF40AH

	7	6	5	4	3	2	1	0
P5	0	0	P55	P54	P53	P52	P51	P50

P5n	Control of output data (in output mode) (n = 0 to 5)
0	0 is output
1	1 is output

(2) Port 5 mode register (PM5)

After reset: FFH R/W Address: FFFFF42AH

	7	6	5	4	3	2	1	0
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50

PM5n	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

(3) Port 5 mode control register (PMC5)

After reset: 00H R/W Address: FFFFF44AH

	7	6	5	4	3	2	1	0
PMC5	0	0	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50

PMC55	Specification of P55 pin operation mode
0	I/O port/KR5 input
1	$\overline{\text{SCKA0}}$ I/O/RTP05 output

PMC54	Specification of P54 pin operation mode
0	I/O port/KR4 input
1	SOA0 output/RTP04 output

PMC53	Specification of P53 pin operation mode
0	I/O port/KR3 input
1	SIA0 input/RTP03 output

PMC52	Specification of P52 pin operation mode
0	I/O port/KR2 input
1	TO50 output/RTP02 output

PMC51	Specification of P51 pin operation mode
0	I/O port/KR1 input
1	TI50 input/RTP01 output

PMC50	Specification of P50 pin operation mode
0	I/O port/KR0 input
1	TI011 input/RTP00 output

(4) Port 5 function register 5 (PF5)

After reset: 00H R/W Address: FFFFFC6AH

	7	6	5	4	3	2	1	0
PF5	0	0	PF55	PF54	0	0	0	0

PF5n	Control of normal output/N-ch open-drain output (n = 4, 5)
0	Normal output
1	N-ch open-drain output

Cautions 1. Always set bits 0 to 3, 6, and 7 of the PF5 register to 0.

2. When using P54 and P55 as N-ch open-drain-output alternate-function pins, set in the following sequence.

Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.

P5n bit = 1 → PF5n bit = 1 → PMC5n bit = 1

(5) Port 5 function control register (PFC5)

After reset: 00H R/W Address: FFFFF46AH

	7	6	5	4	3	2	1	0
PFC5	0	0	PFC55	PFC54	PFC53	PFC52	PFC51	PFC50

PFC55	Specification of alternate-function pin of P55 pin
0	$\overline{\text{SCKA0}}$ I/O
1	RTP05 output

PFC54	Specification of alternate-function pin of P54 pin
0	SOA0 output
1	RTP04 output

PFC53	Specification of alternate-function pin of P53 pin
0	SIA0 input
1	RTP03 output

PFC52	Specification of alternate-function pin of P52 pin
0	TO50 output
1	RTP02 output

PFC51	Specification of alternate-function pin of P51 pin
0	TI50 input
1	RTP01 output

PFC50	Specification of alternate-function pin of P50 pin
0	TI011 input
1	RTP00 output

(6) Pull-up resistor option register 5 (PU5)

After reset: 00H R/W Address: FFFFFC4AH

	7	6	5	4	3	2	1	0
PU5	0	0	PU55	PU54	PU53	PU52	PU51	PU50

PU5n	Control of on-chip pull-up resistor connection (n = 0 to 5)
0	Not connected
1	Connected

4.3.6 Port 7

Port 7 is an 8-bit input-only port for which all the pins are fixed to input.

Port 7 includes the following alternate functions.

Table 4-9. Alternate-Function Pins of Port 7

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
100	2	P70	ANI0	Input	No	–	A-A
99	1	P71	ANI1	Input			A-A
98	100	P72	ANI2	Input			A-A
97	99	P73	ANI3	Input			A-A
96	98	P74	ANI4	Input			A-A
95	97	P75	ANI5	Input			A-A
94	96	P76	ANI6	Input			A-A
93	95	P77	ANI7	Input			A-A

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 7 register (P7)

After reset: Undefined R Address: FFFFF40EH

	7	6	5	4	3	2	1	0
P7	P77	P76	P75	P74	P73	P72	P71	P70

P7n	Input data read (n = 0 to 7)
0	Input low level
1	Input high level

4.3.7 Port 9

Port 9 is a 16-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port 9 includes the following alternate functions.

Table 4-10. Alternate-Function Pins of Port 9

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
43	45	P90	A0/TXD1/KR6	I/O	Yes	–	E00-SUTZ
44	46	P91	A1/RXD1/KR7	I/O			E01-SUHTZ
45	47	P92	A2/TI020/TO02	I/O			E00-SUTZ
46	48	P93	A3/TI021	I/O			E01-SULZ
47	49	P94	A4/TI030/TO03	I/O			E00-SUTZ
48	50	P95	A5/TI031	I/O			E01-SULZ
49	51	P96	A6/TI51/TO51	I/O			E00-SUTZ
50	52	P97	A7/SI01	I/O			E01-SUHTZ
51	53	P98	A8/SO01	Output		N-ch open-drain output can be specified.	E00-UFZ
52	54	P99	A9/$\overline{\text{SCK01}}$	I/O			E02-SUFLZ
53	55	P910	A10/SIA1	I/O		–	E01-SULZ
54	56	P911	A11/SOA1	Output		N-ch open-drain output can be specified.	E00-UFZ
55	57	P912	A12/$\overline{\text{SCKA1}}$	I/O			E02-SUFLZ
56	58	P913	A13/INTP4	I/O		Analog noise elimination	E01-SUILZ
57	59	P914	A14/INTP5	I/O			E01-SUILZ
58	60	P915	A15/INTP6	I/O			E01-SUILZ

Note Software pull-up function

Caution P93, P95, P97, P99, P910, and P912 to P915 have hysteresis characteristics when the alternate function is input, but not in the port mode.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port 9 register (P9)

After reset: 00H (output latch) R/W Address: P9 FFFFF412H,
P9L FFFFF412H, P9H FFFFF413H

	15	14	13	12	11	10	9	8
P9 (P9H[Note])	P915	P914	P913	P912	P911	P910	P99	P98

	7	6	5	4	3	2	1	0
(P9L)	P97	P96	P95	P94	P93	P92	P91	P90

P9n	Control of output data (in output mode) (n = 0 to 15)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the P9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P9H register.

Remark The P9 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the P9 register are used as the P9H register and as the P9L register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(2) Port 9 mode register (PM9)

After reset: FFFFH R/W Address: PM9 FFFFF432H,
PM9L FFFFF432H, PM9H FFFFF433H

	15	14	13	12	11	10	9	8
PM9 (PM9H[Note])	PM915	PM914	PM913	PM912	PM911	PM910	PM99	PM98

	7	6	5	4	3	2	1	0
(PM9L)	PM97	PM96	PM95	PM94	PM93	PM92	PM91	PM90

PM9n	Control of I/O mode (n = 0 to 15)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PM9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PM9H register.

Remark The PM9 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PM9 register are used as the PM9H register and as the PM9L register, respectively, this register can be read or written in 8-bit or 1-bit units.

(3) Port 9 mode control register (PMC9)

Caution When using port 9 as the A0 to A15 pins, set the PMC9 register to FFFFH in 16-bit units.

(1/2)

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H[Note])	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	A15 output/INTP6 input

PMC914	Specification of P914 pin operation mode
0	I/O port
1	A14 output/INTP5 input

PMC913	Specification of P913 pin operation mode
0	I/O port
1	A13 output/INTP4 input

PMC912	Specification of P912 pin operation mode
0	I/O port
1	A12 output/$\overline{\text{SCKA1}}$ I/O

PMC911	Specification of P911 pin operation mode
0	I/O port
1	A11 output/SOA1 output

PMC910	Specification of P910 pin operation mode
0	I/O port
1	A10 output/SIA1 input

PMC99	Specification of P99 pin operation mode
0	I/O port
1	A9 output/$\overline{\text{SCK01}}$ I/O

PMC98	Specification of P98 pin operation mode
0	I/O port
1	A8 output/SO01 output

Note When reading from or writing to bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC9H register.

Remark The PMC9 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PMC9 register are used as the PMC9H register and as the PMC9L register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(2/2)

PMC97	Specification of P97 pin operation mode
0	I/O port
1	A7 output/SI01 input

PMC96	Specification of P96 pin operation mode
0	I/O port/TI51 input
1	A6 output/TO51 output

PMC95	Specification of P95 pin operation mode
0	I/O port
1	A5 output/TI031 input

PMC94	Specification of P94 pin operation mode
0	I/O port/TI030 input
1	A4 output/TO03 output

PMC93	Specification of P93 pin operation mode
0	I/O port
1	A3 output/TI021 input

PMC92	Specification of P92 pin operation mode
0	I/O port/TI020 input
1	A2 output/TO02 output

PMC91	Specification of P91 pin operation mode
0	I/O port/KR7 input
1	A1 output/RXD1 input

PMC90	Specification of P90 pin operation mode
0	I/O port/KR6 input
1	A0 output/TXD1 output

(4) Port 9 function register H (PF9H)

After reset: 00H R/W Address: FFFFFC73H

	7	6	5	4	3	2	1	0
PF9H	0	0	0	PF912	PF911	0	PF99	PF98

PF9n	Control of normal output/N-ch open-drain output (n = 0, 1, 3, 4)
0	Normal output
1	N-ch open-drain output

Caution When using P98, P99, P911, and P912 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P9n bit = 1 → PFC9n bit = 0/1 → PF9n bit = 1 → PMC9n bit = 1

(5) Port 9 function control register (PFC9)

Caution When using port 9 as the A0 to A15 pins, set the PFC9 register to 0000H in 16-bit units.

(1/2)

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H[Note])	PFC915	PFC914	PFC913	PFC912	PFC911	PFC910	PFC99	PFC98

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	PFC95	PFC94	PFC93	PFC92	PFC91	PFC90

PFC915	Specification of alternate-function pin of P915 pin
0	A15 output
1	INTP6 input

PFC914	Specification of alternate-function pin of P914 pin
0	A14 output
1	INTP5 input

PFC913	Specification of alternate-function pin of P913 pin
0	A13 output
1	INTP4 input

PFC912	Specification of alternate-function pin of P912 pin
0	A12 output
1	$\overline{\text{SCKA1}}$ I/O

PFC911	Specification of alternate-function pin of P911 pin
0	A11 output
1	SOA1 output

PFC910	Specification of alternate-function pin of P910 pin
0	A10 output
1	SIA1 input

PFC99	Specification of alternate-function pin of P99 pin
0	A9 output
1	$\overline{\text{SCK01}}$ I/O

PFC98	Specification of alternate-function pin of P98 pin
0	A8 output
1	SO01 output

Note When reading from or writing to bits 8 to 15 of the PFC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PFC9H register.

Remark The PFC9 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PFC9 register are used as the PFC9H register and as the PFC9L register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(2/2)

PFC97	Specification of alternate-function pin of P97 pin
0	A7 output
1	SI01 input

PFC96	Specification of alternate-function pin of P96 pin
0	A6 output
1	TO51 output

PFC95	Specification of alternate-function pin of P95 pin
0	A5 output
1	TI031 input

PFC94	Specification of alternate-function pin of P94 pin
0	A4 output
1	TO03 output

PFC93	Specification of alternate-function pin of P93 pin
0	A3 output
1	TI021 input

PFC92	Specification of alternate-function pin of P92 pin
0	A2 output
1	TO02 output

PFC91	Specification of alternate-function pin of P91 pin
0	A1 output
1	RXD1 input

PFC90	Specification of alternate-function pin of P90 pin
0	A0 output
1	TXD1 output

(6) Pull-up resistor option register 9 (PU9)

After reset: 0000H R/W Address: PU9 FFFFFC52H,
PU9L FFFFFC52H, PU9H FFFFFC53H

	15	14	13	12	11	10	9	8
PU9 (PU9H[Note])	PU915	PU914	PU913	PU912	PU911	PU910	PU99	PU98

	7	6	5	4	3	2	1	0
(PU9L)	PU97	PU96	PU95	PU94	PU93	PU92	PU91	PU90

PU9n	Control of on-chip pull-up resistor connection (n = 0 to 15)
0	Not connected
1	Connected

Note When reading from or writing to bits 8 to 15 of the PU9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PU9H register.

Remark The PU9 register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PU9 register are used as the PU9H register and as the PU9L register, respectively, these registers can be read or written in 8-bit or 1-bit units.

4.3.8 Port CM

Port CM is a 4-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port CM includes the following alternate functions.

Table 4-11. Alternate-Function Pins of Port CM

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
61	63	PCM0	$\overline{WAIT}$	Input	Yes	–	D1-UH
62	64	PCM1	CLKOUT	Output			D0-U
63	65	PCM2	$\overline{HLDAK}$	Output			D0-U
64	66	PCM3	$\overline{HLDRQ}$	Input			D1-UH

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port CM register (PCM)

After reset: 00H (output latch) R/W Address: FFFFF00CH

	7	6	5	4	3	2	1	0
PCM	0	0	0	0	PCM3	PCM2	PCM1	PCM0

PCMn	Control of output data (in output mode) (n = 0 to 3)
0	0 is output
1	1 is output

(2) Port CM mode register (PMCM)

After reset: FFH R/W Address: FFFFF02CH

	7	6	5	4	3	2	1	0
PMCM	1	1	1	1	PMCM3	PMCM2	PMCM1	PMCM0

PMCMn	Control of I/O mode (n = 0 to 3)
0	Output mode
1	Input mode

(3) Port CM mode control register (PMCCM)

After reset: 00H R/W Address: FFFFF04CH

	7	6	5	4	3	2	1	0
PMCCM	0	0	0	0	PMCCM3	PMCCM2	PMCCM1	PMCCM0

PMCCM3	Specification of PCM3 pin operation mode
0	I/O port
1	$\overline{\text{HLDRQ}}$ input

PMCCM2	Specification of PCM2 pin operation mode
0	I/O port
1	$\overline{\text{HLDAK}}$ output

PMCCM1	Specification of PCM1 pin operation mode
0	I/O port
1	CLKOUT output

PMCCM0	Specification of PCM0 pin operation mode
0	I/O port
1	$\overline{\text{WAIT}}$ input

(4) Pull-up resistor option register CM (PUCM)

After reset: 00H R/W Address: FFFFFF4CH

	7	6	5	4	3	2	1	0
PUCM	0	0	0	0	PUCM3	PUCM2	PUCM1	PUCM0

PUCMn	Control of on-chip pull-up resistor connection (n = 0 to 3)
0	Not connected
1	Connected

4.3.9 Port CS

Port CS is a 2-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port CS includes the following alternate functions.

Table 4-12. Alternate-Function Pins of Port CS

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
59	61	PCS0	$\overline{CS0}$	Output	Yes	–	D0-UZ
60	62	PCS1	$\overline{CS1}$	Output			D0-UZ

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port CS register (PCS)

After reset: 00H (output latch) R/W Address: FFFFF008H

	7	6	5	4	3	2	1	0
PCS	0	0	0	0	0	0	PCS1	PCS0

PCSn	Control of output data (in output mode) (n = 0, 1)
0	0 is output
1	1 is output

(2) Port CS mode register (PMCS)

After reset: FFH R/W Address: FFFFF028H

	7	6	5	4	3	2	1	0
PMCS	0	0	0	0	0	0	PMCS1	PMCS0

PMCSn	Control of I/O mode (n = 0, 1)
0	Output mode
1	Input mode

(3) Port CS mode control register (PMCCS)

After reset: 00H R/W Address: FFFFF048H

	7	6	5	4	3	2	1	0
PMCCS	0	0	0	0	0	0	PMCCS1	PMCCS0

PMCCSn	Specification of PCSn pin operation mode (n = 0, 1)
0	I/O port
1	$\overline{\text{CSn}}$ output

(4) Pull-up resistor option register CS (PUCS)

After reset: 00H R/W Address: FFFFFF48H

	7	6	5	4	3	2	1	0
PUCS	0	0	0	0	0	0	PUCS1	PUCS0

PUCSn	Control of on-chip pull-up resistor connection (n = 0, 1)
0	Not connected
1	Connected

4.3.10 Port CT

Port CT is a 4-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port CT includes the following alternate functions.

Table 4-13. Alternate-Function Pins of Port CT

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
65	67	PCT0	$\overline{WR0}$	Output	Yes	–	D0-UZ
66	68	PCT1	$\overline{WR1}$	Output			D0-UZ
67	69	PCT4	$\overline{RD}$	Output			D0-UZ
68	70	PCT6	ASTB	Output			D0-UZ

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port CT register (PCT)

After reset: 00H (output latch) R/W Address: FFFFF00AH

	7	6	5	4	3	2	1	0
PCT	0	PCT6	0	PCT4	0	0	PCT1	PCT0

PCTn	Control of output data (in output mode) (n = 0, 1, 4, 6)
0	0 is output
1	1 is output

(2) Port CT mode register (PMCT)

After reset: FFH R/W Address: FFFFF02AH

	7	6	5	4	3	2	1	0
PMCT	0	PMCT6	0	PMCT4	0	0	PMCT1	PMCT0

PMCTn	Control of I/O mode (n = 0, 1, 4, 6)
0	Output mode
1	Input mode

(3) Port CT mode control register (PMCCT)

After reset: 00H R/W Address: FFFFF04AH

	7	6	5	4	3	2	1	0
PMCCT	0	PMCCT6	0	PMCCT4	0	0	PMCCT1	PMCCT0

PMCCT6	Specification of PCT6 pin operation mode
0	I/O port
1	ASTB output

PMCCT4	Specification of PCT4 pin operation mode
0	I/O port
1	$\overline{RD}$ output

PMCCT1	Specification of PCT1 pin operation mode
0	I/O port
1	$\overline{WR1}$ output

PMCCT0	Specification of PCT0 pin operation mode
0	I/O port
1	$\overline{WR0}$ output

(4) Pull-up resistor option register CT (PUCT)

After reset: 00H R/W Address: FFFFFF4AH

	7	6	5	4	3	2	1	0
PUCT	0	PUCT6	0	PUCT4	0	0	PUCT1	PUCT0

PUCTn	Control of on-chip pull-up resistor connection (n = 0, 1, 4, 6)
0	Not connected
1	Connected

4.3.11 Port DH

Port DH is a 6-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port DH includes the following alternate functions.

Table 4-14. Alternate-Function Pins of Port DH

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
87	89	PDH0	A16	Output	Yes	–	D0-UZ
88	90	PDH1	A17	Output			D0-UZ
89	91	PDH2	A18	Output			D0-UZ
90	92	PDH3	A19	Output			D0-UZ
91	93	PDH4	A20	Output			D0-UZ
92	94	PDH5	A21	Output			D0-UZ

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port DH register (PDH)

After reset: 00H (output latch) R/W Address: FFFFF006H

	7	6	5	4	3	2	1	0
PDH	0	0	PDH5	PDH4	PDH3	PDH2	PDH1	PDH0

PDHn	Control of output data (in output mode) (n = 0 to 5)
0	0 is output
1	1 is output

(2) Port DH mode register (PMDH)

After reset: FFH R/W Address: FFFFF026H

	7	6	5	4	3	2	1	0
PMDH	1	1	PMDH5	PMDH4	PMDH3	PMDH2	PMDH1	PMDH0

PMDHn	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

(3) Port DH mode control register (PMCDH)

After reset: 00H R/W Address: FFFFF046H

	7	6	5	4	3	2	1	0
PMCDH	0	0	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0

PMCDHn	Specification of PDHn pin operation mode (n = 0 to 5)
0	I/O port
1	Am output (address bus output) (m = 16 to 21)

Caution When specifying the port/alternate function for each bit, pay careful attention to the operation of the alternate functions.

(4) Pull-up resistor option register DH (PUDH)

After reset: 00H R/W Address: FFFFFF46H

	7	6	5	4	3	2	1	0
PUDH	0	0	PUDH5	PUDH4	PUDH3	PUDH2	PUDH1	PUDH0

PUDHn	Control of on-chip pull-up resistor connection (n = 0 to 5)
0	Not connected
1	Connected

4.3.12 Port DL

Port DL is a 16-bit I/O port for which I/O settings can be controlled in 1-bit units.

Port DL includes the following alternate functions.

Table 4-15. Alternate-Function Pins of Port DL

Pin No.		Pin Name	Alternate Function	I/O	PULL[Note]	Remark	Block Type
GC	GF						
71	73	PDL0	AD0	I/O	Yes	–	D2-ULZ
72	74	PDL1	AD1	I/O			D2-ULZ
73	75	PDL2	AD2	I/O			D2-ULZ
74	76	PDL3	AD3	I/O			D2-ULZ
75	77	PDL4	AD4	I/O			D2-ULZ
76	78	PDL5	AD5	I/O			D2-ULZ
77	79	PDL6	AD6	I/O			D2-ULZ
78	80	PDL7	AD7	I/O			D2-ULZ
79	81	PDL8	AD8	I/O			D2-ULZ
80	82	PDL9	AD9	I/O			D2-ULZ
81	83	PDL10	AD10	I/O			D2-ULZ
82	84	PDL11	AD11	I/O			D2-ULZ
83	85	PDL12	AD12	I/O			D2-ULZ
84	86	PDL13	AD13	I/O			D2-ULZ
85	87	PDL14	AD14	I/O			D2-ULZ
86	88	PDL15	AD15	I/O			D2-ULZ

Note Software pull-up function

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

(1) Port DL register (PDL)

After reset: 00H (output latch) R/W Address: PDL FFFFF004H,
PDLL FFFFF004H, PDLH FFFFF005H

	15	14	13	12	11	10	9	8
PDL (PDLH[Note])	PDL15	PDL14	PDL13	PDL12	PDL11	PDL10	PDL9	PDL8

	7	6	5	4	3	2	1	0
(PDLL)	PDL7	PDL6	PDL5	PDL4	PDL3	PDL2	PDL1	PDL0

PDLn	Control of output data (in output mode) (n = 0 to 15)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the PDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PDLH register.

Remark The PDL register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PDL register are used as the PDLH register and as the PDLL register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(2) Port DL mode register (PMDL)

After reset: FFFFH R/W Address: PMDL FFFFF024H,
PMDLL FFFFF024H, PMDLH FFFFF025H

	15	14	13	12	11	10	9	8
PMDL (PMDLH[Note])	PMDL15	PMDL14	PMDL13	PMDL12	PMDL11	PMDL10	PMDL9	PMDL8

	7	6	5	4	3	2	1	0
(PMDLL)	PMDL7	PMDL6	PMDL5	PMDL4	PMDL3	PMDL2	PMDL1	PMDL0

PMDLn	Control of I/O mode (n = 0 to 15)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PMDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMDLH register.

Remark The PMDL register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PMDL register are used as the PMDLH register and as the PMDLL register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(3) Port DL mode control register (PMCDL)

After reset: 0000H R/W Address: PMCDL FFFFF044H,
PMCDLL FFFFF044H, PMCDLH FFFFF045H

	15	14	13	12	11	10	9	8
PMCDL (PMCDLH[Note])	PMCDL15	PMCDL14	PMCDL13	PMCDL12	PMCDL11	PMCDL10	PMCDL9	PMCDL8

	7	6	5	4	3	2	1	0
(PMCDLL)	PMCDL7	PMCDL6	PMCDL5	PMCDL4	PMCDL3	PMCDL2	PMCDL1	PMCDL0

PMCDLn	Specification of PDLn pin operation mode (n = 0 to 15)
0	I/O port
1	ADn I/O (address/data bus I/O)

Note When reading from or writing to bits 8 to 15 of the PMCDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMCDLH register.

Caution When specifying the port/alternate function for each bit, pay careful attention to the operation of the alternate functions.

Remark The PMCDL register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PMCDL register are used as the PMCDLH register and as the PMCDLL register, respectively, these registers can be read or written in 8-bit or 1-bit units.

(4) Pull-up resistor option register DL (PUDL)

After reset: 0000H R/W Address: PUDL FFFFFF44H,
PUDLL FFFFFF44H, PUDLH FFFFFF45H

	15	14	13	12	11	10	9	8
PUDL (PUDLH[Note])	PUDL15	PUDL14	PUDL13	PUDL12	PUDL11	PUDL10	PUDL9	PUDL8

	7	6	5	4	3	2	1	0
(PUDLL)	PUDL7	PUDL6	PUDL5	PUDL4	PUDL3	PUDL2	PUDL1	PUDL0

PUDLn	Control of on-chip pull-up resistor connection (n = 0 to 15)
0	Not connected
1	Connected

Note When reading from or writing to bits 8 to 15 of the PUDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PUDLH register.

Remark The PUDL register can be read or written in 16-bit units.
However, when the higher 8 bits and the lower 8 bits of the PUDL register are used as the PUDLH register and as the PUDLL register, respectively, these registers can be read or written in 8-bit or 1-bit units.

4.4 Block Diagrams

Figure 4-2. Block Diagram of Type A-A

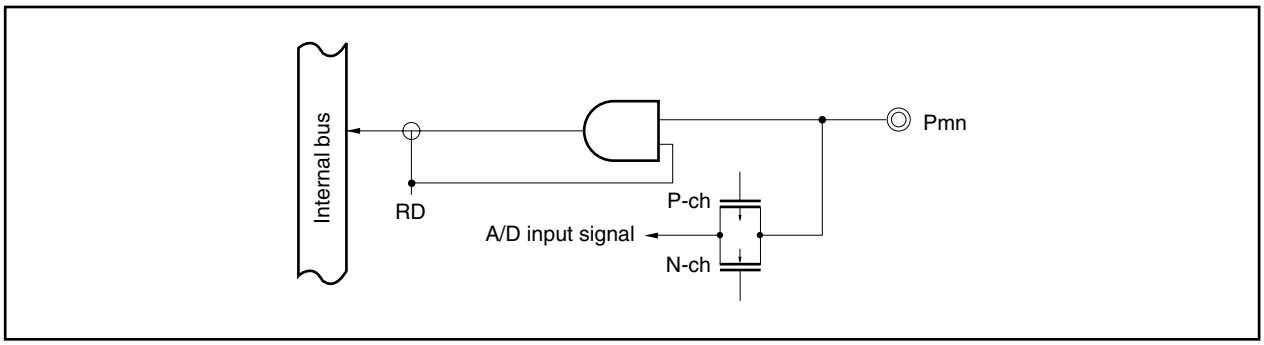


Figure 4-3. Block Diagram of Type C-N

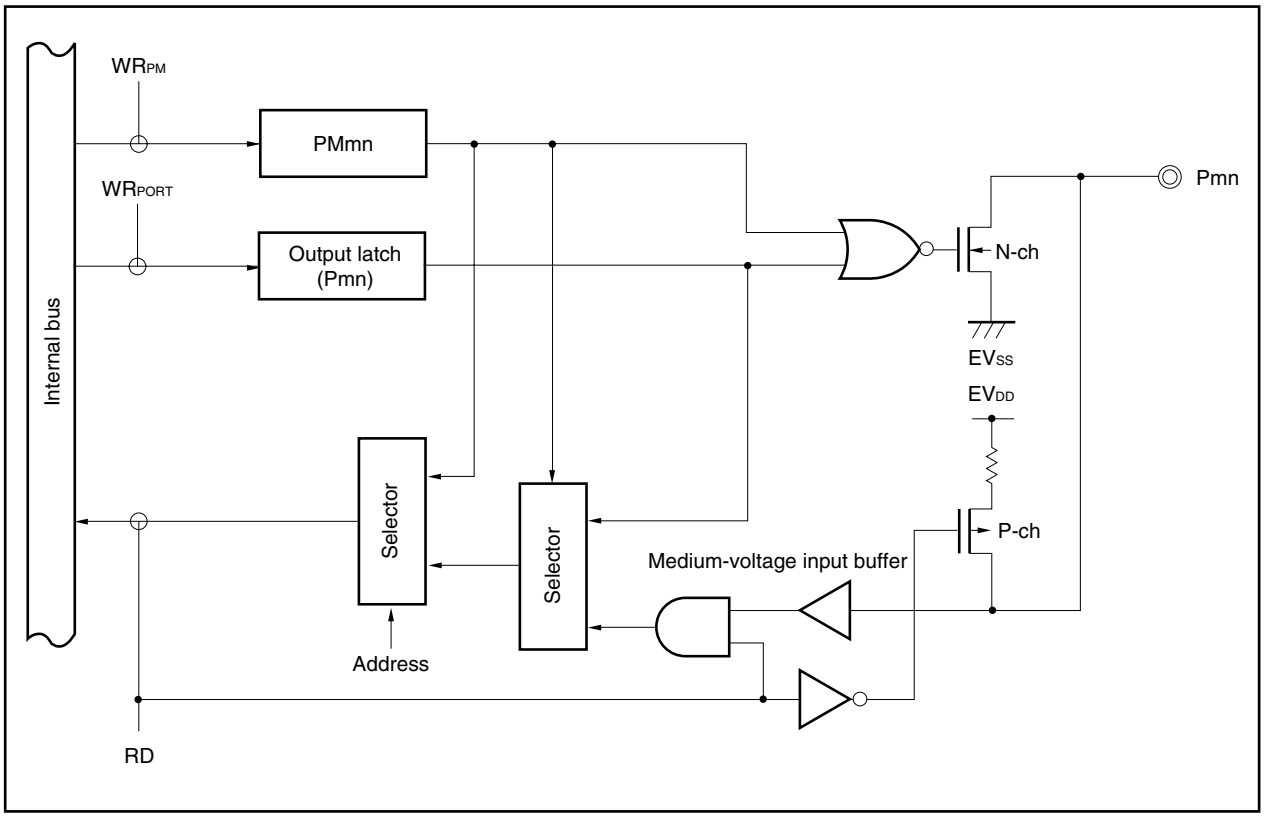


Figure 4-4. Block Diagram of Type C-UA

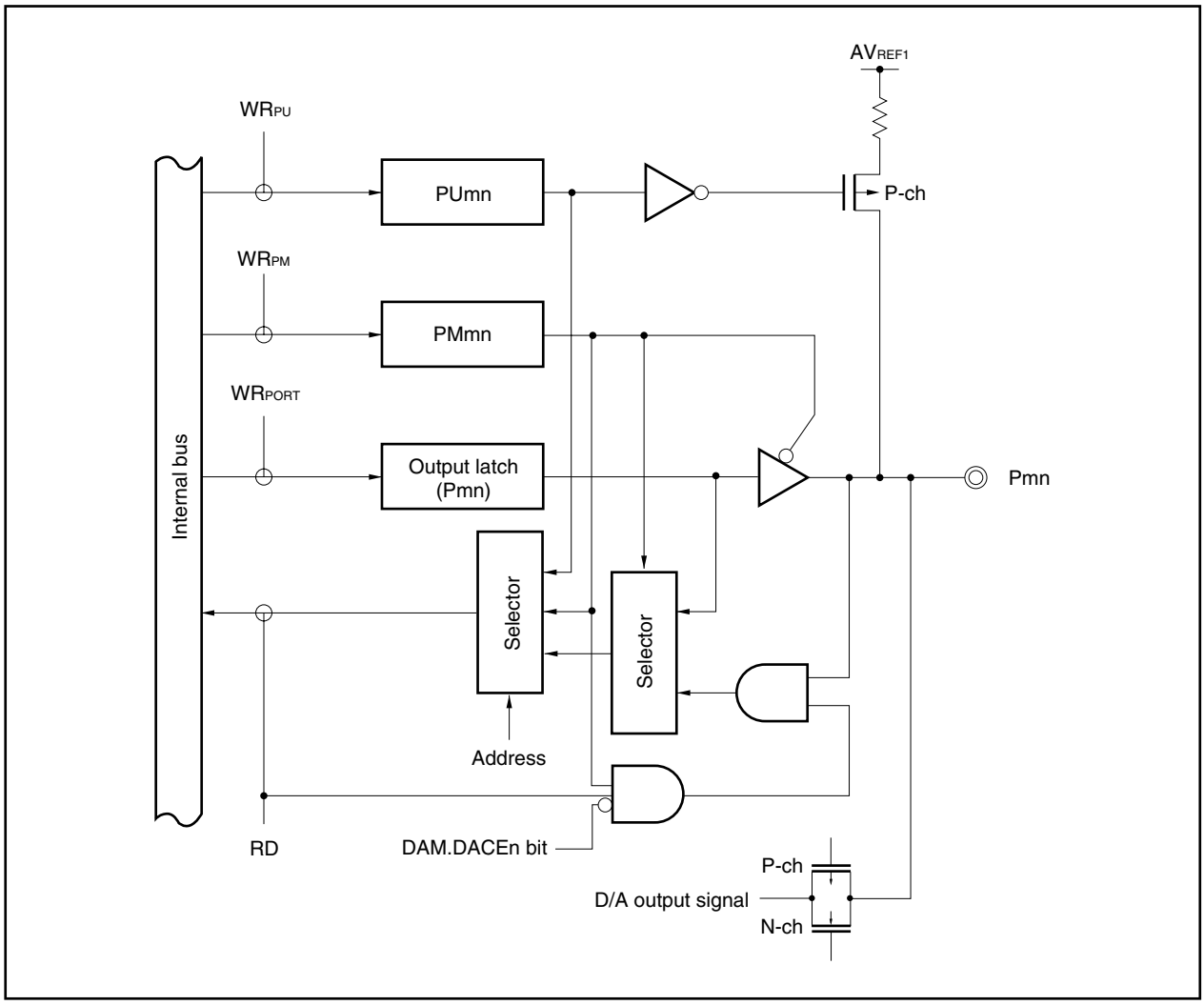
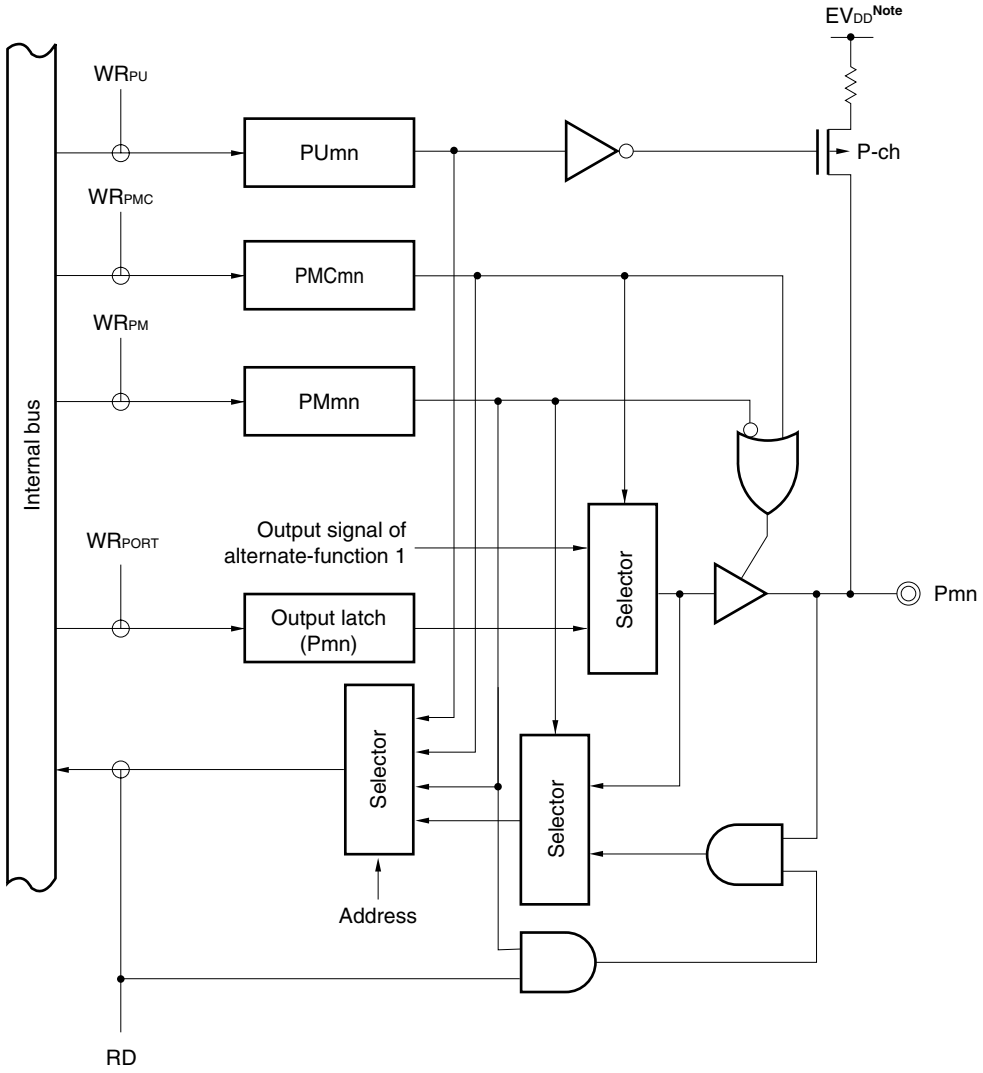
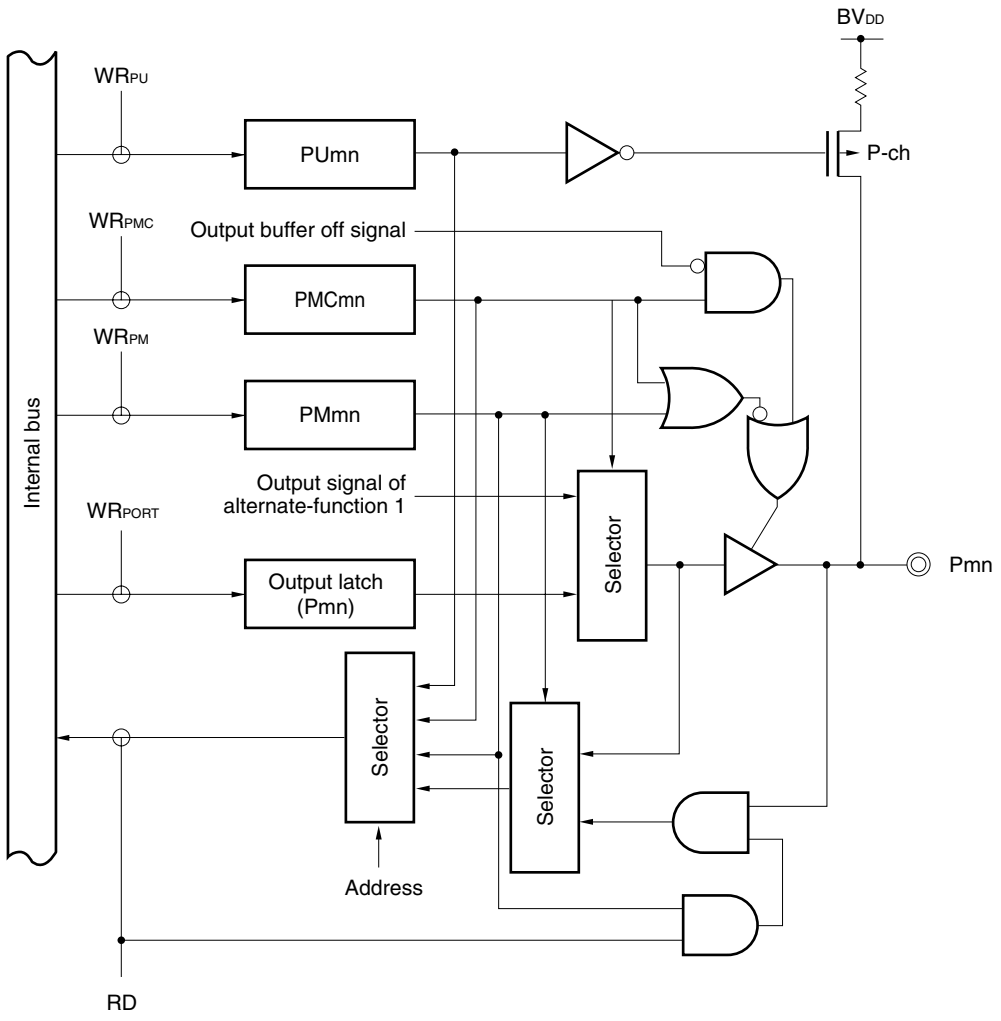


Figure 4-5. Block Diagram of Type D0-U



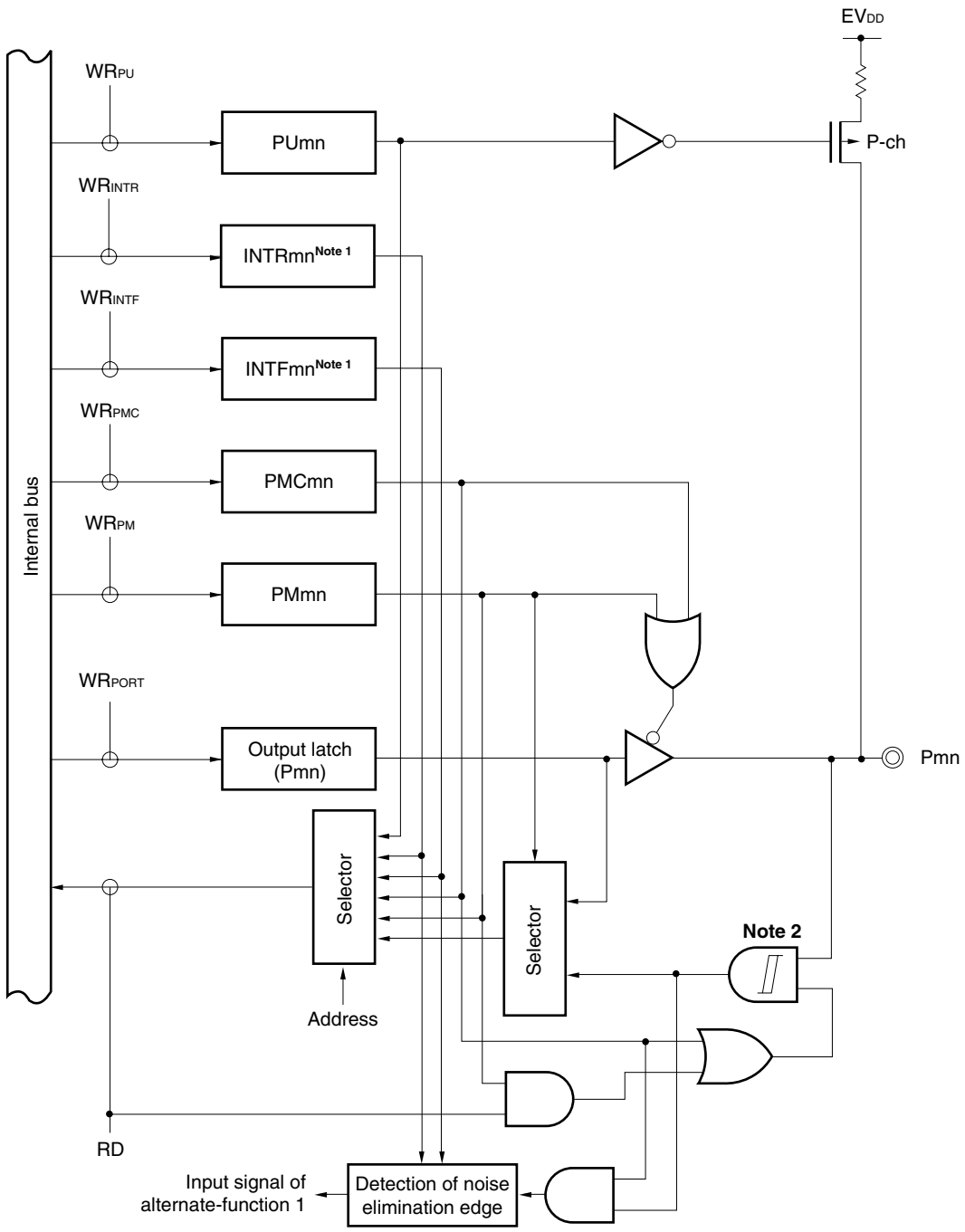
Note BV_{DD} in the case of PCM1 and PCM2

Figure 4-6. Block Diagram of Type D0-UZ



Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

Figure 4-7. Block Diagram of Type D1-SUIL



Notes 1. Refer to **21.4 External Interrupt Request Input Pins (NMI, INTP0 to INTP7**).

2. There are no hysteresis characteristics in the port mode.

Figure 4-8. Block Diagram of Type D1-UH

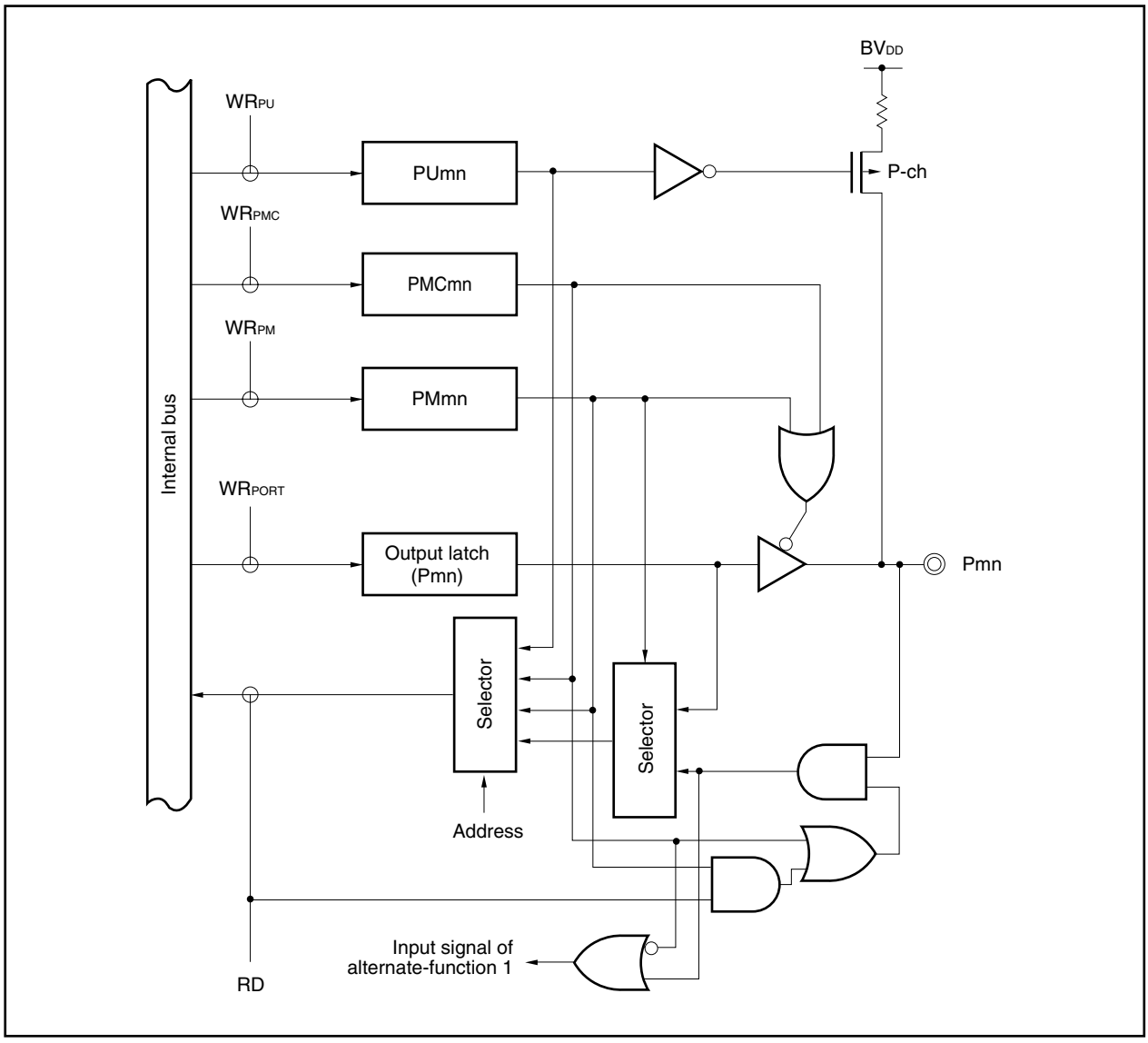
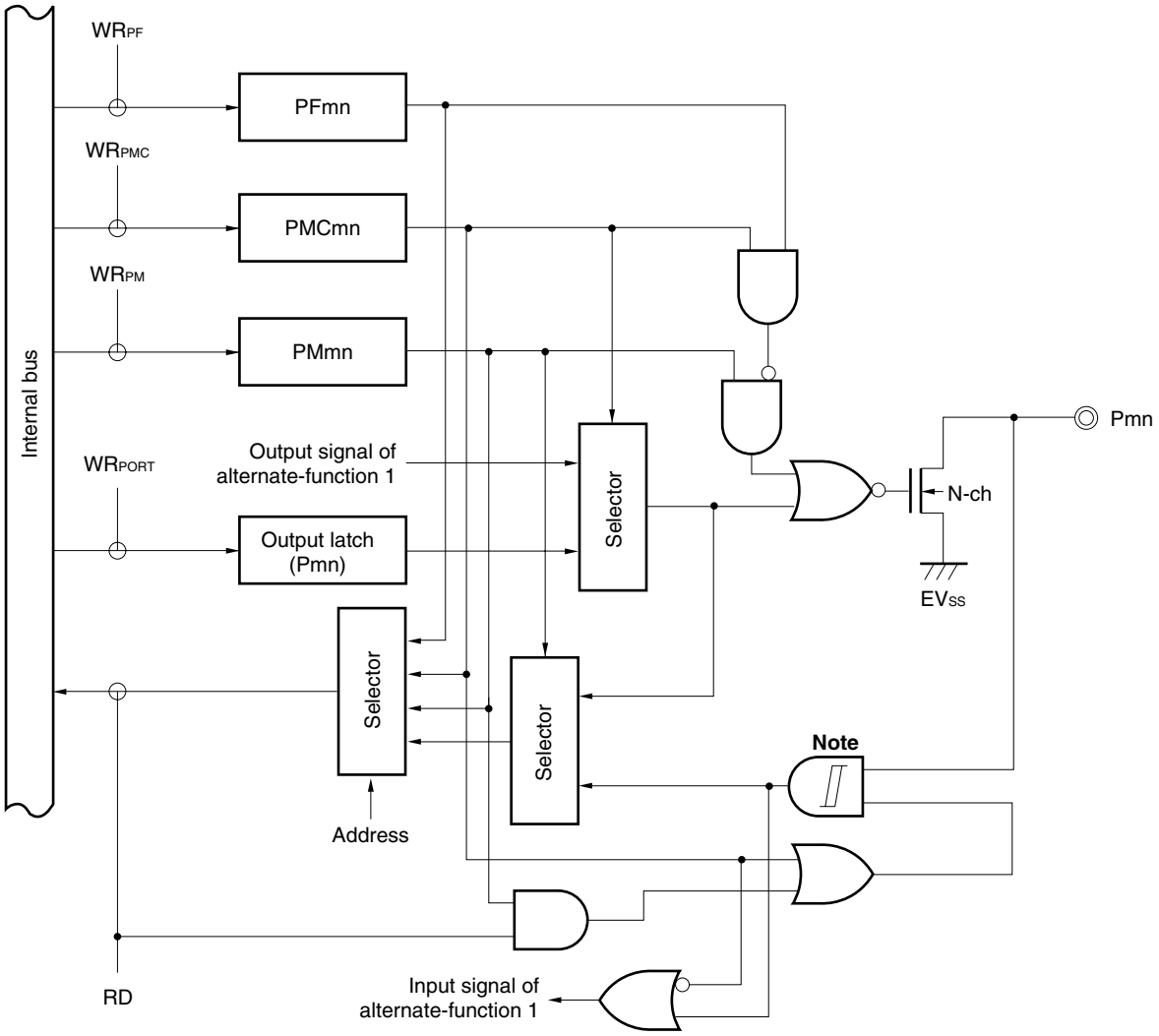
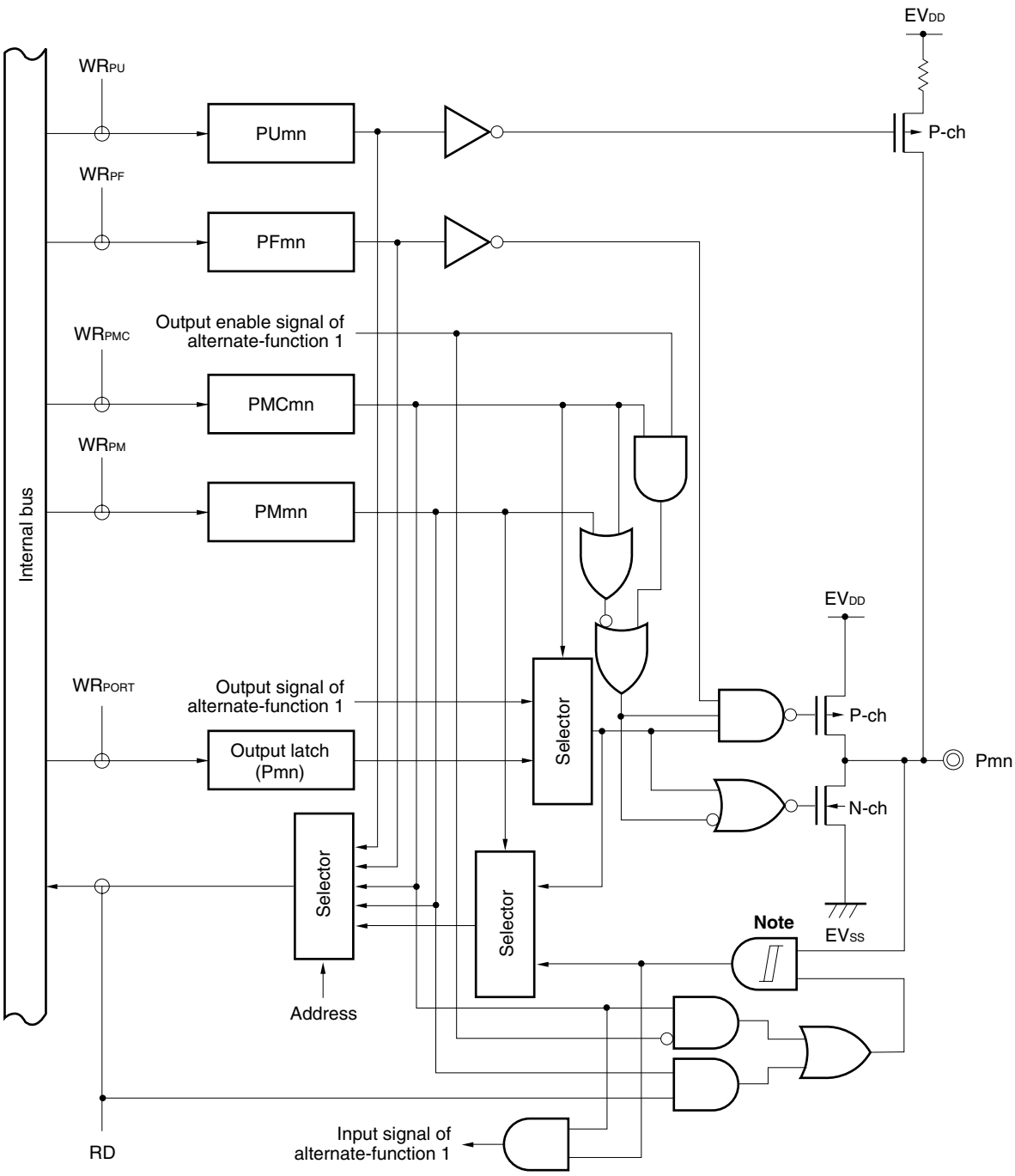


Figure 4-9. Block Diagram of Type D2-SNFH



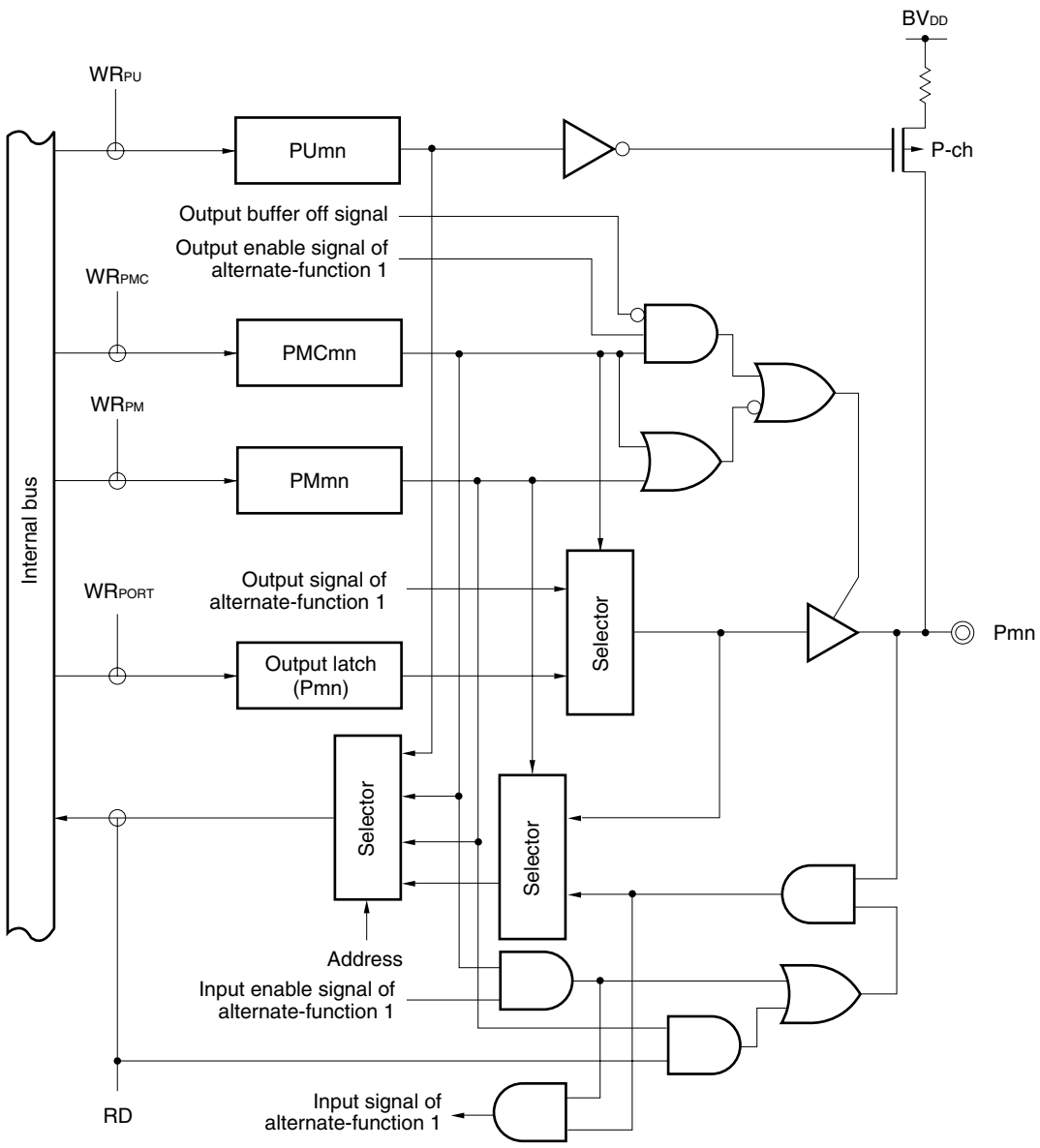
Note There are no hysteresis characteristics in the port mode.

Figure 4-10. Block Diagram of Type D2-SUFL



Note There are no hysteresis characteristics in the port mode.

Figure 4-11. Block Diagram of Type D2-ULZ



Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

Figure 4-12. Block Diagram of Type E00-SUFT

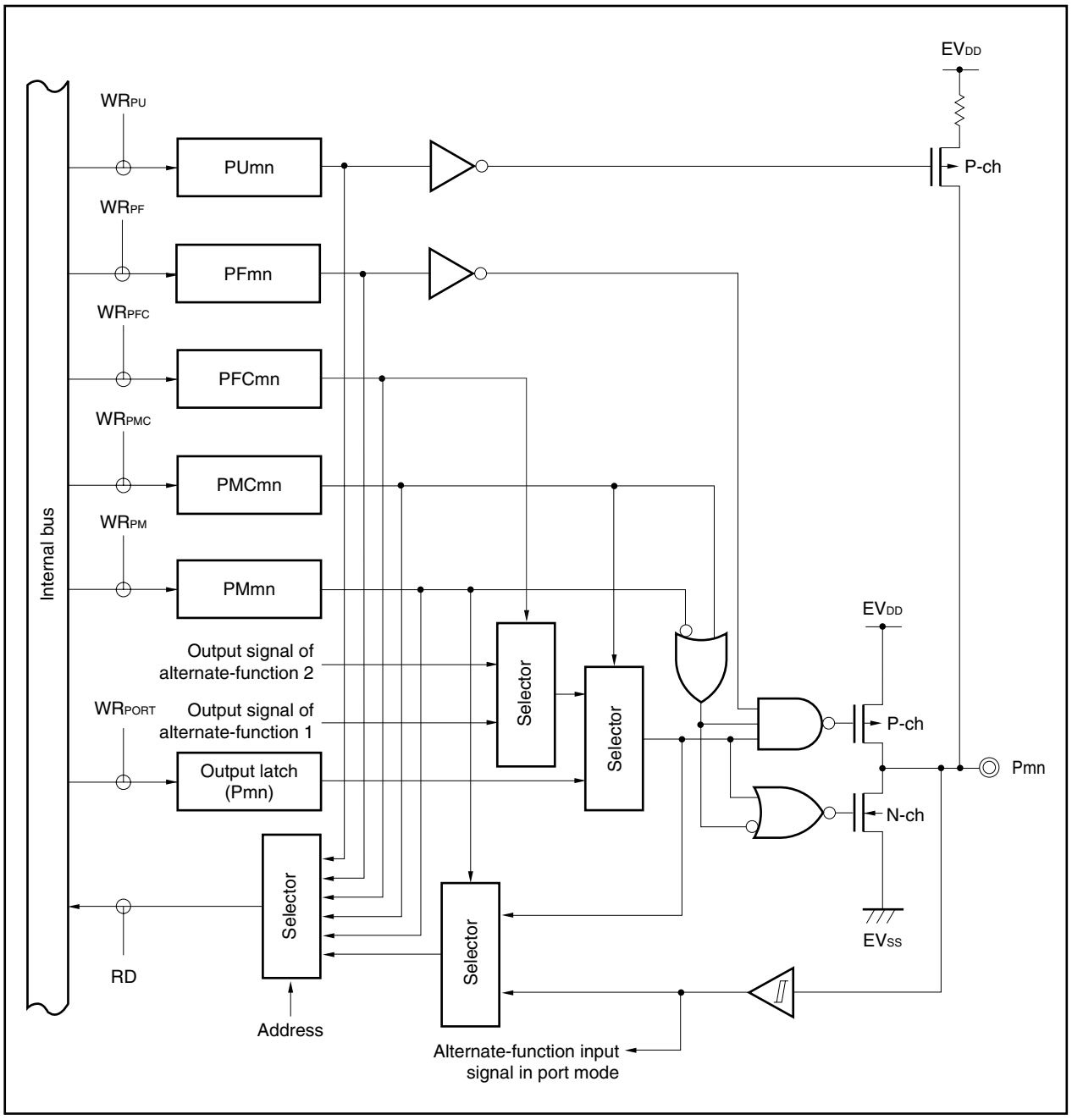


Figure 4-13. Block Diagram of Type E00-SUT

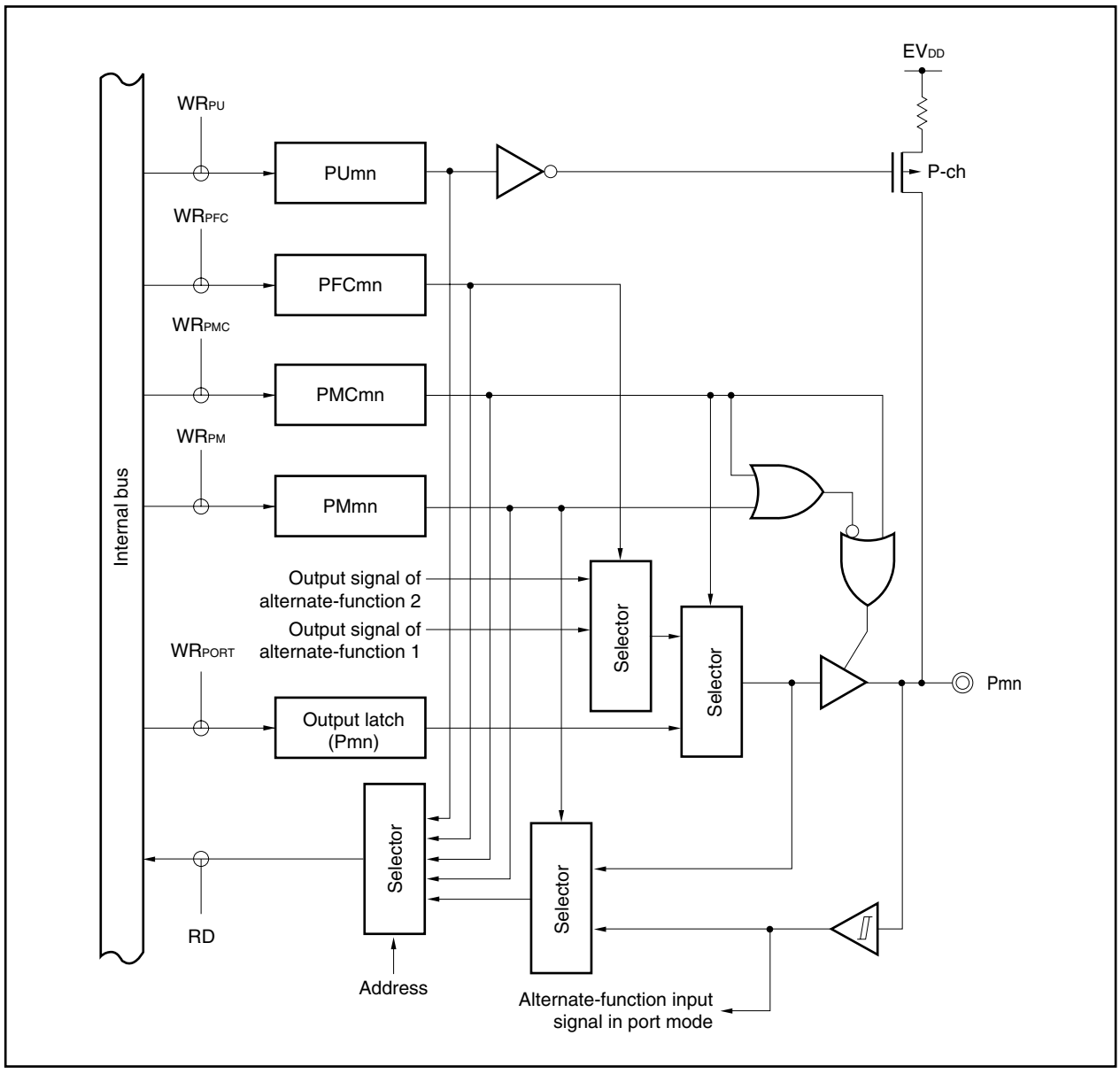
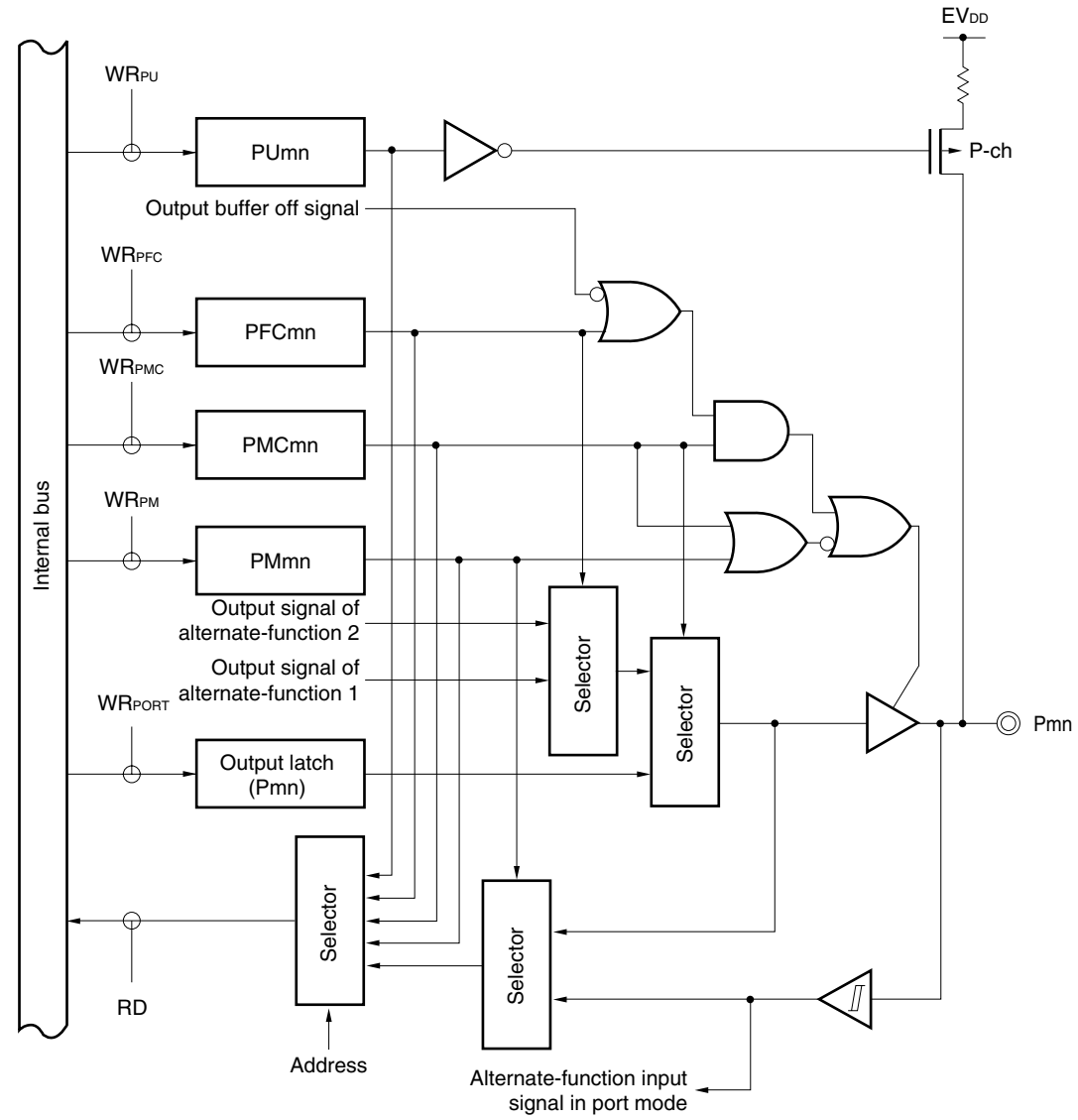


Figure 4-14. Block Diagram of Type E00-SUTZ



Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

Figure 4-15. Block Diagram of Type E00-U

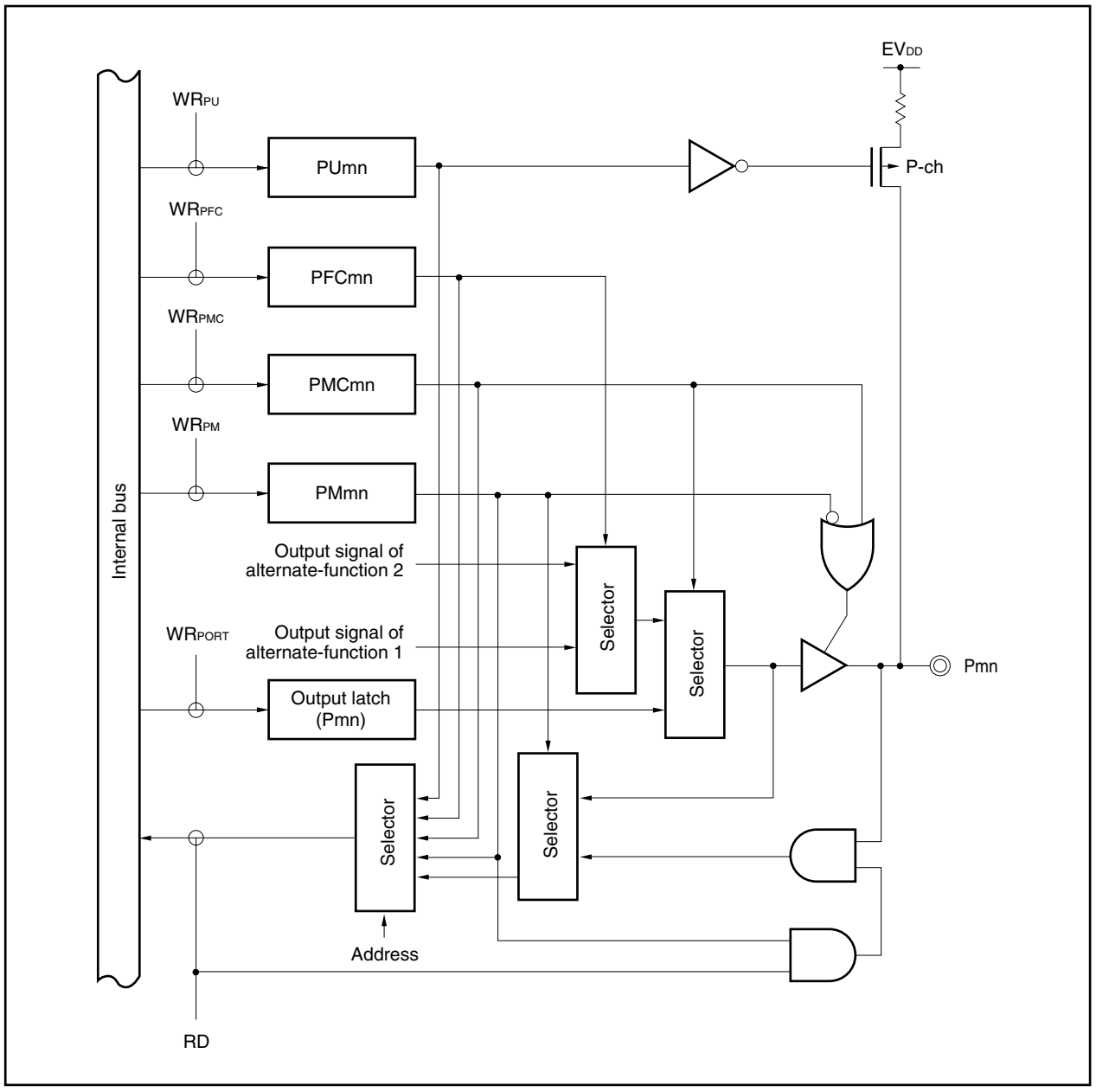


Figure 4-16. Block Diagram of Type E00-UF

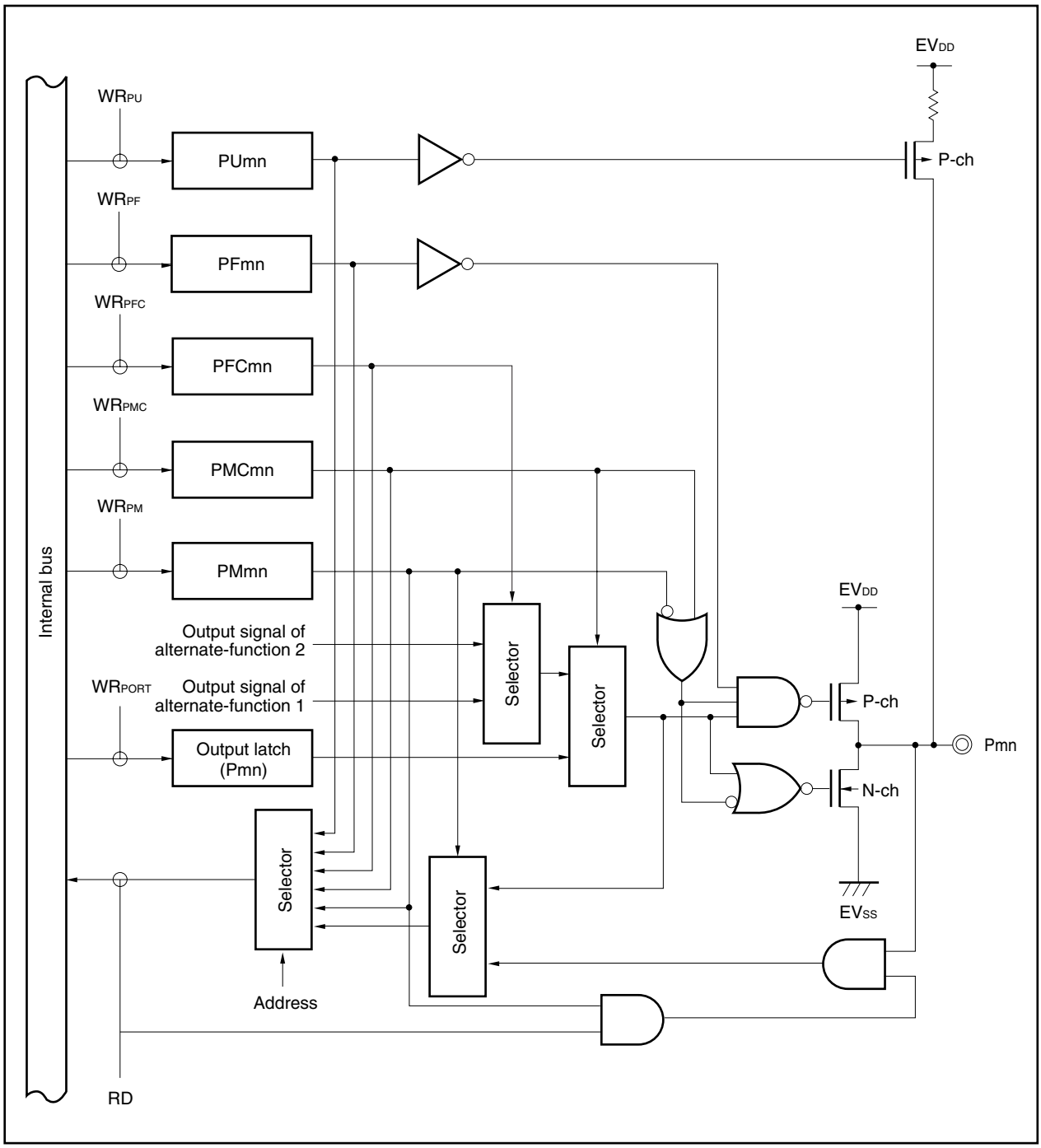
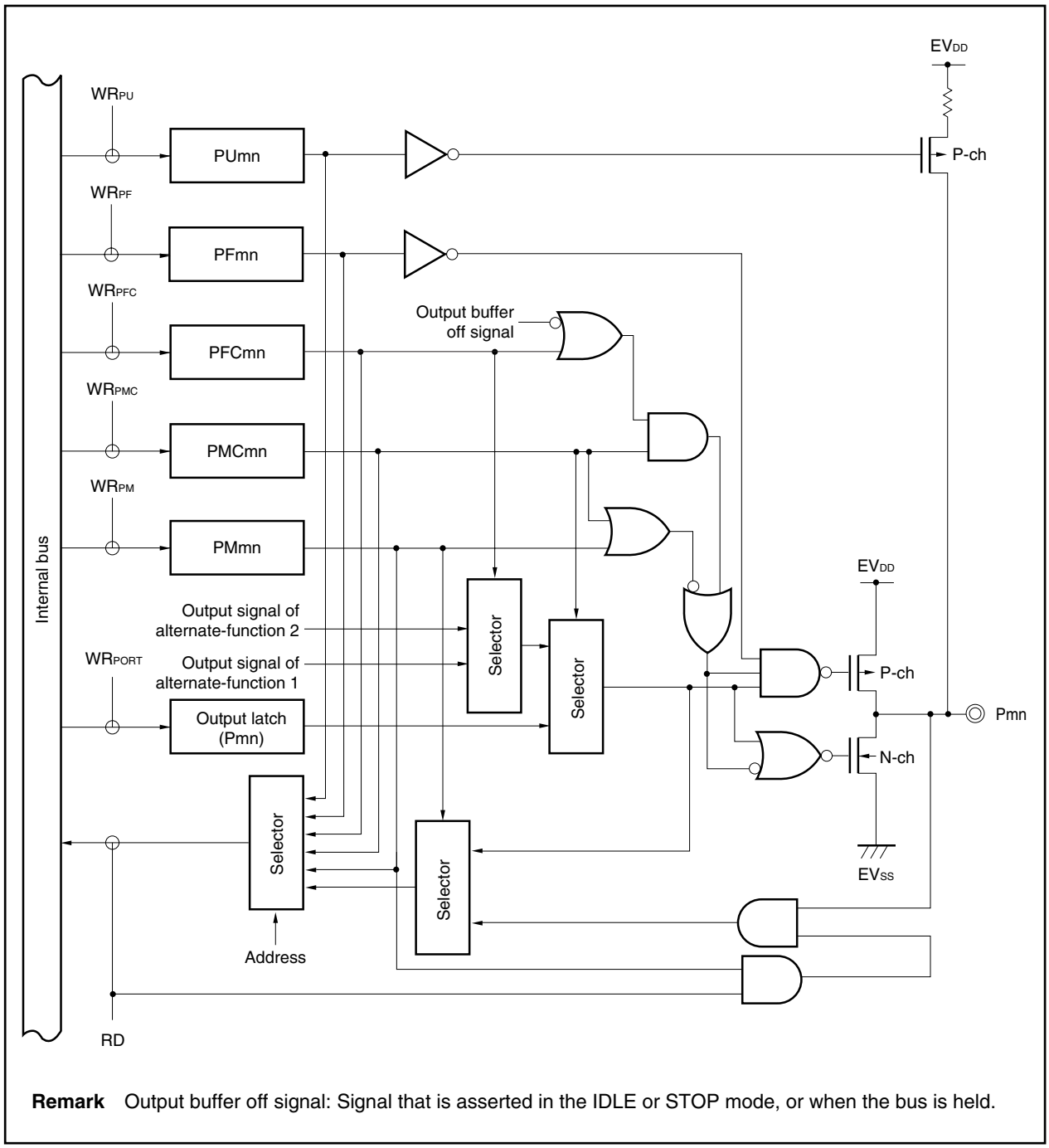
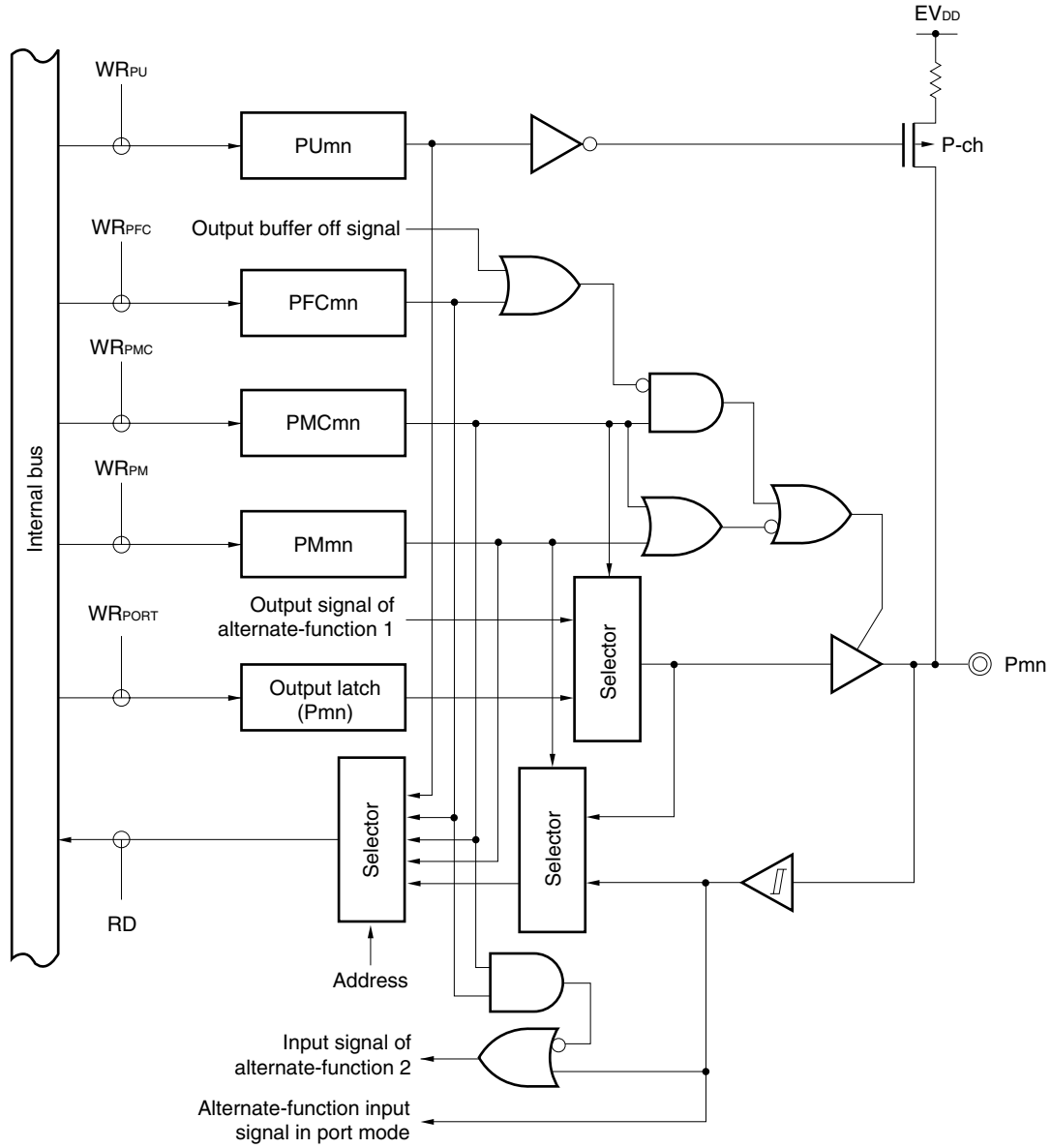


Figure 4-17. Block Diagram of Type E00-UFZ



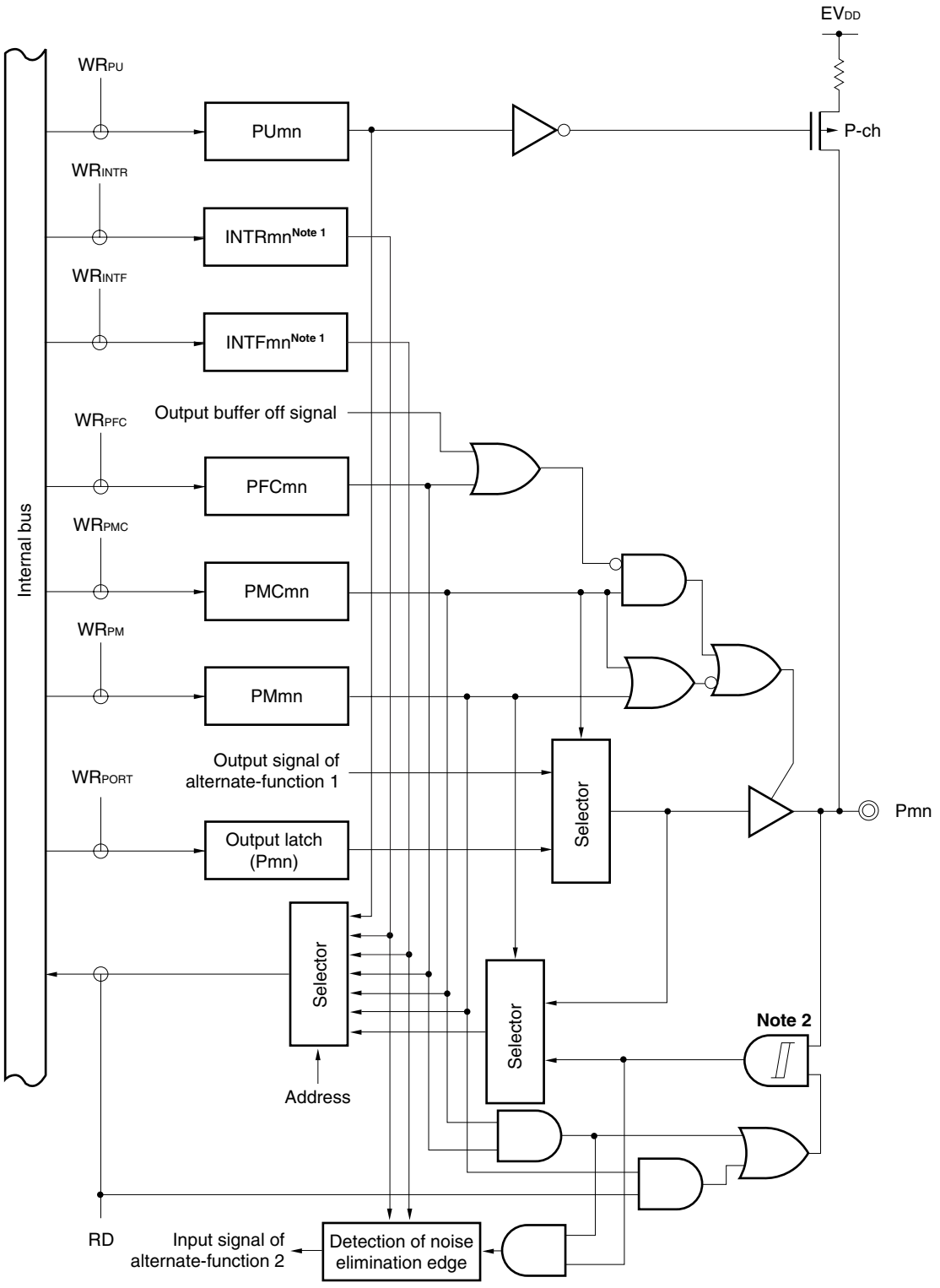
Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

Figure 4-18. Block Diagram of Type E01-SUHTZ



Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

Figure 4-19. Block Diagram of Type E01-SUILZ

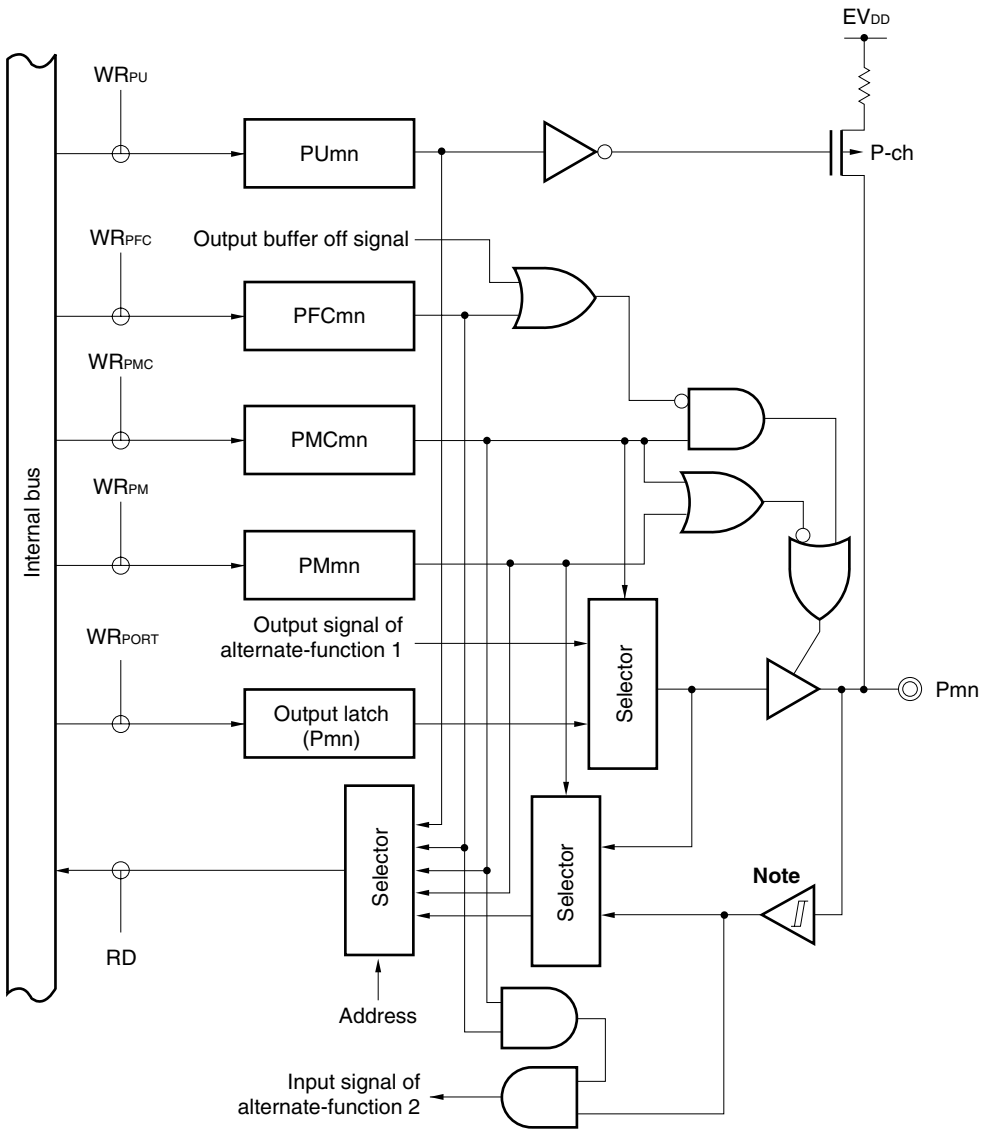


Notes 1. Refer to **21.4 External Interrupt Request Input Pins (NMI, INTP0 to INTP7)**.

2. There are no hysteresis characteristics in the port mode.

Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

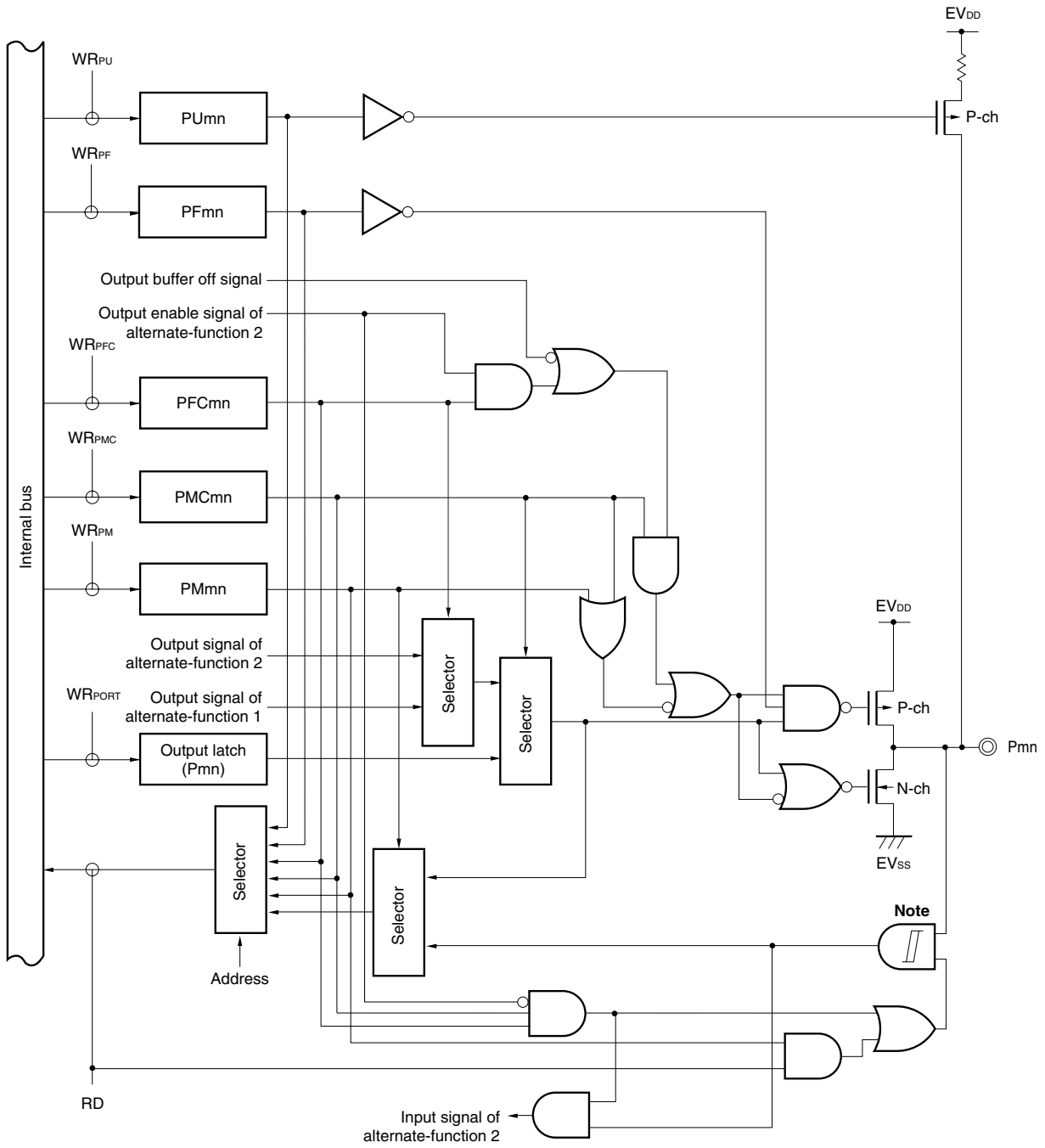
Figure 4-20. Block Diagram of Type E01-SULZ



Note There are no hysteresis characteristics in the port mode.

Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

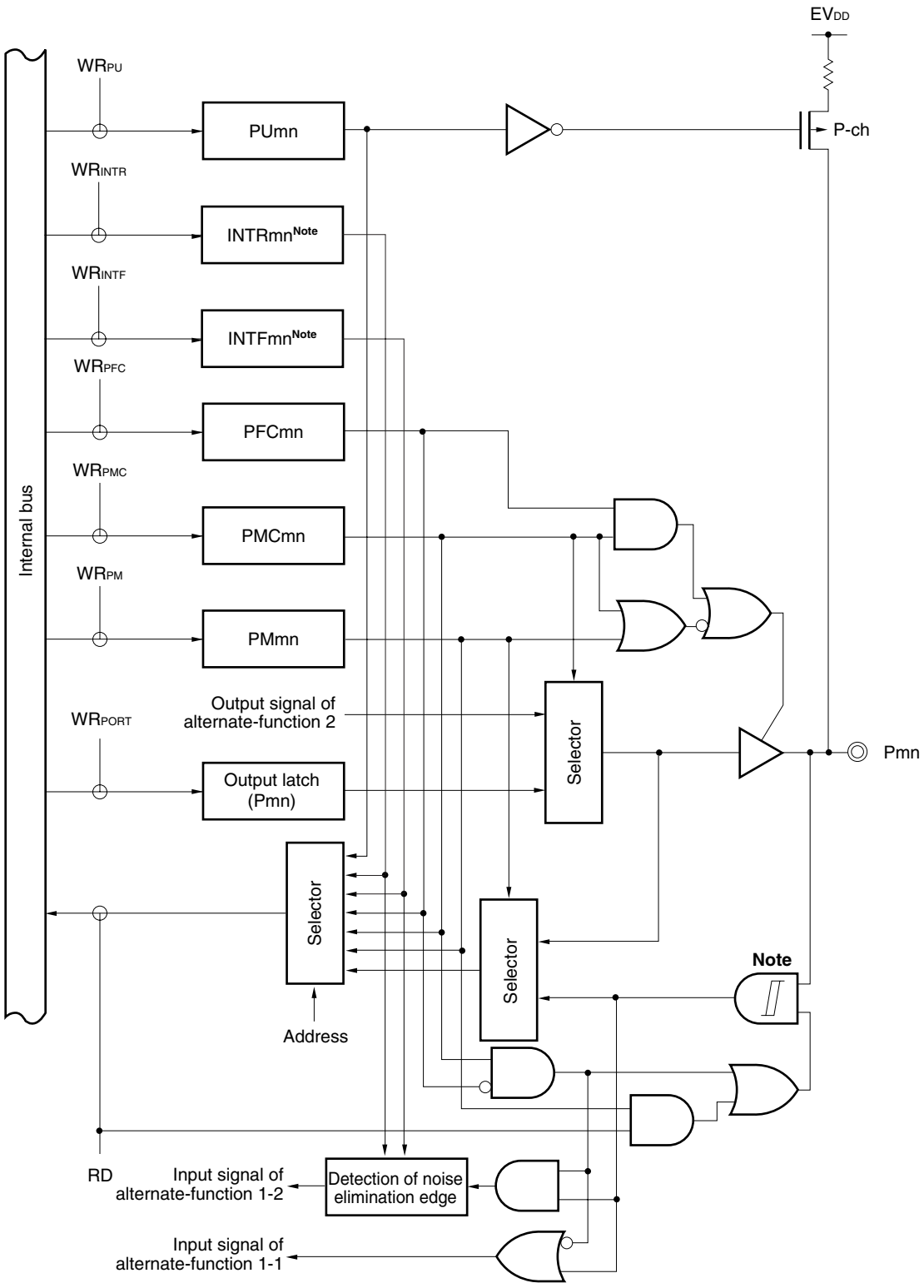
Figure 4-21. Block Diagram of Type E02-SUFLZ



Note There are no hysteresis characteristics in the port mode.

Remark Output buffer off signal: Signal that is asserted in the IDLE or STOP mode, or when the bus is held.

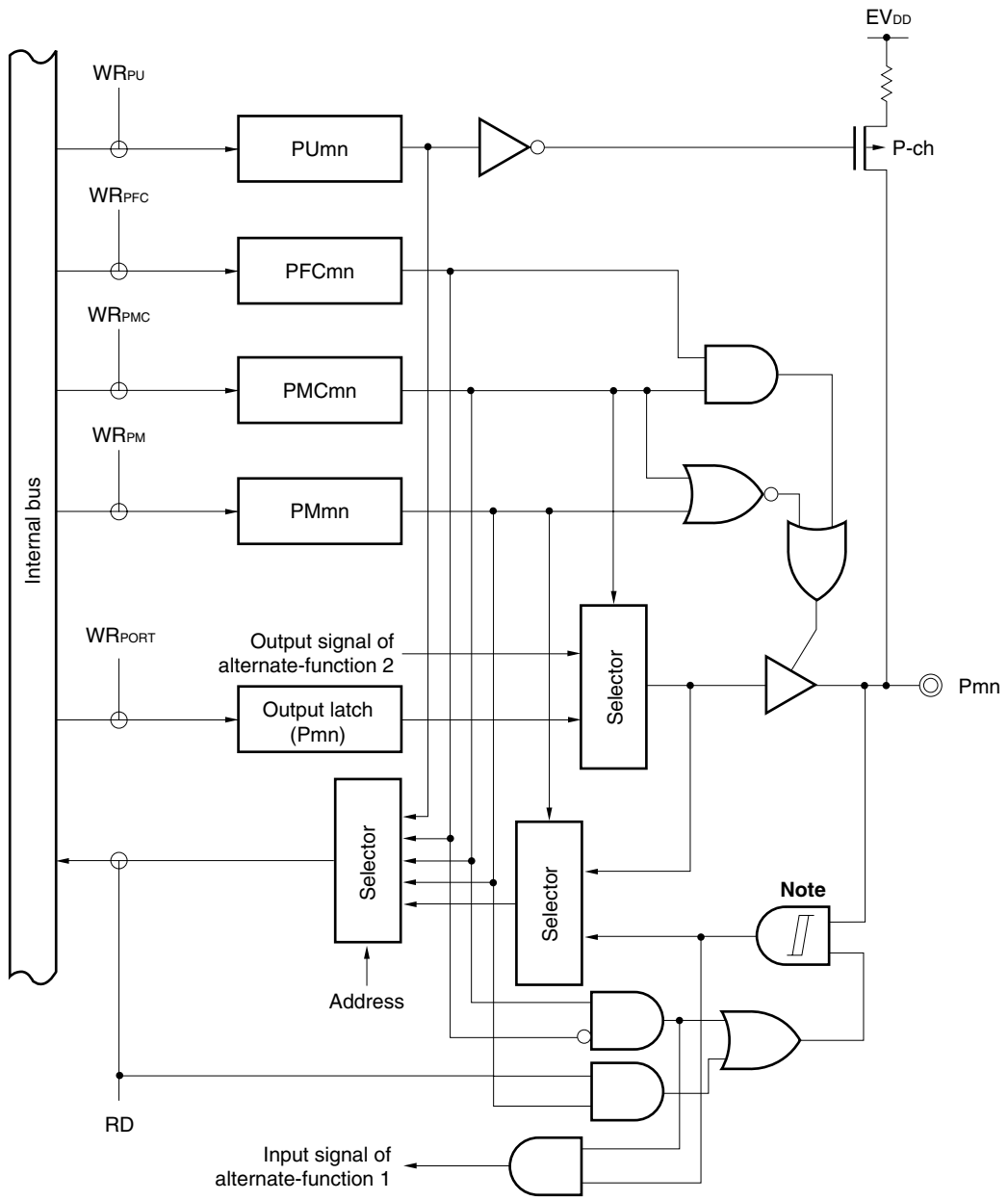
Figure 4-22. Block Diagram of Type E10-SUIHL



Note There are no hysteresis characteristics in the port mode.

Remark Alternate-function 1-1: RXD0 pin
Alternate-function 1-2: INTP7 pin

Figure 4-23. Block Diagram of Type E10-SUL



Note There are no hysteresis characteristics in the port mode.

Figure 4-24. Block Diagram of Type E10-SULT

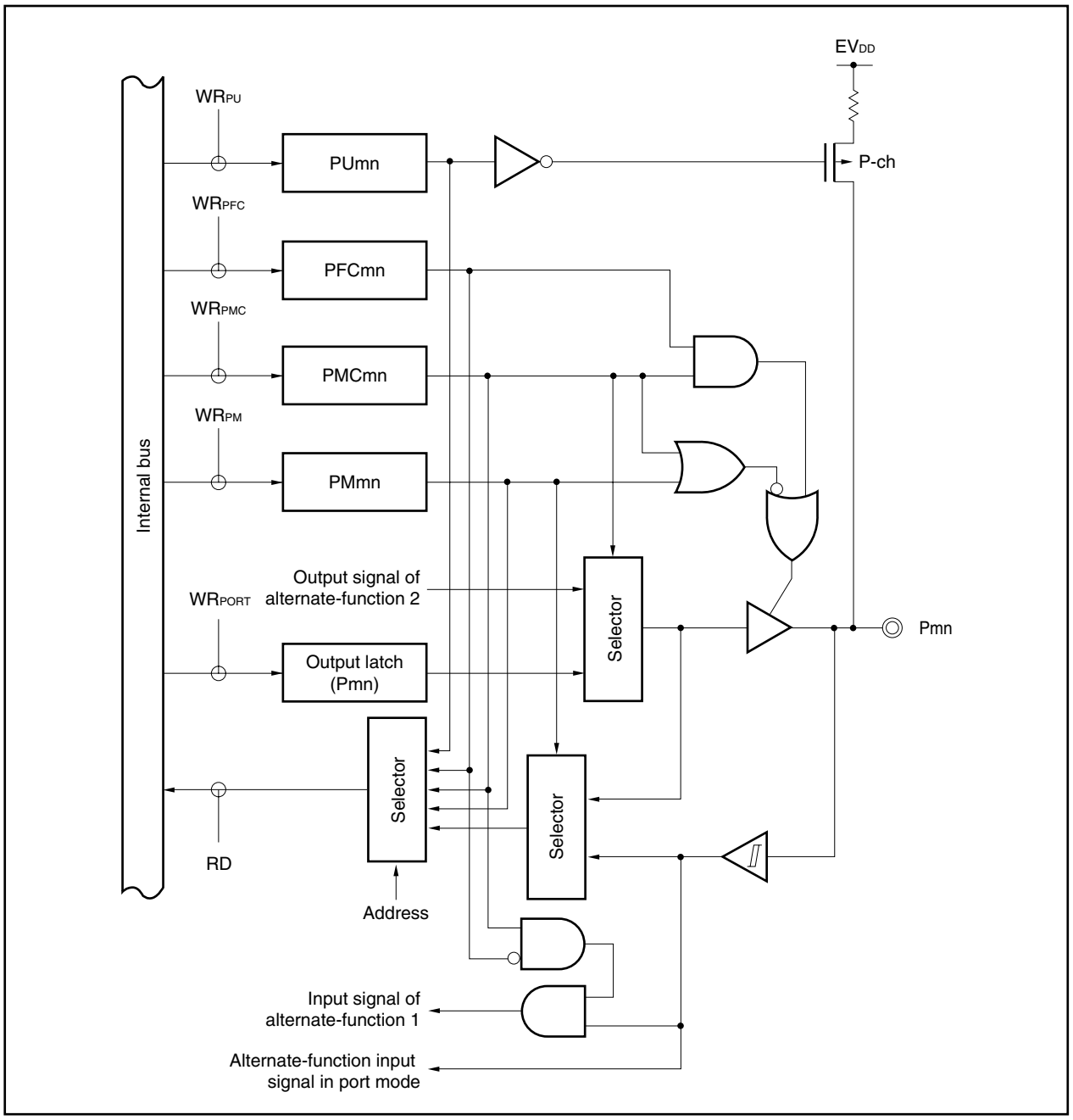
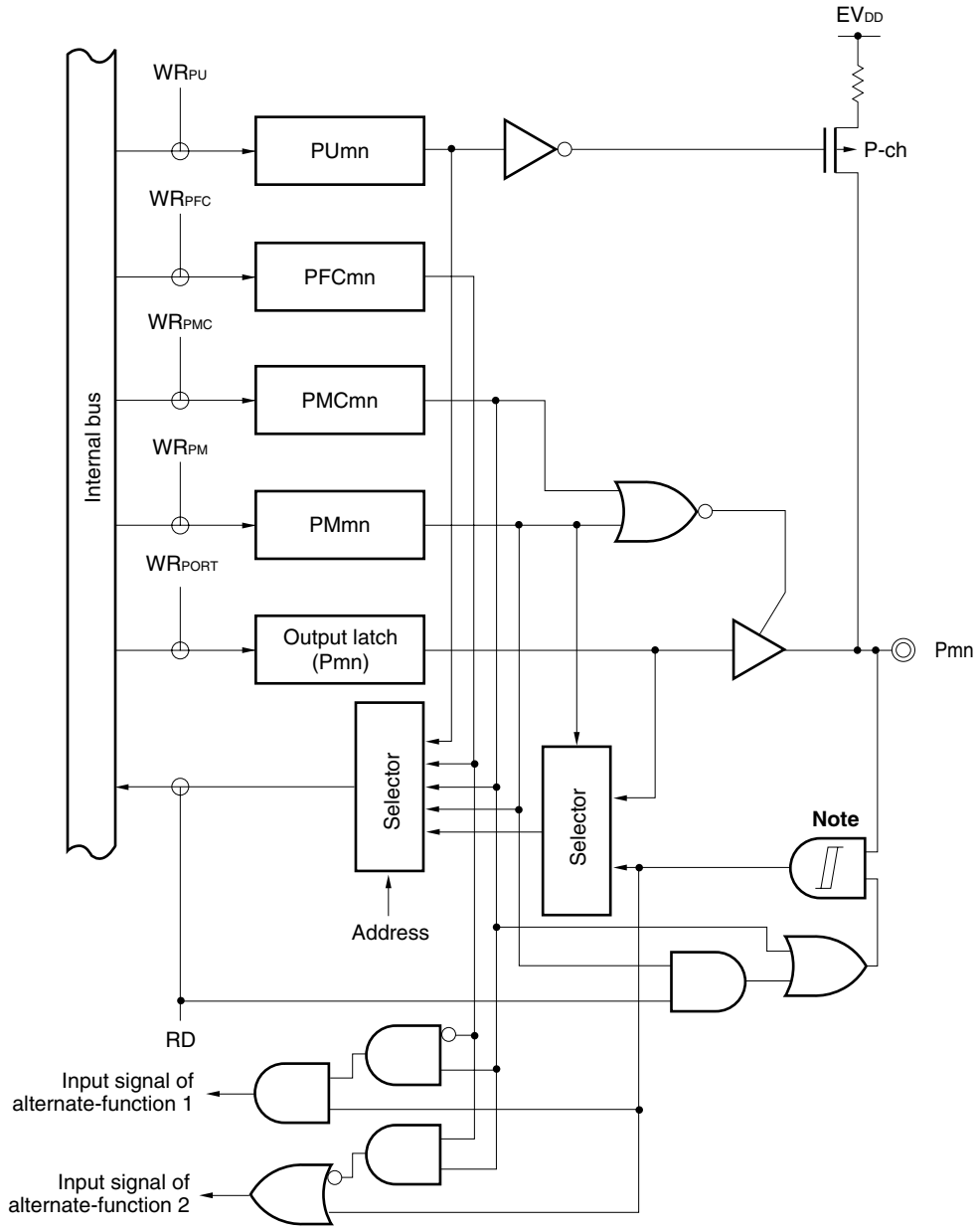


Figure 4-25. Block Diagram of Type E11-SULH



Note There are no hysteresis characteristics in the port mode.

Figure 4-26. Block Diagram of Type E20-SUFLT

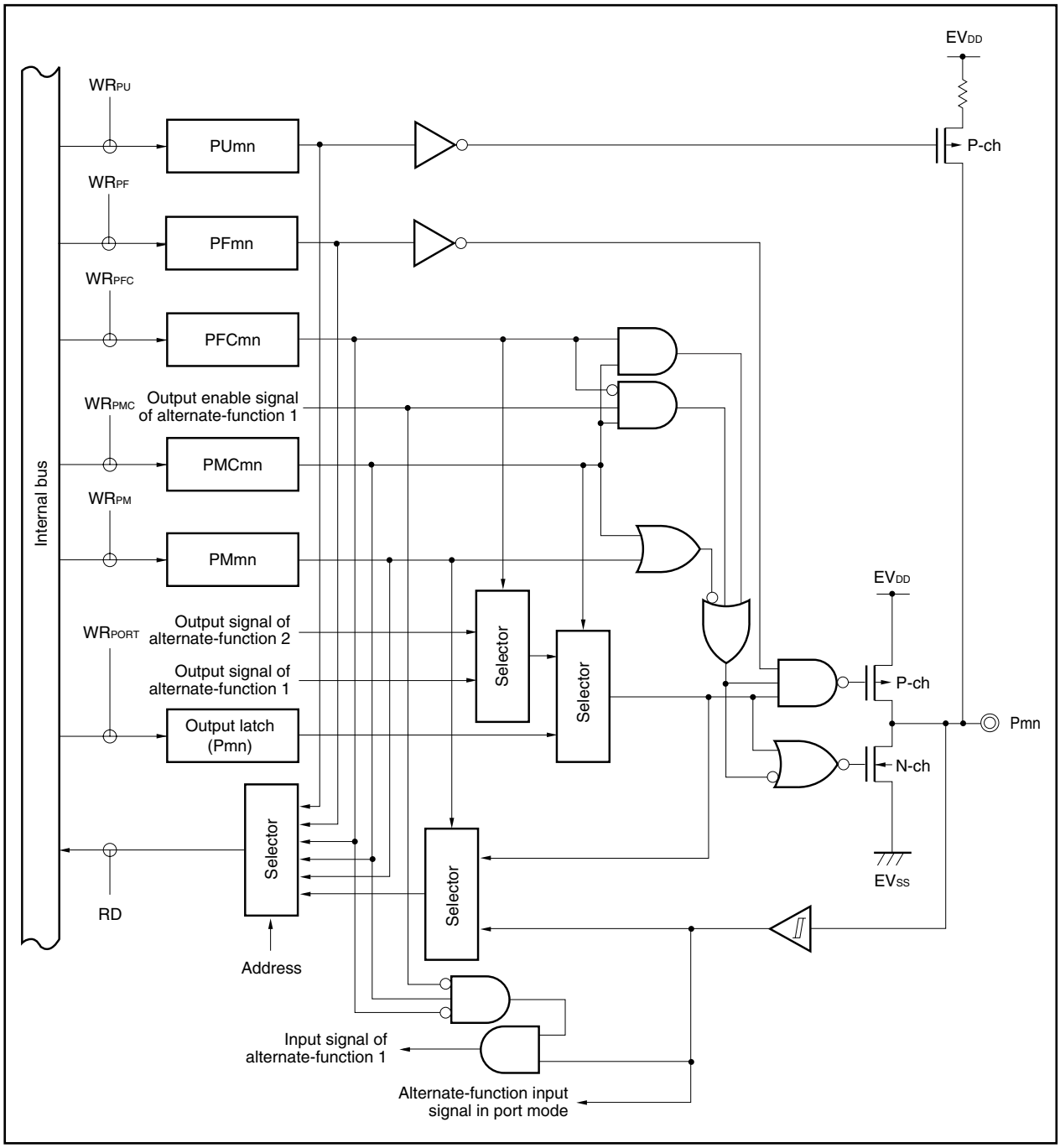
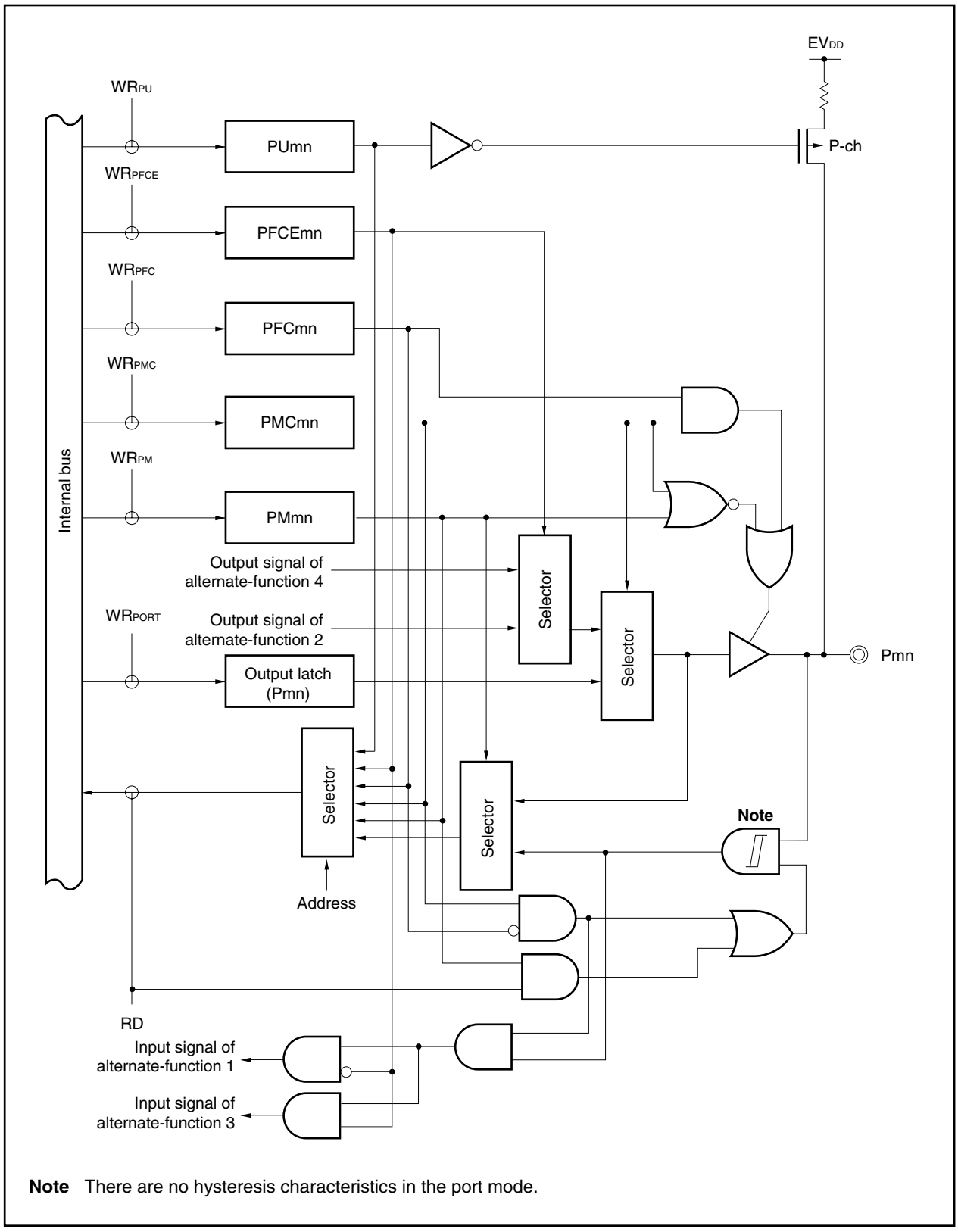


Figure 4-27. Block Diagram of Type G1010-SUL



Note There are no hysteresis characteristics in the port mode.

4.5 Port Register Setting When Alternate Function Is Used

Table 4-16 shows the port register settings when each port is used for an alternate function.
When using a port pin as an alternate-function pin, refer to description of each pin.

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (1/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O						
P00	TOH0	Output	P00 = Setting not required	PM00 = Setting not required	PMC00 = 1	–	–	–
P01	TOH1	Output	P01 = Setting not required	PM01 = Setting not required	PMC01 = 1	–	–	–
P02	NMI	Input	P02 = Setting not required	PM02 = Setting not required	PMC02 = 1	–	–	–
P03	INTP0	Input	P03 = Setting not required	PM03 = Setting not required	PMC03 = 1	–	PFC03 = 0	–
P04	INTP1	Input	P04 = Setting not required	PM04 = Setting not required	PMC04 = 1	–	–	–
P05	INTP2	Input	P05 = Setting not required	PM05 = Setting not required	PMC05 = 1	–	–	–
P06	INTP3	Input	P06 = Setting not required	PM06 = Setting not required	PMC06 = 1	–	–	–
P10	ANO0	Output	P10 = Setting not required	PM1 register = FFH[Note 1]	–	–	–	–
P11	ANO1	Output	P11 = Setting not required	PM1 register = FFH[Note 1]	–	–	–	–
P30	TXD0	Output	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	–	PFC30 = 0	–
	TO02	Output	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	–	PFC30 = 1	–
P31	RXD0	Input	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	–	**Note 2**, PFC31 = 0	–
	INTP7	Input	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	–	**Note 2**, PFC31 = 0	–
	TO03	Output	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	–	PFC31 = 1	–
P32	ASCK0	Input	P32 = Setting not required	PM32 = Setting not required	PMC32 = 1	–	**Note 3**, PFC32 = 0	–
	ADTRG	Input	P32 = Setting not required	PM32 = Setting not required	PMC32 = 1	–	**Note 3**, PFC32 = 0	–
	TO01	Output	P32 = Setting not required	PM32 = Setting not required	PMC32 = 1	–	PFC32 = 1	–

Notes 1. When using the P10 and P11 pins as an alternate function (ANO0 and ANO1 pins), set the PM1 register to FFH.

2. The INTP7 and RXD0 pins are alternate-function pins. When using the pin as the RXD0 pin, disable edge detection of the alternate-function INTP7 pin (clear the INTF3.INTF31 and INTR3.INTR31 bits to 0). When using the pin as the INTP7 pin, stop the UART0 receive operation (clear the ASIM0.RXE0 bit to 0).

3. The ASCK0 and ADTRG pins are alternate-function pins. When using the pin as the ASCK0 pin, disable the trigger input of the alternate-function ADTRG pin (clear the ADS.TRG bit to 0 or set the ADS.ADTMD bit to 1). When using the pin as the ADTRG pin, do not set the UART0 operation clock to external input (set the CKSR0.TPS03 to CKSR0.TPS00 bits to other than 1011).

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (2/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O						
P33	TI000	Input	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFCE33 = 0	PFC33 = 0	–
	TO00	Output	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFCE33 = 0	PFC33 = 1	–
	TIP00	Input	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFCE33 = 1	PFC33 = 0	–
	TOP00	Output	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFCE33 = 1	PFC33 = 1	–
P34	TI001	Input	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	PFCE34 = 0	PFC34 = 0	–
	TO00	Output	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	PFCE34 = 0	PFC34 = 1	–
	TIP10	Input	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	PFCE34 = 1	PFC34 = 0	–
	TOP10	Output	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	PFCE34 = 1	PFC34 = 1	–
P35	TI010	Input	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	–	PFC35 = 0	–
	TO01	Output	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	–	PFC35 = 1	–
P38	SDA0	I/O	P38 = Setting not required	PM38 = Setting not required	PMC38 = 1	–	–	PF38 (PF3H) = 1
P39	SCL0	I/O	P39 = Setting not required	PM39 = Setting not required	PMC39 = 1	–	–	PF39 (PF3H) = 1
P40	SI00	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 0	–
	RXD2	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 1	–
P41	SO00	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 0	PF41 (PF4) = Don’t care
	TXD2	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 1	PF41 (PF4) = 0
P42	$\overline{\text{SCK00}}$	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	–	–	PF42 (PF4) = Don’t care

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (3/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P50	TI011	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFC50 = 0	–
	RTP00	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFC50 = 1	–
	KR0	Input	P50 = Setting not required	PM50 = 1	PMC50 = 0	PFC50 = Setting not required	KRM0 (KRM) = 1
P51	TI50	Input	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFC51 = 0	–
	RTP01	Output	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFC51 = 1	–
	KR1	Input	P51 = Setting not required	PM51 = 1	PMC51 = 0	PFC51 = Setting not required	KRM1 (KRM) = 1
P52	TO50	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFC52 = 0	–
	RTP02	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFC52 = 1	–
	KR2	Input	P52 = Setting not required	PM52 = 1	PMC52 = 0	PFC52 = Setting not required	KRM2 (KRM) = 1
P53	SIA0	Input	P53 = Setting not required	PM53 = Setting not required	PMC53 = 1	PFC53 = 0	–
	RTP03	Output	P53 = Setting not required	PM53 = Setting not required	PMC53 = 1	PFC53 = 1	–
	KR3	Input	P53 = Setting not required	PM53 = 1	PMC53 = 0	PFC53 = Setting not required	KRM3 (KRM) = 1
P54	SOA0	Output	P54 = Setting not required	PM54 = Setting not required	PMC54 = 1	PFC54 = 0	PF54 (PF5) = Don't care
	RTP04	Output	P54 = Setting not required	PM54 = Setting not required	PMC54 = 1	PFC54 = 1	PF54 (PF5) = 0
	KR4	Input	P54 = Setting not required	PM54 = 1	PMC54 = 0	PFC54 = Setting not required	PF54 (PF5) = 0, KRM4 (KRM) = 1
P55	$\overline{\text{SCKA0}}$	I/O	P55 = Setting not required	PM55 = Setting not required	PMC55 = 1	PFC55 = 0	PF55 (PF5) = Don't care
	RTP05	Output	P55 = Setting not required	PM55 = Setting not required	PMC55 = 1	PFC55 = 1	PF55 (PF5) = 0
	KR5	Input	P55 = Setting not required	PM55 = 1	PMC55 = 0	PFC55 = Setting not required	PF55 (PF5) = 0, KRM5 (KRM) = 1
P70	ANI0	Input	P70 = Setting not required	–	–	–	–
P71	ANI1	Input	P71 = Setting not required	–	–	–	–
P72	ANI2	Input	P72 = Setting not required	–	–	–	–
P73	ANI3	Input	P73 = Setting not required	–	–	–	–
P74	ANI4	Input	P74 = Setting not required	–	–	–	–
P75	ANI5	Input	P75 = Setting not required	–	–	–	–
P76	ANI6	Input	P76 = Setting not required	–	–	–	–
P77	ANI7	Input	P77 = Setting not required	–	–	–	–

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (4/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P90	A0	Output	P90 = Setting not required	PM90 = Setting not required	PMC90 = 1	PFC90 = 0	**Note**
	TXD1	Output	P90 = Setting not required	PM90 = Setting not required	PMC90 = 1	PFC90 = 1	–
	KR6	Input	P90 = Setting not required	PM90 = 1	PMC90 = 0	PFC90 = Setting not required	KRM6 (KRM) = 1
P91	A1	Output	P91 = Setting not required	PM91 = Setting not required	PMC91 = 1	PFC91 = 0	**Note**
	RXD1	Input	P91 = Setting not required	PM91 = Setting not required	PMC91 = 1	PFC91 = 1	–
	KR7	Input	P91 = Setting not required	PM91 = 1	PMC91 = 0	PFC91 = Setting not required	KRM7 (KRM) = 1
P92	A2	Output	P92 = Setting not required	PM92 = Setting not required	PMC92 = 1	PFC92 = 0	**Note**
	TI020	Input	P92 = Setting not required	PM92 = 1	PMC92 = 0	PFC92 = Setting not required	–
	TO02	Output	P92 = Setting not required	PM92 = Setting not required	PMC92 = 1	PFC92 = 1	–
P93	A3	Output	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFC93 = 0	**Note**
	TI021	Input	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFC93 = 1	–
P94	A4	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFC94 = 0	**Note**
	TI030	Input	P94 = Setting not required	PM94 = 1	PMC94 = 0	PFC94 = Setting not required	–
	TO03	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFC94 = 1	–
P95	A5	Output	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFC95 = 0	**Note**
	TI031	Input	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFC95 = 1	–
P96	A6	Output	P96 = Setting not required	PM96 = Setting not required	PMC96 = 1	PFC96 = 0	**Note**
	TI51	Input	P96 = Setting not required	PM96 = 1	PMC96 = 0	PFC96 = Setting not required	–
	TO51	Output	P96 = Setting not required	PM96 = Setting not required	PMC96 = 1	PFC96 = 1	–
P97	A7	Output	P97 = Setting not required	PM97 = Setting not required	PMC97 = 1	PFC97 = 0	**Note**
	SI01	Input	P97 = Setting not required	PM97 = Setting not required	PMC97 = 1	PFC97 = 1	–
P98	A8	Output	P98 = Setting not required	PM98 = Setting not required	PMC98 = 1	PFC98 = 0	**Note**, PF98 (PF9) = 0
	SO01	Output	P98 = Setting not required	PM98 = Setting not required	PMC98 = 1	PFC98 = 1	PF98 (PF9) = Don't care
P99	A9	Output	P99 = Setting not required	PM99 = Setting not required	PMC99 = 1	PFC99 = 0	**Note**, PF99 (PF9) = 0
	$\overline{\text{SCK01}}$	I/O	P99 = Setting not required	PM99 = Setting not required	PMC99 = 1	PFC99 = 1	PF99 (PF9) = Don't care

Note When setting the A0 to A15 pins, set the PFC9 register to 0000H and the PMC9 register to FFFFH in 16-bit units.

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (5/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P910	A10	Output	P910 = Setting not required	PM910 = Setting not required	PMC910 = 1	PFC910 = 0	**Note**
	SIA1	Input	P910 = Setting not required	PM910 = Setting not required	PMC910 = 1	PFC910 = 1	–
P911	A11	Output	P911 = Setting not required	PM911 = Setting not required	PMC911 = 1	PFC911 = 0	**Note**, PF911 (PF9) = 0
	SOA1	Output	P911 = Setting not required	PM911 = Setting not required	PMC911 = 1	PFC911 = 1	PF911 (PF9) = Don't care
P912	A12	Output	P912 = Setting not required	PM912 = Setting not required	PMC912 = 1	PFC912 = 0	**Note**, PF912 (PF9) = 0
	$\overline{\text{SCKA1}}$	I/O	P912 = Setting not required	PM912 = Setting not required	PMC912 = 1	PFC912 = 1	PF912 (PF9) = Don't care
P913	A13	Output	P913 = Setting not required	PM913 = Setting not required	PMC913 = 1	PFC913 = 0	**Note**
	INTP4	Input	P913 = Setting not required	PM913 = Setting not required	PMC913 = 1	PFC913 = 1	–
P914	A14	Output	P914 = Setting not required	PM914 = Setting not required	PMC914 = 1	PFC914 = 0	**Note**
	INTP5	Input	P914 = Setting not required	PM914 = Setting not required	PMC914 = 1	PFC914 = 1	–
P915	A15	Output	P915 = Setting not required	PM915 = Setting not required	PMC915 = 1	PFC915 = 0	**Note**
	INTP6	Input	P915 = Setting not required	PM915 = Setting not required	PMC915 = 1	PFC915 = 1	–
PCM0	$\overline{\text{WAIT}}$	Input	PCM0 = Setting not required	PMCM0 = Setting not required	PMCCM0 = 1	–	–
PCM1	CLKOUT	Output	PCM1 = Setting not required	PMCM1 = Setting not required	PMCCM1 = 1	–	–
PCM2	$\overline{\text{HLDAK}}$	Output	PCM2 = Setting not required	PMCM2 = Setting not required	PMCCM2 = 1	–	–
PCM3	$\overline{\text{HLDRQ}}$	Input	PCM3 = Setting not required	PMCM3 = Setting not required	PMCCM3 = 1	–	–
PCS0	$\overline{\text{CS0}}$	Output	PCS0 = Setting not required	PMCS0 = Setting not required	PMCCS0 = 1	–	–
PCS1	$\overline{\text{CS1}}$	Output	PCS1 = Setting not required	PMCS1 = Setting not required	PMCCS1 = 1	–	–
PCT0	$\overline{\text{WR0}}$	Output	PCT0 = Setting not required	PMCT0 = Setting not required	PMCCT0 = 1	–	–
PCT1	$\overline{\text{WR1}}$	Output	PCT1 = Setting not required	PMCT1 = Setting not required	PMCCT1 = 1	–	–
PCT4	$\overline{\text{RD}}$	Output	PCT4 = Setting not required	PMCT4 = Setting not required	PMCCT4 = 1	–	–
PCT6	ASTB	Output	PCT6 = Setting not required	PMCT6 = Setting not required	PMCCT6 = 1	–	–

Note When setting the A0 to A15 pins, set the PFC9 register to 0000H and the PMC9 register to FFFFH in 16-bit units.

Table 4-16. Settings When Port Pins Are Used for Alternate Functions (6/6)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
PDH0	A16	Output	PDH0 = Setting not required	PMDH0 = Setting not required	PMCDH0 = 1	–	–
PDH1	A17	Output	PDH1 = Setting not required	PMDH1 = Setting not required	PMCDH1 = 1	–	–
PDH2	A18	Output	PDH2 = Setting not required	PMDH2 = Setting not required	PMCDH2 = 1	–	–
PDH3	A19	Output	PDH3 = Setting not required	PMDH3 = Setting not required	PMCDH3 = 1	–	–
PDH4	A20	Output	PDH4 = Setting not required	PMDH4 = Setting not required	PMCDH4 = 1	–	–
PDH5	A21	Output	PDH5 = Setting not required	PMDH5 = Setting not required	PMCDH5 = 1	–	–
PDL0	AD0	I/O	PDL0 = Setting not required	PMDL0 = Setting not required	PMCDL0 = 1	–	–
PDL1	AD1	I/O	PDL1 = Setting not required	PMDL1 = Setting not required	PMCDL1 = 1	–	–
PDL2	AD2	I/O	PDL2 = Setting not required	PMDL2 = Setting not required	PMCDL2 = 1	–	–
PDL3	AD3	I/O	PDL3 = Setting not required	PMDL3 = Setting not required	PMCDL3 = 1	–	–
PDL4	AD4	I/O	PDL4 = Setting not required	PMDL4 = Setting not required	PMCDL4 = 1	–	–
PDL5	AD5	I/O	PDL5 = Setting not required	PMDL5 = Setting not required	PMCDL5 = 1	–	–
PDL6	AD6	I/O	PDL6 = Setting not required	PMDL6 = Setting not required	PMCDL6 = 1	–	–
PDL7	AD7	I/O	PDL7 = Setting not required	PMDL7 = Setting not required	PMCDL7 = 1	–	–
PDL8	AD8	I/O	PDL8 = Setting not required	PMDL8 = Setting not required	PMCDL8 = 1	–	–
PDL9	AD9	I/O	PDL9 = Setting not required	PMDL9 = Setting not required	PMCDL9 = 1	–	–
PDL10	AD10	I/O	PDL10 = Setting not required	PMDL10 = Setting not required	PMCDL10 = 1	–	–
PDL11	AD11	I/O	PDL11 = Setting not required	PMDL11 = Setting not required	PMCDL11 = 1	–	–
PDL12	AD12	I/O	PDL12 = Setting not required	PMDL12 = Setting not required	PMCDL12 = 1	–	–
PDL13	AD13	I/O	PDL13 = Setting not required	PMDL13 = Setting not required	PMCDL13 = 1	–	–
PDL14	AD14	I/O	PDL14 = Setting not required	PMDL14 = Setting not required	PMCDL14 = 1	–	–
PDL15	AD15	I/O	PDL15 = Setting not required	PMDL15 = Setting not required	PMCDL15 = 1	–	–

4.6 Cautions

4.6.1 Cautions on bit manipulation instruction for port n register (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the value of the output latch of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P90 is an output port, P91 to P97 are input ports (all pin statuses are high level), and the value of the port latch is 00H, if the output of output port P90 is changed from low level to high level via a bit manipulation instruction, the value of the port latch is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A bit manipulation instruction is executed in the following order in the V850ES/KG2.

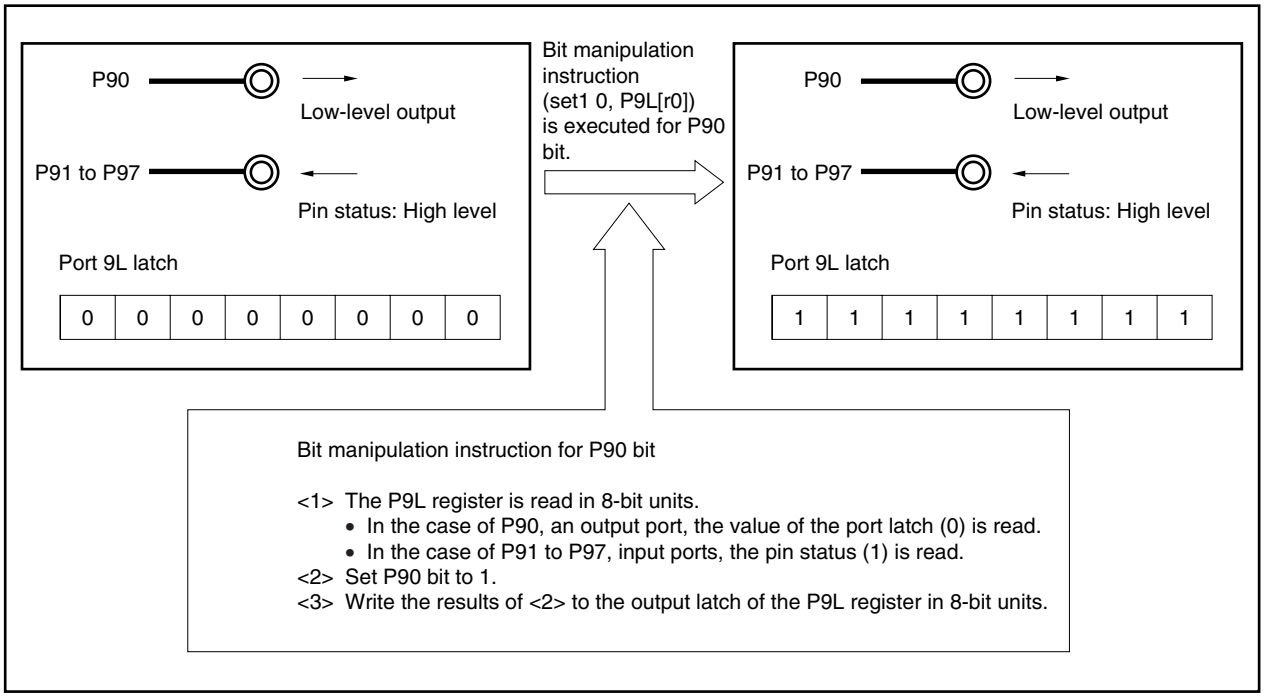
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the value of the output latch (0) of P90, which is an output port, is read, while the pin statuses of P91 to P97, which are input ports, are read. If the pin statuses of P91 to P97 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-28. Bit Manipulation Instruction (P90)



4.6.2 Hysteresis characteristics

In port mode, the following ports do not have hysteresis characteristics.

P02 to P06
P31 to P35, P38, P39
P40, P42
P93, P95, P97, P99, P910, P912 to P915

CHAPTER 5 BUS CONTROL FUNCTION

The V850ES/KG2 is provided with an external bus interface function by which external memories such as ROM and RAM, and I/O can be connected.

5.1 Features

- 16-bit data bus
- Output is selectable from a multiplex bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles
- Chip select function for up to 2 spaces
- 8-bit/16-bit data bus selectable (for each area selected by chip select function)
- Wait function
  - Programmable wait function of up to 7 states (selectable for each area selected by chip select function)
  - External wait function using $\overline{\text{WAIT}}$ pin
- Idle state function
- Bus hold function
- The bus can be controlled using a different voltage from the operating voltage by setting $BV_{DD} \leq V_{DD} = EV_{DD}$ (however, only in multiplex bus mode).
- Can be connected to the external device with port alternate-function pins.
- Misalign access possible

5.2 Bus Control Pins

The pins used to connect an external device are listed in the table below.

Table 5-1. Bus Control Pins (When Multiplex Bus Selected)

Bus Control Pin	Alternate-Function Pin	I/O	Function	Register to Switch Between Port Mode/ Alternate-Function Mode
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus	PMCDL register
A16 to A21	PDH0 to PDH5	Output	Address bus	PMCDH register
$\overline{\text{WAIT}}$	PCM0	Input	External wait control	PMCCM register
CLKOUT	PCM1	Output	Internal system clock output	PMCCM register
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	PCS0, PCS1	Output	Chip select	PMCCS register
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal	PMCCT register
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal	PMCCT register
ASTB	PCT6	Output	Address strobe signal	PMCCT register
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control	PMCCM register
$\overline{\text{HLDAK}}$	PCM2	Output		

Table 5-2. Bus Control Pins (When Separate Bus Selected)

Bus Control Pin	Alternate-Function Pin	I/O	Function	Register to Switch Between Port Mode/ Alternate-Function Mode
AD0 to AD15	PDL0 to PDL15	I/O	Data bus	PMCDL register
A0 to A15	P90 to P915	Output	Address bus	PMC9 register
A16 to A21	PDH0 to PDH5	Output	Address bus	PMCDH register
$\overline{\text{WAIT}}$	PCM0	Input	External wait control	PMCCM register
CLKOUT	PCM1	Output	Internal system clock output	PMCCM register
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	PCS0, PCS1	Output	Chip select	PMCCS register
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal	PMCCT register
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal	PMCCT register
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control	PMCCM register
$\overline{\text{HLDAK}}$	PCM2	Output		

5.2.1 Pin status when internal ROM, internal RAM, or on-chip peripheral I/O is accessed

When the internal ROM, internal RAM, or on-chip peripheral I/O are accessed, the status of each pin is as follows.

Table 5-3. Pin Statuses When Internal ROM, Internal RAM, or On-Chip Peripheral I/O Is Accessed

Separate Bus Mode		Multiplex Bus Mode	
Address bus (A21 to A0)	Undefined	Address bus (A21 to A16)	Undefined
Data bus (AD15 to AD0)	Hi-Z	Address/data bus (AD15 to AD0)	Undefined
Control signal	Inactive	Control signal	Inactive

Caution When a write access is performed to the internal ROM area, address, data, and control signals are activated in the same way as access to the external memory area.

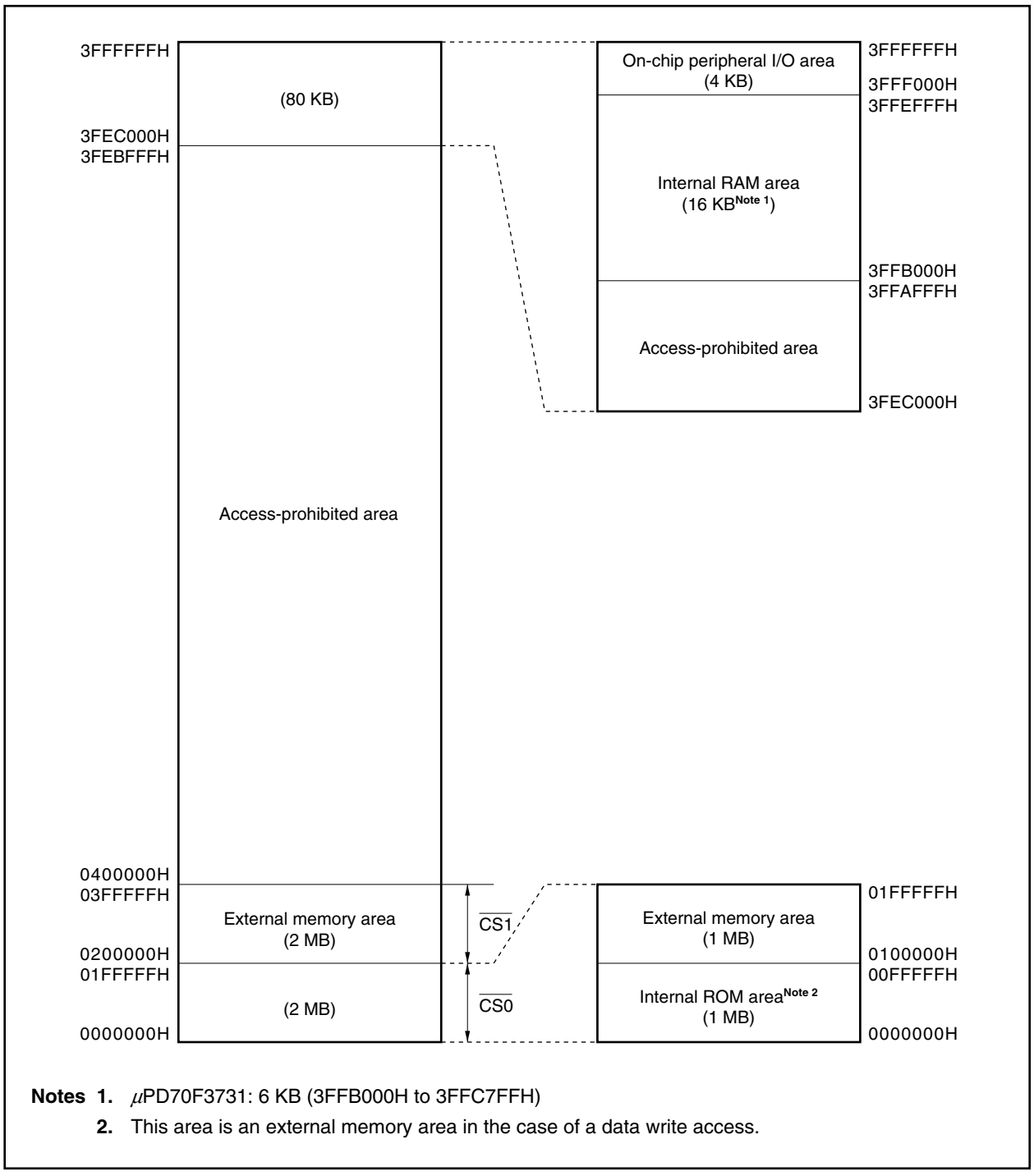
5.2.2 Pin status in each operation mode

For the pin status of the V850ES/KG2 in each operation mode, refer to **2.2 Pin Status**.

5.3 Memory Block Function

The 64 MB memory space is divided into chip select areas of (lower) 2 MB and 2 MB. The programmable wait function and bus cycle operation mode for each of these chip select areas can be independently controlled.

Figure 5-1. Data Memory Map: Physical Address



Notes 1. μPD70F3731: 6 KB (3FFB000H to 3FFC7FFH)

2. This area is an external memory area in the case of a data write access.

5.3.1 Chip select control function

Of the 64 MB (linear) address space, the lower 4 MB (0000000H to 03FFFFFH) include two chip select control functions, $\overline{CS0}$ and $\overline{CS1}$. The areas that can be selected by $\overline{CS0}$ and $\overline{CS1}$ are fixed.

By using these chip select control functions, the memory space can be used effectively. The allocation of the chip select areas is shown in the table below.

$\overline{CS0}$	0000000H to 01FFFFFH (2 MB)
$\overline{CS1}$	0200000H to 03FFFFFH (2 MB)

5.4 External Bus Interface Mode Control Function

The V850ES/KG2 includes the following two external bus interface modes.

- Multiplex bus mode
- Separate bus mode

These two modes can be selected by using the EXIMC register.

(1) External bus interface mode control register (EXIMC)

This register can be read or written in 8-bit or 1-bit units.

Reset sets EXIMC to 00H.

After reset: 00H R/W Address: FFFFFFBEH

	7	6	5	4	3	2	1	0
EXIMC	0	0	0	0	0	0	0	SMSEL

SMSEL	Mode selection
0	Multiplex bus mode
1	Separate bus mode

Caution Set the EXIMC register from the internal ROM or internal RAM area before external access.
After setting the EXIMC register, be sure to set a NOP instruction.

5.5 Bus Access

5.5.1 Number of clocks for access

The following table shows the number of basic clocks required for accessing each resource.

Area (Bus Width) / Bus Cycle Type	Internal ROM (32 Bits)	Internal RAM (32 Bits)	External Memory (16 Bits)	On-Chip Peripheral I/O (16 Bits)
Instruction fetch (normal access)	1	1 Note 1	3 + n Note 2	–
Instruction fetch (branch)	2	2 Note 1	3+ n Note 2	–
Operand data access	3	1	3 +n Note 2	3 Note 3

Notes 1. If the access conflicts with a data access, the number of clock is increased by 1.

2. Value when the multiplexed bus is selected. 2 + n clocks (n: Number of wait states) when the separate bus mode is selected.

3. This value varies depending on the setting of the VSWC register.

Remark Unit: Clocks/access

5.5.2 Bus size setting function

The bus size of each external memory area selected by $\overline{CSn}$ can be set to 8 bits or 16 bits by using the BSC register.

The external memory area of the V850ES/KG2 is selected by $\overline{CS0}$ and $\overline{CS1}$.

(1) Bus size configuration register (BSC)

This register can be read or written in 16-bit units.

Reset sets BSC to 5555H.

Caution Write to the BSC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BSC register are complete.

After reset: 5555H R/W Address: FFFFF066H

	15	14	13	12	11	10	9	8
BSC	0	1	0	1	0	1	0	1

7	6	5	4	3	2	1	0
0	0/1 Note	0	0/1 Note	0	BS10	0	BS00

$\overline{CSn}$ signal: BS10 → $\overline{CS1}$, BS00 → $\overline{CS0}$

BSn0	Data bus width of CSn space (n = 0, 1)
0	8 bits
1	16 bits

Note Changing the value does not affect the operation.

Caution Be sure to set bits 14, 12, 10, and 8 to "1", and clear bits 15, 13, 11, 9, 7, 5, 3, and 1 to "0".

5.5.3 Access by bus size

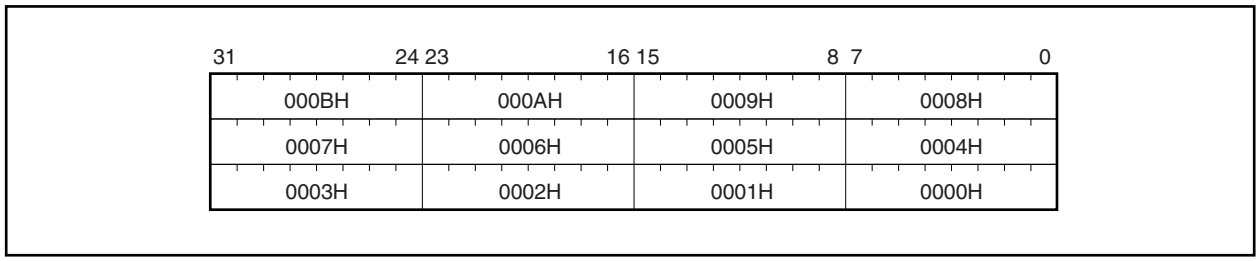
The V850ES/KG2 accesses the on-chip peripheral I/O and external memory in 8-bit, 16-bit, or 32-bit units. The bus size is as follows.

- The bus size of the on-chip peripheral I/O is fixed to 16 bits.
- The bus size of the external memory is selectable from 8 bits or 16 bits (by using the BSC register).

The operation when each of the above is accessed is described below. All data is accessed starting from the lower side.

The V850ES/KG2 supports only the little endian format.

Figure 5-2. Little Endian Address in Word



(1) Data space

The V850ES/KG2 has an address misalign function.

With this function, data can be placed at all addresses, regardless of the format of the data (word data or halfword data). However, if the word data or halfword data is not aligned at the boundary, a bus cycle is generated at least twice, causing the bus efficiency to drop.

(a) Halfword-length data access

A byte-length bus cycle is generated twice if the least significant bit of the address is 1.

(b) Word-length data access

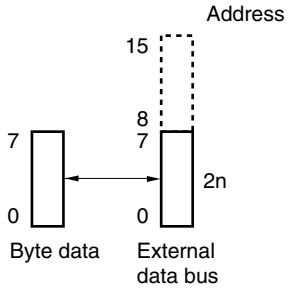
(i) A byte-length bus cycle, halfword-length bus cycle, and byte-length bus cycle are generated in that order if the least significant bit of the address is 1.

(ii) A halfword-length bus cycle is generated twice if the lower 2 bits of the address are 10.

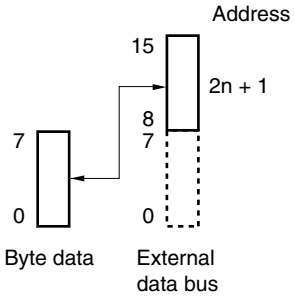
(2) Byte access (8 bits)

(a) 16-bit data bus width

<1> Access to even address (2n)

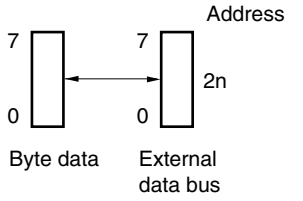


<2> Access to odd address (2n + 1)

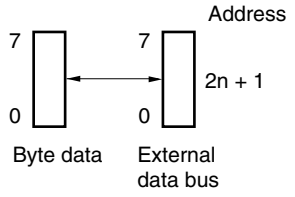


(b) 8-bit data bus width

<1> Access to even address (2n)

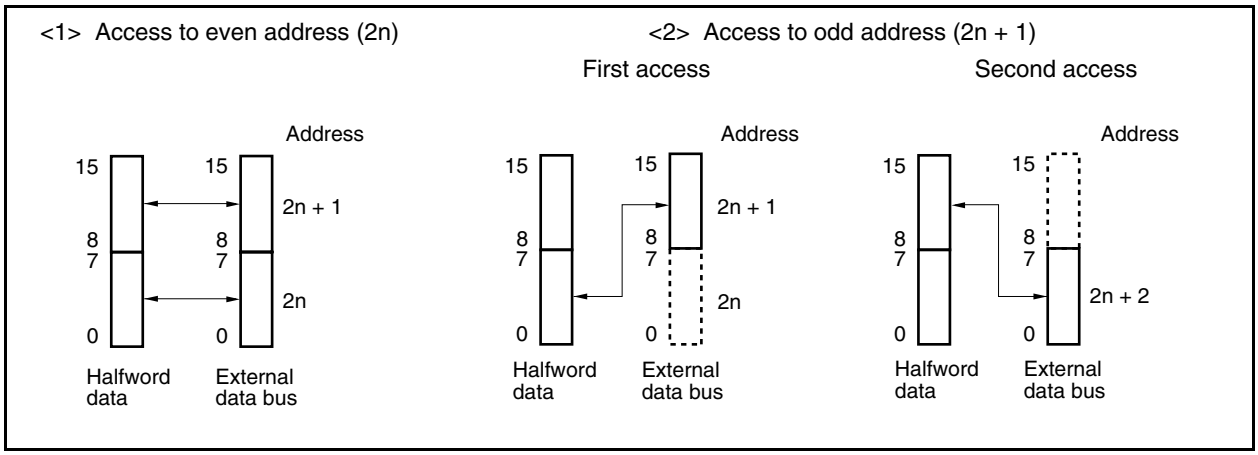


<2> Access to odd address (2n + 1)

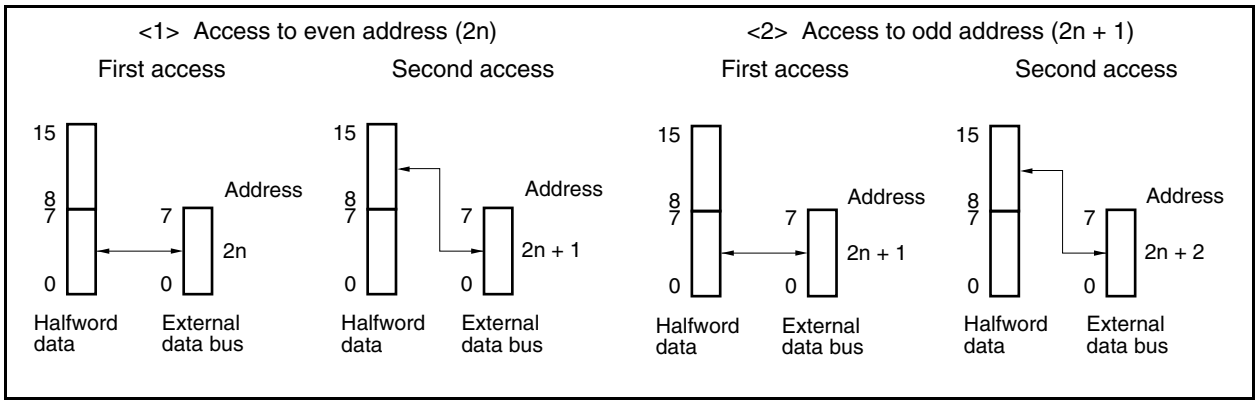


(3) Halfword access (16 bits)

(a) With 16-bit data bus width



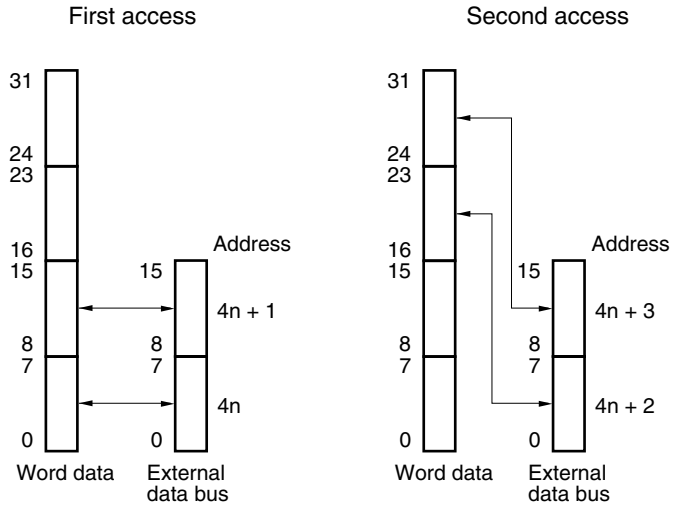
(b) 8-bit data bus width



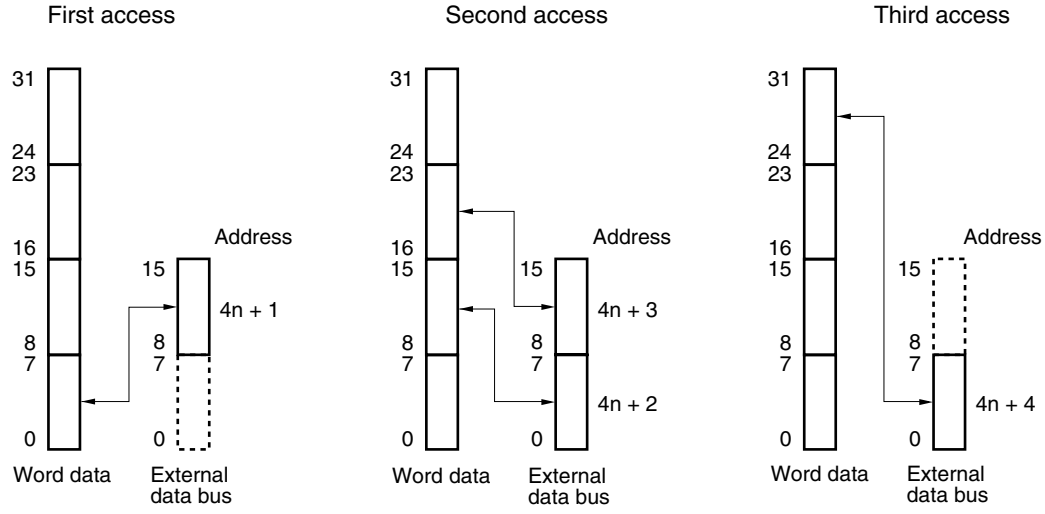
(4) Word access (32 bits)

(a) 16-bit data bus width (1/2)

<1> Access to address (4n)

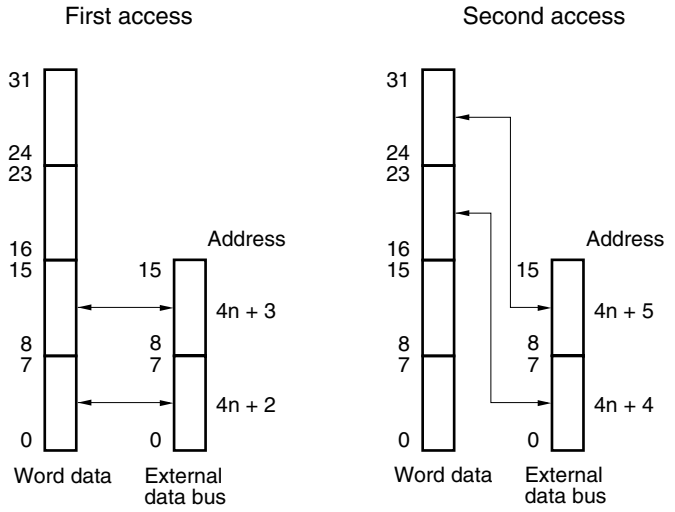


<2> Access to address (4n + 1)

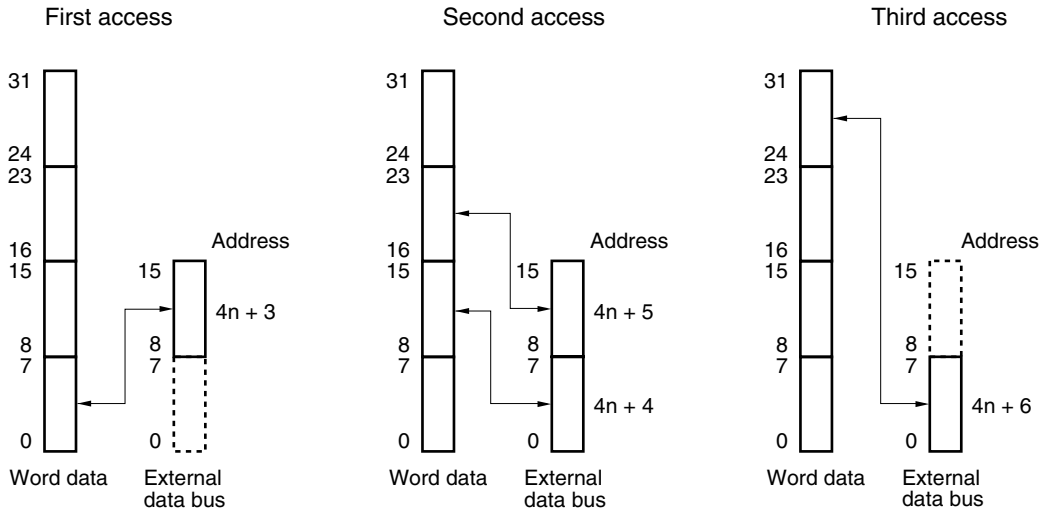


(a) 16-bit data bus width (2/2)

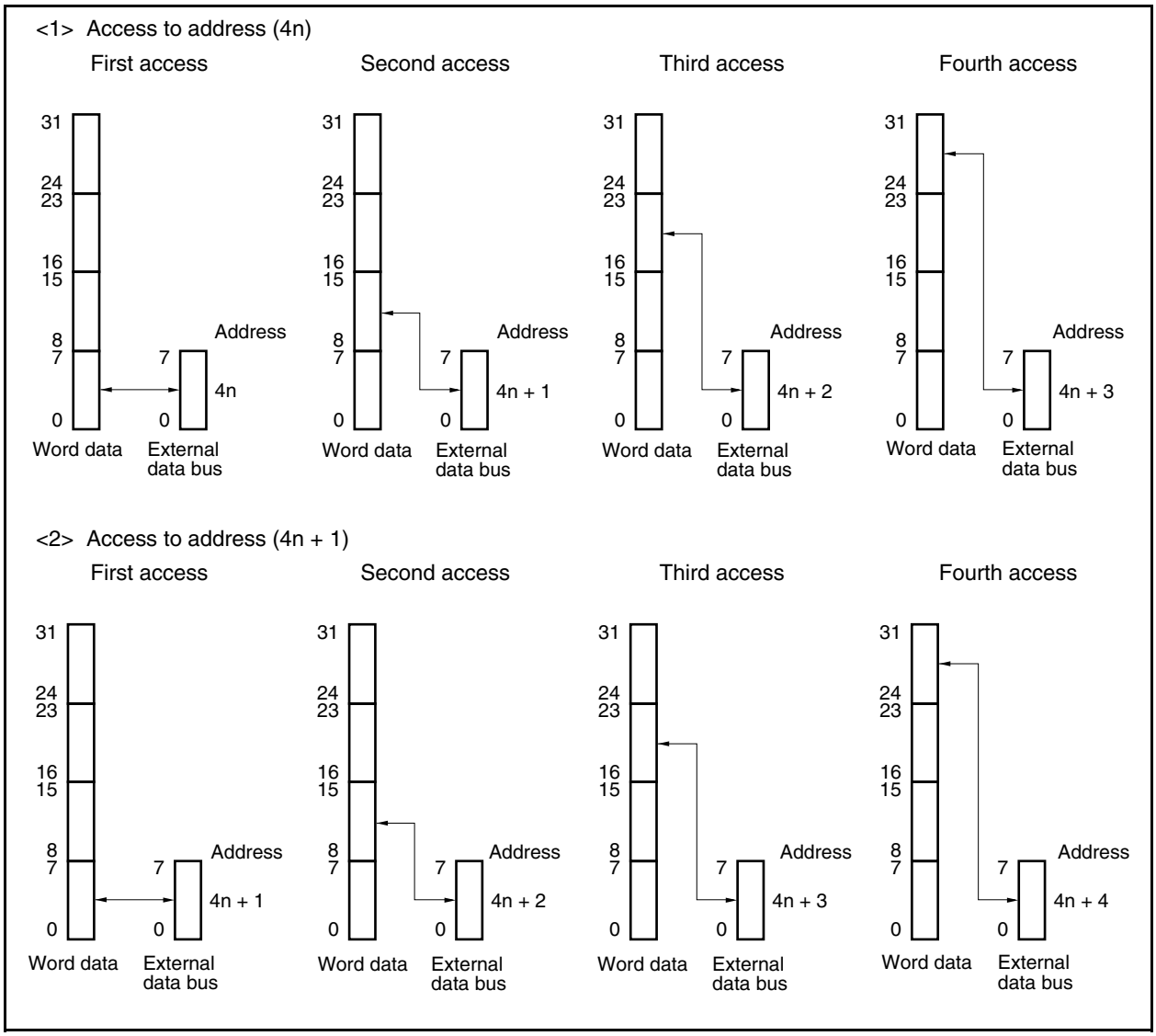
<3> Access to address (4n + 2)



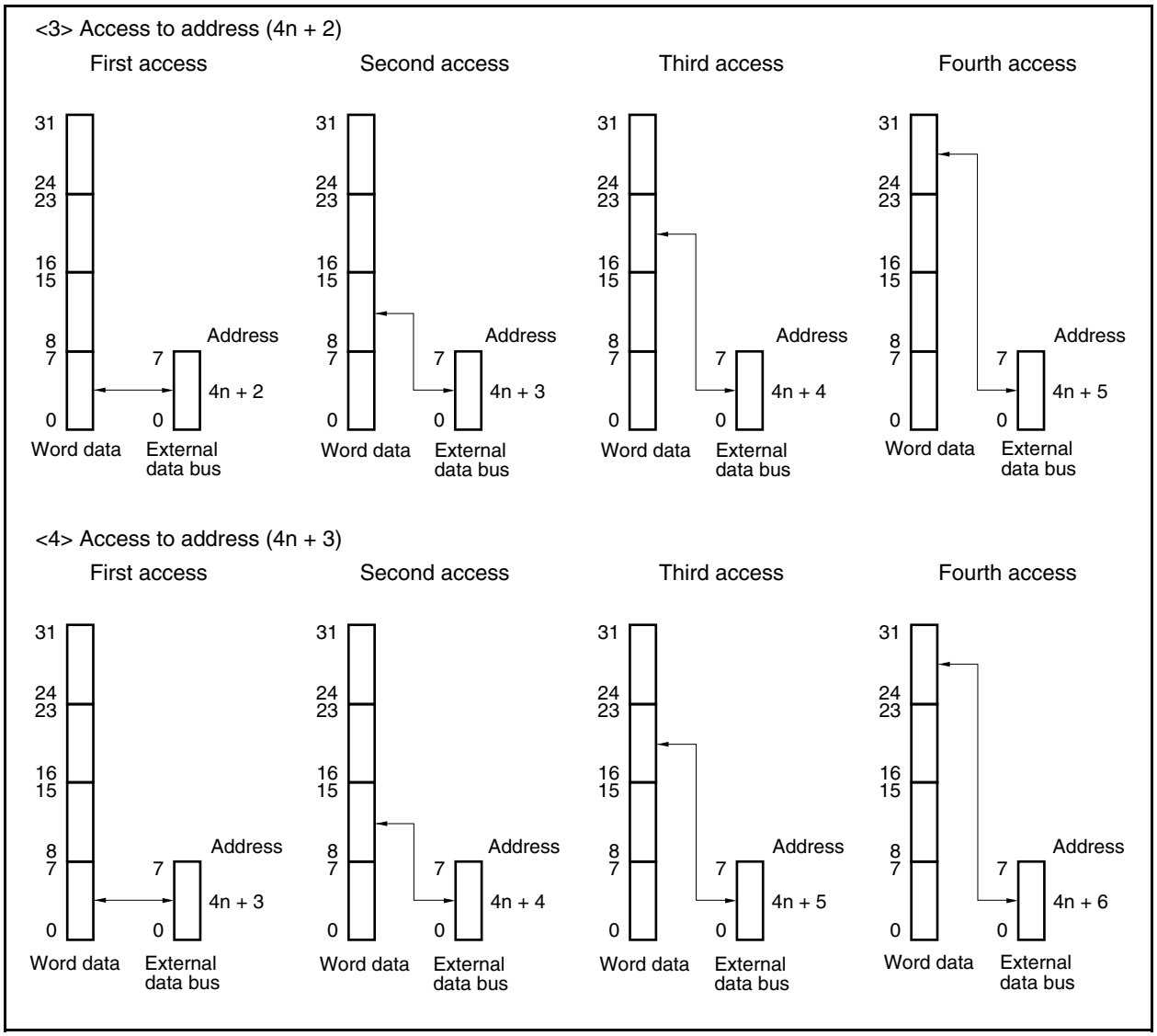
<4> Access to address (4n + 3)



(b) 8-bit data bus width (1/2)



(b) 8-bit data bus width (2/2)



5.6 Wait Function

5.6.1 Programmable wait function

(1) Data wait control register 0 (DWC0)

To realize interfacing with a low-speed memory or I/O, up to seven data wait states can be inserted in the bus cycle that is executed for each CS space.

The number of wait states can be programmed by using the DWC0 register. Immediately after system reset, 7 data wait states are inserted for all the chip select areas.

The DWC0 register can be read or written in 16-bit units.

Reset sets DWC0 to 7777H.

Cautions 1. The internal ROM and internal RAM areas are not subject to programmable wait, and are always accessed without a wait state. The on-chip peripheral I/O area is also not subject to programmable wait, and only wait control from each peripheral function is performed.

2. Write to the DWC0 register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the DWC0 register are complete.

After reset: 7777H R/W Address: FFFFF484H

	15	14	13	12	11	10	9	8
DWC0	0	0/1 Note	0/1 Note	0/1 Note	0	0/1 Note	0/1 Note	0/1 Note
	7	6	5	4	3	2	1	0
	0	DW12	DW11	DW10	0	DW02	DW01	DW00
$\overline{CSn}$ signal			$\overline{CS1}$				$\overline{CS0}$	

DWn2	DWn1	DWn0	Number of wait states inserted in CSn space (n = 0, 1)
0	0	0	None
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Note Changing the value does not affect the operation.

Caution Be sure to clear bits 15, 11, 7, and 3 to "0".

5.6.2 External wait function

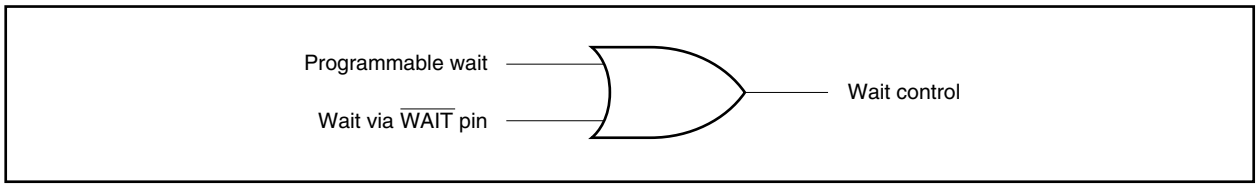
To synchronize an extremely slow memory, I/O, or asynchronous system, any number of wait states can be inserted in the bus cycle by using the external wait pin ($\overline{\text{WAIT}}$).

Access to each area of the internal ROM, internal RAM, and on-chip peripheral I/O is not subject to control by the external wait function, in the same manner as the programmable wait function.

The $\overline{\text{WAIT}}$ signal can be input asynchronously to CLKOUT, and is sampled at the falling edge of the clock in the T2 and TW states of the bus cycle in the multiplex bus mode. In the separate bus mode, it is sampled at the rising edge of the clock immediately after the T1 and TW states of the bus cycle. If the setup/hold time of the sampling timing is not satisfied, a wait state is inserted in the next state, or not inserted at all.

5.6.3 Relationship between programmable wait and external wait

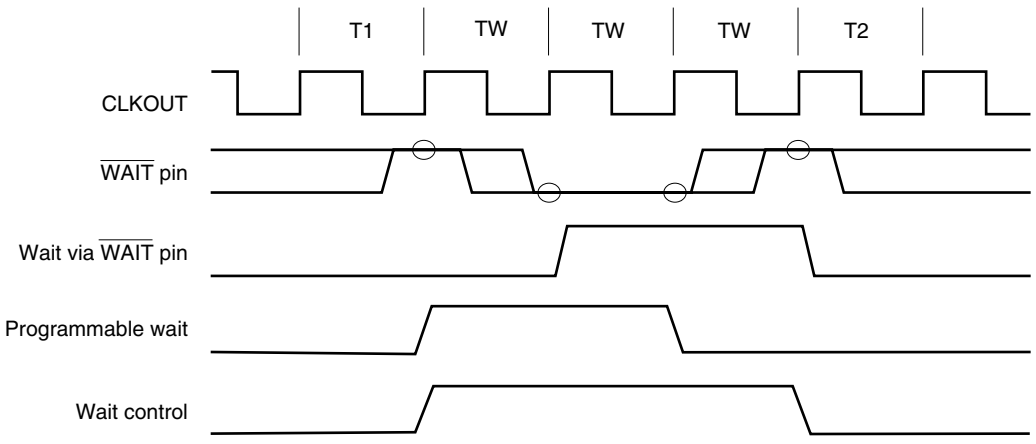
Wait cycles are inserted as the result of an OR operation between the wait cycles specified by the set value of the programmable wait and the wait cycles controlled by the $\overline{\text{WAIT}}$ pin.



For example, if the timing of the programmable wait and the $\overline{\text{WAIT}}$ pin signal is as illustrated below, three wait states will be inserted in the bus cycle.

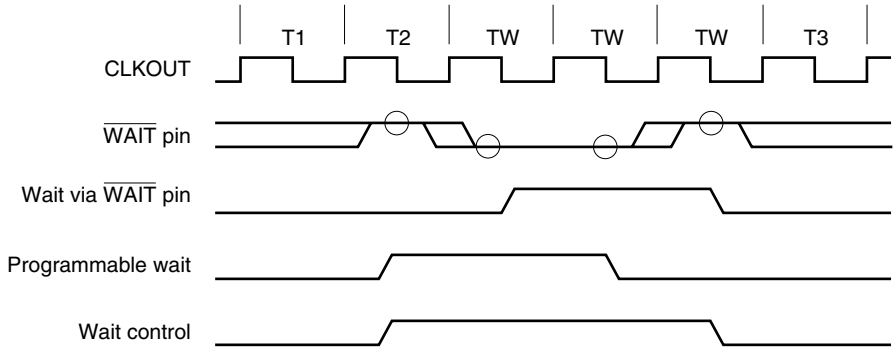
Figure 5-3. Example of Inserting Wait States

(a) In separate bus mode



Remark The circles indicate the sampling timing.

(b) In multiplex bus mode



Remark The circles indicate the sampling timing.

5.6.4 Programmable address wait function

Address-setup or address-hold waits to be inserted in each bus cycle can be set by using the AWC register. Address wait insertion is set for each chip select area ($\overline{CS0}$ and $\overline{CS1}$).

If an address setup wait is inserted, it seems that the high-clock period of T1 state is extended by 1 clock. If an address hold wait is inserted, it seems that the low-clock period of T1 state is extended by 1 clock.

(1) Address wait control register (AWC)

This register can be read or written in 16-bit units.

Reset sets AWC to FFFFH.

Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to address setup wait or address hold wait insertion.

2. Write the AWC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the AWC register are complete.

After reset: FFFFH R/W Address: FFFFF488H

	15	14	13	12	11	10	9	8
AWC	1	1	1	1	1	1	1	1

7	6	5	4	3	2	1	0
0/1[Note]	0/1[Note]	0/1[Note]	0/1[Note]	AHW1	ASW1	AHW0	ASW0

$\overline{CSn}$ signal: AHW1 → $\overline{CS1}$, AHW0 → $\overline{CS0}$

AHWn	Specifies insertion of address hold wait (n = 0, 1)
0	Not inserted
1	Inserted

ASWn	Specifies insertion of address setup wait (n = 0, 1)
0	Not inserted
1	Inserted

Note Changing the value does not affect the operation.

Caution Be sure to set bits 15 to 8 to 1.

5.7 Idle State Insertion Function

To facilitate interfacing with low-speed memories, one idle state (TI) can be inserted after the T3 state in the bus cycle that is executed for each space selected by $\overline{CSn}$ in the multiplex address/data bus mode. In the separate bus mode, one idle state (TI) can be inserted after the T2 state. By inserting idle states, the data output float delay time of the memory can be secured during read access (an idle state cannot be inserted during write access).

Whether the idle state is to be inserted can be programmed by using the BCC register.

An idle state is inserted for all the areas immediately after system reset.

(1) Bus cycle control register (BCC)

This register can be read or written in 16-bit units.

Reset sets BCC to AAAAH.

Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.

2. Write to the BCC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BCC register are complete.

After reset: AAAAH R/W Address: FFFFF48AH

	15	14	13	12	11	10	9	8
BCC	1	0	1	0	1	0	1	0

7	6	5	4	3	2	1	0
0/1[Note]	0	0/1[Note]	0	BC11	0	BC01	0

$\overline{CSn}$ signal: $\overline{CS1}$ (BC11), $\overline{CS0}$ (BC01)

BCn1	Specifies insertion of idle state (n = 0, 1)
0	Not inserted
1	Inserted

Note Changing the value does not affect the operation.

Caution Be sure to set bits 15, 13, 11, and 9 to "1", and clear bits 14, 12, 10, 8, 6, 4, 2, and 0 to "0".

5.8 Bus Hold Function

5.8.1 Functional outline

The $\overline{\text{HLDRQ}}$ and $\overline{\text{HLDAK}}$ functions are valid if the PCM2 and PCM3 pins are set to their alternate functions.

When the $\overline{\text{HLDRQ}}$ pin is asserted (low level), indicating that another bus master has requested bus mastership, the external address/data bus goes into a high-impedance state and is released (bus hold status). If the request for the bus mastership is cleared and the $\overline{\text{HLDRQ}}$ pin is deasserted (high level), driving these pins is started again.

During the bus hold period, execution of the program in the internal ROM and internal RAM is continued until a peripheral I/O register or the external memory is accessed.

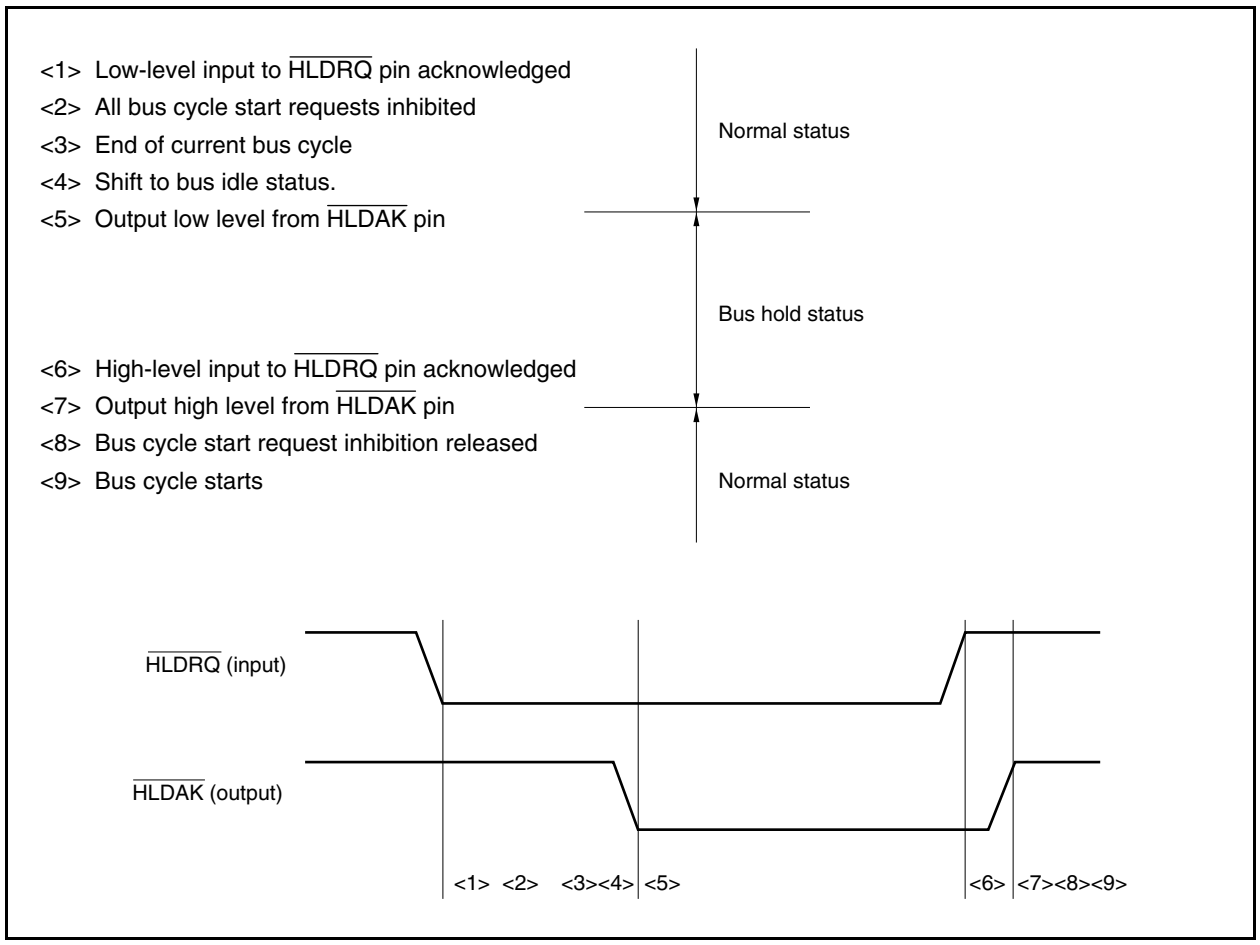
The bus hold status is indicated by assertion (low level) of the $\overline{\text{HLDAK}}$ pin. The bus hold function enables the configuration of multi-processor type systems in which two or more bus masters exist.

Note that the bus hold request is not acknowledged during a multiple-access cycle initiated by the bus sizing function or a bit manipulation instruction.

Status	Data Bus Width	Access Type	Timing in Which Bus Hold Request Not Acknowledged
CPU bus lock	16 bits	Word access to even address	Between first and second access
		Word access to odd address	Between first and second access
			Between second and third access
		Halfword access to odd address	Between first and second access
	8 bits	Word access	Between first and second access
			Between second and third access
			Between third and fourth access
		Halfword access	Between first and second access
Read-modify-write access of bit manipulation instruction	–	–	Between read access and write access

5.8.2 Bus hold procedure

The bus hold status transition procedure is shown below.



5.8.3 Operation in power save mode

Because the internal system clock is stopped in the STOP and IDLE modes, the bus hold status is not entered even if the $\overline{\text{HLDRQ}}$ pin is asserted.

In the HALT mode, the $\overline{\text{HLDAK}}$ pin is asserted as soon as the $\overline{\text{HLDRQ}}$ pin has been asserted, and the bus hold status is entered. When the $\overline{\text{HLDRQ}}$ pin is later deasserted, the $\overline{\text{HLDAK}}$ pin is also deasserted, and the bus hold status is cleared.

5.9 Bus Priority

Bus hold, instruction fetch (branch), instruction fetch (successive), operand data access, and DMA transfer are executed in the external bus cycle.

Bus hold has the highest priority, followed by DMA transfer, operand data access, instruction fetch (branch), and instruction fetch (successive).

An instruction fetch may be inserted between the read access and write access in a read-modify-write access.

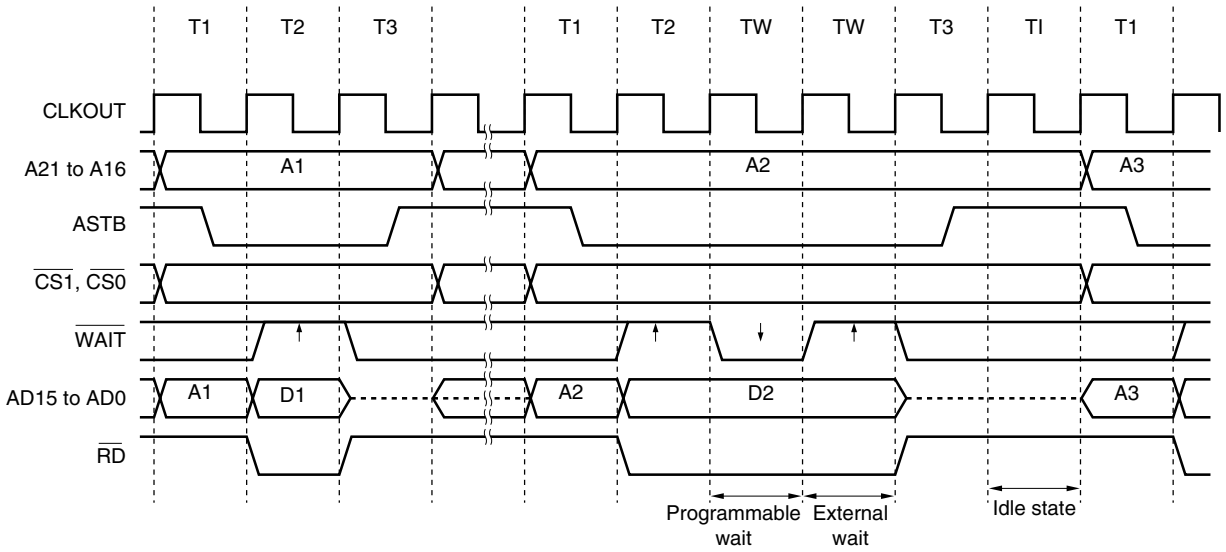
If an instruction is executed for two or more accesses, an instruction fetch and bus hold are not inserted between accesses due to bus size limitations.

Table 5-4. Bus Priority

Priority	External Bus Cycle	Bus Master
High	Bus hold	External device
↕	DMA transfer	DMAC
	Operand data access	CPU
	Instruction fetch (branch)	CPU
Low	Instruction fetch (successive)	CPU

5.10 Bus Timing

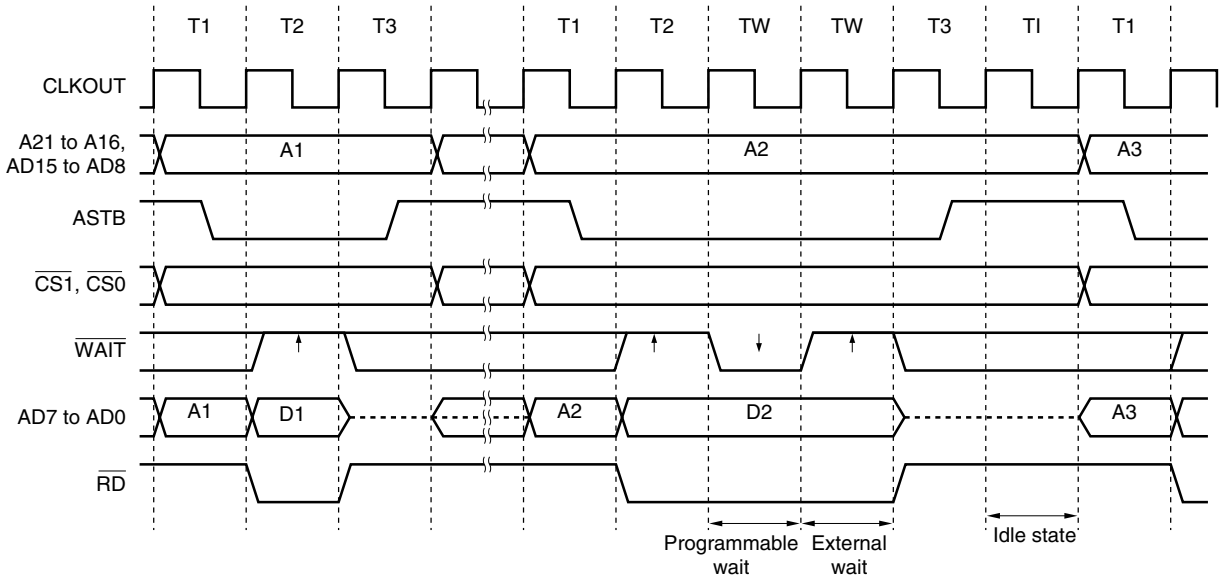
Figure 5-4. Multiplex Bus Read Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Hi-Z
AD7 to AD0	Hi-Z	Active

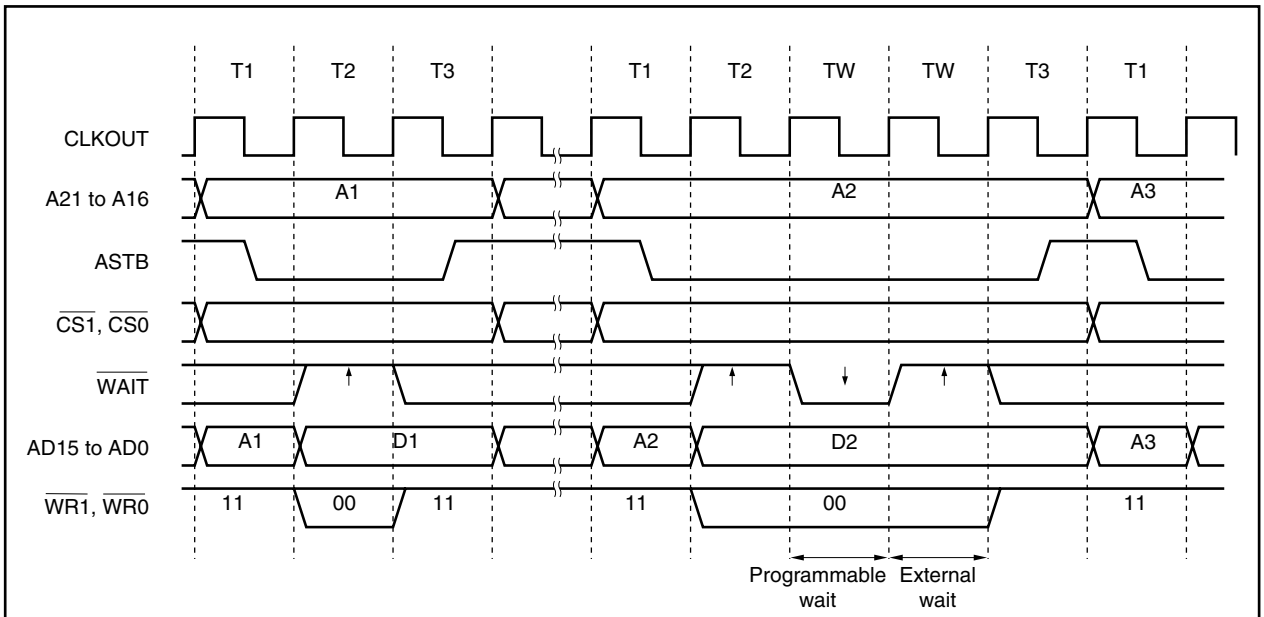
Remark The broken lines indicate high impedance.

Figure 5-5. Multiplex Bus Read Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

Figure 5-6. Multiplex Bus Write Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Undefined
AD7 to AD0	Undefined	Active
$\overline{WR1}$, $\overline{WR0}$	01	10

Figure 5-7. Multiplex Bus Write Timing (Bus Size: 8 Bits)

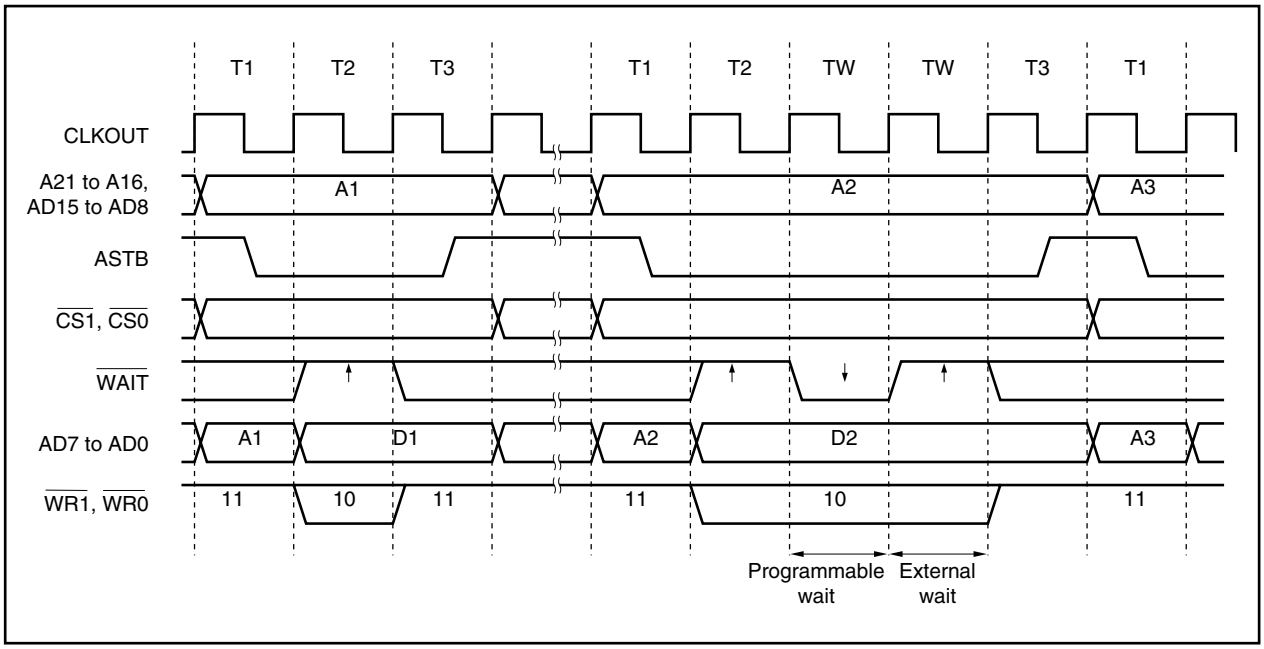
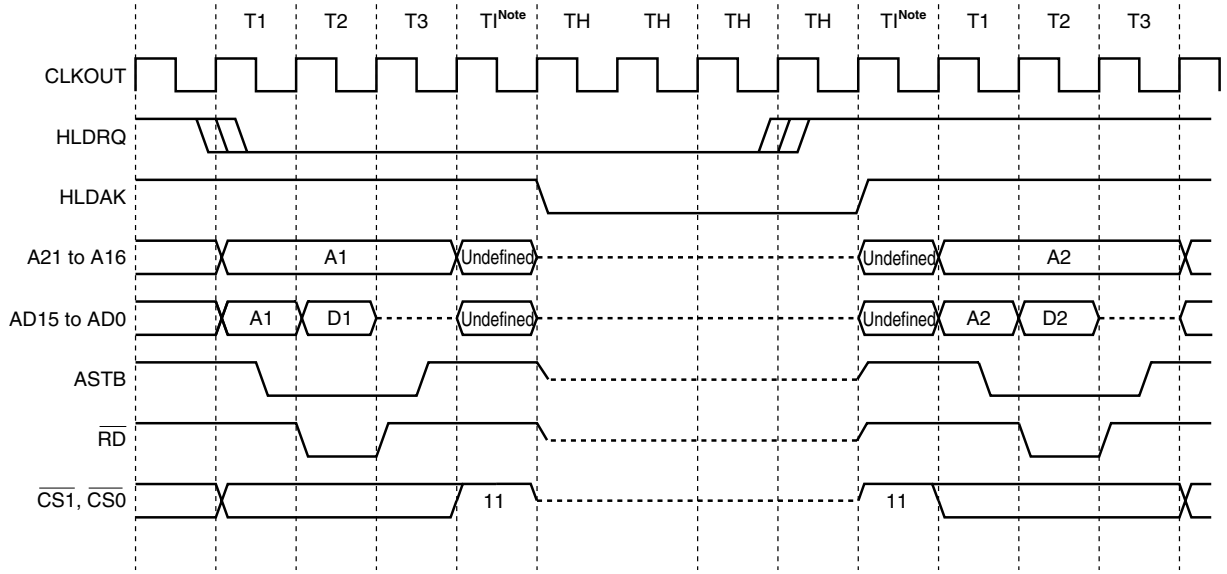


Figure 5-8. Multiplex Bus Hold Timing (Bus Size: 16 Bits, 16-Bit Access)

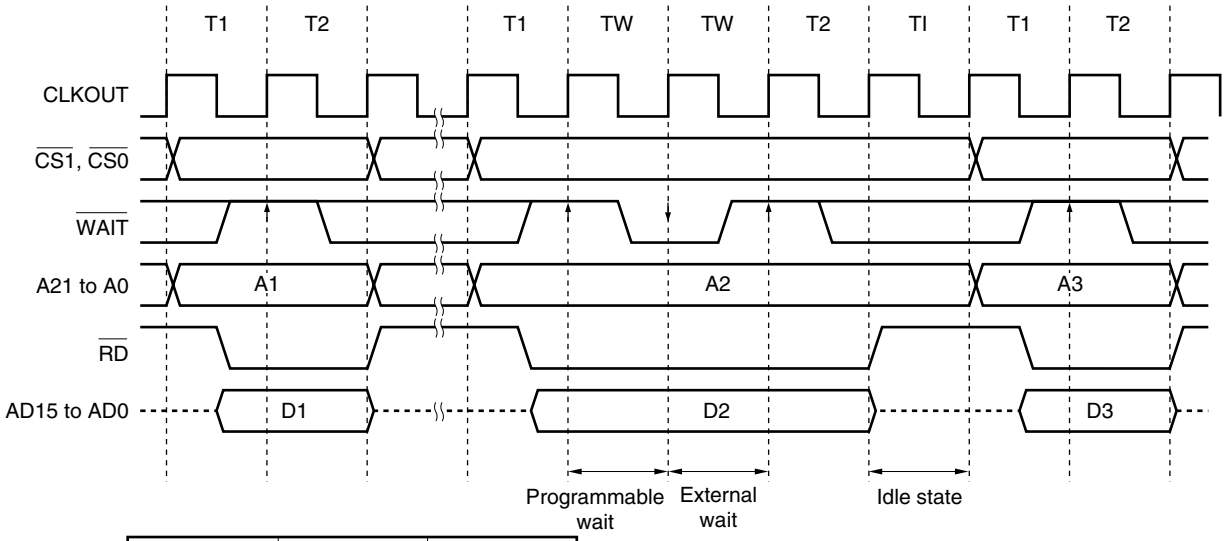


Note This idle state (TI) does not depend on the BCC register settings.

Remarks 1. Refer to **Table 2-2 Pin Operation Status in Operation Modes** for the pin statuses in the bus hold mode.

2. The broken lines indicate high impedance.

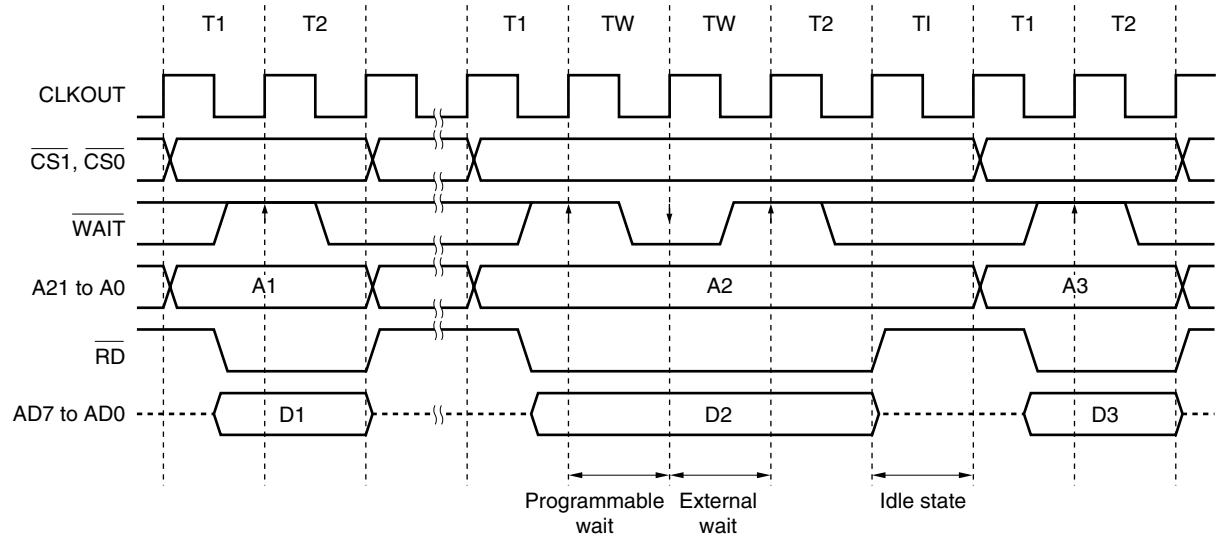
Figure 5-9. Separate Bus Read Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Hi-Z
AD7 to AD0	Hi-Z	Active

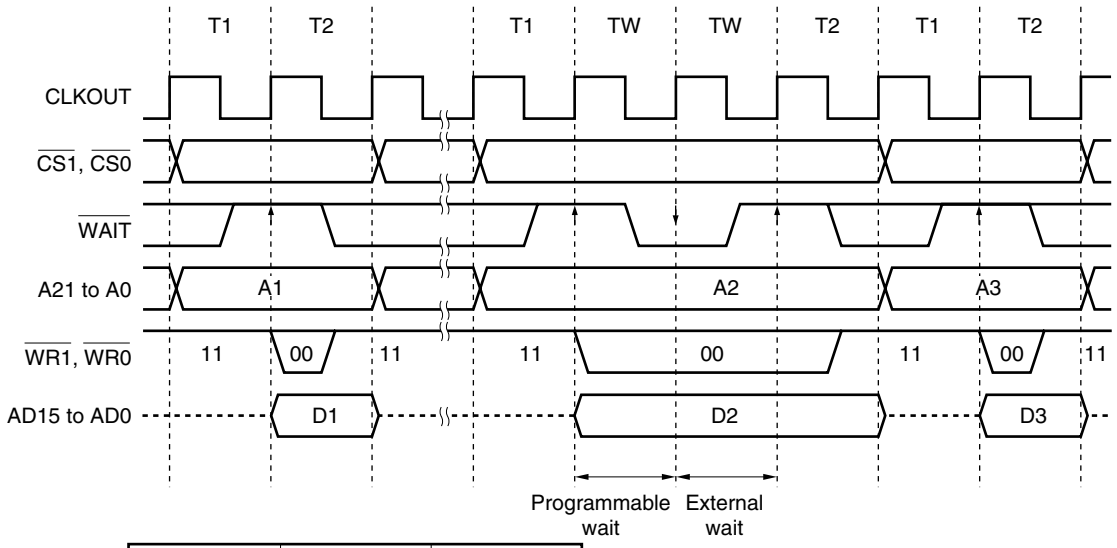
Remark The broken lines indicate high impedance.

Figure 5-10. Separate Bus Read Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

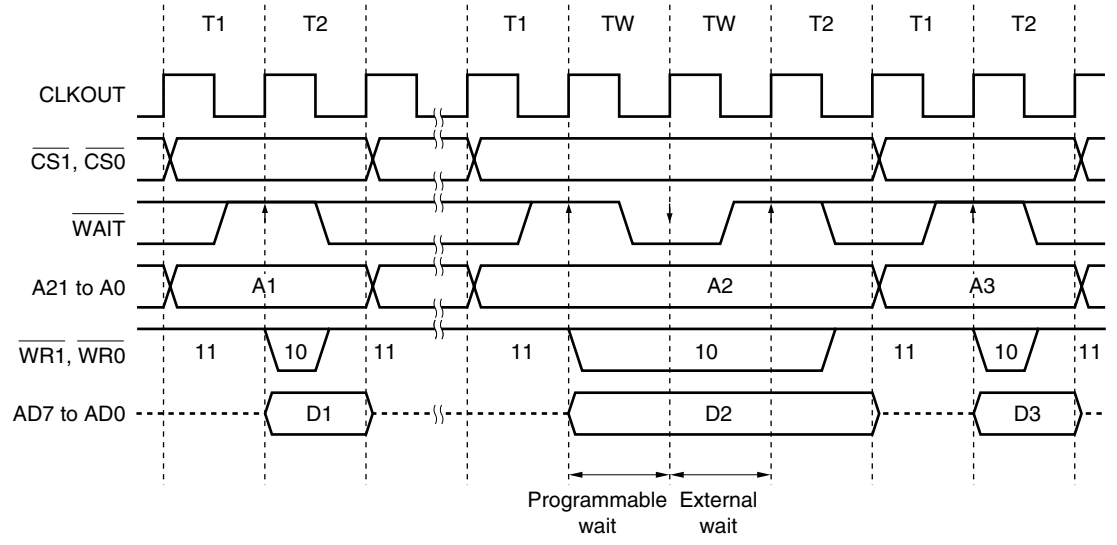
Figure 5-11. Separate Bus Write Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Undefined
AD7 to AD0	Undefined	Active
WR1, WR0	01	10

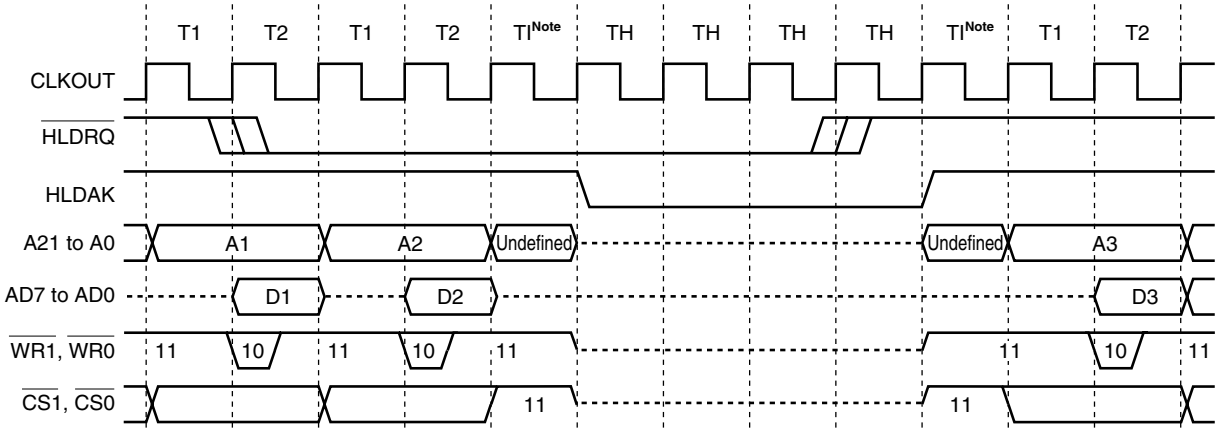
Remark The broken lines indicate high impedance.

Figure 5-12. Separate Bus Write Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

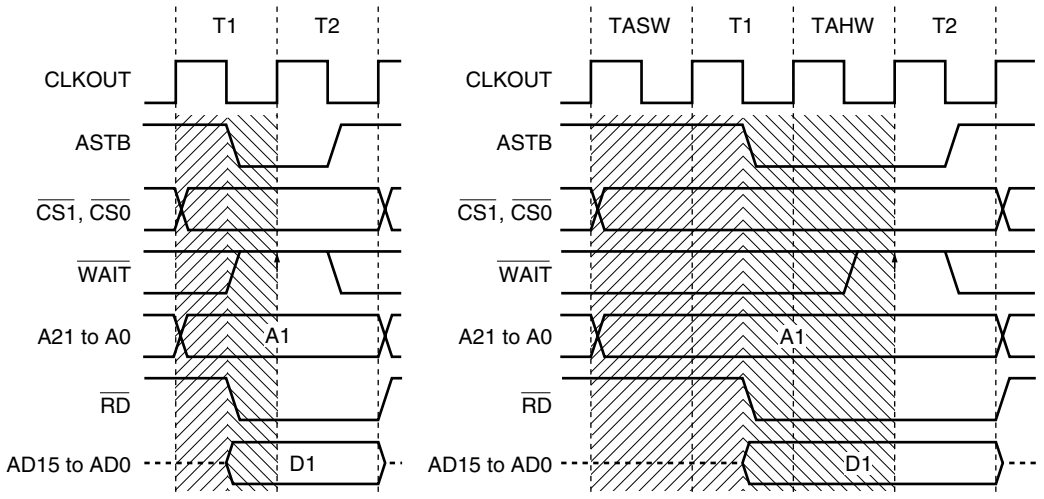
Figure 5-13. Separate Bus Hold Timing (Bus Size: 8 Bits, Write)



Note This idle state (TI) does not depend on the BCC register settings.

Remark The broken lines indicate high impedance.

Figure 5-14. Address Wait Timing (Separate Bus Read, Bus Size: 16 Bits, 16-Bit Access)



Remarks 1. TASW (address setup wait): Image of high-level width of T1 state expanded.

2. TAHW (address hold wait): Image of low-level width of T1 state expanded.

3. The broken lines indicate high impedance.

5.11 Cautions

With the external bus function, signals may not be output at the correct timing under the following conditions.

<Operating conditions>

- Multiplex bus mode
  - <1> CLKOUT asynchronous (2.7 V ≤ V_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V, 2.7 V ≤ BV_{DD} ≤ 5.5 V)
    When 1/f_{CPU} < 84 ns
- Separate bus mode
  - <1> Read cycle, CLKOUT asynchronous (4.0 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
    When 1/f_{CPU} < 100 ns
  - <2> Write cycle, CLKOUT asynchronous (4.0 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
    When 1/f_{CPU} < 60 ns
  - <3> Read cycle, CLKOUT asynchronous (2.7 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
    When 1/f_{CPU} < 200 ns
  - <4> Write cycle, CLKOUT asynchronous (2.7 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
    When 1/f_{CPU} < 100 ns

<Countermeasure>

When used under the above conditions, be sure to insert an address setup/hold wait using the AWC register (n = 0, 1).

- When used in multiplex bus mode and under condition <1>
  - 70 ns < 1/f_{CPU} < 84 ns
    Set an address setup wait (ASWn bit = 1).
  - 62.5 ns < 1/f_{CPU} < 70 ns
    Set an address setup wait (ASWn bit = 1) and address hold wait (AHWn bit = 1).
- When used in separate bus mode and under conditions <1> to <4>
  Set an address setup wait (ASWn bit = 1).

CHAPTER 6 CLOCK GENERATION FUNCTION

6.1 Overview

The following clock generation functions are available.

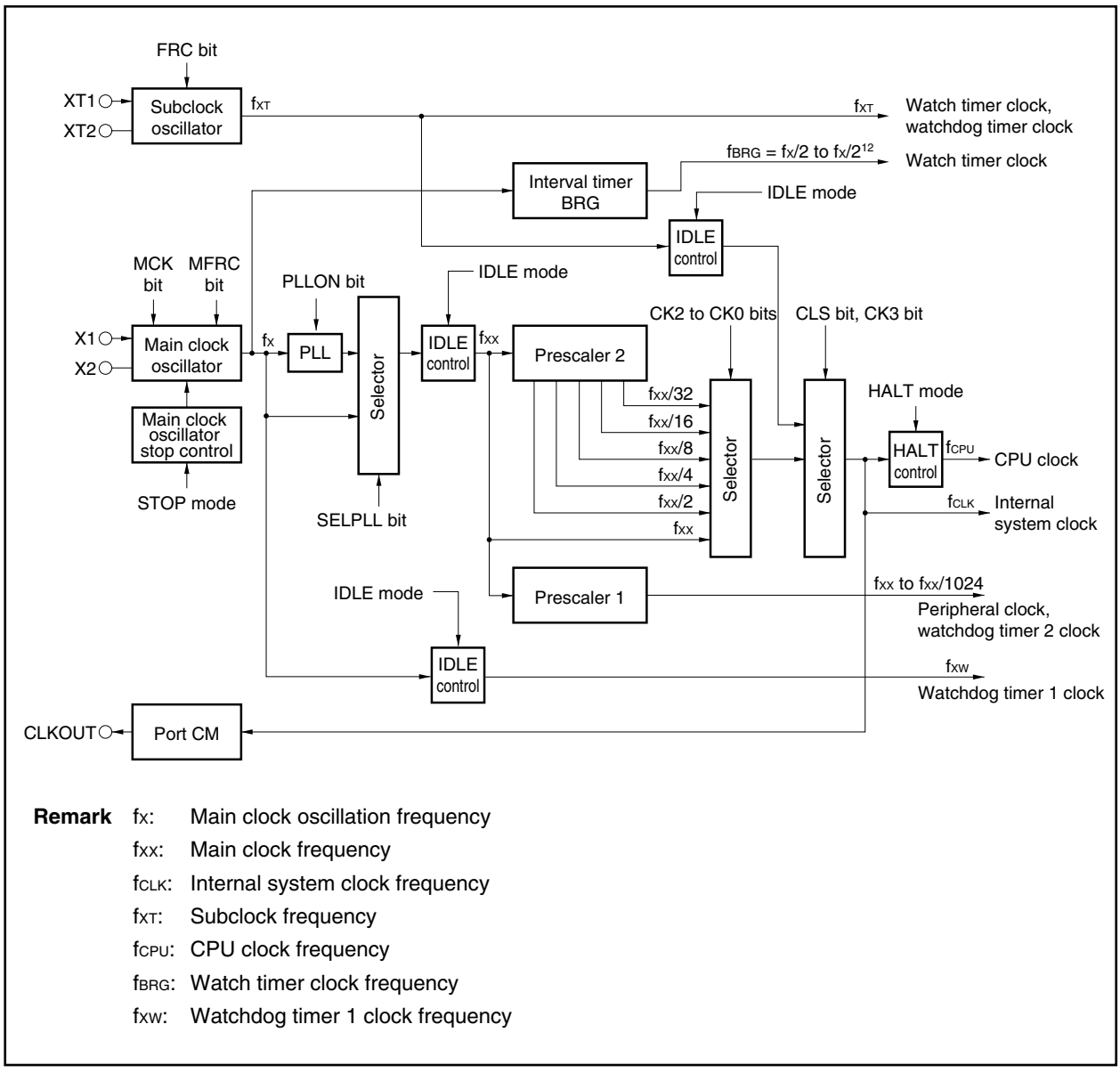
- Main clock oscillator
  <In PLL (×4) mode>
  - f_X = 2 to 5 MHz (f_{XX} = 8 to 20 MHz: 4.5 V ≤ V_{DD} ≤ 5.5 V, REGC = V_{DD})
  - f_X = 2 to 4 MHz (f_{XX} = 8 to 16 MHz: 4.0 V ≤ V_{DD} ≤ 5.5 V, REGC = V_{DD})
  - f_X = 2 to 4 MHz (f_{XX} = 8 to 16 MHz: 4.0 V ≤ V_{DD} ≤ 5.5 V, REGC = 10 μF)
  - f_X = 2 to 2.5 MHz (f_{XX} = 8 to 10 MHz: 2.7 V ≤ V_{DD} ≤ 5.5 V, REGC = V_{DD})

  <In clock through mode>
  - f_X = 2 to 10 MHz (f_{XX} = 2 to 10 MHz: 2.7 V ≤ V_{DD} ≤ 5.5 V, REGC = V_{DD})
  - f_X = 2 to 10 MHz (f_{XX} = 2 to 10 MHz: 4.0 V ≤ V_{DD} ≤ 5.5 V, REGC = 10 μF)
- Subclock oscillator
  - f_{XT} = 32.768 kHz
- Multiplication (×4) function by PLL (Phase Locked Loop)
  - Clock-through mode/PLL mode selectable
  - Usable voltage: V_{DD} = 2.7 to 5.5 V
- Internal system clock generation
  - 7 steps (f_{XX}, f_{XX}/2, f_{XX}/4, f_{XX}/8, f_{XX}/16, f_{XX}/32, f_{XT})
- Peripheral clock generation
- Clock output function

Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency
f_{XT}: Subclock frequency

6.2 Configuration

Figure 6-1. Clock Generator



Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency
f_{CLK}: Internal system clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_{BRG}: Watch timer clock frequency
f_{XW}: Watchdog timer 1 clock frequency

(1) Main clock oscillator

The main clock oscillator oscillates the following frequencies (f_X):

- f_X = 2 to 5 MHz (REGC = V_{DD} = 4.5 to 5.5 V, in PLL mode)
- f_X = 2 to 4 MHz (REGC = V_{DD} = 4.0 to 5.5 V, in PLL mode)
- f_X = 2 to 4 MHz (REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, in PLL mode)
- f_X = 2 to 2.5 MHz (REGC = V_{DD} = 2.7 to 5.5 V, in PLL mode)
- f_X = 2 to 10 MHz (REGC = V_{DD} = 2.7 to 5.5 V, in clock through mode)
- f_X = 2 to 10 MHz (REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, in clock through mode)

(2) Subclock oscillator

The subclock oscillator oscillates a frequency of 32.768 kHz (f_{XT}).

(3) Main clock oscillator stop control

This circuit generates a control signal that stops oscillation of the main clock oscillator.

Oscillation of the main clock oscillator is stopped in the STOP mode or when the PCC.MCK bit = 1 (valid only when the PCC.CLS bit = 1).

(4) Prescaler 1

This prescaler generates the clock (f_{XX} to f_{XX}/1024) to be supplied to the following on-chip peripheral functions: TMP0, TM00 to TM03, TM50, TM51, TMH0, TMH1, CSI00, CSI01, CSIA0, CSIA1, UART0 to UART2, I^2C0, ADC, DAC, and WDT2

(5) Prescaler 2

This circuit divides the main clock (f_{XX}).

The clock generated by prescaler 2 (f_{XX} to f_{XX}/32) is supplied to the selector that generates the CPU clock (f_{CPU}) and internal system clock (f_{CLK}).

f_{CLK} is the clock supplied to the INTC, DMA controller, ROM, and RAM blocks, and can be output from the CLKOUT pin.

(6) Interval timer BRG

This circuit divides the clock (f_X) generated by the main clock oscillator to a specific frequency (32.768 kHz) and supplies that clock to the watch timer block.

For details, refer to **CHAPTER 11 INTERVAL TIMER, WATCH TIMER**.

(7) PLL

This circuit multiplies the clock (f_X) generated by the main clock oscillator.

It operates in two modes: clock-through mode in which f_X is output as is, and PLL mode in which a multiplied clock is output. These modes can be selected by using the PLLCTL.SELPLL bit.

Operation of the PLL can be started or stopped by the PLLCTL.PLLON bit.

6.3 Registers

(1) Processor clock control register (PCC)

The PCC register is a special register. Data can be written to this register only in combination of specific sequences (refer to **3.4.7 Special registers**).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 03H.

(1/2)

After reset: 03H R/W After reset: FFFFF828H

	7	<6>	5	<4>	<3>	2	1	0
PCC	FRC	MCK	MFRC	CLS[Note]	CK3	CK2	CK1	CK0

FRC	Use of subclock on-chip feedback resistor
0	Used
1	Not used

MCK	Control of main clock oscillator
0	Oscillation enabled
1	Oscillation stopped

- Even if the MCK bit is set to 1 while the system is operating with the main clock as the CPU clock, the operation of the main clock does not stop. It stops after the CPU clock has been changed to the subclock.
- When the main clock is stopped and the device is operating on the subclock, clear the MCK bit to 0 and wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

MFRC	Use of main clock on-chip feedback resistor
0	Used
1	Not used

CLS[Note]	Status of CPU clock (f_{CPU})
0	Main clock operation
1	Subclock operation

Note The CLS bit is a read-only bit.

(2/2)

CK3	CK2	CK1	CK0	Clock selection (f_{CLK}/f_{CPU})
0	0	0	0	f_{XX}
0	0	0	1	$f_{XX}/2$
0	0	1	0	$f_{XX}/4$
0	0	1	1	$f_{XX}/8$ (default value)
0	1	0	0	$f_{XX}/16$
0	1	0	1	$f_{XX}/32$
0	1	1	×	Setting prohibited
1	×	×	×	f_{XT}

Cautions 1. Do not change the CPU clock (by using the CK3 to CK0 bits) while CLKOUT is being output.

2. Use a bit manipulation instruction to manipulate the CK3 bit. When using an 8-bit manipulation instruction, do not change the set values of the CK2 to CK0 bits.

3. When the CPU operates on the subclock and no clock is input to the X1 pin, do not access a register in which a wait occurs (refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register for details of the access methods). If a wait occurs, it can only be released by a reset.

Remark ×: don't care

(a) Example of setting main clock operation → subclock operation

<1> CK3 bit ← 1: Use of a bit manipulation instruction is recommended. Do not change the CK2 to CK0 bits.

<2> Subclock operation: Read the CLS bit to check if subclock operation has started. It takes the following time after the CK3 bit is set until subclock operation is started.

Max.: 1/f_{XT} (1/subclock frequency)

<3> MCK bit ← 1: Set the MCK bit to 1 only when stopping the main clock.

Cautions 1. When stopping the main clock, stop the PLL.

2. If the following conditions are not satisfied, change the CK2 to CK0 bits so that the conditions are satisfied, then change to the subclock operation mode.

Internal system clock (f_{CLK}) > Subclock (f_{XT}: 32.768 kHz) × 4

Remark Internal system clock (f_{CLK}): Clock generated from the main clock (f_{XX}) by setting bits CK2 to CK0

[Description example]

```
<1>  _SET_SUB_RUN :
     st.b        r0, PRCMD[r0]
     set1        3, PCC[r0]          -- CK3 bit ← 1
<2>  _CHECK_CLS :
     tst1        4, PCC[r0]          -- Wait until subclock operation starts.
     bz          _CHECK_CLS
<3>  _STOP_MAIN_CLOCK :
     st.b        r0, PRCMD[r0]
     set1        6, PCC[r0]          -- MCK bit ← 1, main clock is stopped
```

Remark The above description is an example. Note with caution that the CLS bit is read in a closed loop in <2>.

(b) Example of setting subclock operation → main clock operation

<1> MCK bit ← 0: Main clock starts oscillating

<2> Insert waits by the program and wait until the oscillation stabilization time of the main clock elapses.

<3> CK3 bit ← 0: Use of a bit manipulation instruction is recommended. Do not change the CK2 to CK0 bits.

<4> Main clock operation: It takes the following time after the CK3 bit is set until main clock operation is started.

Max.: 1/f_{XT} (1/subclock frequency)

Therefore, insert one NOP instruction immediately after setting the CK3 bit to 0 or read the CLS bit to check if main clock operation has started.

[Description example]

```
<1> _START_MAIN_OSC :
    st.b        r0, PRCMD[r0]       -- Release of protection of special registers
    clr1        6, PCC[r0]          -- Main clock starts oscillating
<2> movea       0x55, r0, r11       -- Wait for oscillation stabilization time
    _WAIT_OST :
    nop
    nop
    nop
    addi        -1, r11, r11
    mp          r0, r11
    bne         _PROGRAM_WAIT
<3> st.b        r0, PRCMD[r0]
    clr1        3, PCC[r0]          -- CK3 ← 0
<4> _CHECK_CLS :
    tst1        4, PCC[r0]          -- Wait until main clock operation starts
    bnz         _CHECK_CLS
```

Remark The above description is an example. Note with caution that the CLS bit is read in a closed loop in <4>.

6.4 Operation

6.4.1 Operation of each clock

The following table shows the operation status of each clock.

Table 6-1. Operation Status of Each Clock

Register Setting and Operation Status / Target Clock	PCC Register								
	CLS bit = 0, MCK bit = 0					CLS bit = 1, MCK bit = 0		CLS bit = 1, MCK bit = 1	
	During reset	During oscillation stabilization time count	HALT mode	IDLE mode	STOP mode	Subclock mode	Sub-IDLE mode	Subclock mode	Sub-IDLE mode
Main clock oscillator (f_X)	×	○	○	○	×	○	○	×	×
Subclock oscillator (f_{XT})	○	○	○	○	○	○	○	○	○
CPU clock (f_{CPU})	×	×	×	×	×	○	×	○	×
Internal system clock (f_{CLK})	×	×	○	×	×	○	×	○	×
Peripheral clock (f_{XX} to f_{XX}/1024)	×	×	○	×	×	○	×	×	×
WT clock (main)	×	○	○	○	×	○	○	×	×
WT clock (sub)	○	○	○	○	○	○	○	○	○
WDT1 clock (f_{XW})	×	○	○	○	×	○	○	×	×
WDT2 clock (main)	×	×	○	×	×	○	×	×	×
WDT2 clock (sub)	○	○	○	○	○	○	○	○	○

Remark ○: Operable
×: Stopped

6.4.2 Clock output function

The clock output function is used to output the internal system clock (f_{CLK}) from the CLKOUT pin.

The internal system clock (f_{CLK}) is selected by using the PCC.CK3 to PCC.CK0 bits.

The CLKOUT pin functions alternately as the PCM1 pin and functions as a clock output pin if so specified by the control register of port CM.

The status of the CLKOUT pin is the same as the internal system clock in Table 6-1 and the pin can output the clock when it is in the operable status. It outputs a low level in the stopped status. However, the port mode (PCM1: input mode) is selected until the CLKOUT pin output is set after reset. Consequently, the CLKOUT pin goes into a high-impedance state.

6.4.3 External clock input function

An external clock can be directly input to the oscillator. Input the clock to the X1 pin and its inverse signal to the X2 pin. Set the PCC.MFRC bit to 1 (on-chip feedback resistor not used). Note, however, that oscillation stabilization time is inserted even in the external clock mode. Connect V_{DD} directly to the REGC pin.

6.5 PLL Function

6.5.1 Overview

The PLL function is used to output the operating clock of the CPU and on-chip peripheral function at a frequency 4 times higher than the oscillation frequency, and select the clock-through mode.

When PLL function is used: Input clock = 2 to 5 MHz (f_{XX}: 8 to 20 MHz)
Clock-through mode: Input clock = 2 to 10 MHz (f_{XX}: 2 to 10 MHz)

6.5.2 Register

(1) PLL control register (PLLCTL)

The PLLCTL register is an 8-bit register that controls the security function of PLL and RTO.
This register can be read or written in 8-bit or 1-bit units.
Reset sets this register to 01H.

After reset: 01H R/W Address: FFFFF806H

	7	6	5	4	3	<2>	<1>	<0>
PLLCTL	0	0	0	0	0	RTOST0[Note]	SELPLL	PLLON

PLLON	PLL operation control
0	PLL stopped
1	PLL operating

SELPLL	PLL clock selection
0	Clock-through operation
1	PLL operation

Note For the RTOST0 bit, refer to **CHAPTER 13 REAL-TIME OUTPUT FUNCTION (RTO)**.

Caution Be sure to clear bits 4 to 7 to "0". Changing bit 3 does not affect the operation.

6.5.3 Usage

(1) When PLL is used

- After reset has been released, the PLL operates (PLLCTL.PLLON bit = 1), but because the default mode is the clock-through mode (PLLCTL.SELPLL bit = 0), select the PLL mode (SELPLL bit = 1).
- To set the STOP mode in which the main clock is stopped, or to set the IDLE mode, first select the clock-through mode and then stop the PLL. To return from the IDLE or STOP mode, first enable PLL operation (PLLON bit = 1), and then select the PLL mode (SELPLL bit = 1).
- To enable the PLL operation, first set the PLLON bit to 1, wait for 200 μs, and then set the SELPLL bit to 1. To stop the PLL, first select the clock-through mode (SELPLL bit = 0), wait for 8 clocks or more, and then stop the PLL (PLLON bit = 0).

(2) When PLL is not used

- The clock-through mode (SELPLL bit = 0) is selected after reset has been released, but the PLL is operating (PLLON bit = 1) and must therefore be stopped (PLLON bit = 0).

Remark The PLL is operable in the IDLE mode. To realize low power consumption, stop the PLL. Be sure to stop the PLL when shifting to the STOP mode.

CHAPTER 7 16-BIT TIMER/EVENT COUNTER P (TMP)

Timer P (TMP) is a 16-bit timer/event counter.

7.1 Overview

An outline of TMP0 is shown below.

- Clock selection: 8 ways
- Capture trigger input pins: 2
- External event count input pins: 1
- External trigger input pins: 1
- Timer/counters: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins: 2

7.2 Functions

TMP0 has the following functions.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement

7.3 Configuration

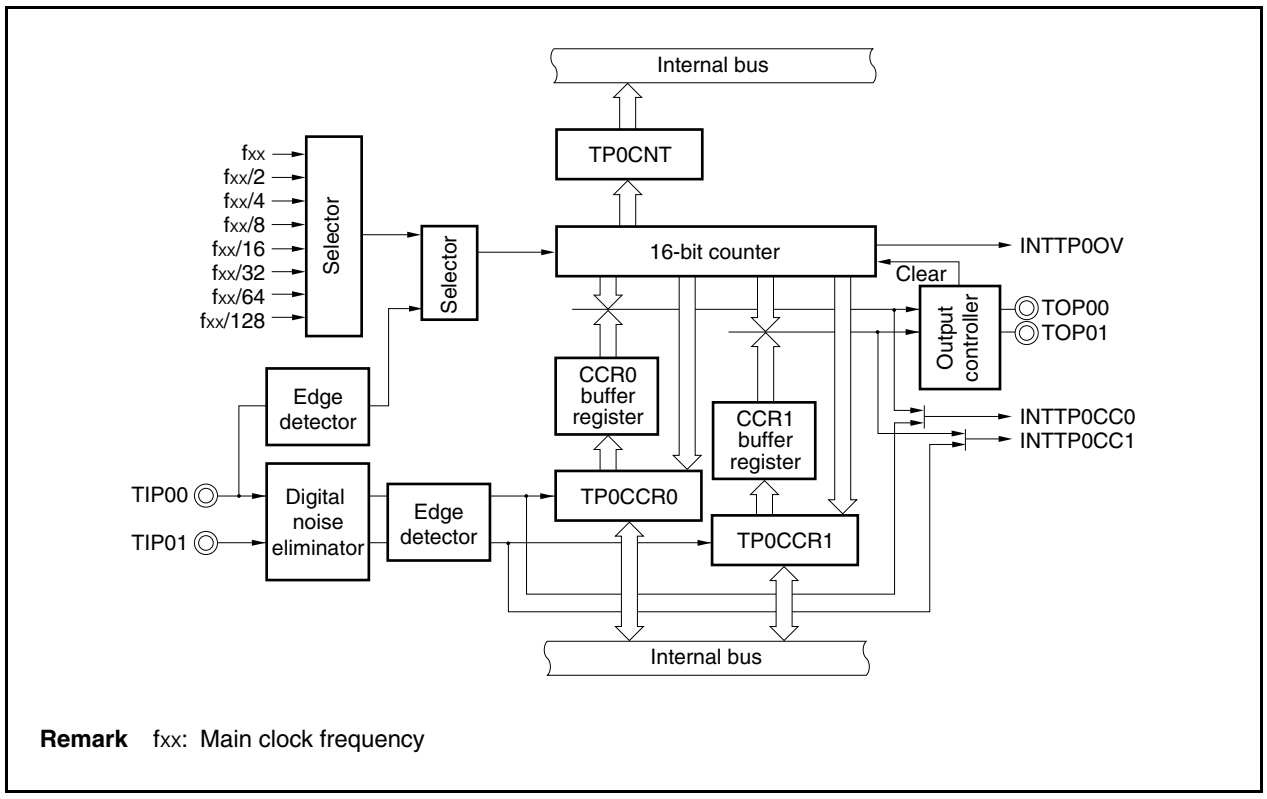
TMP0 includes the following hardware.

Table 7-1. Configuration of TMP0

Item	Configuration
Timer register	16-bit counter
Registers	TMP0 capture/compare registers 0, 1 (TP0CCR0, TP0CCR1) TMP0 counter read buffer register (TP0CNT) CCR0, CCR1 buffer registers
Timer inputs	2 (TIP00[Note], TIP01 pins)
Timer outputs	2 (TOP00, TOP01 pins)
Control registers	TMP0 control registers 0, 1 (TP0CTL0, TP0CTL1) TMP0 I/O control registers 0 to 2 (TP0IOC0 to TP0IOC2) TMP0 option register 0 (TP0OPT0)

Note The TIP00 pin functions alternately as a capture trigger input signal, external event count input signal, and external trigger input signal.

Figure 7-1. Block Diagram of TMP0



Remark fxx: Main clock frequency

(1) 16-bit counter

This 16-bit counter can count internal clocks or external events.

The count value of this counter can be read by using the TP0CNT register.

When the TP0CTL0.TP0CE bit = 0, the value of the 16-bit counter is FFFFH. If the TP0CNT register is read at this time, 0000H is read.

Reset sets the TP0CE bit to 0. Therefore, the 16-bit counter is set to FFFFH.

(2) CCR0 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TP0CCR0 register is used as a compare register, the value written to the TP0CCR0 register is transferred to the CCR0 buffer register. When the count value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTP0CC0) is generated.

The CCR0 buffer register cannot be read or written directly.

The CCR0 buffer register is cleared to 0000H after reset, as the TP0CCR0 register is cleared to 0000H.

(3) CCR1 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TP0CCR1 register is used as a compare register, the value written to the TP0CCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTP0CC1) is generated.

The CCR1 buffer register cannot be read or written directly.

The CCR1 buffer register is cleared to 0000H after reset, as the TP0CCR1 register is cleared to 0000H.

(4) Edge detector

This circuit detects the valid edges input to the TIP00 and TIP01 pins. No edge, rising edge, falling edge, or both the rising and falling edges can be selected as the valid edge by using the TP0IOC1 and TP0IOC2 registers.

(5) Output controller

This circuit controls the output of the TOP00 and TOP01 pins. The output controller is controlled by the TP0IOC0 register.

(6) Selector

This selector selects the count clock for the 16-bit counter. Eight types of internal clocks or an external event can be selected as the count clock.

(7) Digital noise eliminator

This circuit is valid only when the TIP0a pin is used as a capture trigger input pin.

This circuit is controlled by the TIP0a noise elimination register (PaNFC).

Remark a = 0, 1

7.4 Registers

(1) TMP0 control register 0 (TP0CTL0)

The TP0CTL0 register is an 8-bit register that controls the operation of TMP0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TP0CTL0 register by software.

After reset: 00H R/W Address: FFFFF5A0H

	<7>	6	5	4	3	2	1	0
TP0CTL0	TP0CE	0	0	0	0	TP0CKS2	TP0CKS1	TP0CKS0

TP0CE	TMP0 operation control
0	TMP0 operation disabled (TMP0 reset asynchronously[Note]).
1	TMP0 operation enabled. TMP0 operation started.

TP0CKS2	TP0CKS1	TP0CKS0	Internal count clock selection
0	0	0	f_{XX}
0	0	1	$f_{XX}/2$
0	1	0	$f_{XX}/4$
0	1	1	$f_{XX}/8$
1	0	0	$f_{XX}/16$
1	0	1	$f_{XX}/32$
1	1	0	$f_{XX}/64$
1	1	1	$f_{XX}/128$

Note TP0OPT0.TP0OVF bit, 16-bit counter, timer output (TOP00, TOP01 pins)

Cautions 1. Set the TP0CKS2 to TP0CKS0 bits when the TP0CE bit = 0. When the value of the TP0CE bit is changed from 0 to 1, the TP0CKS2 to TP0CKS0 bits can be set simultaneously.

2. Be sure to clear bits 3 to 6 to "0".

Remark f_{XX}: Main clock frequency

(2) TMP0 control register 1 (TP0CTL1)

The TP0CTL1 register is an 8-bit register that controls the operation of TMP0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF5A1H

	7	<6>	<5>	4	3	2	1	0
TP0CTL1	0	TP0EST	TP0EEE	0	0	TP0MD2	TP0MD1	TP0MD0

TP0EST	Software trigger control
0	–
1	Generate a valid signal for external trigger input. • In one-shot pulse output mode: A one-shot pulse is output with writing 1 to the TP0EST bit as the trigger. • In external trigger pulse output mode: A PWM waveform is output with writing 1 to the TP0EST bit as the trigger.

TP0EEE	Count clock selection
0	Disable operation with external event count input. (Perform counting with the count clock selected by the TP0CTL0.TP0CK0 to TP0CTL0.TP0CK2 bits.)
1	Enable operation with external event count input. (Perform counting at the valid edge of the external event count input signal.)
The TP0EEE bit selects whether counting is performed with the internal count clock or the valid edge of the external event count input.	

TP0MD2	TP0MD1	TP0MD0	Timer mode selection
0	0	0	Interval timer mode
0	0	1	External event count mode
0	1	0	External trigger pulse output mode
0	1	1	One-shot pulse output mode
1	0	0	PWM output mode
1	0	1	Free-running timer mode
1	1	0	Pulse width measurement mode
1	1	1	Setting prohibited

Cautions 1. The TP0EST bit is valid only in the external trigger pulse output mode or one-shot pulse output mode. In any other mode, writing 1 to this bit is ignored.

2. External event count input is selected in the external event count mode regardless of the value of the TP0EEE bit.

3. Set the TP0EEE and TP0MD2 to TP0MD0 bits when the TP0CTL0.TP0CE bit = 0. (The same value can be written when the TP0CE bit = 1.) The operation is not guaranteed when rewriting is performed with the TP0CE bit = 1. If rewriting was mistakenly performed, clear the TP0CE bit to 0 and then set the bits again.

4. Be sure to clear bits 3, 4, and 7 to "0".

(3) TMP0 I/O control register 0 (TP0IOC0)

The TP0IOC0 register is an 8-bit register that controls the timer output (TOP00, TOP01 pins).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF5A2H

	7	6	5	4	3	<2>	1	<0>
TP0IOC0	0	0	0	0	TP0OL1	TP0OE1	TP0OL0	TP0OE0

TP0OL1	TOP01 pin output level setting
0	TOP01 pin output inversion disabled
1	TOP01 pin output inversion enabled

TP0OE1	TOP01 pin output setting
0	Timer output disabled • When TP0OL1 bit = 0: Low level is output from the TOP01 pin • When TP0OL1 bit = 1: High level is output from the TOP01 pin
1	Timer output enabled (a square wave is output from the TOP01 pin).

TP0OL0	TOP00 pin output level setting
0	TOP00 pin output inversion disabled
1	TOP00 pin output inversion enabled

TP0OE0	TOP00 pin output setting
0	Timer output disabled • When TP0OL0 bit = 0: Low level is output from the TOP00 pin • When TP0OL0 bit = 1: High level is output from the TOP00 pin
1	Timer output enabled (a square wave is output from the TOP00 pin).

Cautions 1. Rewrite the TP0OL1, TP0OE1, TP0OL0, and TP0OE0 bits when the TP0CTL0.TP0CE bit = 0. (The same value can be written when the TP0CE bit = 1.) If rewriting was mistakenly performed, clear the TP0CE bit to 0 and then set the bits again.

2. Even if the TP0OLa bit is manipulated when the TP0CE and TP0OEa bits are 0, the TOP0a pin output level varies (a = 0, 1).

(4) TMP0 I/O control register 1 (TP0IOC1)

The TP0IOC1 register is an 8-bit register that controls the valid edge of the capture trigger input signals (TIP00, TIP01 pins).

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF5A3H

	7	6	5	4	3	2	1	0
TP0IOC1	0	0	0	0	TP0IS3	TP0IS2	TP0IS1	TP0IS0

TP0IS3	TP0IS2	Capture trigger input signal (TIP01 pin) valid edge setting
0	0	No edge detection (capture operation invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TP0IS1	TP0IS0	Capture trigger input signal (TIP00 pin) valid edge setting
0	0	No edge detection (capture operation invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions 1. Rewrite the TP0IS3 to TP0IS0 bits when the TP0CTL0.TP0CE bit = 0. (The same value can be written when the TP0CE bit = 1.) If rewriting was mistakenly performed, clear the TP0CE bit to 0 and then set the bits again.

2. The TP0IS3 to TP0IS0 bits are valid only in the free-running timer mode and the pulse width measurement mode. In all other modes, a capture operation is not possible.

(5) TMP0 I/O control register 2 (TP0IOC2)

The TP0IOC2 register is an 8-bit register that controls the valid edge of the external event count input signal (TIP00 pin) and external trigger input signal (TIP00 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF5A4H

	7	6	5	4	3	2	1	0
TP0IOC2	0	0	0	0	TP0EES1	TP0EES0	TP0ETS1	TP0ETS0

TP0EES1	TP0EES0	External event count input signal (TIP00 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TP0ETS1	TP0ETS0	External trigger input signal (TIP00 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions 1. Rewrite the TP0EES1, TP0EES0, TP0ETS1, and TP0ETS0 bits when the TP0CTL0.TP0CE bit = 0. (The same value can be written when the TP0CE bit = 1.) If rewriting was mistakenly performed, clear the TP0CE bit to 0 and then set the bits again.

2. The TP0EES1 and TP0EES0 bits are valid only when the TP0CTL1.TP0EEE bit = 1 or when the external event count mode (TP0CTL1.TP0MD2 to TP0CTL1.TP0MD0 bits = 001) has been set.

3. The TP0ETS1 and TP0ETS0 bits are valid only when the external trigger pulse output mode (TP0MD2 to TP0MD0 bits = 010) or the one-shot pulse output mode (TP0MD2 to TP0MD0 bits = 011) is set.

(6) TMP0 option register 0 (TP0OPT0)

The TP0OPT0 register is an 8-bit register used to set the capture/compare operation and detect an overflow.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF5A5H

	7	6	5	4	3	2	1	<0>
TP0OPT0	0	0	TP0CCS1	TP0CCS0	0	0	0	TP0OVF

TP0CCS1	TP0CCR1 register capture/compare selection
0	Compare register selected
1	Capture register selected
The TP0CCS1 bit setting is valid only in the free-running timer mode.	

TP0CCS0	TP0CCR0 register capture/compare selection
0	Compare register selected
1	Capture register selected
The TP0CCS0 bit setting is valid only in the free-running timer mode.	

TP0OVF	TMP0 overflow detection flag
Set (1)	Overflow occurred
Reset (0)	TP0OVF bit 0 written or TP0CTL0.TP0CE bit = 0
• The TP0OVF bit is reset when the 16-bit counter count value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode. • An interrupt request signal (INTTP0OV) is generated at the same time that the TP0OVF bit is set to 1. The INTTP0OV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode. • The TP0OVF bit is not cleared even when the TP0OVF bit or the TP0OPT0 register are read when the TP0OVF bit = 1. • The TP0OVF bit can be both read and written, but the TP0OVF bit cannot be set to 1 by software. Writing 1 has no influence on the operation of TMP0.	

Cautions 1. Rewrite the TP0CCS1 and TP0CCS0 bits when the TP0CE bit = 0. (The same value can be written when the TP0CE bit = 1.) If rewriting was mistakenly performed, clear the TP0CE bit to 0 and then set the bits again.

2. Be sure to clear bits 1 to 3, 6, and 7 to "0".

(7) TMP0 capture/compare register 0 (TP0CCR0)

The TP0CCR0 register can be used as a capture register or a compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TP0OPT0.TP0CCS0 bit. In the pulse width measurement mode, the TP0CCR0 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TP0CCR0 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TP0CCR0 register is disabled during subclock operation with the main clock stopped. For details, refer to 3.4.8 (1) (b).

After reset: 0000H R/W Address: FFFFF5A6H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP0CCR0																

(a) Function as compare register

The TP0CCR0 register can be rewritten even when the TP0CTL0.TP0CE bit = 1.

The set value of the TP0CCR0 register is transferred to the CCR0 buffer register. When the value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTP0CC0) is generated. If TOP00 pin output is enabled at this time, the output of the TOP00 pin is inverted.

When the TP0CCR0 register is used as a cycle register in the interval timer mode, external event count mode, external trigger pulse output mode, one-shot pulse output mode, or PWM output mode, the value of the 16-bit counter is cleared (0000H) if its count value matches the value of the CCR0 buffer register.

(b) Function as capture register

When the TP0CCR0 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TP0CCR0 register if the valid edge of the capture trigger input pin (TIP00 pin) is detected. In the pulse width measurement mode, the count value of the 16-bit counter is stored in the TP0CCR0 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIP00 pin) is detected.

Even if the capture operation and reading the TP0CCR0 register conflict, the correct value of the TP0CCR0 register can be read.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 7-2. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	–

(8) TMP0 capture/compare register 1 (TP0CCR1)

The TP0CCR1 register can be used as a capture register or a compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TP0OPT0.TP0CCS1 bit. In the pulse width measurement mode, the TP0CCR1 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TP0CCR1 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TP0CCR1 register is disabled during subclock operation with the main clock stopped. For details, refer to 3.4.8 (1) (b).

After reset: 0000H R/W Address: FFFFF5A8H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP0CCR1																

(a) Function as compare register

The TP0CCR1 register can be rewritten even when the TP0CTL0.TP0CE bit = 1.

The set value of the TP0CCR1 register is transferred to the CCR1 buffer register. When the value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTP0CC1) is generated. If TOP01 pin output is enabled at this time, the output of the TOP01 pin is inverted.

(b) Function as capture register

When the TP0CCR1 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TP0CCR1 register if the valid edge of the capture trigger input pin (TIP01 pin) is detected. In the pulse width measurement mode, the count value of the 16-bit counter is stored in the TP0CCR1 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIP01 pin) is detected.

Even if the capture operation and reading the TP0CCR1 register conflict, the correct value of the TP0CCR1 register can be read.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 7-3. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	–

(9) TMP0 counter read buffer register (TP0CNT)

The TP0CNT register is a read buffer register that can read the count value of the 16-bit counter.

If this register is read when the TP0CTL0.TP0CE bit = 1, the count value of the 16-bit timer can be read.

This register is read-only, in 16-bit units.

The value of the TP0CNT register is cleared to 0000H when the TP0CE bit = 0. If the TP0CNT register is read at this time, the value of the 16-bit counter (FFFFH) is not read, but 0000H is read.

The value of the TP0CNT register is cleared to 0000H after reset, as the TP0CE bit is cleared to 0.

Caution Accessing the TP0CNT register is disabled during subclock operation with the main clock stopped. For details, refer to 3.4.8 (1) (b).

After reset: 0000H R Address: FFFFF5AAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP0CNT																

7.5 Operation

TMP0 can perform the following operations.

Operation	TP0CTL1.TP0EST Bit (Software Trigger Bit)	TIP00 Pin (External Trigger Input)	Capture/Compare Register Setting	Compare Register Write
Interval timer mode	Invalid	Invalid	Compare only	Anytime write
External event count mode[Note 1]	Invalid	Invalid	Compare only	Anytime write
External trigger pulse output mode[Note 2]	Valid	Valid	Compare only	Batch write
One-shot pulse output mode[Note 2]	Valid	Valid	Compare only	Anytime write
PWM output mode	Invalid	Invalid	Compare only	Batch write
Free-running timer mode	Invalid	Invalid	Switching enabled	Anytime write
Pulse width measurement mode[Note 2]	Invalid	Invalid	Capture only	Not applicable

Notes 1. To use the external event count mode, specify that the valid edge of the TIP00 pin capture trigger input is not detected (by clearing the TP0IOC1.TP0IS1 and TP0IOC1.TP0IS0 bits to “00”).

2. When using the external trigger pulse output mode, one-shot pulse output mode, and pulse width measurement mode, select the internal clock as the count clock (by clearing the TP0CTL1.TP0EEE bit to 0).

7.5.1 Interval timer mode (TP0MD2 to TP0MD0 bits = 000)

In the interval timer mode, an interrupt request signal (INTTP0CC0) is generated at the specified interval if the TP0CTL0.TP0CE bit is set to 1. A square wave whose half cycle is equal to the interval can be output from the TOP00 pin.

Usually, the TP0CCR1 register is not used in the interval timer mode.

Figure 7-2. Configuration of Interval Timer

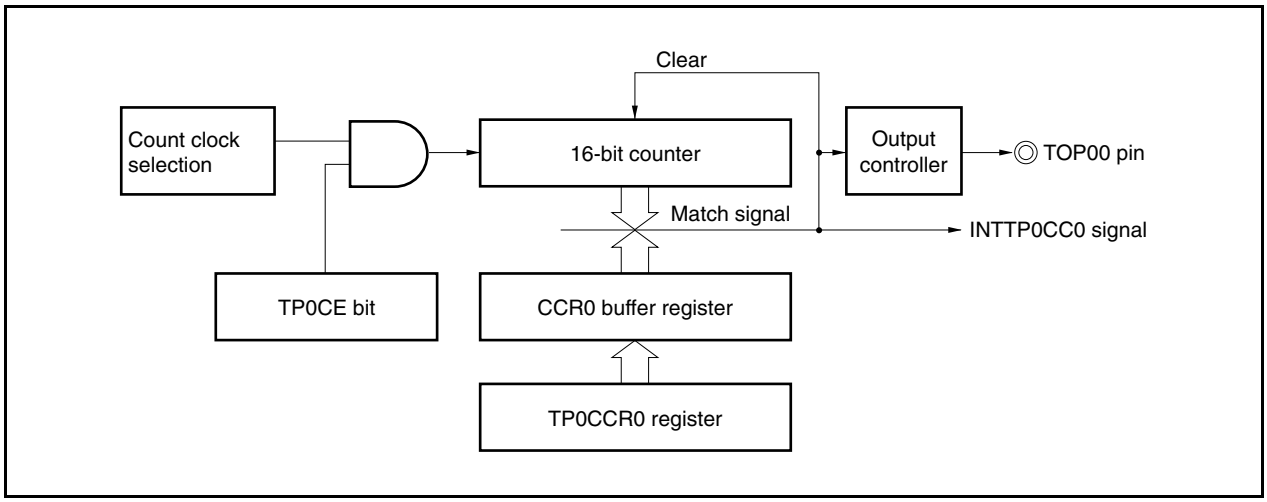
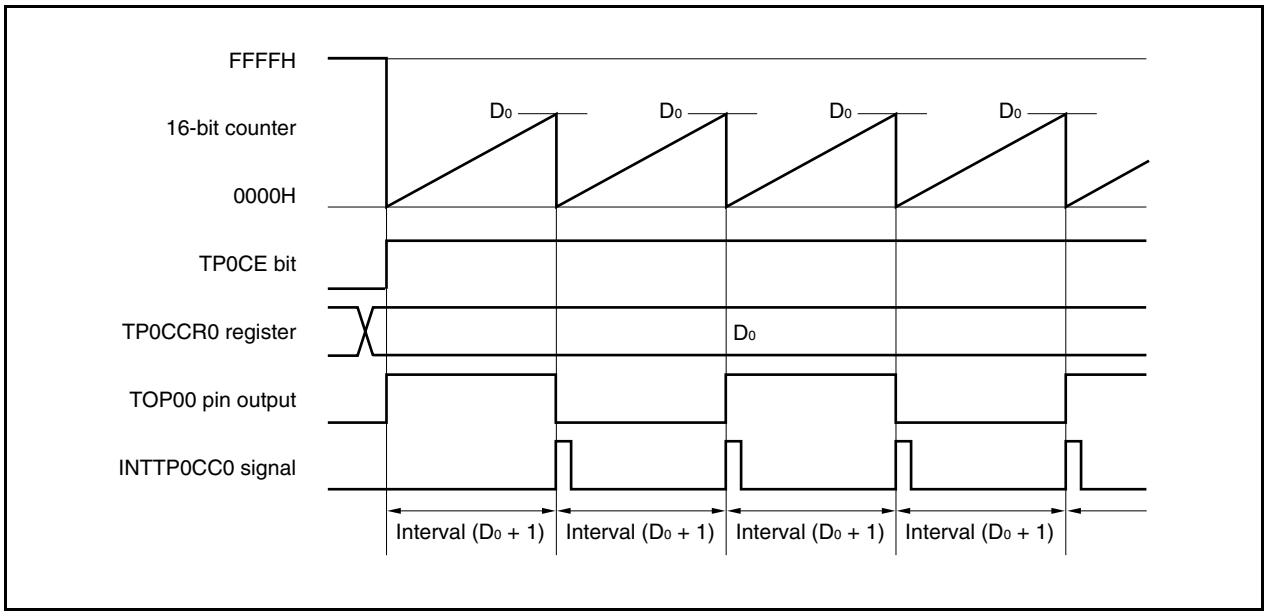


Figure 7-3. Basic Timing of Operation in Interval Timer Mode



When the TP0CE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H in synchronization with the count clock, and the counter starts counting. At this time, the output of the TOP00 pin is inverted. Additionally, the set value of the TP0CCR0 register is transferred to the CCR0 buffer register.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, the output of the TOP00 pin is inverted, and a compare match interrupt request signal (INTTP0CC0) is generated.

The interval can be calculated by the following expression.

Interval = (Set value of TP0CCR0 register + 1) × Count clock cycle

Figure 7-4. Register Setting for Interval Timer Mode Operation (1/2)

(a) TMP0 control register 0 (TP0CTL0)

	TP0CE					TP0CKS2	TP0CKS1	TP0CKS0
TP0CTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock

0: Stop counting
1: Enable counting

(b) TMP0 control register 1 (TP0CTL1)

			TP0EST	TP0EEE			TP0MD2	TP0MD1	TP0MD0
TP0CTL1	0	0	0	0/1[Note]	0	0	0	0	0

0, 0, 0:
Interval timer mode

0: Operate on count clock selected by TP0CKS0 to TP0CKS2 bits
1: Count with external event count input signal

(c) TMP0 I/O control register 0 (TP0IOC0)

					TP0OL1	TP0OE1	TP0OL0	TP0OE0
TP0IOC0	0	0	0	0	0/1	0/1	0/1	0/1

0: Disable TOP00 pin output
1: Enable TOP00 pin output

Setting of output level with operation of TOP00 pin disabled
0: Low level
1: High level

0: Disable TOP01 pin output
1: Enable TOP01 pin output

Setting of output level with operation of TOP01 pin disabled
0: Low level
1: High level

Note This bit can be set to 1 only when the interrupt request signals (INTTP0CC0 and INTTP0CC1) are masked by the interrupt mask flags (TP0CCMK0 and TP0CCMK1) and timer output (TOP01) is performed at the same time. However, set the TP0CCR0 and TP0CCR1 registers to the same value (refer to **7.5.1 (2) (d) Operation of TP0CCR1 register**).

Figure 7-4. Register Setting for Interval Timer Mode Operation (2/2)

(d) TMP0 counter read buffer register (TP0CNT)

By reading the TP0CNT register, the count value of the 16-bit counter can be read.

(e) TMP0 capture/compare register 0 (TP0CCR0)

If the TP0CCR0 register is set to D_0, the interval is as follows.

Interval = $(D_0 + 1) \times$ Count clock cycle

(f) TMP0 capture/compare register 1 (TP0CCR1)

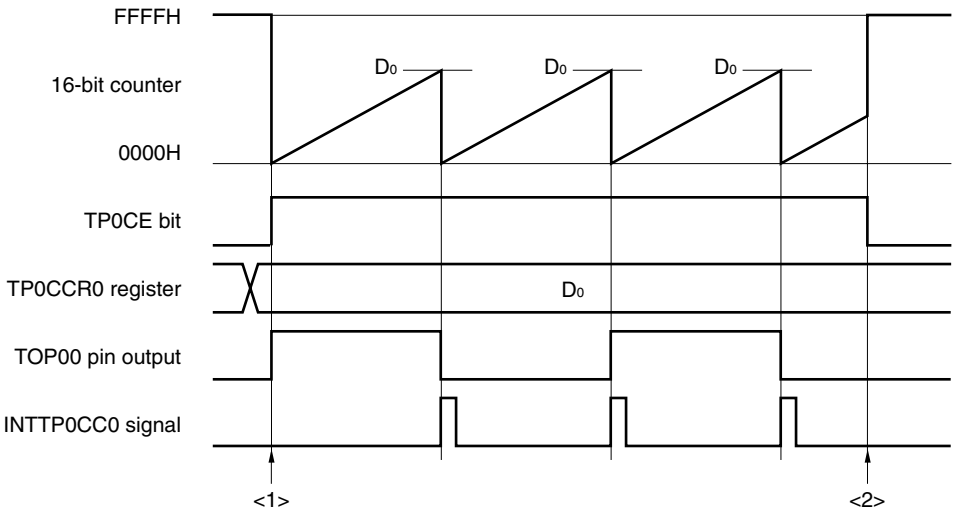
Usually, the TP0CCR1 register is not used in the interval timer mode. However, the set value of the TP0CCR1 register is transferred to the CCR1 buffer register. A compare match interrupt request signal (INTTP0CC1) is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

Therefore, mask the interrupt request by using the corresponding interrupt mask flag (TP0CCMK1).

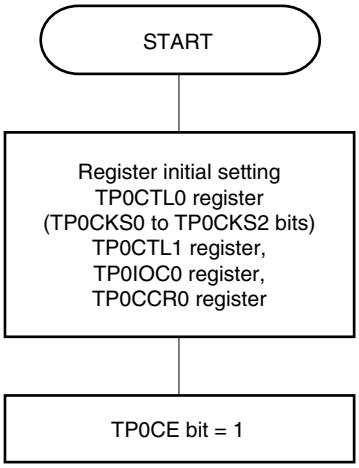
Remark TMP0 I/O control register 1 (TP0IOC1), TMP0 I/O control register 2 (TP0IOC2), and TMP0 option register 0 (TP0OPT0) are usually not used in the interval timer mode.
However, set the TP0IOC2 register to use the external event count input.

(1) Interval timer mode operation flow

Figure 7-5. Software Processing Flow in Interval Timer Mode



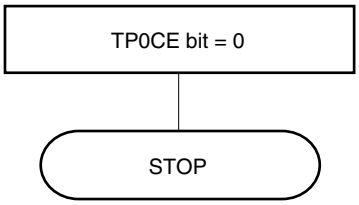
<1> Count operation start flow



Initial setting of these registers is performed before setting the TP0CE bit to 1.

The TP0CKS0 to TP0CKS2 bits can be set at the same time when counting has been started (TP0CE bit = 1).

<2> Count operation stop flow



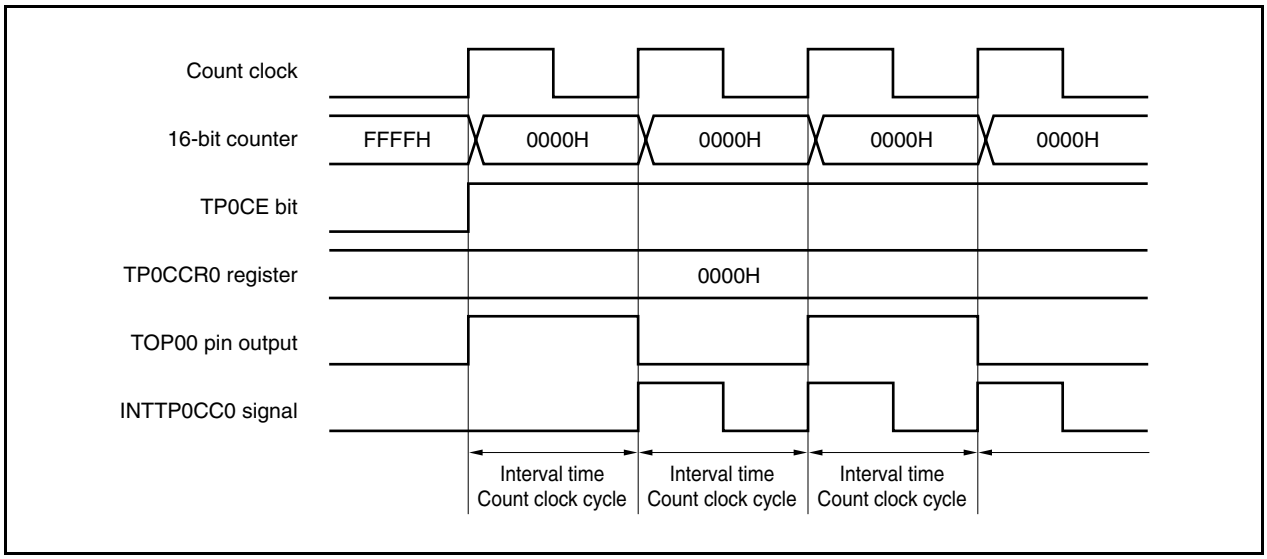
The counter is initialized and counting is stopped by clearing the TP0CE bit to 0.

(2) Interval timer mode operation timing

(a) Operation if TP0CCR0 register is cleared to 0000H

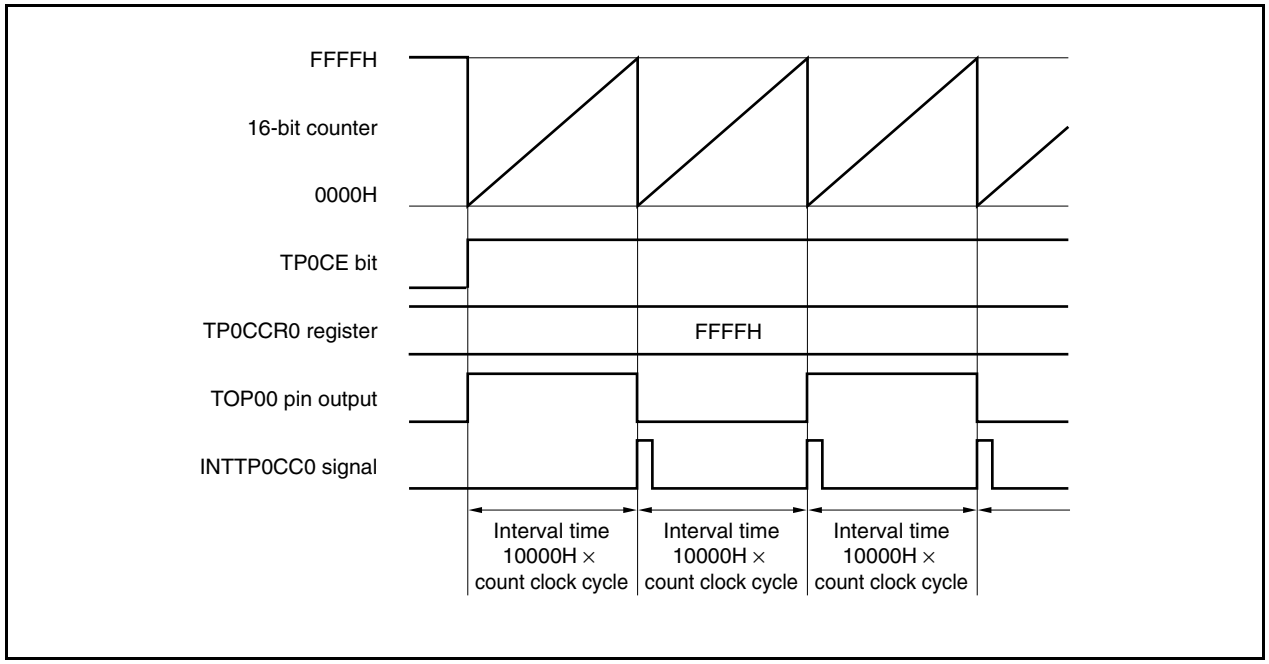
If the TP0CCR0 register is cleared to 0000H, the INTTP0CC0 signal is generated at each count clock, and the output of the TOP00 pin is inverted.

The value of the 16-bit counter is always 0000H.



(b) Operation if TP0CCR0 register is set to FFFFH

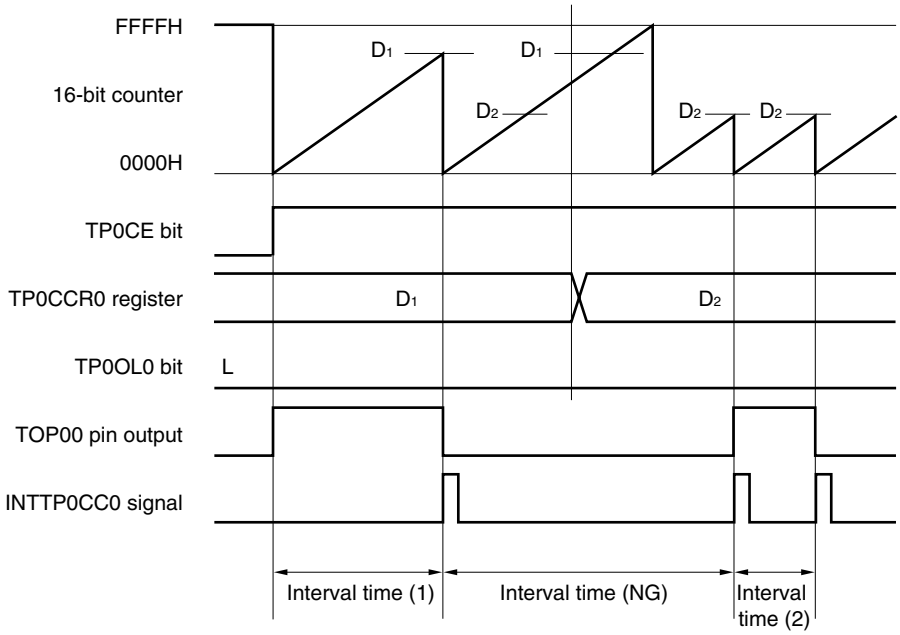
If the TP0CCR0 register is set to FFFFH, the 16-bit counter counts up to FFFFH. The counter is cleared to 0000H in synchronization with the next count-up timing. The INTTP0CC0 signal is generated and the output of the TOP00 pin is inverted. At this time, an overflow interrupt request signal (INTTP0OV) is not generated, nor is the overflow flag (TP0OPT0.TP0OVF bit) set to 1.



(c) Notes on rewriting TP0CCR0 register

To change the value of the TP0CCR0 register to a smaller value, stop counting once and then change the set value.

If the value of the TP0CCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



Remark Interval time (1): $(D_1 + 1) \times$ Count clock cycle
Interval time (NG): $(10000H + D_2 + 1) \times$ Count clock cycle
Interval time (2): $(D_2 + 1) \times$ Count clock cycle

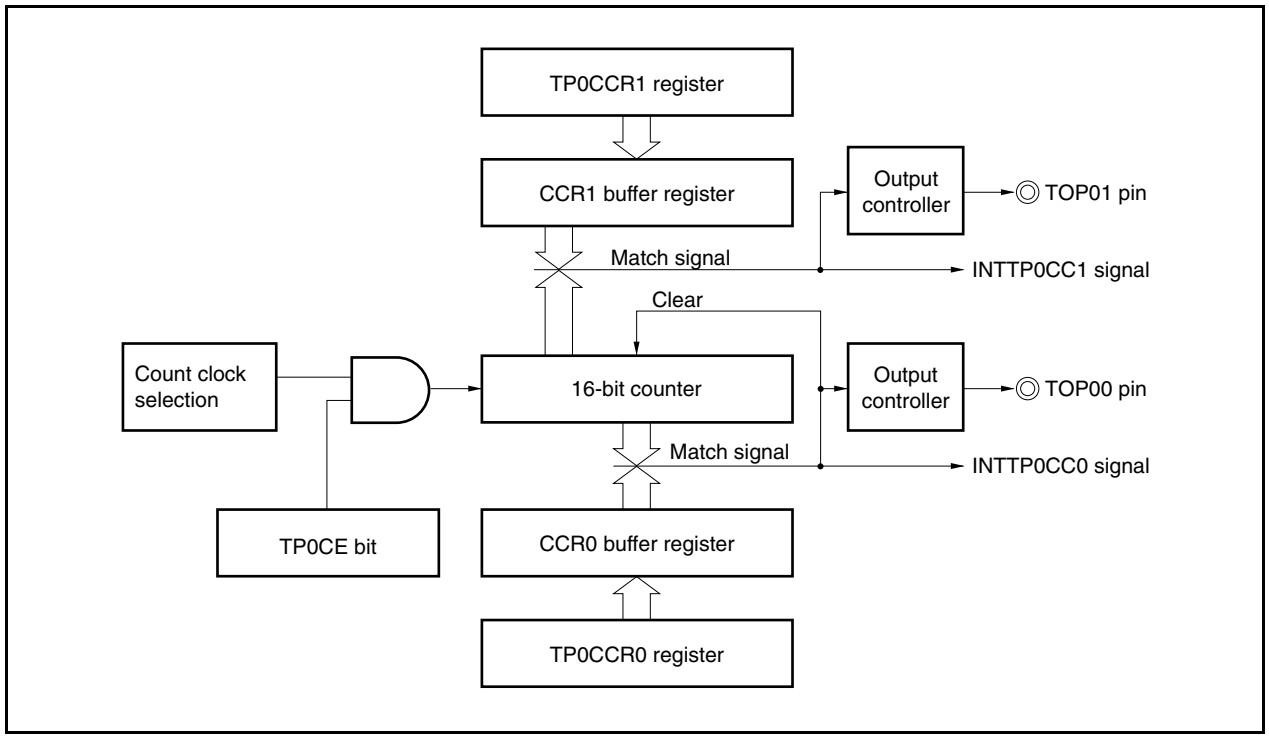
If the value of the TP0CCR0 register is changed from D_1 to D_2 while the count value is greater than D_2 but less than D_1, the count value is transferred to the CCR0 buffer register as soon as the TP0CCR0 register has been rewritten. Consequently, the value of the 16-bit counter that is compared is D_2.

Because the count value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the count value matches D_2, the INTTP0CC0 signal is generated and the output of the TOP00 pin is inverted.

Therefore, the INTTP0CC0 signal may not be generated at the interval time "$(D_1 + 1) \times$ Count clock cycle" or "$(D_2 + 1) \times$ Count clock cycle" originally expected, but may be generated at an interval of "$(10000H + D_2 + 1) \times$ Count clock period".

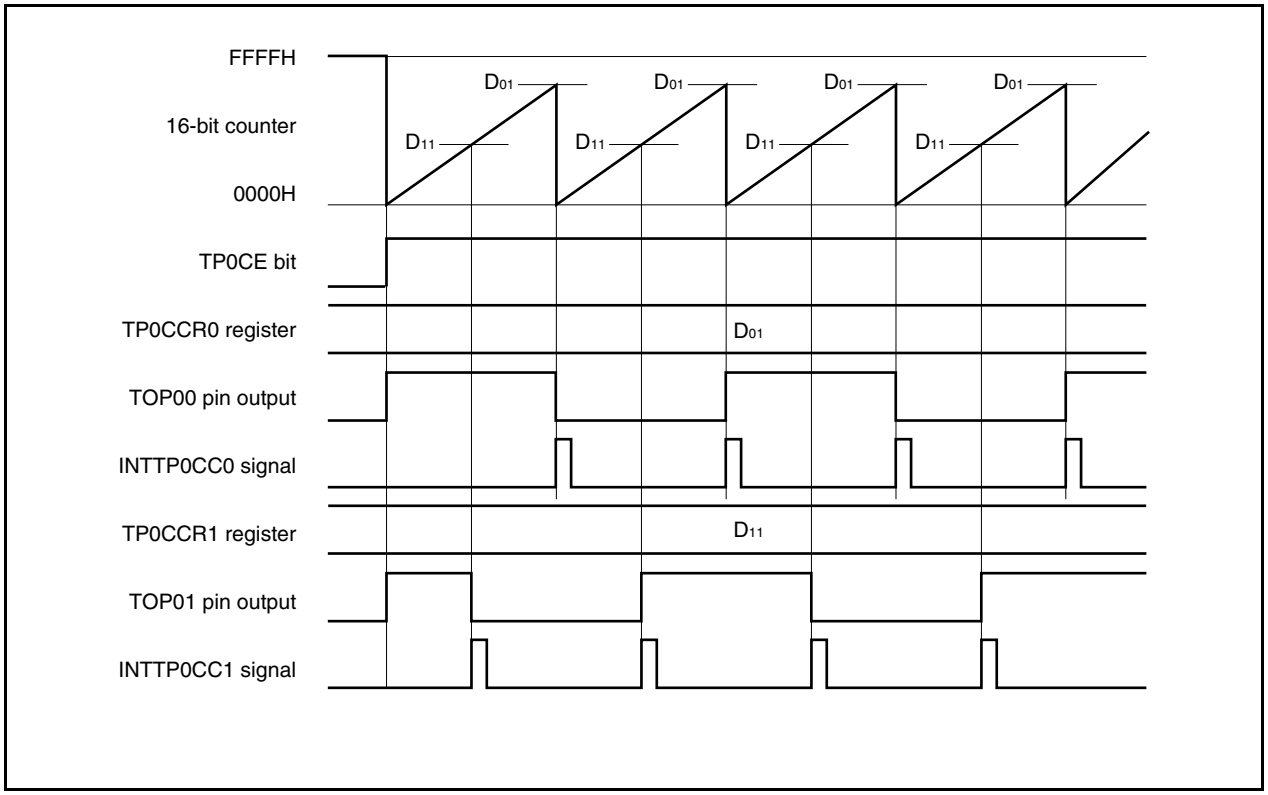
(d) Operation of TP0CCR1 register

Figure 7-6. Configuration of TP0CCR1 Register



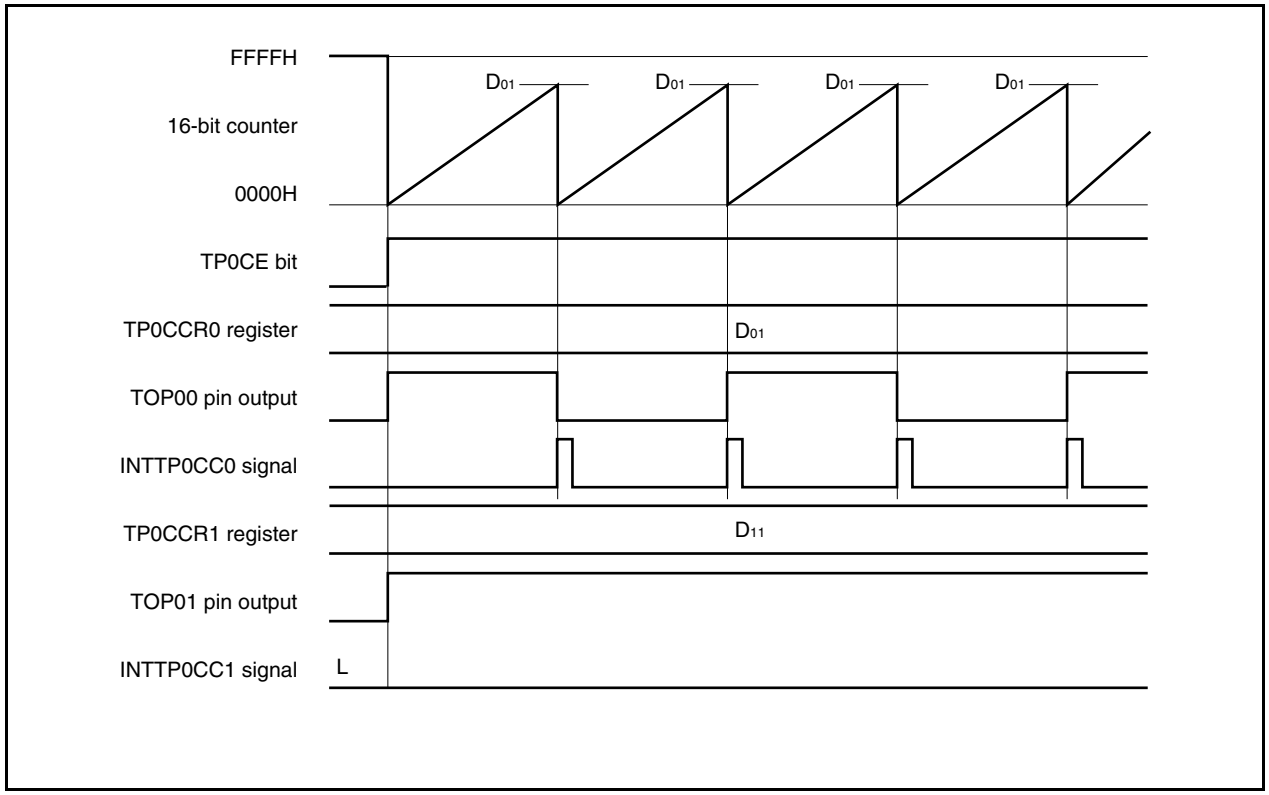
If the set value of the TP0CCR1 register is less than the set value of the TP0CCR0 register, the INTTP0CC1 signal is generated once per cycle. At the same time, the output of the TOP01 pin is inverted. The TOP01 pin outputs a square wave with the same cycle as that output by the TOP00 pin.

Figure 7-7. Timing Chart When $D_{01} \geq D_{11}$



If the set value of the TP0CCR1 register is greater than the set value of the TP0CCR0 register, the count value of the 16-bit counter does not match the value of the TP0CCR1 register. Consequently, the INTTP0CC1 signal is not generated, nor is the output of the TOP01 pin changed.

Figure 7-8. Timing Chart When $D_{01} < D_{11}$



7.5.2 External event count mode (TP0MD2 to TP0MD0 bits = 001)

In the external event count mode, the valid edge of the external event count input is counted when the TP0CTL0.TP0CE bit is set to 1, and an interrupt request signal (INTTP0CC0) is generated each time the specified number of edges have been counted. The timer output (TOP00, TOP01 pins) cannot be used.

Usually, the TP0CCR1 register is not used in the external event count mode.

Figure 7-9. Configuration in External Event Count Mode

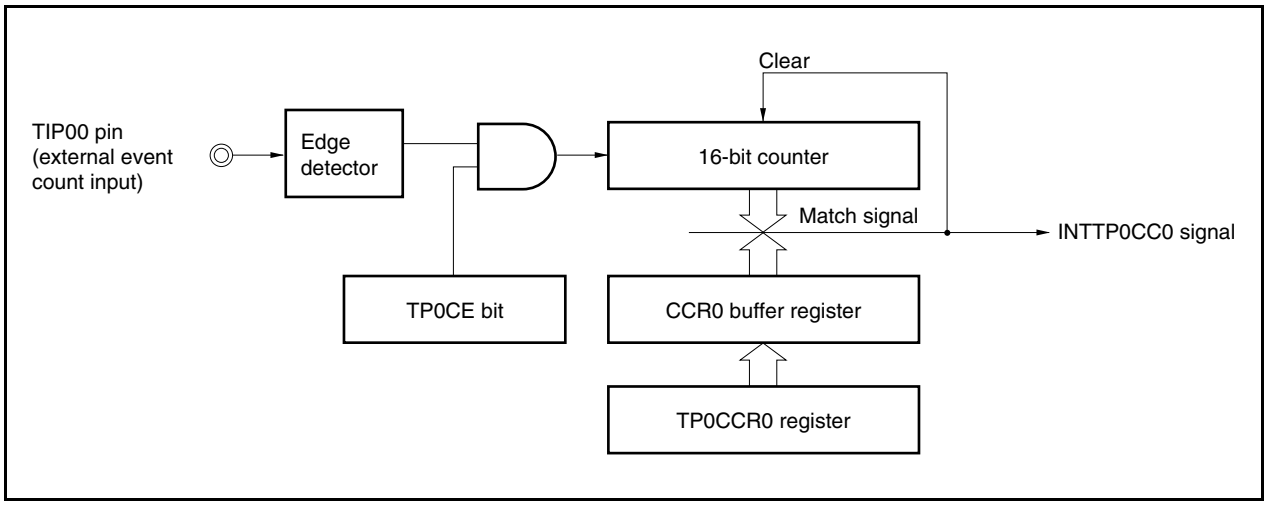
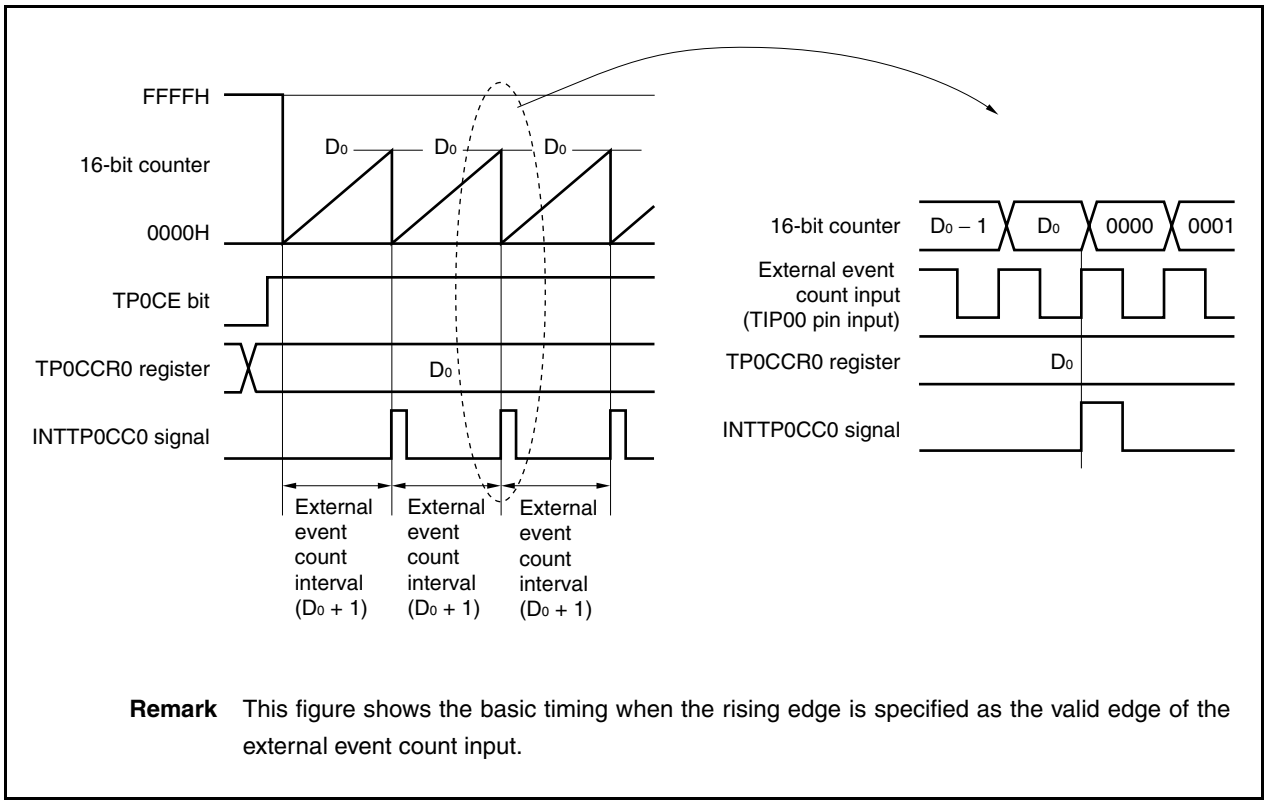


Figure 7-10. Basic Timing in External Event Count Mode



Remark This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.

When the TP0CE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H. The counter counts each time the valid edge of external event count input is detected. Additionally, the set value of the TP0CCR0 register is transferred to the CCR0 buffer register.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, and a compare match interrupt request signal (INTTP0CC0) is generated.

The INTTP0CC0 signal is generated each time the valid edge of the external event count input has been detected (set value of TP0CCR0 register + 1) times.

Figure 7-11. Register Setting for Operation in External Event Count Mode (1/2)

(a) TMP0 control register 0 (TP0CTL0)

	TP0CE					TP0CKS2	TP0CKS1	TP0CKS0
TP0CTL0	0/1	0	0	0	0	0	0	0

0: Stop counting
1: Enable counting

(b) TMP0 control register 1 (TP0CTL1)

		TP0EST	TP0EEE			TP0MD2	TP0MD1	TP0MD0
TP0CTL1	0	0	0	0	0	0	0	1

0, 0, 1:
External event count mode

(c) TMP0 I/O control register 0 (TP0IOC0)

					TP0OL1	TP0OE1	TP0OL0	TP0OE0
TP0IOC0	0	0	0	0	0	0	0	0

0: Disable TOP00 pin output
0: Disable TOP01 pin output

(d) TMP0 I/O control register 2 (TP0IOC2)

					TP0EES1	TP0EES0	TP0ETS1	TP0ETS0
TP0IOC2	0	0	0	0	0/1	0/1	0	0

Select valid edge
of external event
count input

Figure 7-11. Register Setting for Operation in External Event Count Mode (2/2)

(e) TMP0 counter read buffer register (TP0CNT)

The count value of the 16-bit counter can be read by reading the TP0CNT register.

(f) TMP0 capture/compare register 0 (TP0CCR0)

If D_0 is set to the TP0CCR0 register, the counter is cleared and a compare match interrupt request signal (INTTP0CC0) is generated when the number of external event counts reaches (D_0 + 1).

(g) TMP0 capture/compare register 1 (TP0CCR1)

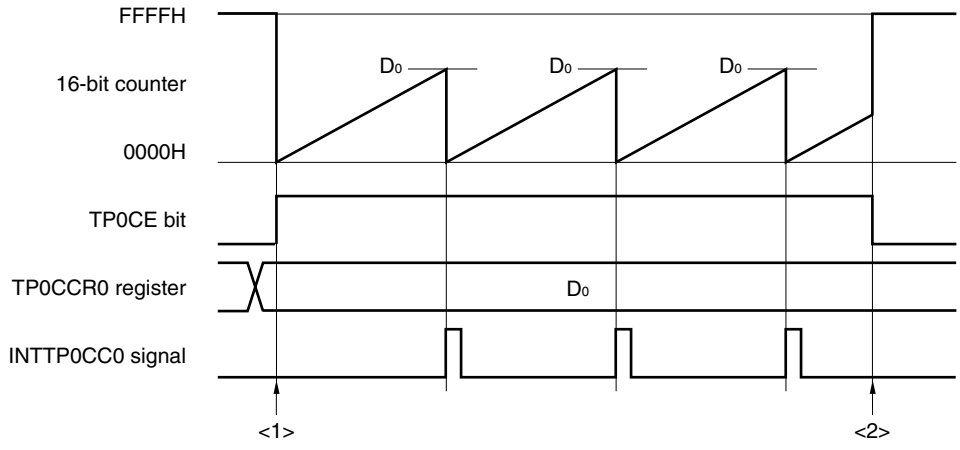
Usually, the TP0CCR1 register is not used in the external event count mode. However, the set value of the TP0CCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTP0CC1) is generated.

Therefore, mask the interrupt signal by using the interrupt mask flag (TP0CCMK1).

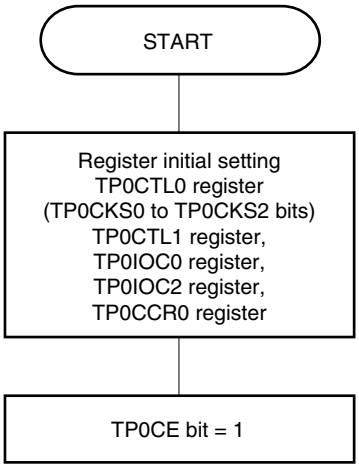
Remark TMP0 I/O control register 1 (TP0IOC1) and TMP0 option register 0 (TP0OPT0) are not used in the external event count mode.

(1) External event count mode operation flow

Figure 7-12. Flow of Software Processing in External Event Count Mode



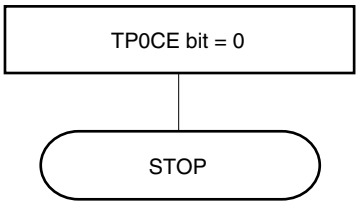
<1> Count operation start flow



Initial setting of these registers is performed before setting the TP0CE bit to 1.

The TP0CKS0 to TP0CKS2 bits can be set at the same time when counting has been started (TP0CE bit = 1).

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TP0CE bit to 0.

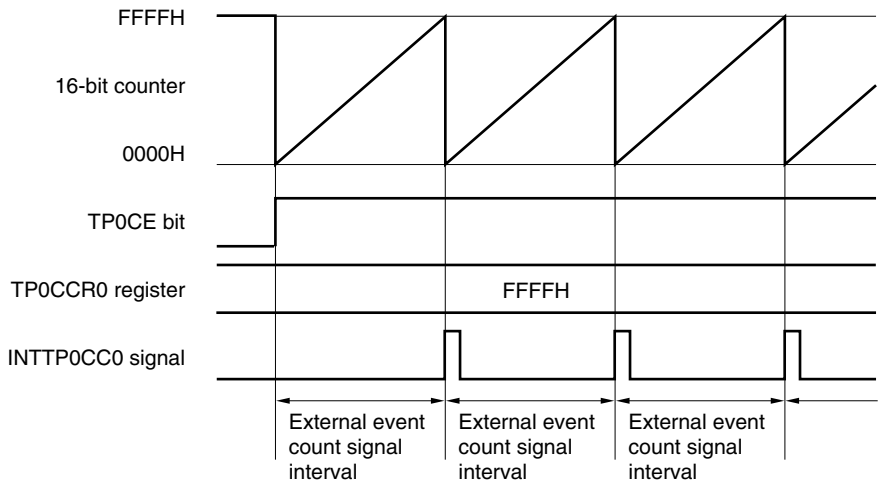
(2) Operation timing in external event count mode

Cautions 1. In the external event count mode, do not set the TP0CCR0 and TP0CCR1 registers to 0000H.

2. In the external event count mode, use of the timer output is disabled. If performing timer output using external event count input, set the interval timer mode, and select the operation enabled by the external event count input for the count clock (TP0CTL1.TP0MD2 to TP0CTL1.TP0MD0 bits = 000, TP0CTL1.TP0EEE bit = 1).

(a) Operation if TP0CCR0 register is set to FFFFH

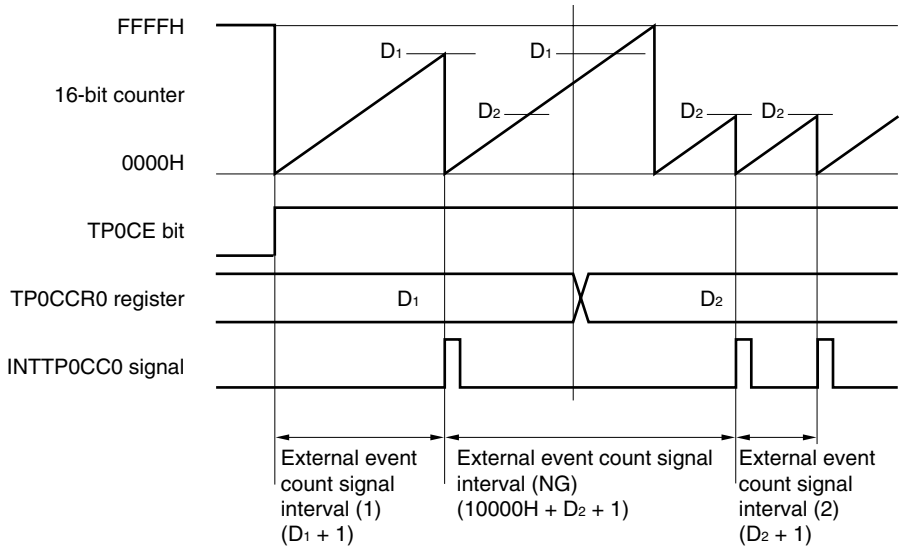
If the TP0CCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTP0CC0 signal is generated. At this time, the TP0OPT0.TP0OVF bit is not set.



(b) Notes on rewriting the TP0CCR0 register

To change the value of the TP0CCR0 register to a smaller value, stop counting once and then change the set value.

If the value of the TP0CCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



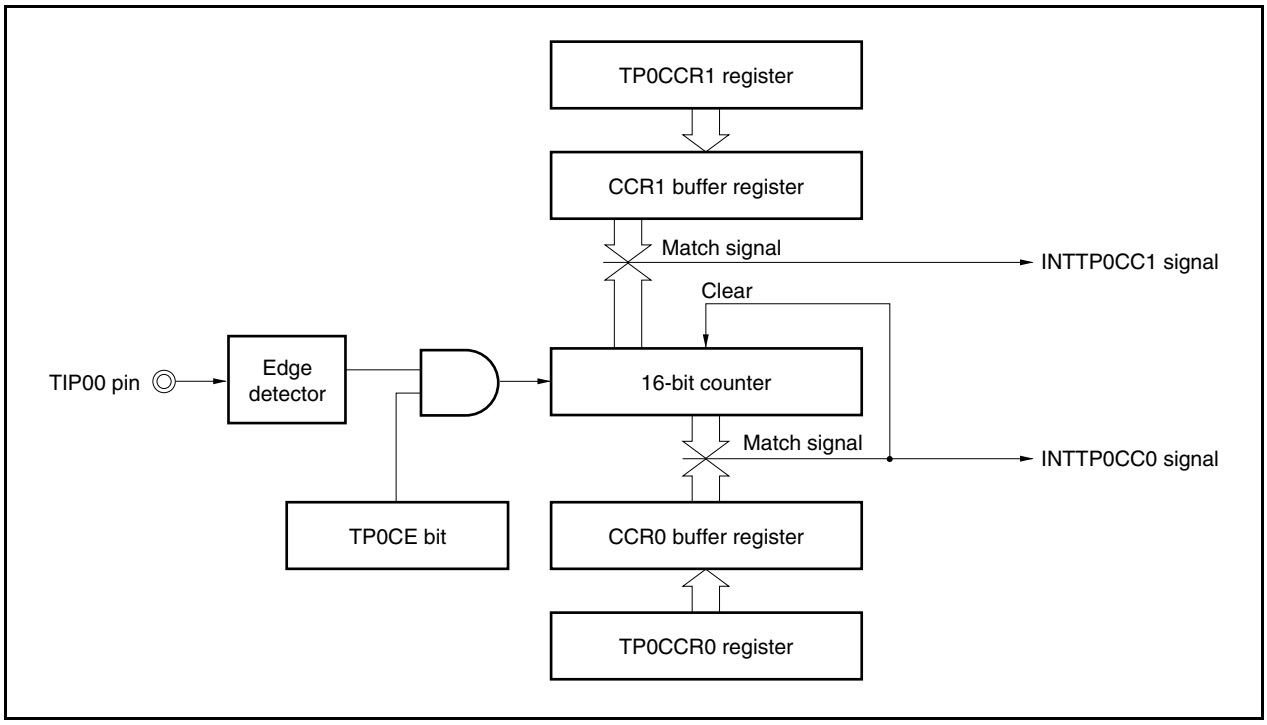
If the value of the TP0CCR0 register is changed from D_1 to D_2 while the count value is greater than D_2 but less than D_1, the count value is transferred to the CCR0 buffer register as soon as the TP0CCR0 register has been rewritten. Consequently, the value that is compared with the 16-bit counter is D_2.

Because the count value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the count value matches D_2, the INTTP0CC0 signal is generated.

Therefore, the INTTP0CC0 signal may not be generated at the valid edge count of "(D_1 + 1) times" or "(D_2 + 1) times" originally expected, but may be generated at the valid edge count of "(10000H + D_2 + 1) times".

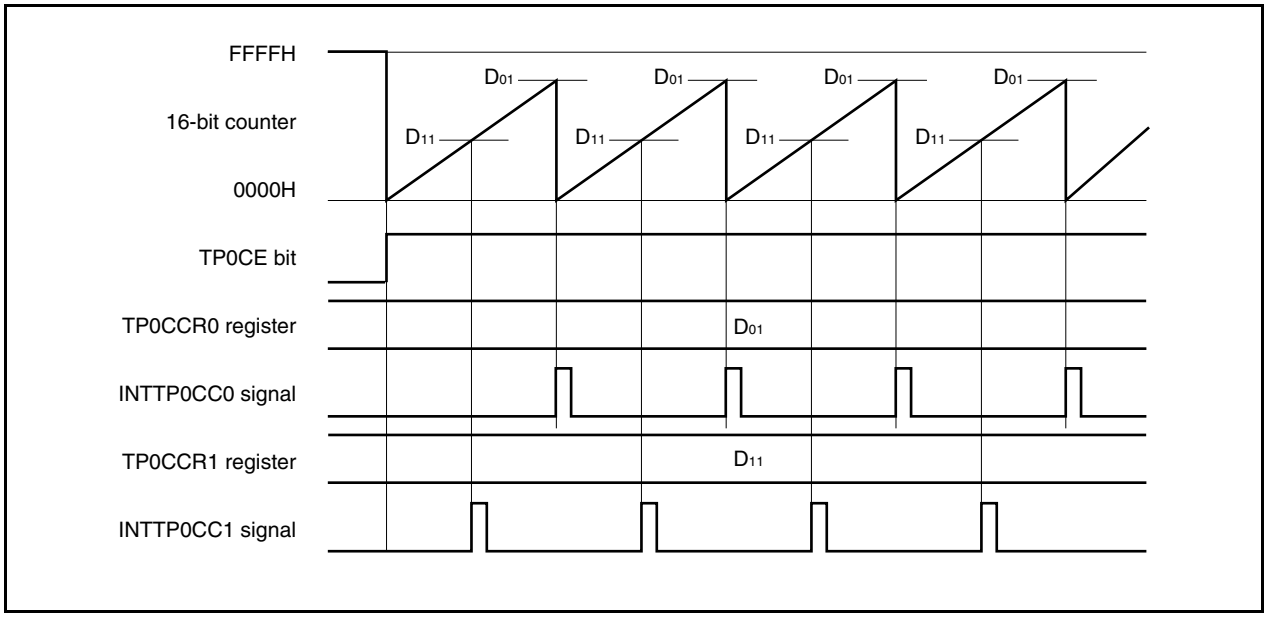
(c) Operation of TP0CCR1 register

Figure 7-13. Configuration of TP0CCR1 Register



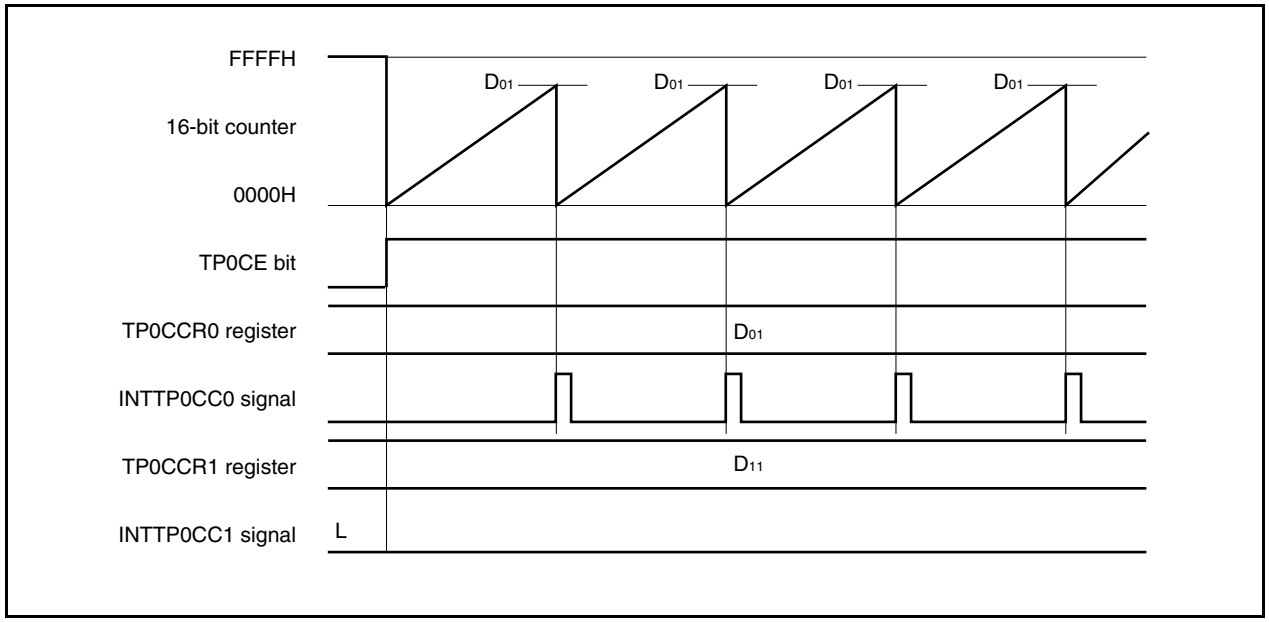
If the set value of the TP0CCR1 register is smaller than the set value of the TP0CCR0 register, the INTTP0CC1 signal is generated once per cycle.

Figure 7-14. Timing Chart When $D_{01} \geq D_{11}$



If the set value of the TP0CCR1 register is greater than the set value of the TP0CCR0 register, the INTTP0CC1 signal is not generated because the count value of the 16-bit counter and the value of the TP0CCR1 register do not match.

Figure 7-15. Timing Chart When $D_{01} < D_{11}$



7.5.3 External trigger pulse output mode (TP0MD2 to TP0MD0 bits = 010)

In the external trigger pulse output mode, 16-bit timer/event counter P waits for a trigger when the TP0CTL0.TP0CE bit is set to 1. When the valid edge of an external trigger input signal is detected, 16-bit timer/event counter P starts counting, and outputs a PWM waveform from the TOP01 pin.

Pulses can also be output by generating a software trigger instead of using the external trigger. When using a software trigger, a square wave that has one cycle of the PWM waveform as half its cycle can also be output from the TOP00 pin.

Figure 7-16. Configuration in External Trigger Pulse Output Mode

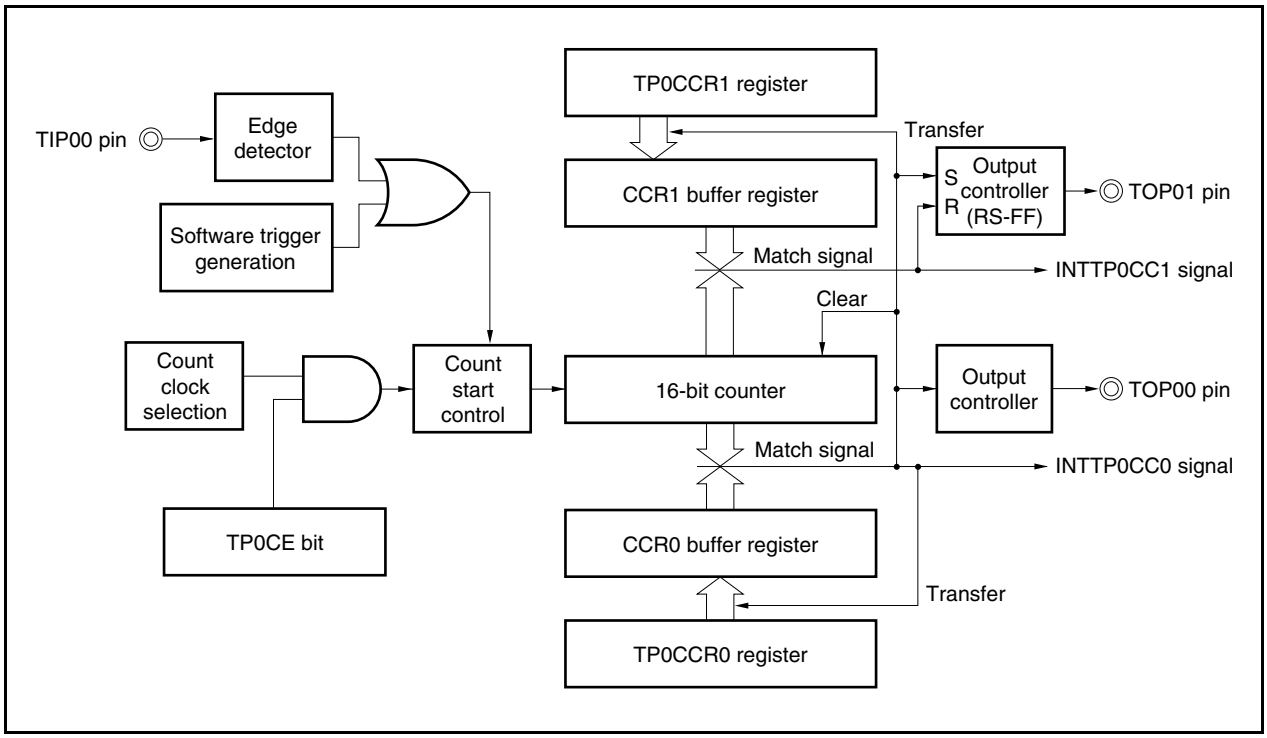
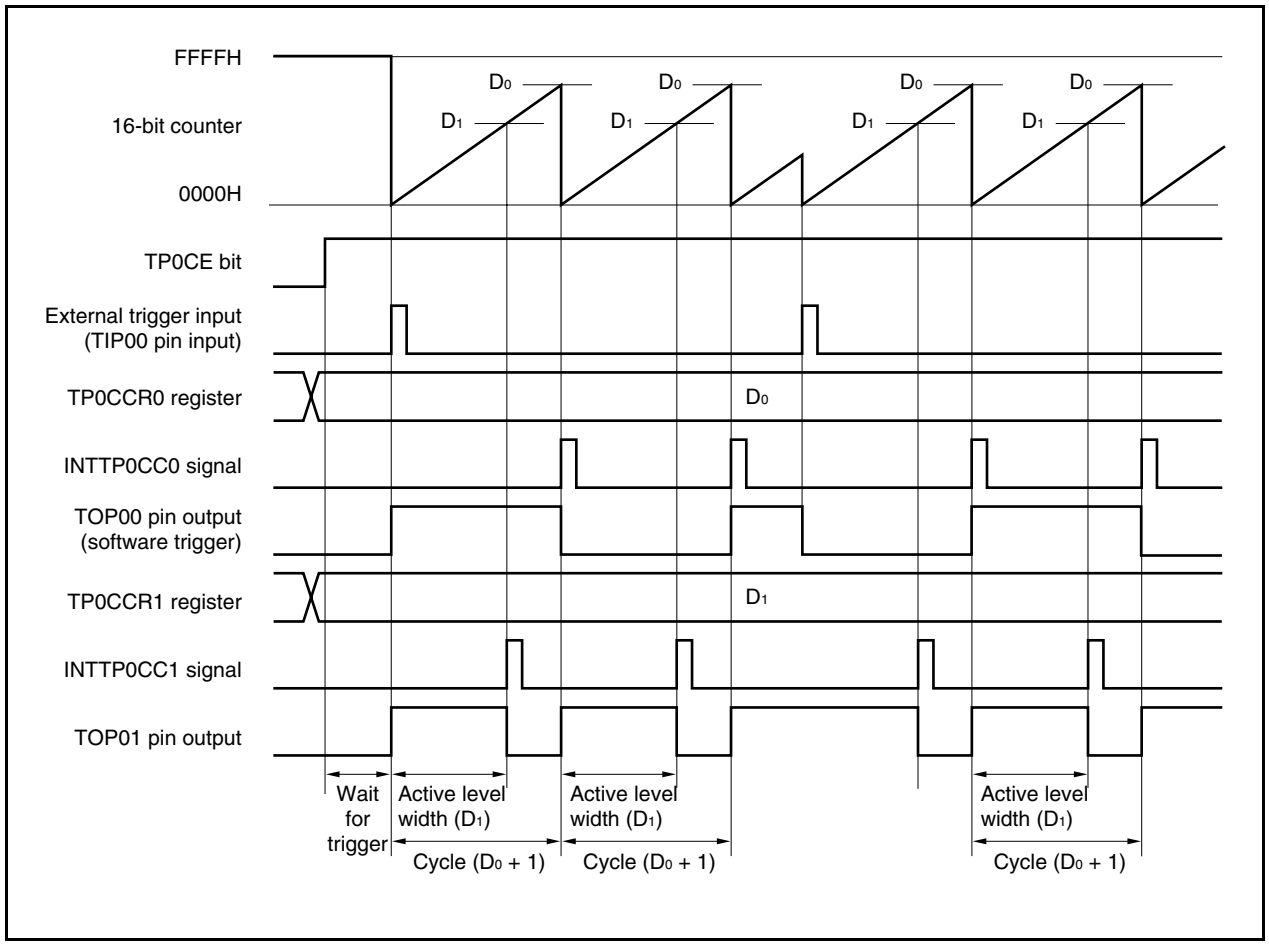


Figure 7-17. Basic Timing in External Trigger Pulse Output Mode



16-bit timer/event counter P waits for a trigger when the TP0CE bit is set to 1. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting at the same time, and outputs a PWM waveform from the TOP01 pin. If the trigger is generated again while the counter is operating, the counter is cleared to 0000H and restarted. (The output of the TOP00 pin is inverted. The TOP01 pin outputs a high level regardless of the status (high/low) when a trigger occurs.)

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TP0CCR1 register) × Count clock cycle
Cycle = (Set value of TP0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)

The compare match interrupt request signal INTTP0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTP0CC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

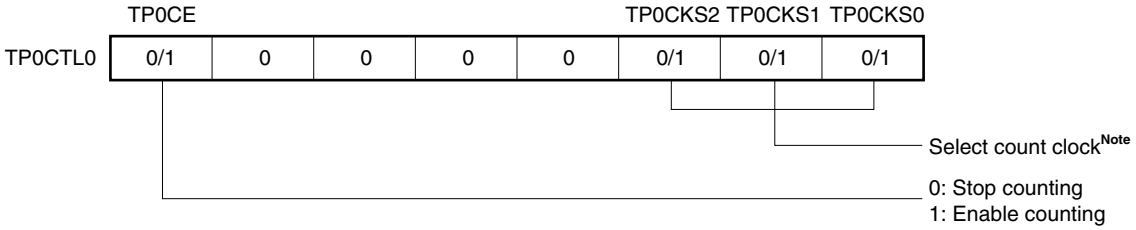
The value set to the TP0CCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

The valid edge of an external trigger input signal, or setting the software trigger (TP0CTL1.TP0EST bit) to 1 is used as the trigger.

Remark a = 0, 1

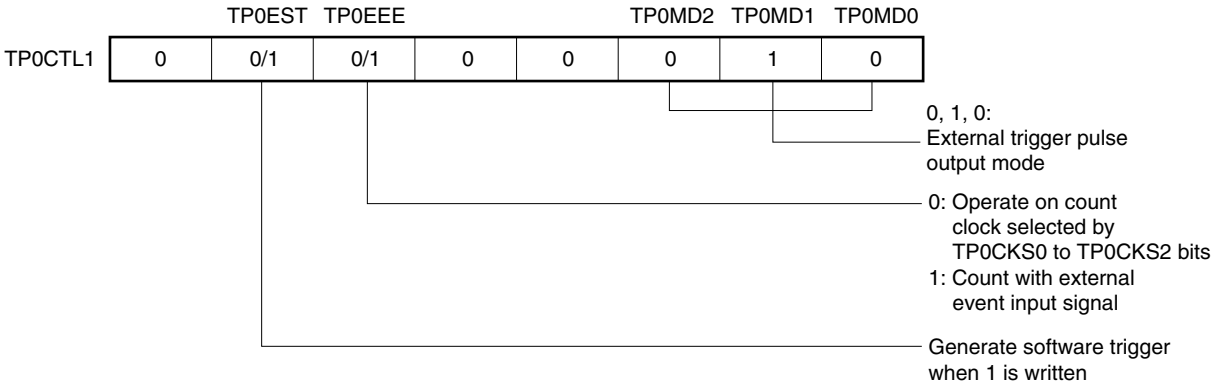
Figure 7-18. Setting of Registers in External Trigger Pulse Output Mode (1/2)

(a) TMP0 control register 0 (TP0CTL0)

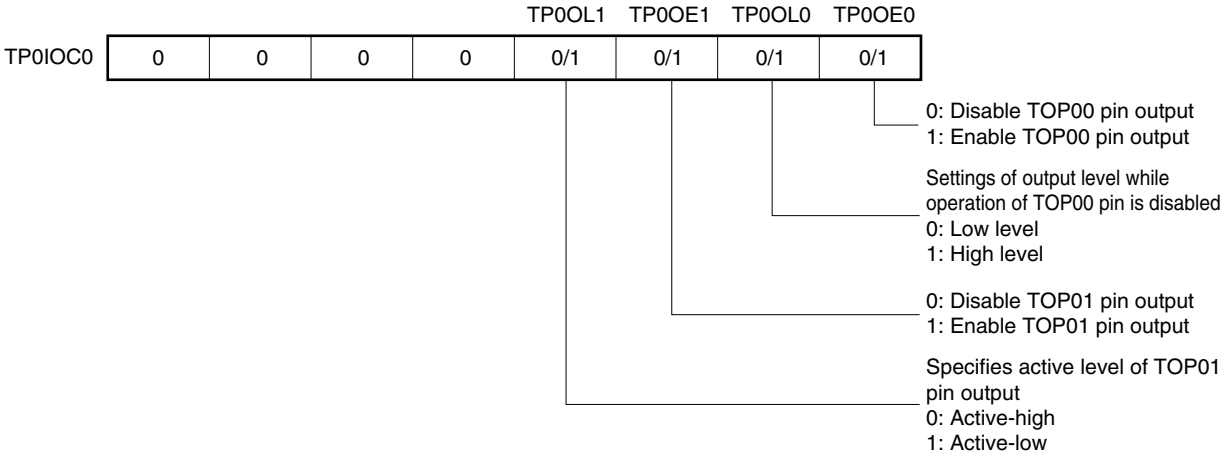


Note The setting is invalid when the TP0CTL1.TP0EEE bit = 1.

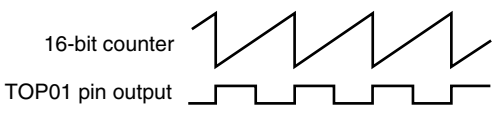
(b) TMP0 control register 1 (TP0CTL1)



(c) TMP0 I/O control register 0 (TP0IOC0)



- When TP0OL1 bit = 0



- When TP0OL1 bit = 1

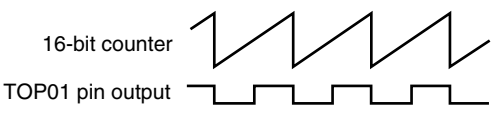
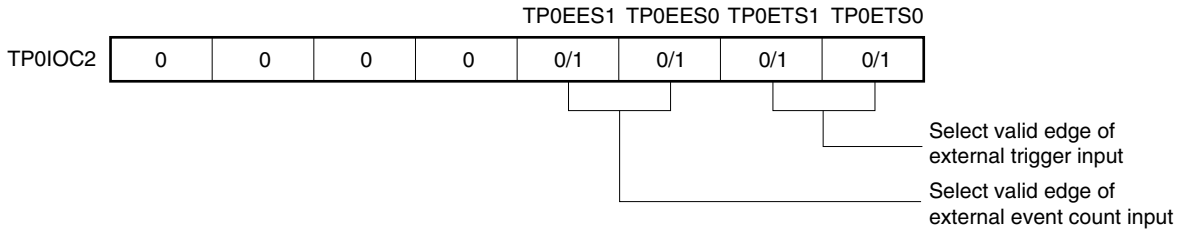


Figure 7-18. Setting of Registers in External Trigger Pulse Output Mode (2/2)

(d) TMP0 I/O control register 2 (TP0IOC2)



(e) TMP0 counter read buffer register (TP0CNT)

The value of the 16-bit counter can be read by reading the TP0CNT register.

(f) TMP0 capture/compare registers 0 and 1 (TP0CCR0 and TP0CCR1)

If D_0 is set to the TP0CCR0 register and D_1 to the TP0CCR1 register, the cycle and active level of the PWM waveform are as follows.

Cycle = $(D_0 + 1) \times$ Count clock cycle
Active level width = $D_1 \times$ Count clock cycle

Remark TMP0 I/O control register 1 (TP0IOC1) and TMP0 option register 0 (TP0OPT0) are not used in the external trigger pulse output mode.

(1) Operation flow in external trigger pulse output mode

Figure 7-19. Software Processing Flow in External Trigger Pulse Output Mode (1/2)

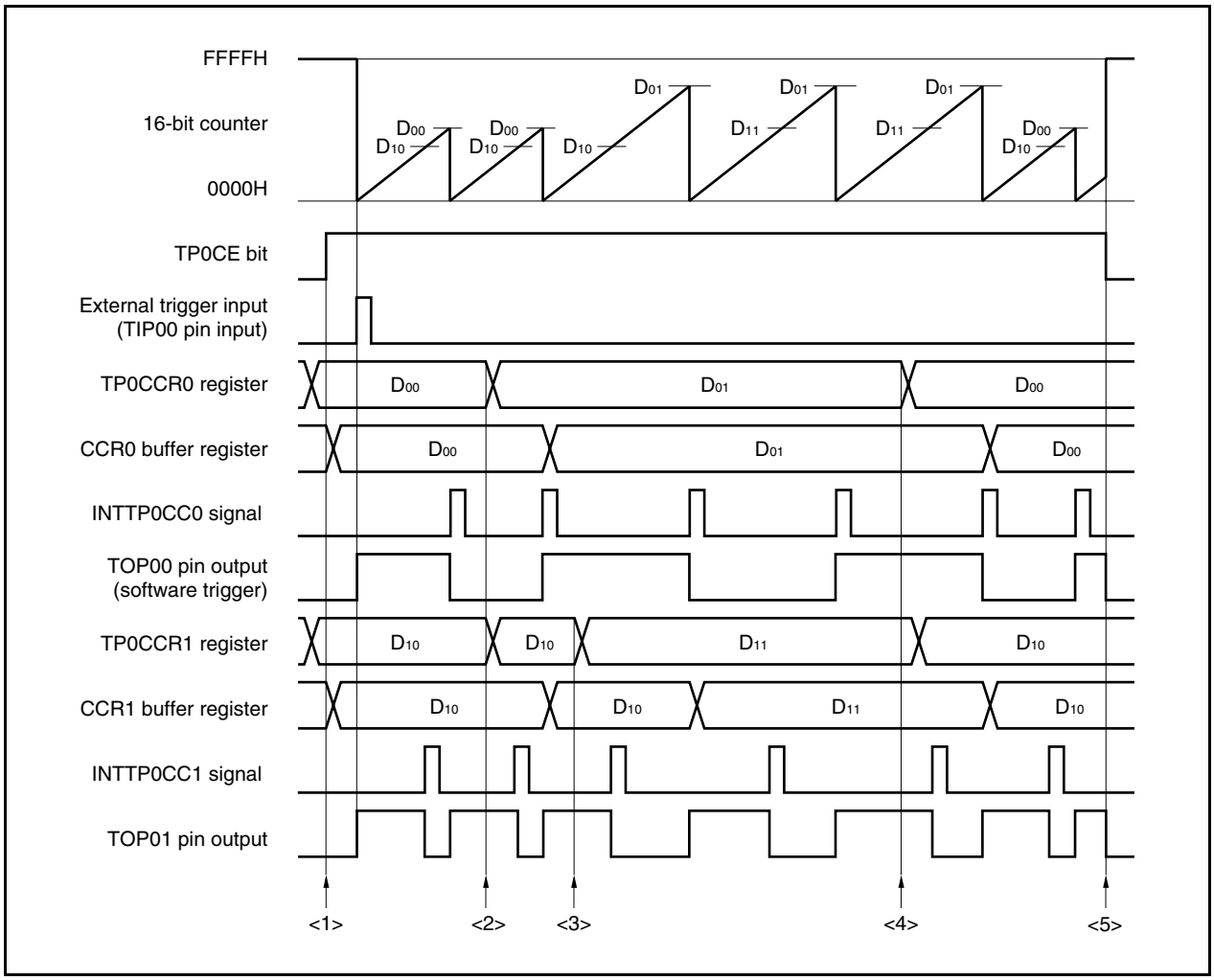
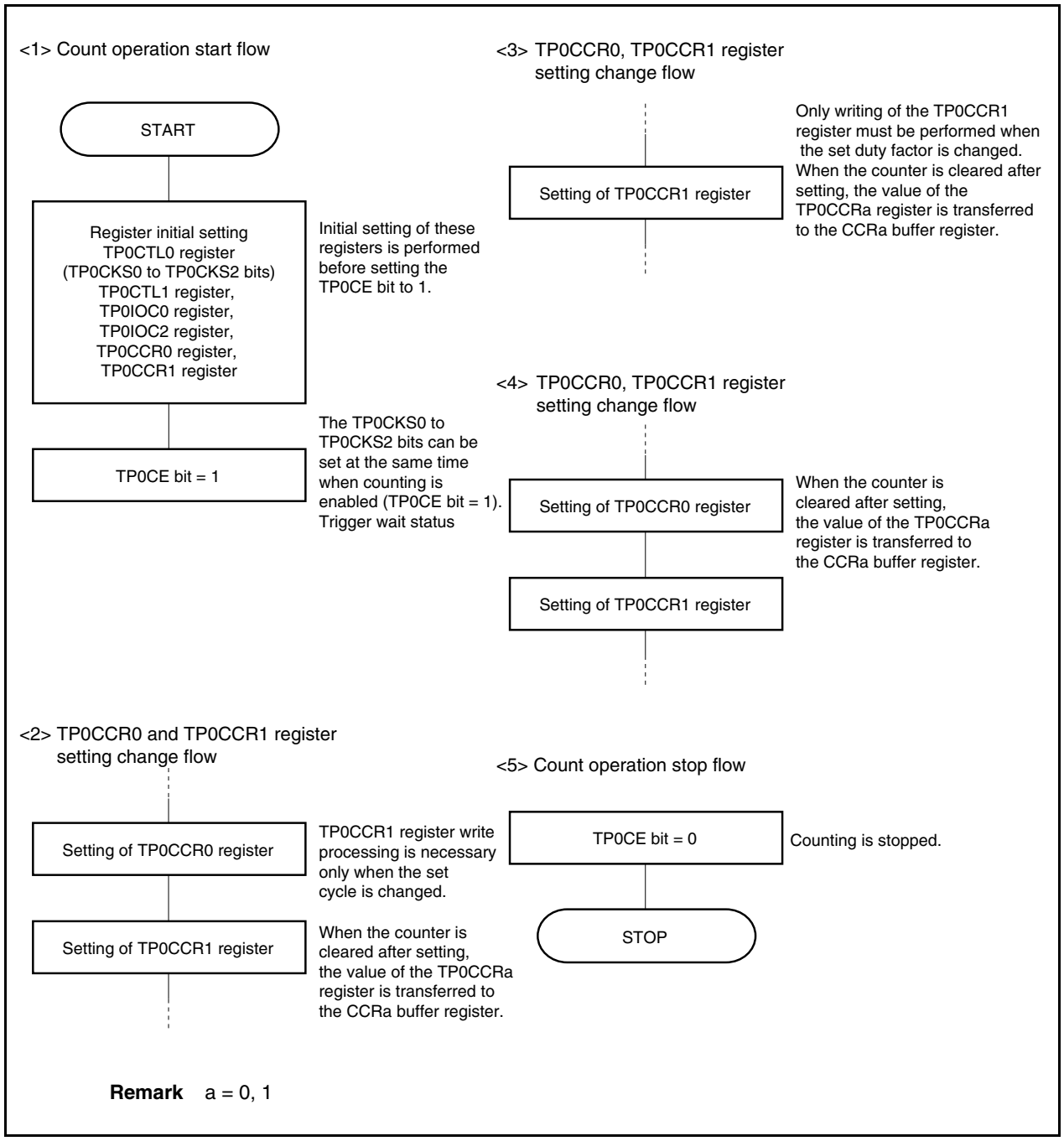


Figure 7-19. Software Processing Flow in External Trigger Pulse Output Mode (2/2)



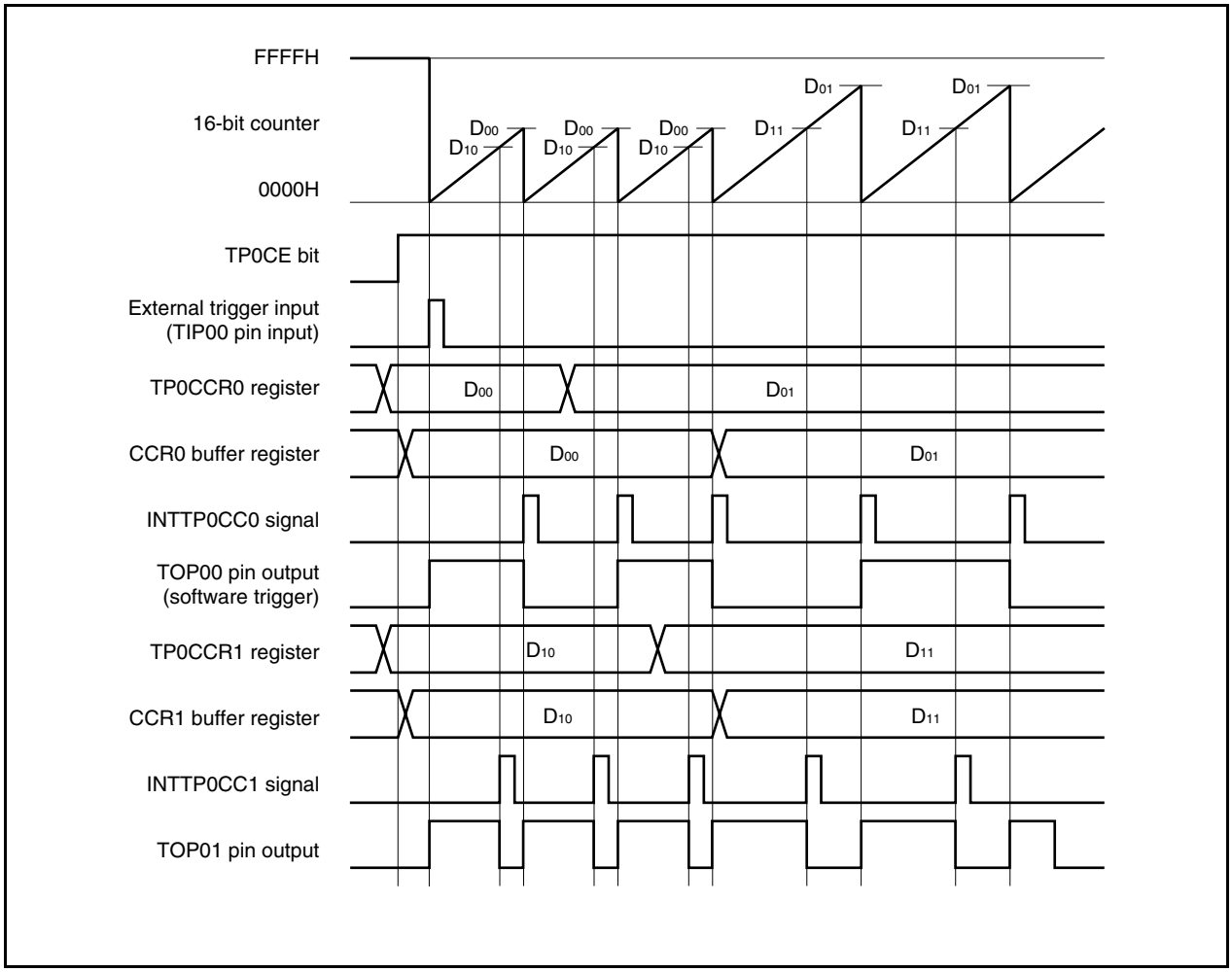
Remark a = 0, 1

(2) External trigger pulse output mode operation timing

(a) Note on changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TP0CCR1 register last.

Rewrite the TP0CCRa register after writing the TP0CCR1 register after the INTTP0CC0 signal is detected.



In order to transfer data from the TP0CCRa register to the CCRa buffer register, the TP0CCR1 register must be written.

To change both the cycle and active level width of the PWM waveform at this time, first set the cycle to the TP0CCR0 register and then set the active level width to the TP0CCR1 register.

To change only the cycle of the PWM waveform, first set the cycle to the TP0CCR0 register, and then write the same value to the TP0CCR1 register.

To change only the active level width (duty factor) of the PWM waveform, only the TP0CCR1 register has to be set.

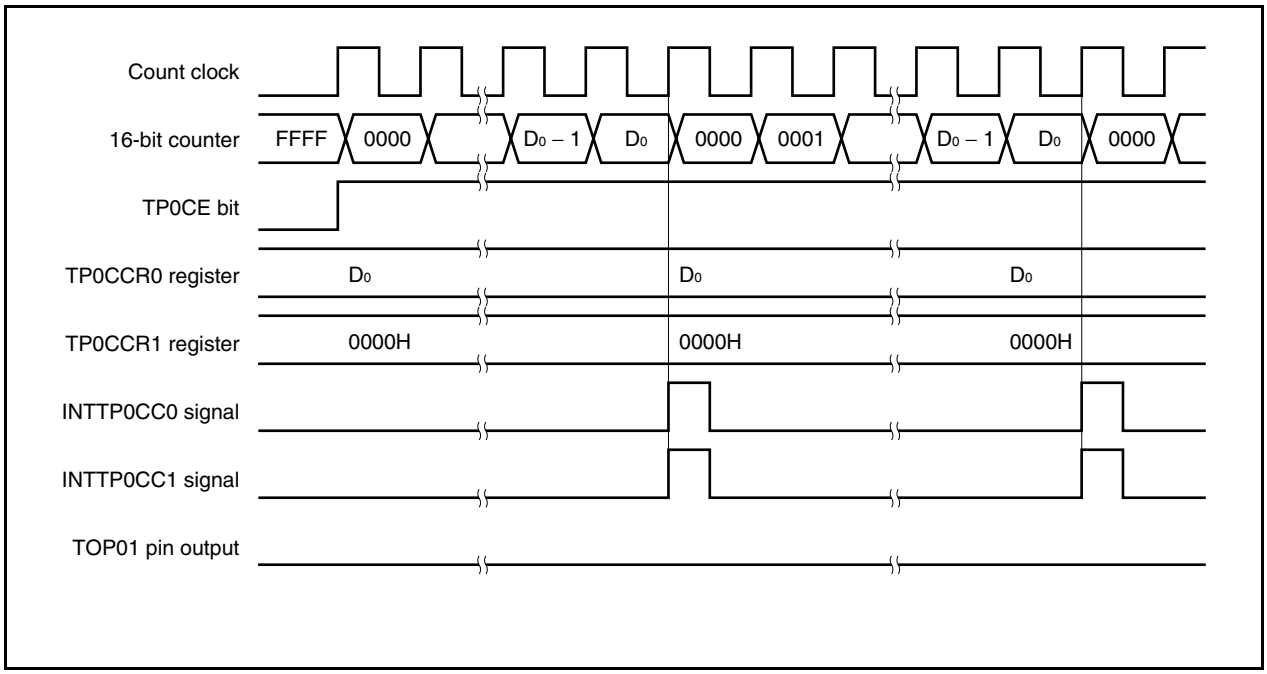
After data is written to the TP0CCR1 register, the value written to the TP0CCRa register is transferred to the CCRa buffer register in synchronization with clearing of the 16-bit counter, and is used as the value compared with the 16-bit counter.

To write the TP0CCR0 or TP0CCR1 register again after writing the TP0CCR1 register once, do so after the INTTP0CC0 signal is generated. Otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TP0CCRa register to the CCRa buffer register conflicts with writing the TP0CCRa register.

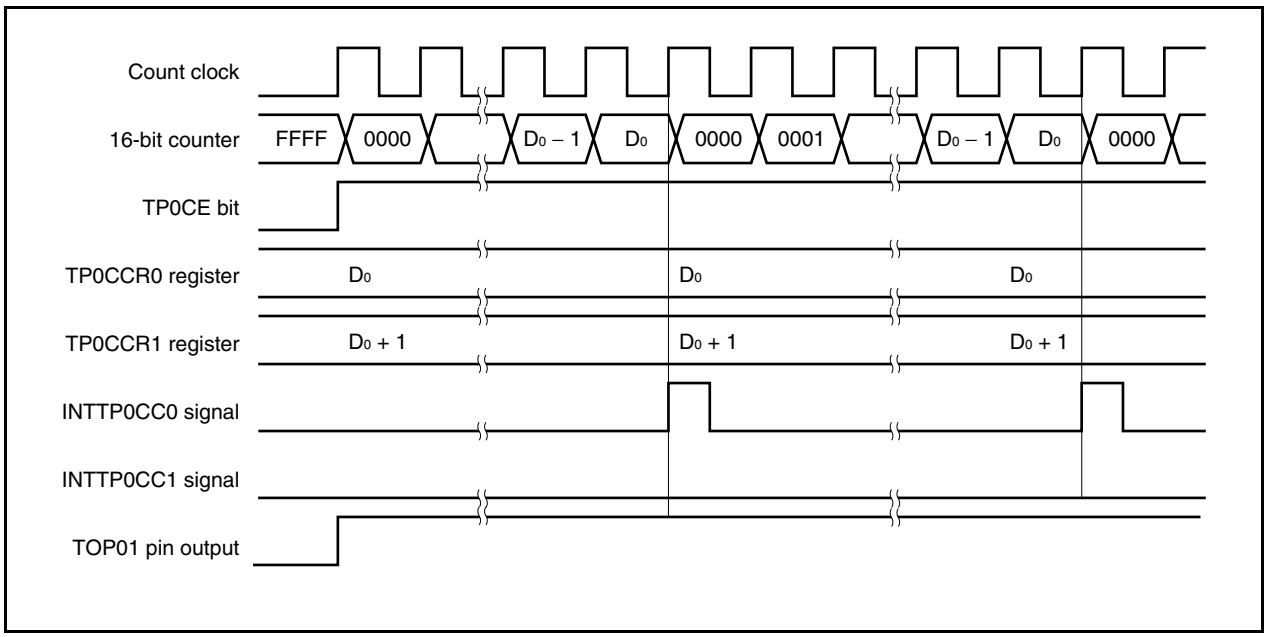
Remark a = 0, 1

(b) 0%/100% output of PWM waveform

To output a 0% waveform, clear the TP0CCR1 register to 0000H. If the set value of the TP0CCR0 register is FFFFH, the INTTP0CC1 signal is generated periodically.

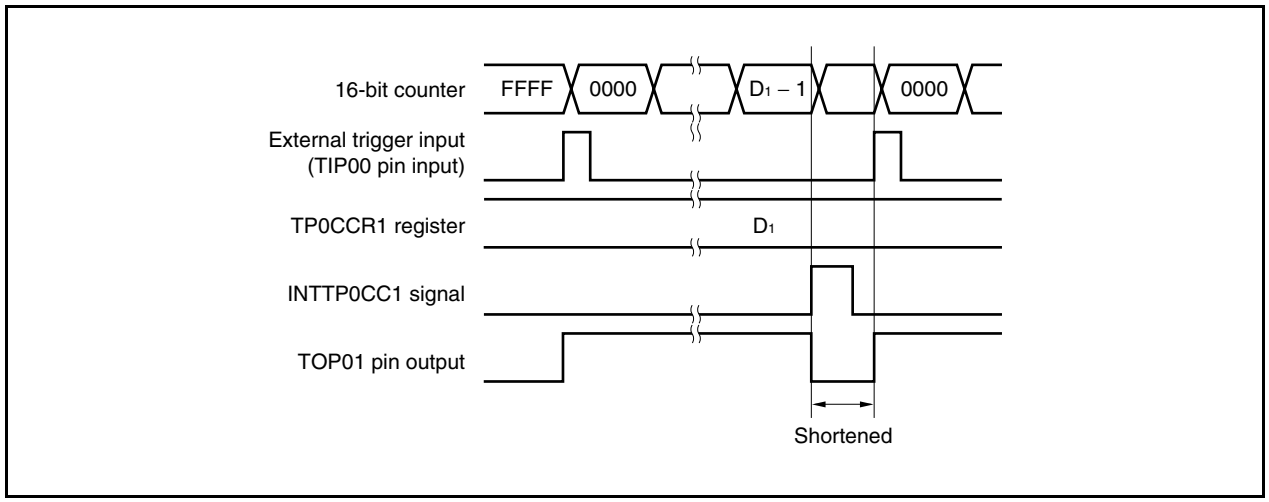


To output a 100% waveform, set a value of (set value of TP0CCR0 register + 1) to the TP0CCR1 register. If the set value of the TP0CCR0 register is FFFFH, 100% output cannot be produced.

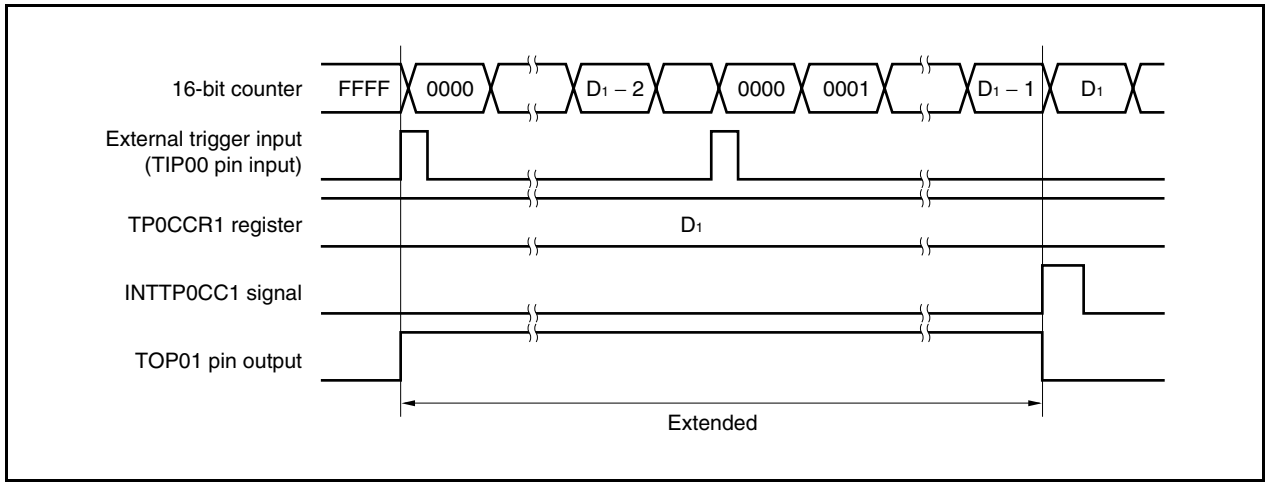


(c) Conflict between trigger detection and match with TP0CCR1 register

If the trigger is detected immediately after the INTTP0CC1 signal is generated, the 16-bit counter is immediately cleared to 0000H, the output signal of the TOP01 pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.

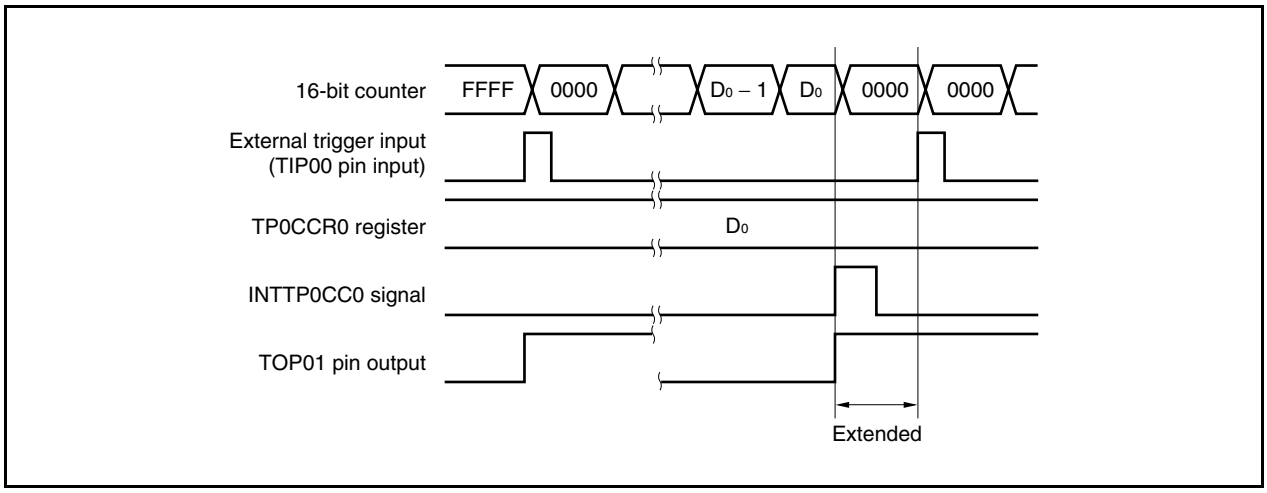


If the trigger is detected immediately before the INTTP0CC1 signal is generated, the INTTP0CC1 signal is not generated, and the 16-bit counter is cleared to 0000H and continues counting. The output signal of the TOP01 pin remains active. Consequently, the active period of the PWM waveform is extended.

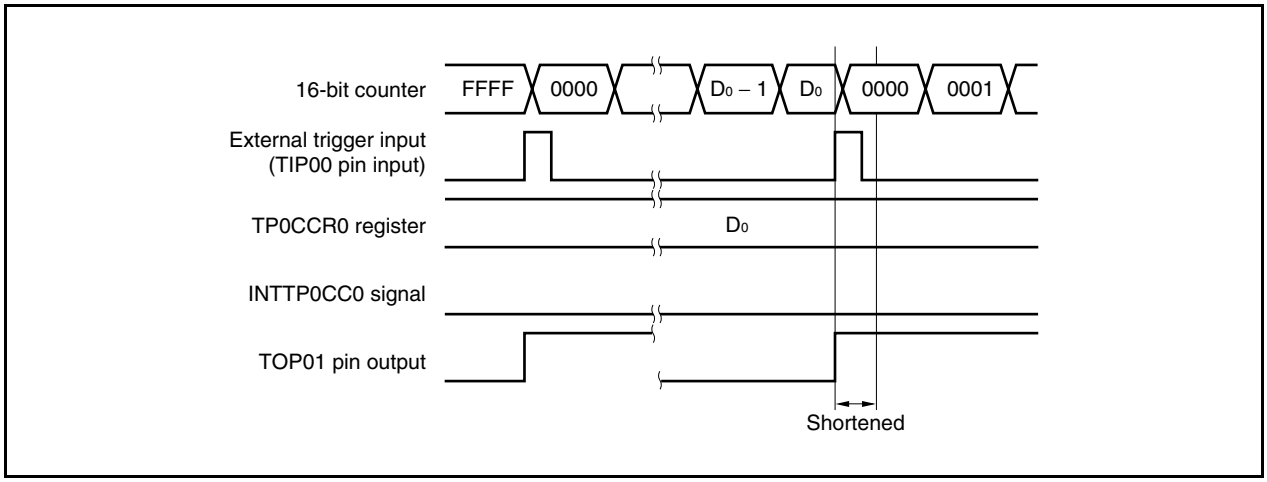


(d) Conflict between trigger detection and match with TP0CCR0 register

If the trigger is detected immediately after the INTTP0CC0 signal is generated, the 16-bit counter is cleared to 0000H and continues counting up. Therefore, the active period of the TOP01 pin is extended by time from generation of the INTTP0CC0 signal to trigger detection.

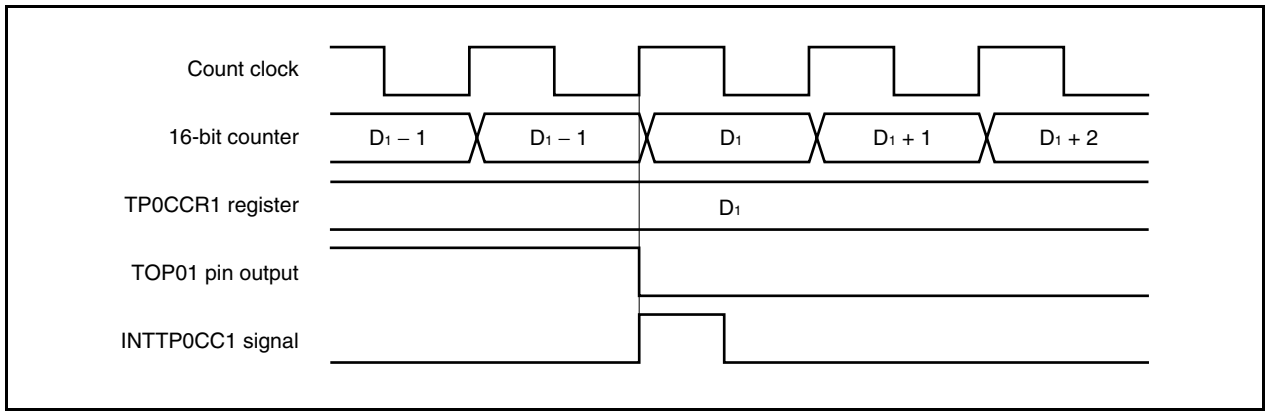


If the trigger is detected immediately before the INTTP0CC0 signal is generated, the INTTP0CC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOP01 pin is asserted, and the counter continues counting. Consequently, the inactive period of the PWM waveform is shortened.



(e) Generation timing of compare match interrupt request signal (INTTP0CC1)

The timing of generation of the INTTP0CC1 signal in the external trigger pulse output mode differs from the timing of other INTTP0CC1 signals; the INTTP0CC1 signal is generated when the count value of the 16-bit counter matches the value of the TP0CCR1 register.



Usually, the INTTP0CC1 signal is generated in synchronization with the next count up, after the count value of the 16-bit counter matches the value of the TP0CCR1 register.

In the external trigger pulse output mode, however, it is generated one clock earlier. This is because the timing is changed to match the timing of changing the output signal of the TOP01 pin.

7.5.4 One-shot pulse output mode (TP0MD2 to TP0MD0 bits = 011)

In the one-shot pulse output mode, 16-bit timer/event counter P waits for a trigger when the TP0CTL0.TP0CE bit is set to 1. When the valid edge of an external trigger input is detected, 16-bit timer/event counter P starts counting, and outputs a one-shot pulse from the TOP01 pin.

Instead of the external trigger, a software trigger can also be generated to output the pulse. When the software trigger is used, the TOP00 pin outputs the active level while the 16-bit counter is counting, and the inactive level when the counter is stopped (waiting for a trigger).

Figure 7-20. Configuration in One-Shot Pulse Output Mode

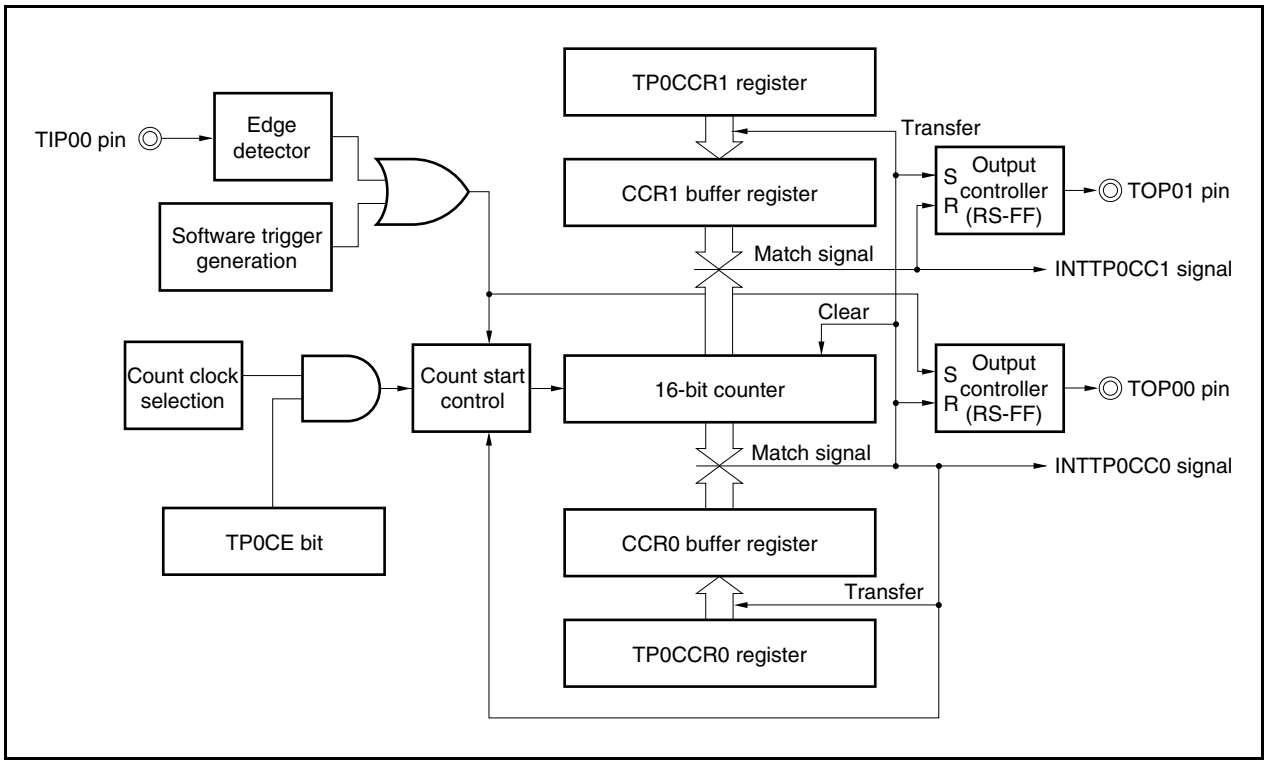
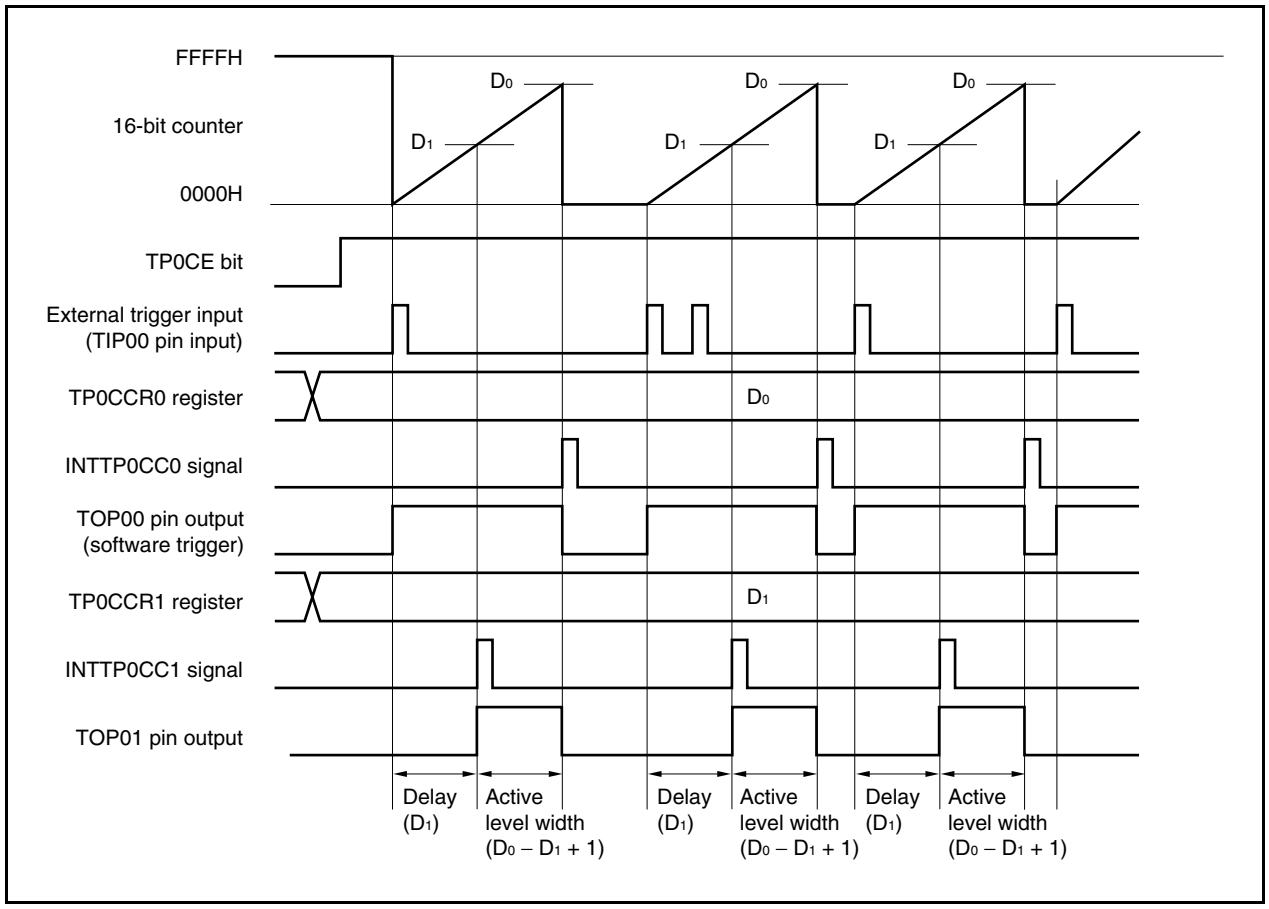


Figure 7-21. Basic Timing in One-Shot Pulse Output Mode



When the TP0CE bit is set to 1, 16-bit timer/event counter P waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a one-shot pulse from the TOP01 pin. After the one-shot pulse is output, the 16-bit counter is set to FFFFH, stops counting, and waits for a trigger. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows.

Output delay period = (Set value of TP0CCR1 register) × Count clock cycle

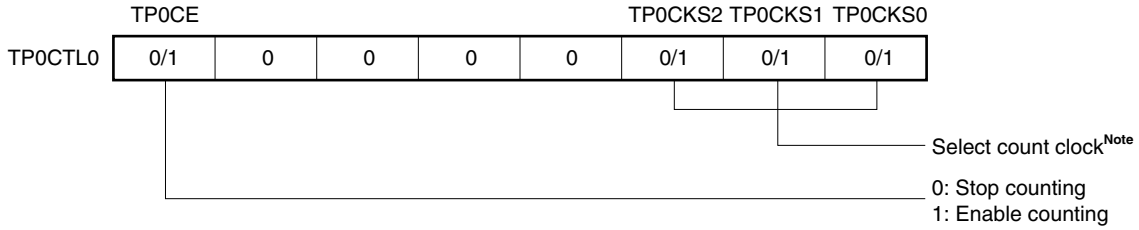
Active level width = (Set value of TP0CCR0 register − Set value of TP0CCR1 register + 1) × Count clock cycle

The compare match interrupt request signal INTTP0CC0 is generated when the 16-bit counter counts after its count value matches the value of the CCR0 buffer register. The compare match interrupt request signal INTTP0CC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The valid edge of an external trigger input or setting the software trigger (TP0CTL1.TP0EST bit) to 1 is used as the trigger.

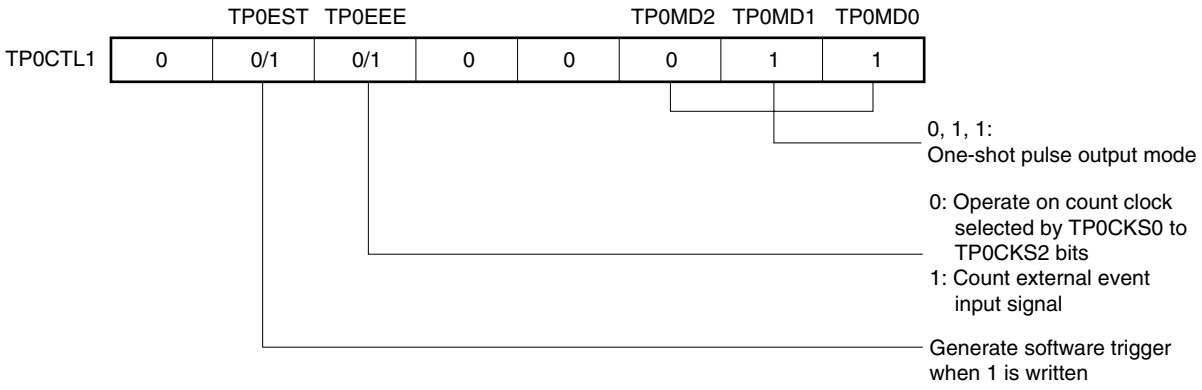
Figure 7-22. Setting of Registers in One-Shot Pulse Output Mode (1/2)

(a) TMP0 control register 0 (TP0CTL0)

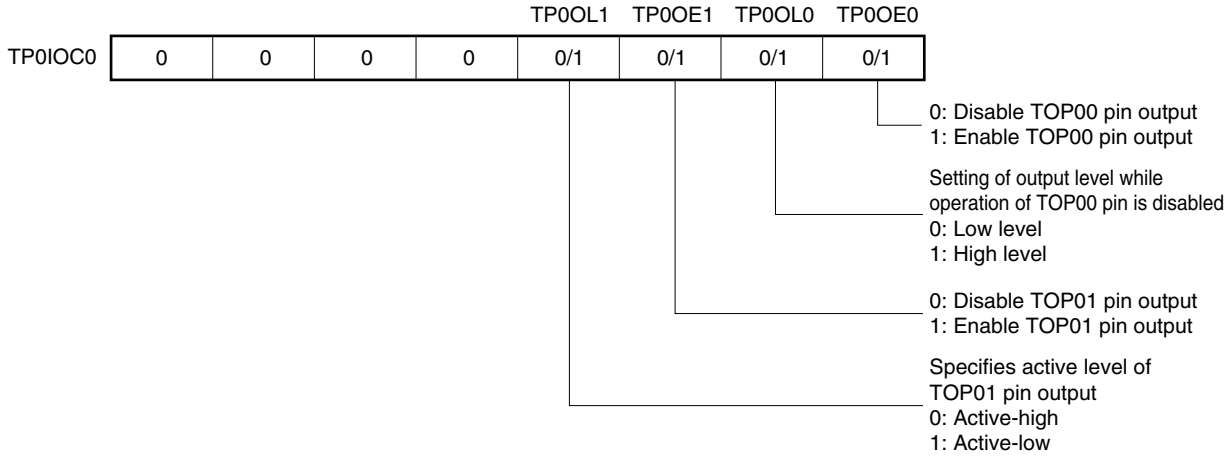


Note The setting is invalid when the TP0CTL1.TP0EEE bit = 1.

(b) TMP0 control register 1 (TP0CTL1)



(c) TMP0 I/O control register 0 (TP0IOC0)



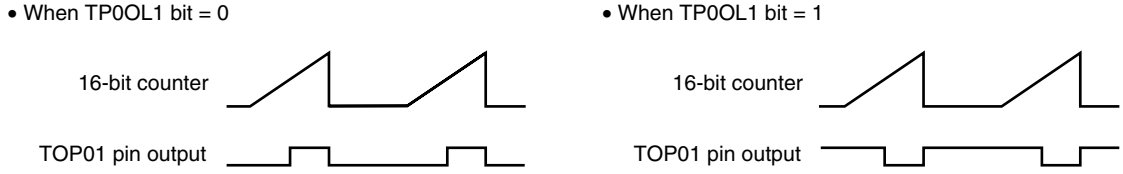
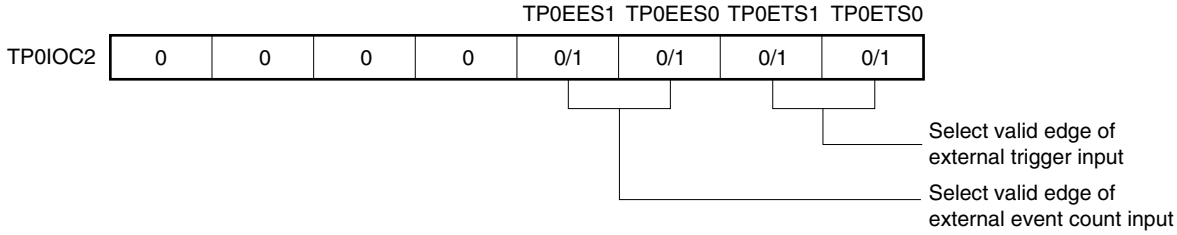


Figure 7-22. Setting of Registers in One-Shot Pulse Output Mode (2/2)

(d) TMP0 I/O control register 2 (TP0IOC2)



(e) TMP0 counter read buffer register (TP0CNT)

The value of the 16-bit counter can be read by reading the TP0CNT register.

(f) TMP0 capture/compare registers 0 and 1 (TP0CCR0 and TP0CCR1)

If D_0 is set to the TP0CCR0 register and D_1 to the TP0CCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

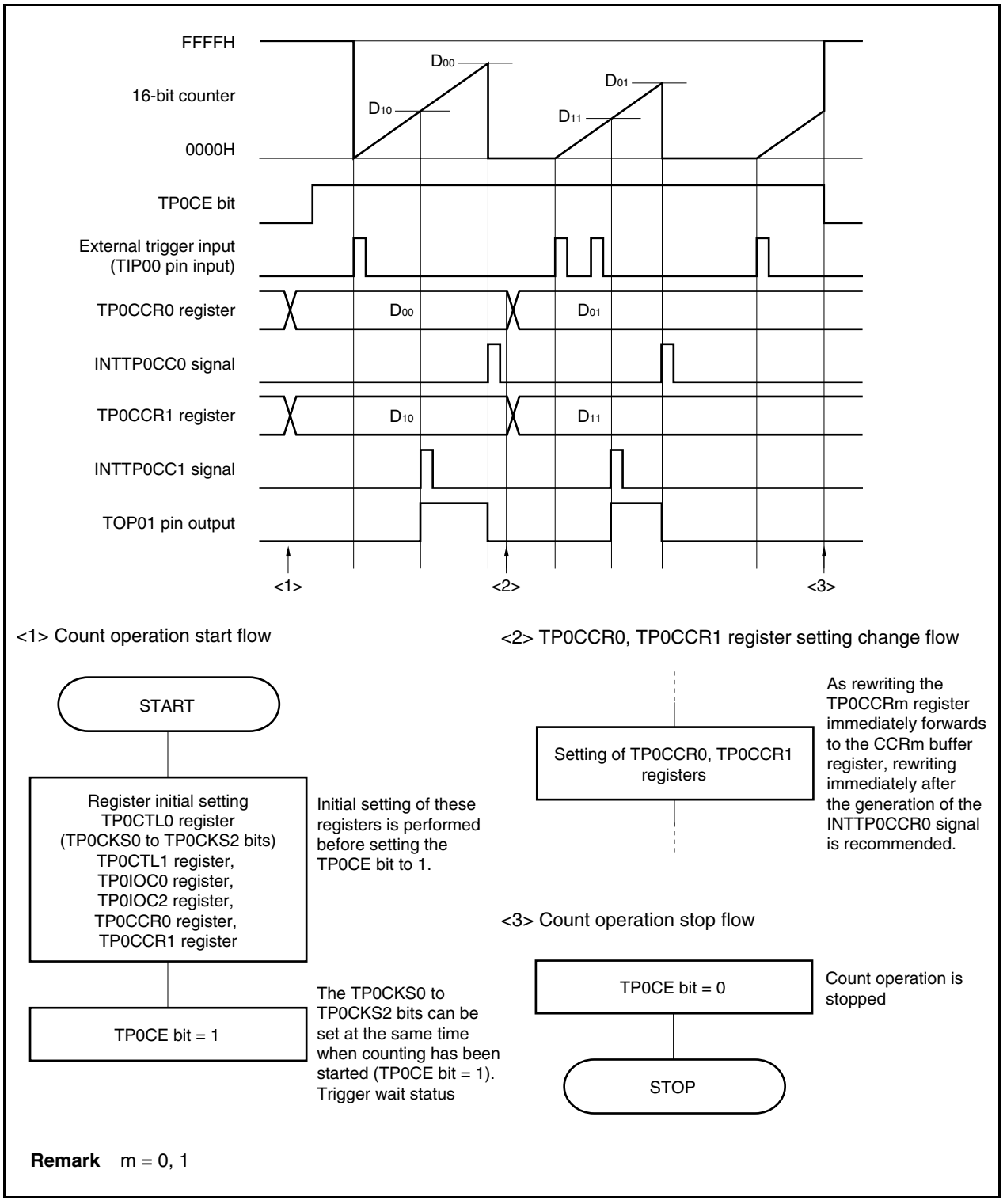
Active level width = $(D_1 - D_0 + 1) \times$ Count clock cycle

Output delay period = $D_1 \times$ Count clock cycle

Remark TMP0 I/O control register 1 (TP0IOC1) and TMP0 option register 0 (TP0OPT0) are not used in the one-shot pulse output mode.

(1) Operation flow in one-shot pulse output mode

Figure 7-23. Software Processing Flow in One-Shot Pulse Output Mode



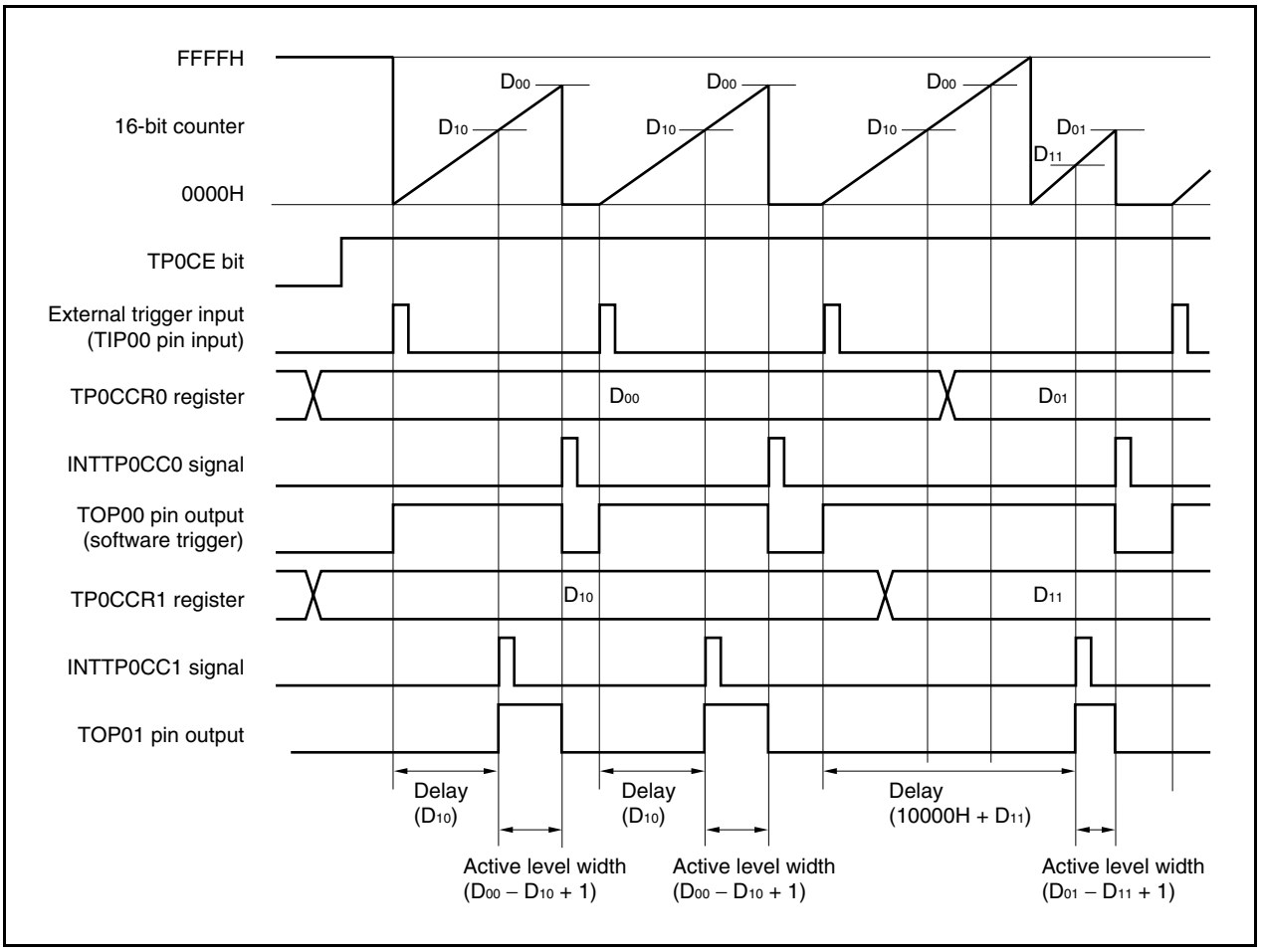
Remark m = 0, 1

(2) Operation timing in one-shot pulse output mode

(a) Note on rewriting TP0CCRa register

To change the set value of the TP0CCRa register to a smaller value, stop counting once, and then change the set value.

If the value of the TP0CCRa register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



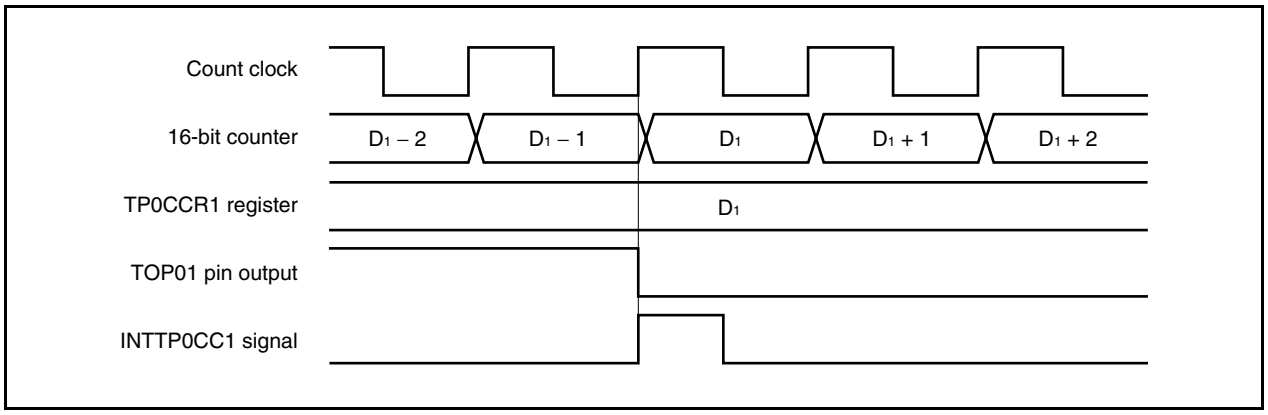
When the TP0CCR0 register is rewritten from D_{00} to D_{01} and the TP0CCR1 register from D_{10} to D_{11} where $D_{00} > D_{01}$ and $D_{10} > D_{11}$, if the TP0CCR1 register is rewritten when the count value of the 16-bit counter is greater than D_{11} and less than D_{10} and if the TP0CCR0 register is rewritten when the count value is greater than D_{01} and less than D_{00}, each set value is reflected as soon as the register has been rewritten and compared with the count value. The counter counts up to FFFFH and then counts up again from 0000H. When the count value matches D_{11}, the counter generates the INTTP0CC1 signal and asserts the TOP01 pin. When the count value matches D_{01}, the counter generates the INTTP0CC0 signal, deasserts the TOP01 pin, and stops counting.

Therefore, the counter may output a pulse with a delay period or active period different from that of the one-shot pulse that is originally expected.

Remark a = 0, 1

(b) Generation timing of compare match interrupt request signal (INTTP0CC1)

The generation timing of the INTTP0CC1 signal in the one-shot pulse output mode is different from other INTTP0CC1 signals; the INTTP0CC1 signal is generated when the count value of the 16-bit counter matches the value of the TP0CCR1 register.



Usually, the INTTP0CC1 signal is generated when the 16-bit counter counts up next time after its count value matches the value of the TP0CCR1 register.

In the one-shot pulse output mode, however, it is generated one clock earlier. This is because the timing is changed to match the change timing of the TOP01 pin.

7.5.5 PWM output mode (TP0MD2 to TP0MD0 bits = 100)

In the PWM output mode, a PWM waveform is output from the TOP01 pin when the TP0CTL0.TP0CE bit is set to 1. In addition, a pulse with one cycle of the PWM waveform as half its cycle is output from the TOP00 pin.

Figure 7-24. Configuration in PWM Output Mode

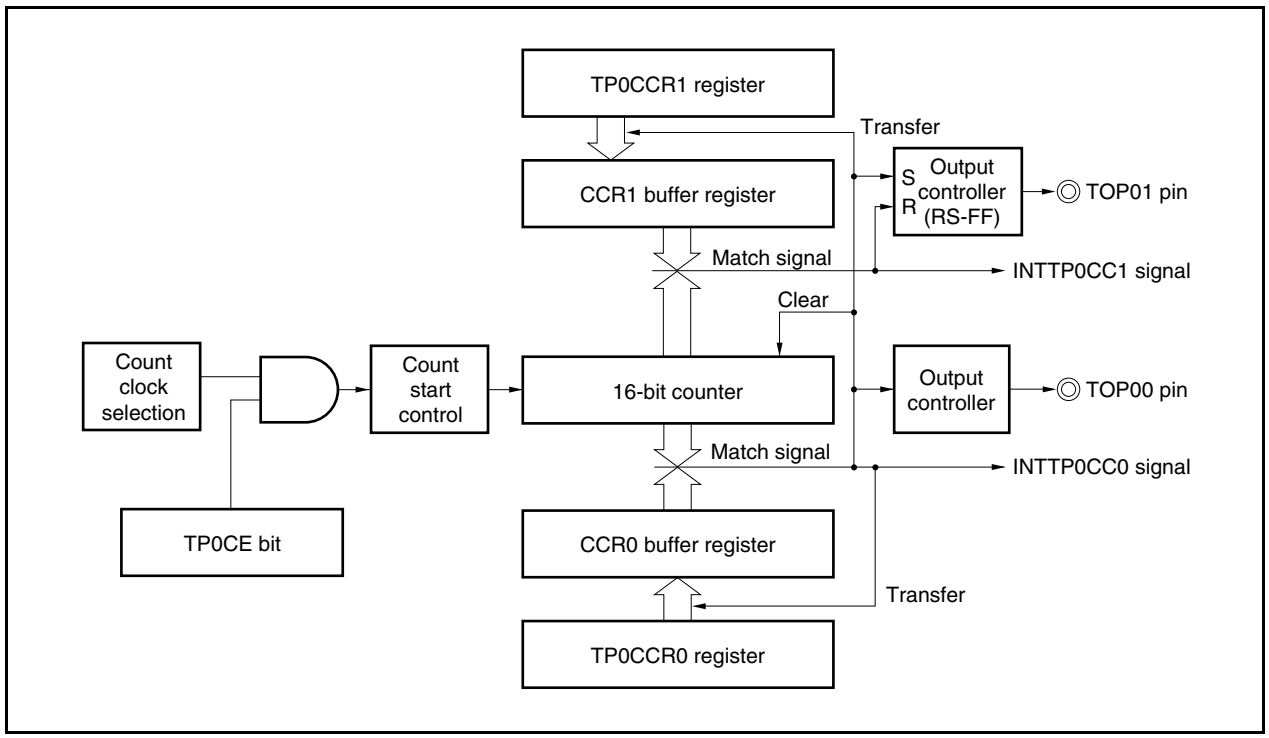
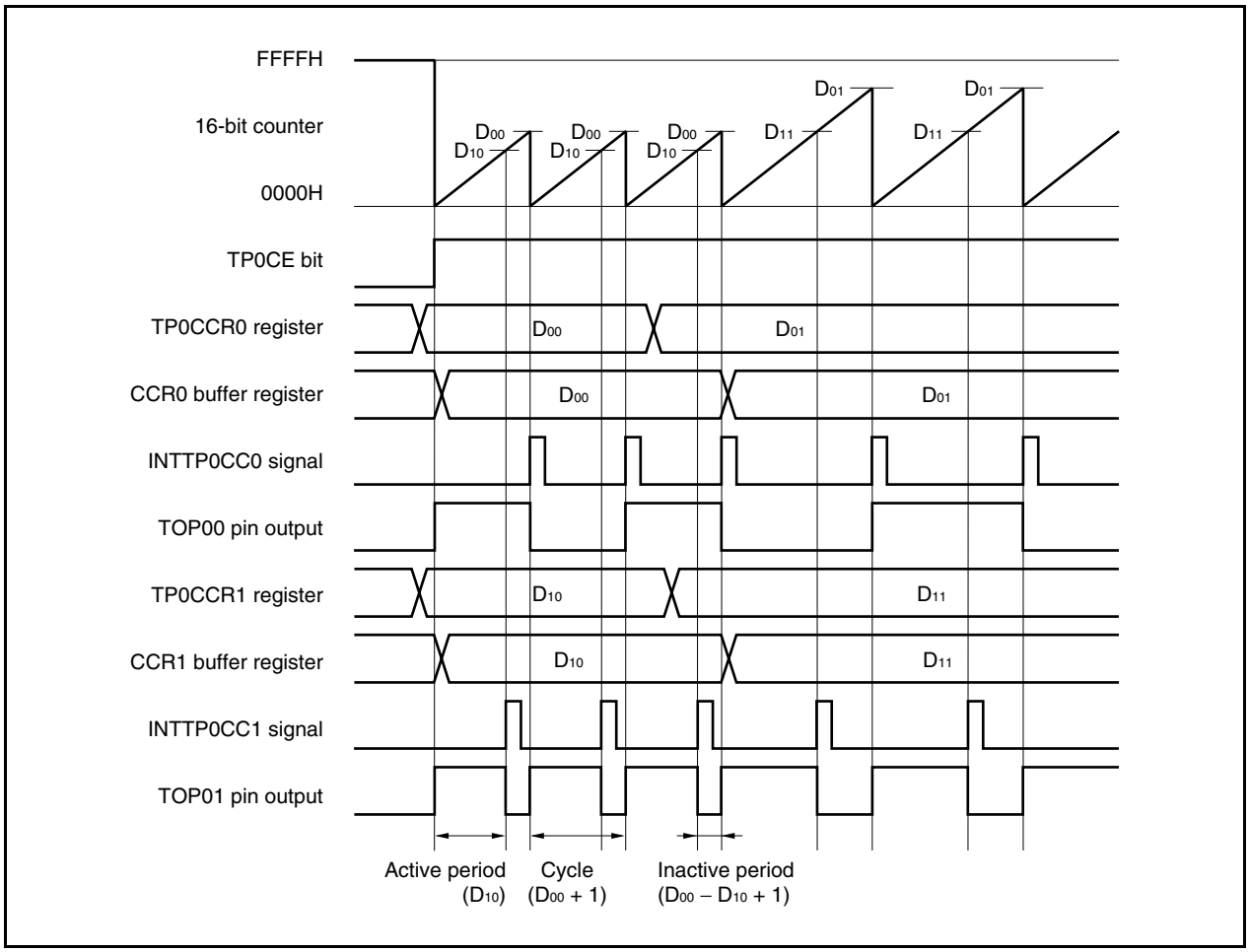


Figure 7-25. Basic Timing in PWM Output Mode



When the TP0CE bit is set to 1, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a PWM waveform from the TOP01 pin.

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TP0CCR1 register) × Count clock cycle
Cycle = (Set value of TP0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TP0CCR1 register)/(Set value of TP0CCR0 register + 1)

The PWM waveform can be changed by rewriting the TP0CCRa register while the counter is operating. The newly written value is reflected when the count value of the 16-bit counter matches the value of the CCR0 buffer register and the 16-bit counter is cleared to 0000H.

The compare match interrupt request signal INTTP0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTP0CC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The value set to the TP0CCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

Remark a = 0, 1

Figure 7-26. Register Setting in PWM Output Mode (1/2)

(a) TMP0 control register 0 (TP0CTL0)

	TP0CE					TP0CKS2	TP0CKS1	TP0CKS0
TP0CTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock[Note]

0: Stop counting
1: Enable counting

Note The setting is invalid when the TP0CTL1.TP0EEE bit = 1.

(b) TMP0 control register 1 (TP0CTL1)

		TP0EST	TP0EEE				TP0MD2	TP0MD1	TP0MD0
TP0CTL1	0	0	0/1	0	0	1	0	0

1, 0, 0:
PWM output mode

0: Operate on count clock selected by TP0CKS0 to TP0CKS2 bits
1: Count with external event count input signal

(c) TMP0 I/O control register 0 (TP0IOC0)

					TP0OL1	TP0OE1	TP0OL0	TP0OE0
TP0IOC0	0	0	0	0	0/1	0/1	0/1	0/1

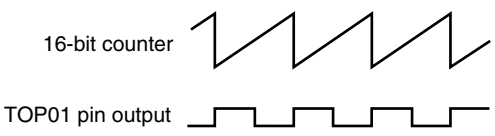
0: Disable TOP00 pin output
1: Enable TOP00 pin output

Setting of output level while operation of TOP00 pin is disabled
0: Low level
1: High level

0: Disable TOP01 pin output
1: Enable TOP01 pin output

Specifies active level of TOP01 pin output
0: Active-high
1: Active-low

- When TP0OL1 bit = 0



- When TP0OL1 bit = 1

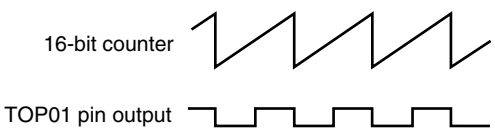


Figure 7-26. Register Setting in PWM Output Mode (2/2)

(d) TMP0 I/O control register 2 (TP0IOC2)

					TP0EES1	TP0EES0	TP0ETS1	TP0ETS0
TP0IOC2	0	0	0	0	0/1	0/1	0	0

Select valid edge of external event count input.

(e) TMP0 counter read buffer register (TP0CNT)

The value of the 16-bit counter can be read by reading the TP0CNT register.

(f) TMP0 capture/compare registers 0 and 1 (TP0CCR0 and TP0CCR1)

If D_0 is set to the TP0CCR0 register and D_1 to the TP0CCR1 register, the cycle and active level of the PWM waveform are as follows.

Cycle = $(D_0 + 1) \times$ Count clock cycle

Active level width = $D_1 \times$ Count clock cycle

Remark TMP0 I/O control register 1 (TP0IOC1) and TMP0 option register 0 (TP0OPT0) are not used in the PWM output mode.

(1) Operation flow in PWM output mode

Figure 7-27. Software Processing Flow in PWM Output Mode (1/2)

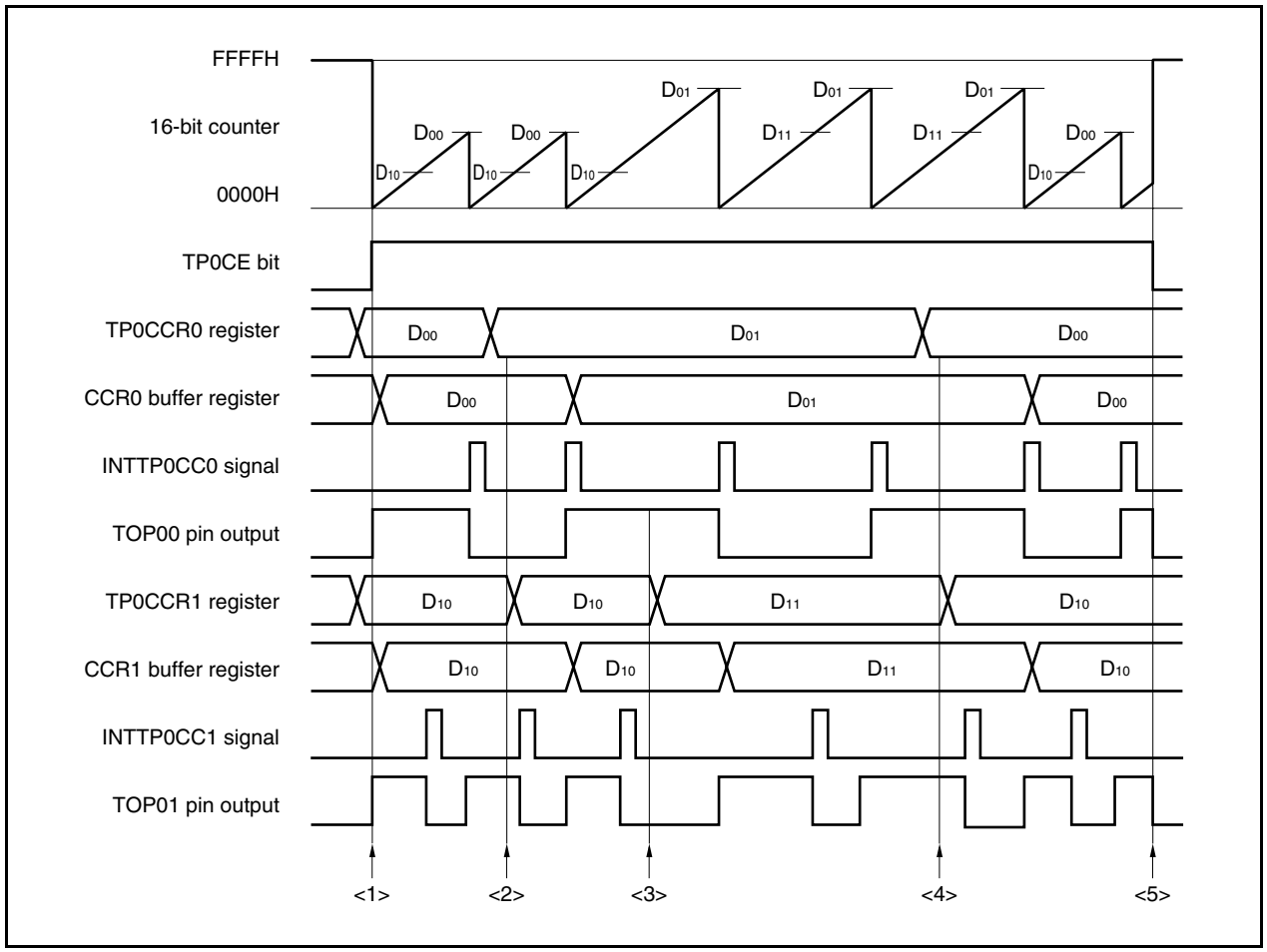
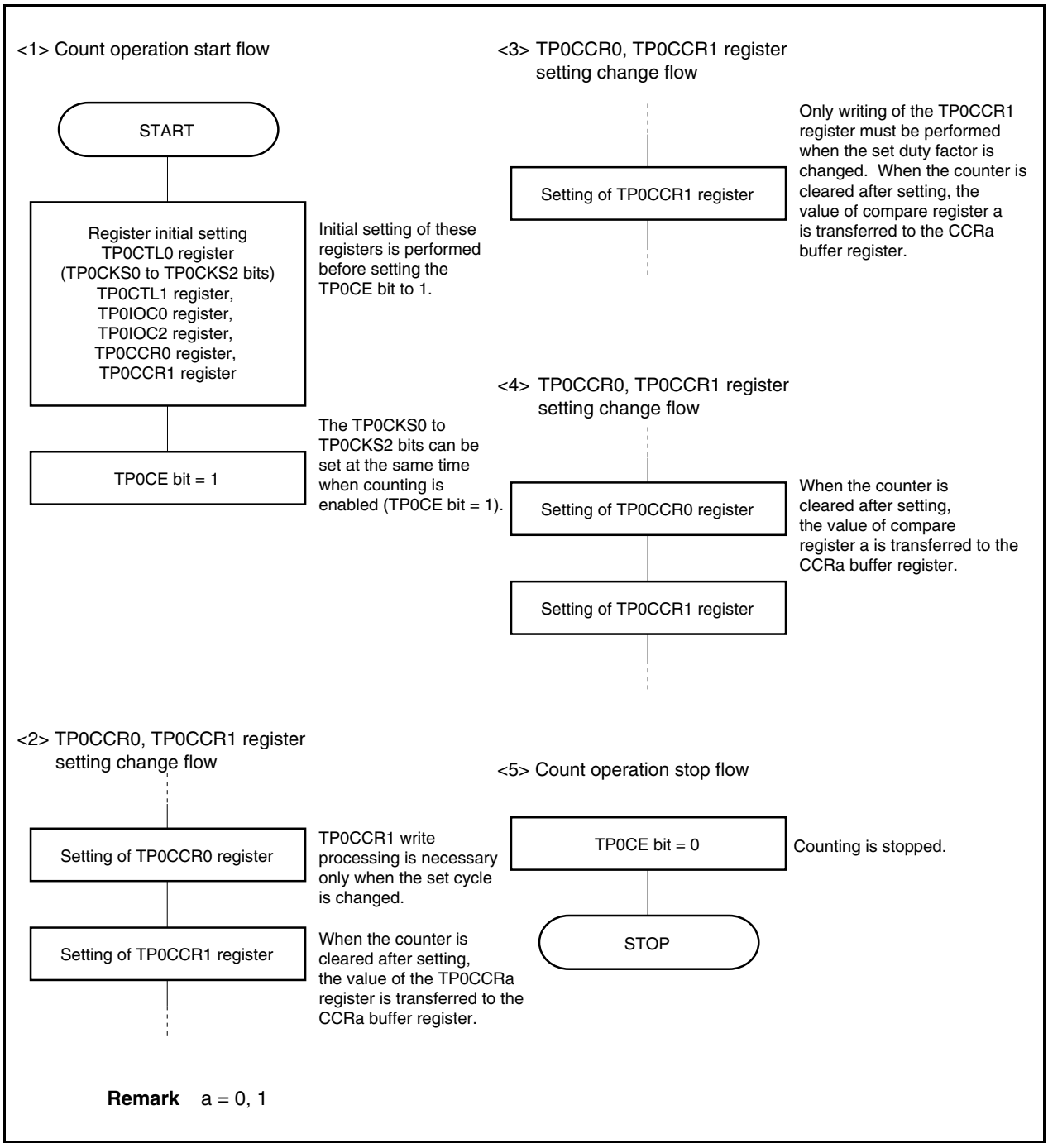


Figure 7-27. Software Processing Flow in PWM Output Mode (2/2)



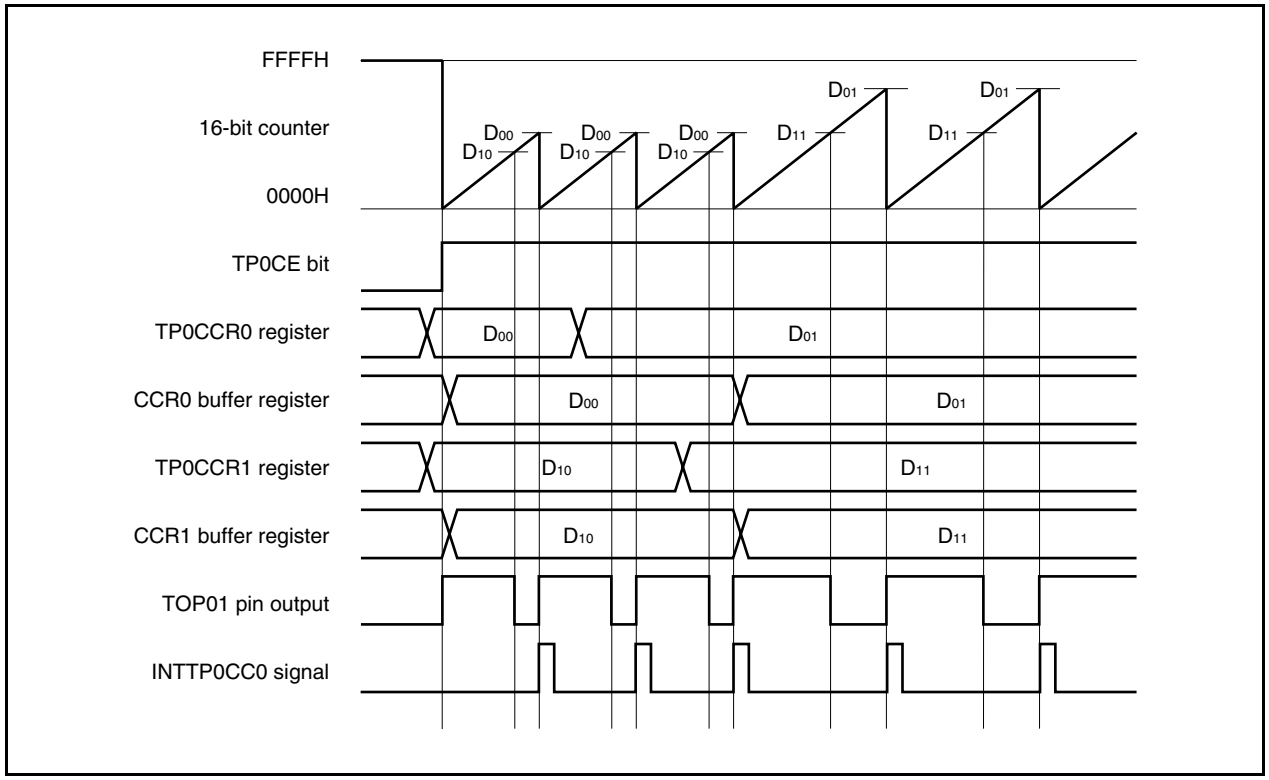
Remark a = 0, 1

(2) PWM output mode operation timing

(a) Changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TP0CCR1 register last.

Rewrite the TP0CCRa register after writing the TP0CCR1 register after the INTTP0CC1 signal is detected.



To transfer data from the TP0CCRa register to the CCRa buffer register, the TP0CCR1 register must be written.

To change both the cycle and active level of the PWM waveform at this time, first set the cycle to the TP0CCR0 register and then set the active level to the TP0CCR1 register.

To change only the cycle of the PWM waveform, first set the cycle to the TP0CCR0 register, and then write the same value to the TP0CCR1 register.

To change only the active level width (duty factor) of the PWM waveform, only the TP0CCR1 register has to be set.

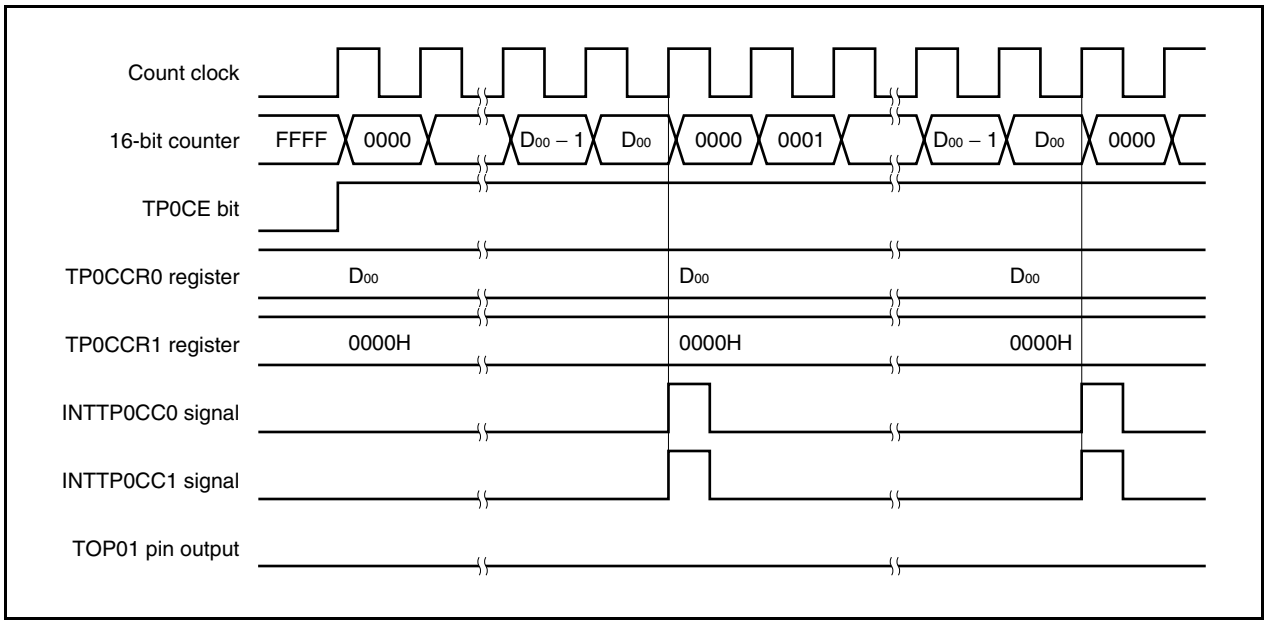
After data is written to the TP0CCR1 register, the value written to the TP0CCRa register is transferred to the CCRa buffer register in synchronization with clearing of the 16-bit counter, and is used as the value compared with the 16-bit counter.

To write the TP0CCR0 or TP0CCR1 register again after writing the TP0CCR1 register once, do so after the INTTP0CC0 signal is generated. Otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TP0CCRa register to the CCRa buffer register conflicts with writing the TP0CCRa register.

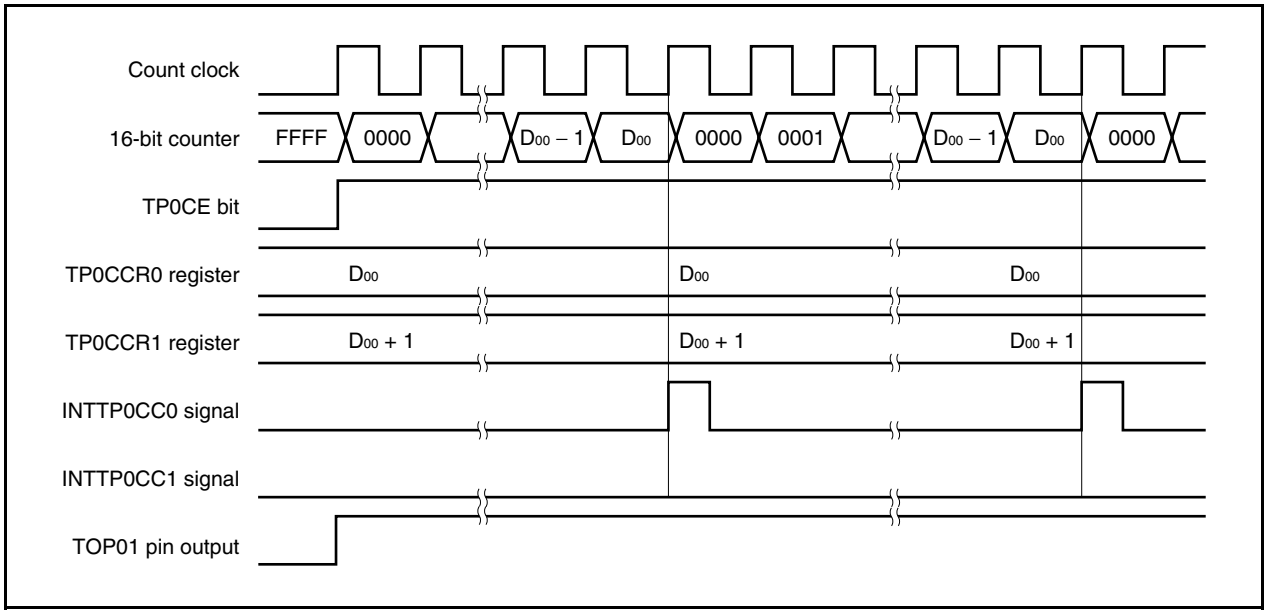
Remark a = 0, 1

(b) 0%/100% output of PWM waveform

To output a 0% waveform, set the TP0CCR1 register to 0000H. If the set value of the TP0CCR0 register is FFFFH, the INTTP0CC1 signal is generated periodically.

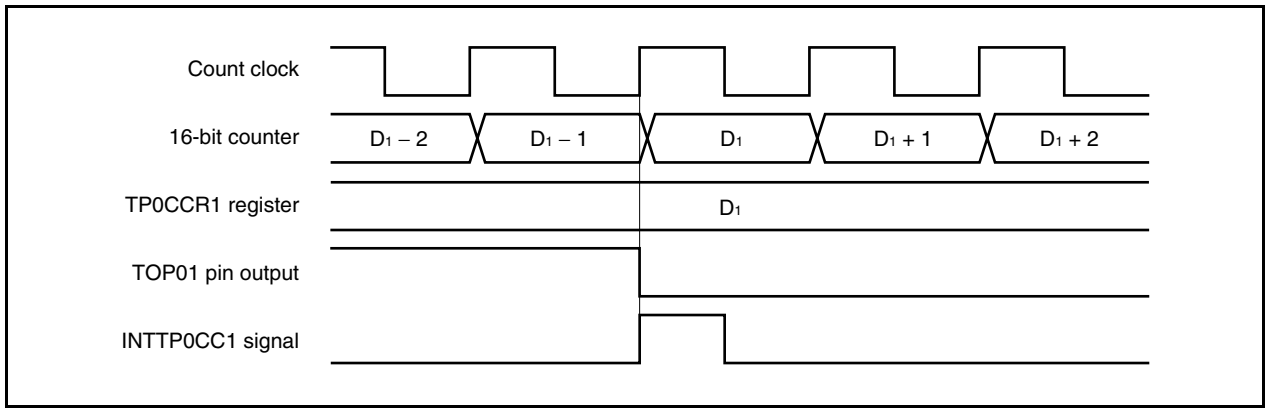


To output a 100% waveform, set a value of (set value of TP0CCR0 register + 1) to the TP0CCR1 register. If the set value of the TP0CCR0 register is FFFFH, 100% output cannot be produced.



(c) Generation timing of compare match interrupt request signal (INTTP0CC1)

The timing of generation of the INTTP0CC1 signal in the PWM output mode differs from the timing of other INTTP0CC1 signals; the INTTP0CC1 signal is generated when the count value of the 16-bit counter matches the value of the TP0CCR1 register.



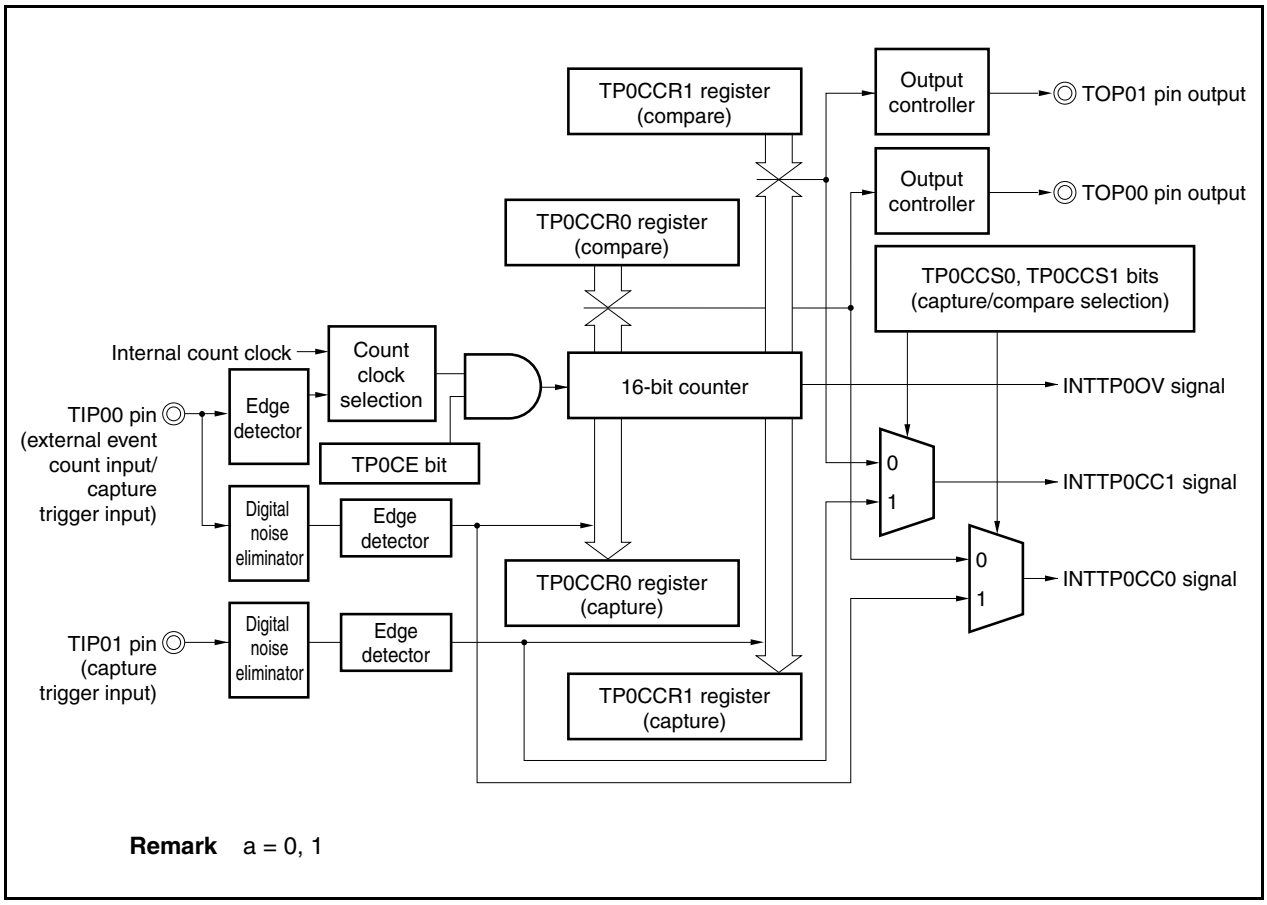
Usually, the INTTP0CC1 signal is generated in synchronization with the next counting up after the count value of the 16-bit counter matches the value of the TP0CCR1 register.

In the PWM output mode, however, it is generated one clock earlier. This is because the timing is changed to match the change timing of the output signal of the TOP01 pin.

7.5.6 Free-running timer mode (TP0MD2 to TP0MD0 bits = 101)

In the free-running timer mode, 16-bit timer/event counter P starts counting when the TP0CTL0.TP0CE bit is set to 1. At this time, the TP0CCRa register can be used as a compare register or a capture register, depending on the setting of the TP0OPT0.TP0CCS0 and TP0OPT0.TP0CCS1 bits.

Figure 7-28. Configuration in Free-Running Timer Mode



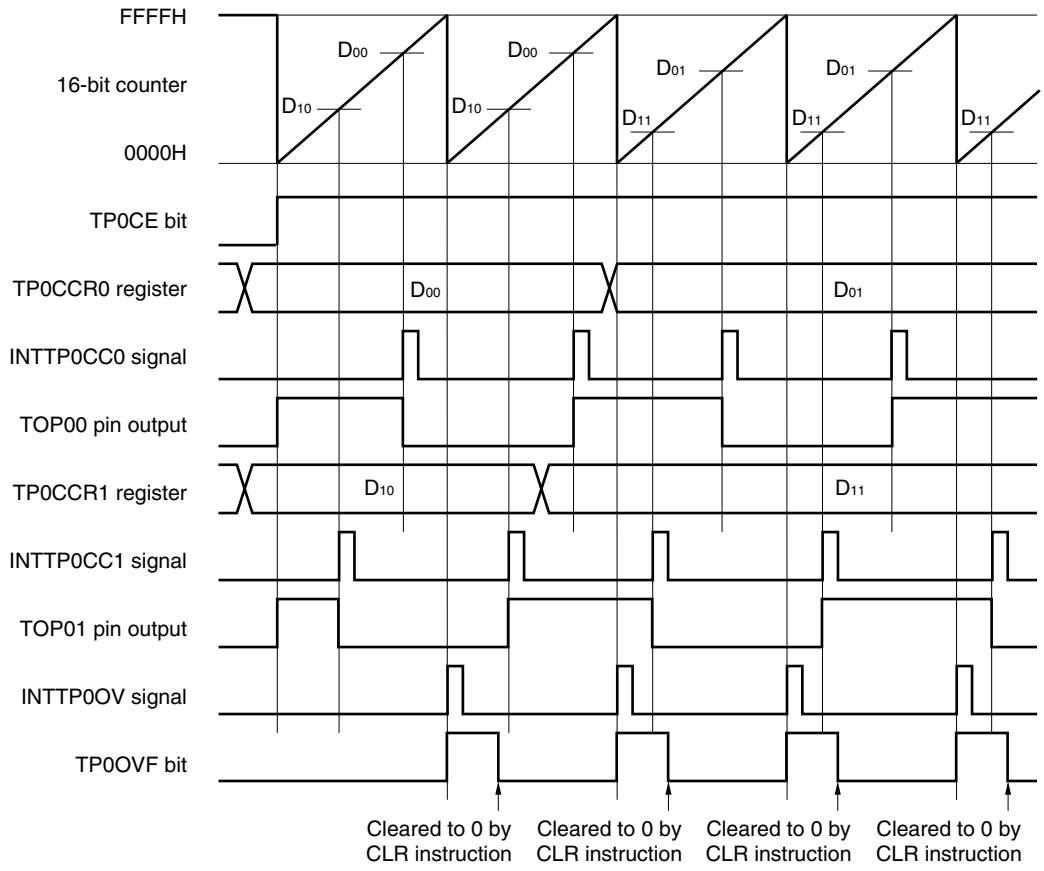
Remark a = 0, 1

When the TP0CE bit is set to 1, 16-bit timer/event counter P starts counting, and the output signals of the TOP00 and TOP01 pins are inverted. When the count value of the 16-bit counter later matches the set value of the TP0CCRa register, a compare match interrupt request signal (INTTP0CCa) is generated, and the output signal of the TOP0a pin is inverted.

The 16-bit counter continues counting in synchronization with the count clock. When it counts up to FFFFH, it generates an overflow interrupt request signal (INTTP0OV) at the next clock, is cleared to 0000H, and continues counting. At this time, the overflow flag (TP0OPT0.TP0OVF bit) is also set to 1. Clear the overflow flag to 0 by executing the CLR instruction by software.

The TP0CCRa register can be rewritten while the counter is operating. If it is rewritten, the new value is reflected at that time, and compared with the count value.

Figure 7-29. Basic Timing in Free-Running Timer Mode (Compare Function)



Remark a = 0, 1

When the TP0CE bit is set to 1, the 16-bit counter starts counting. When the valid edge input to the TIP0a pin is detected, the count value of the 16-bit counter is stored in the TP0CCRa register, and a capture interrupt request signal (INTTP0CCa) is generated.

The 16-bit counter continues counting in synchronization with the count clock. When it counts up to FFFFH, it generates an overflow interrupt request signal (INTTP0OV) at the next clock, is cleared to 0000H, and continues counting. At this time, the overflow flag (TP0OPT0.TP0OVF bit) is also set to 1. Clear the overflow flag to 0 by executing the CLR instruction by software.

Figure 7-30. Basic Timing in Free-Running Timer Mode (Capture Function)

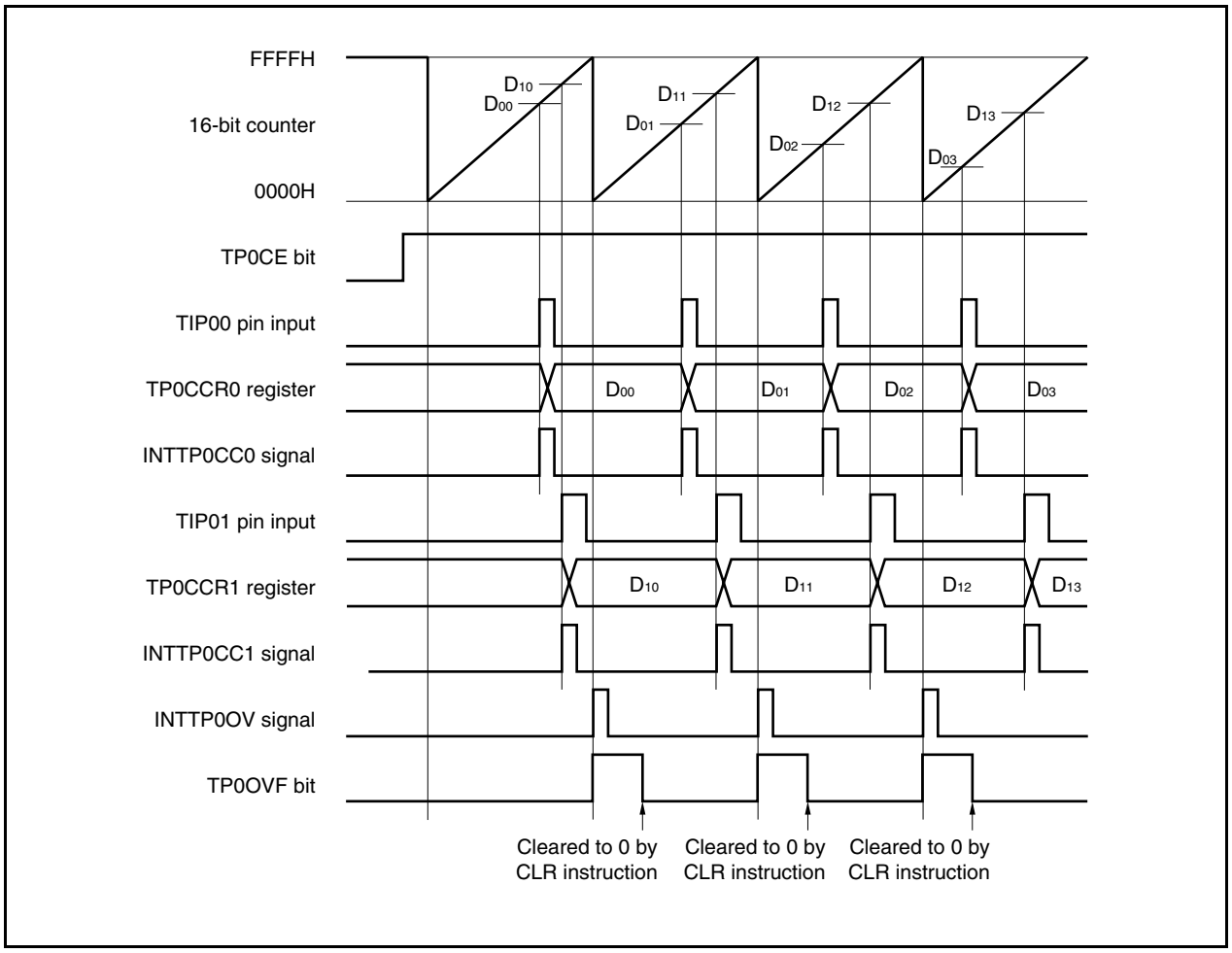
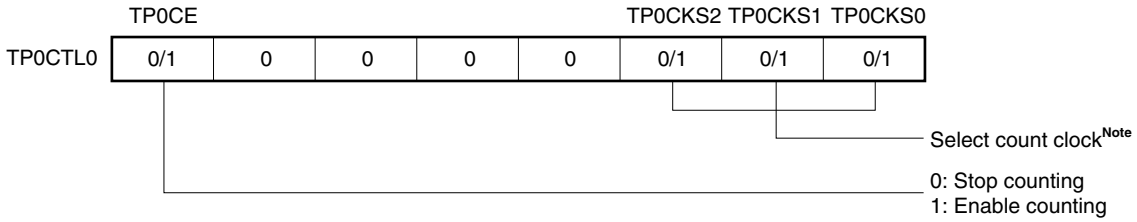


Figure 7-31. Register Setting in Free-Running Timer Mode (1/2)

(a) TMP0 control register 0 (TP0CTL0)



Note The setting is invalid when the TP0CTL1.TP0EEE bit = 1

(b) TMP0 control register 1 (TP0CTL1)

(c) TMP0 I/O control register 0 (TP0IOC0)

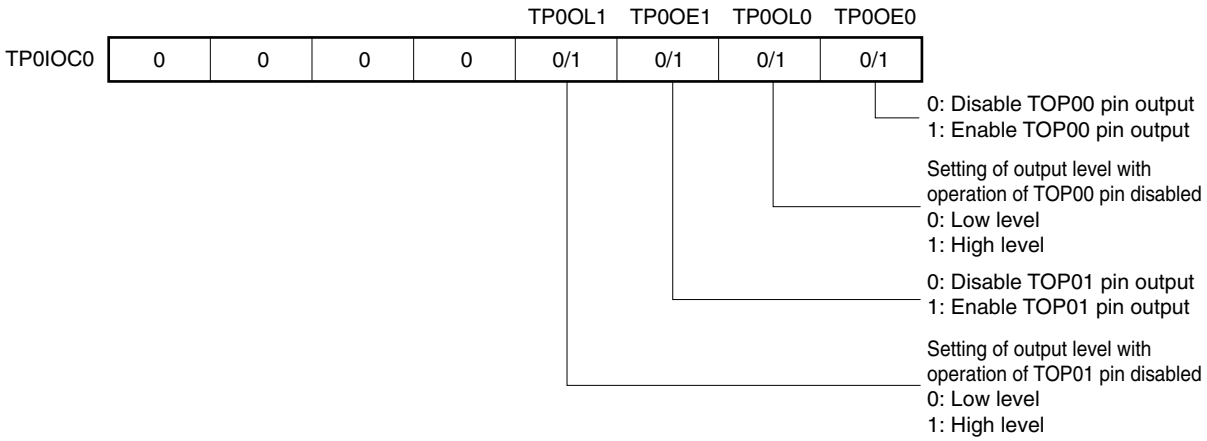
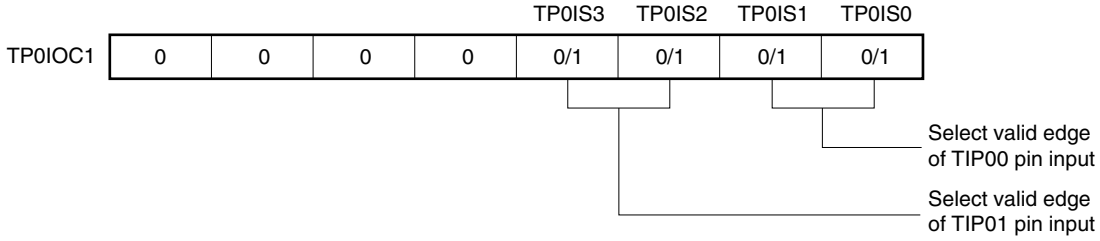
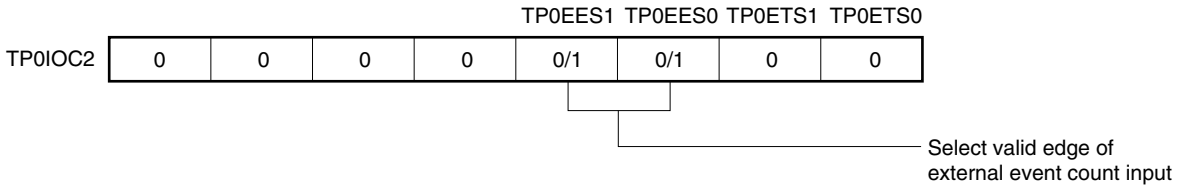


Figure 7-31. Register Setting in Free-Running Timer Mode (2/2)

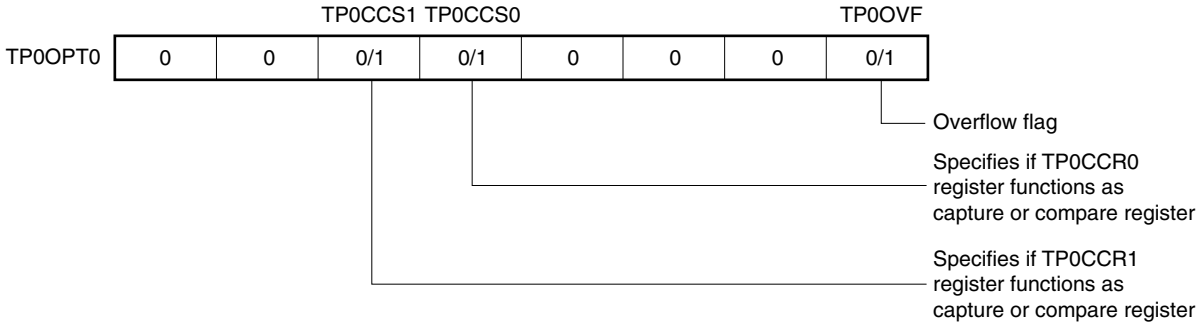
(d) TMP0 I/O control register 1 (TP0IOC1)



(e) TMP0 I/O control register 2 (TP0IOC2)



(f) TMP0 option register 0 (TP0OPT0)



(g) TMP0 counter read buffer register (TP0CNT)

The value of the 16-bit counter can be read by reading the TP0CNT register.

(h) TMP0 capture/compare registers 0 and 1 (TP0CCR0 and TP0CCR1)

These registers function as capture registers or compare registers depending on the setting of the TP0OPT0.TP0CCSa bit.

When the registers function as capture registers, they store the count value of the 16-bit counter when the valid edge input to the TIP0a pin is detected.

When the registers function as compare registers and when D_a is set to the TP0CCRa register, the INTTP0CCa signal is generated when the counter reaches (D_a + 1), and the output signal of the TOP0a pin is inverted.

Remark a = 0, 1

(1) Operation flow in free-running timer mode

(a) When using capture/compare register as compare register

Figure 7-32. Software Processing Flow in Free-Running Timer Mode (Compare Function) (1/2)

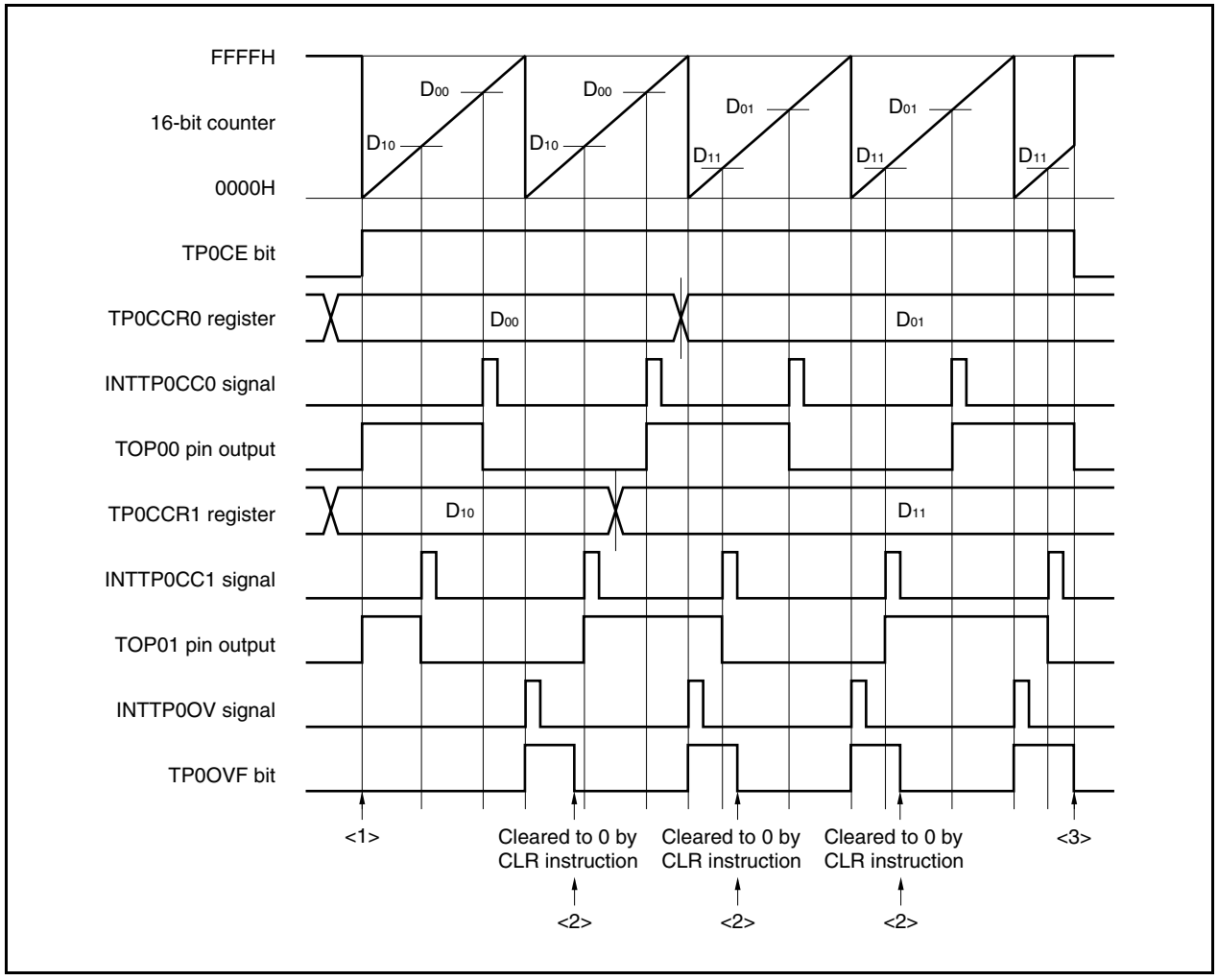
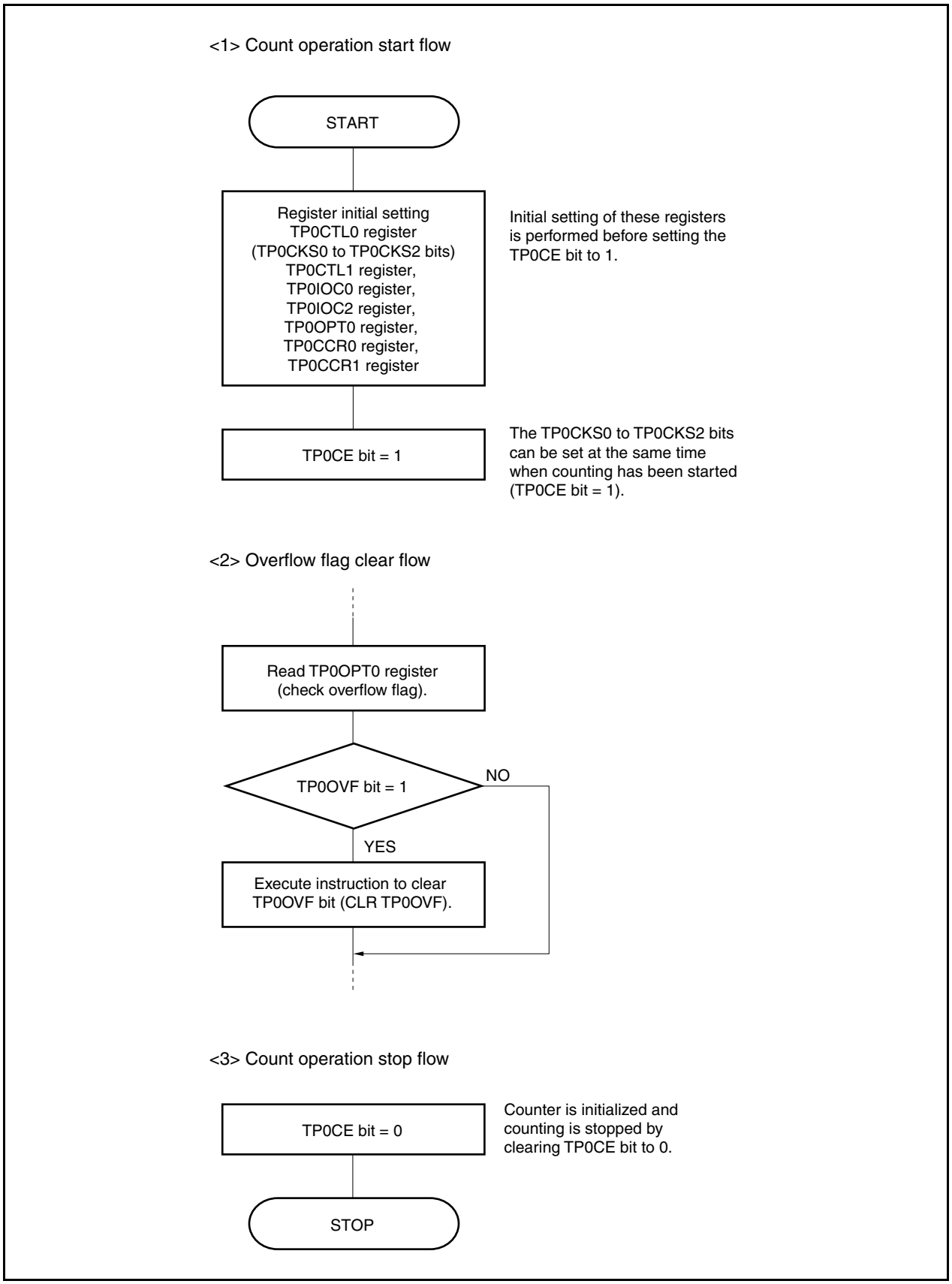


Figure 7-32. Software Processing Flow in Free-Running Timer Mode (Compare Function) (2/2)



(b) When using capture/compare register as capture register

Figure 7-33. Software Processing Flow in Free-Running Timer Mode (Capture Function) (1/2)

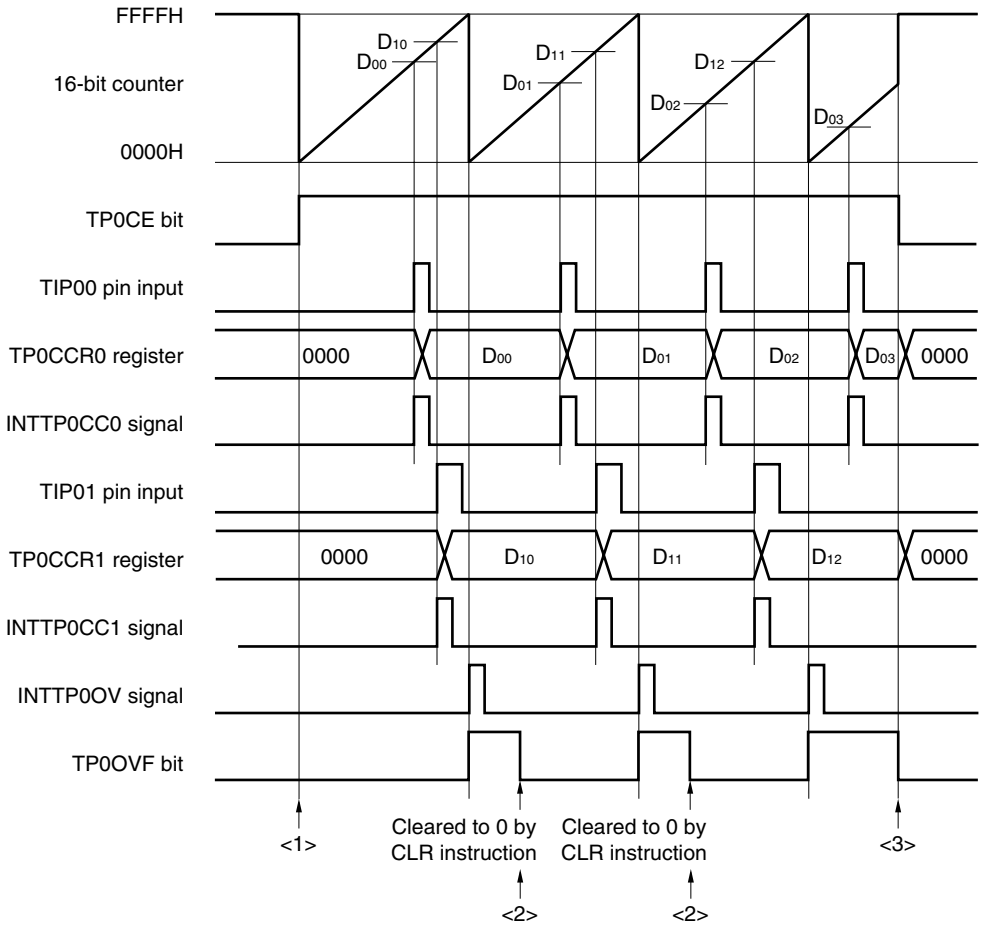
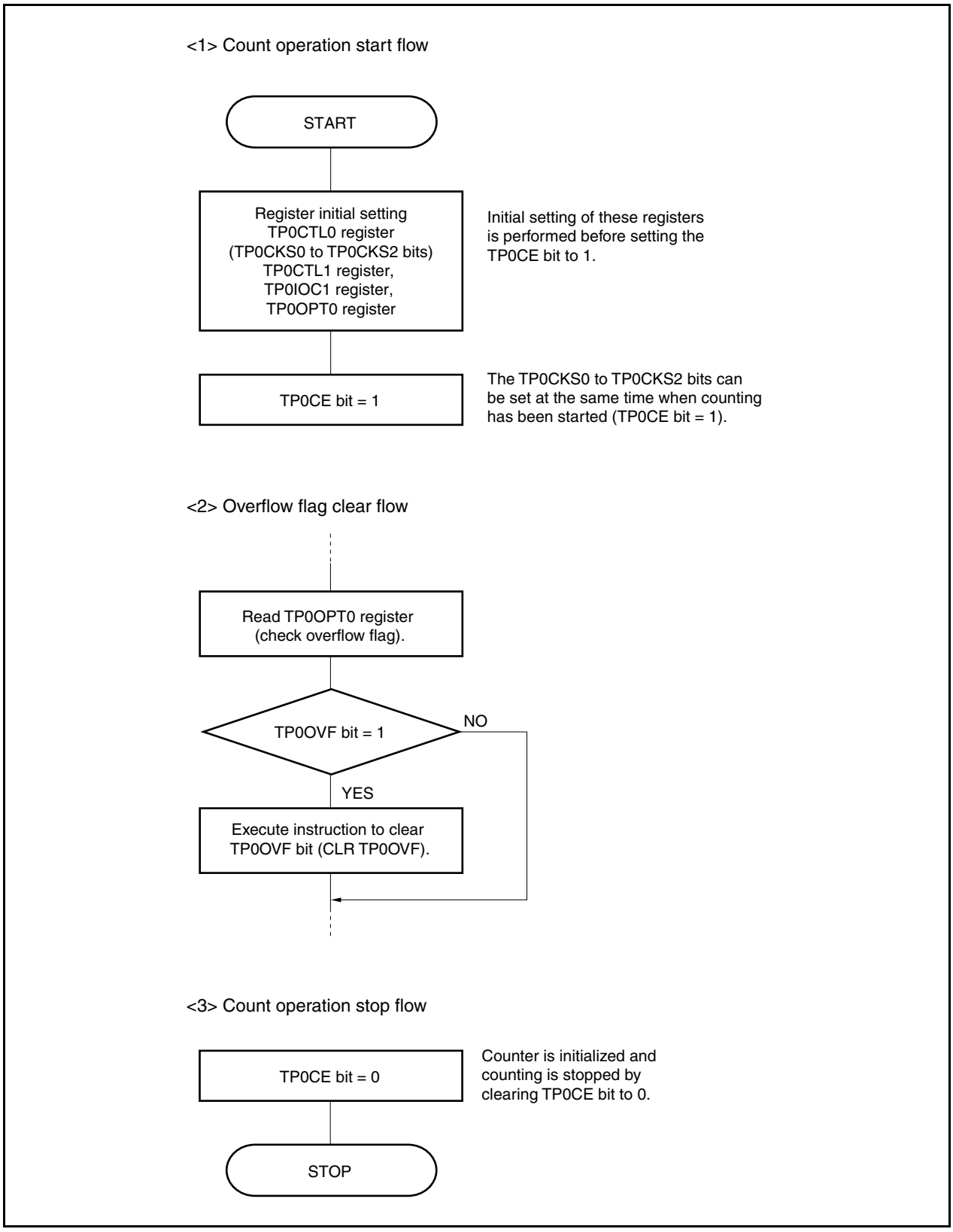


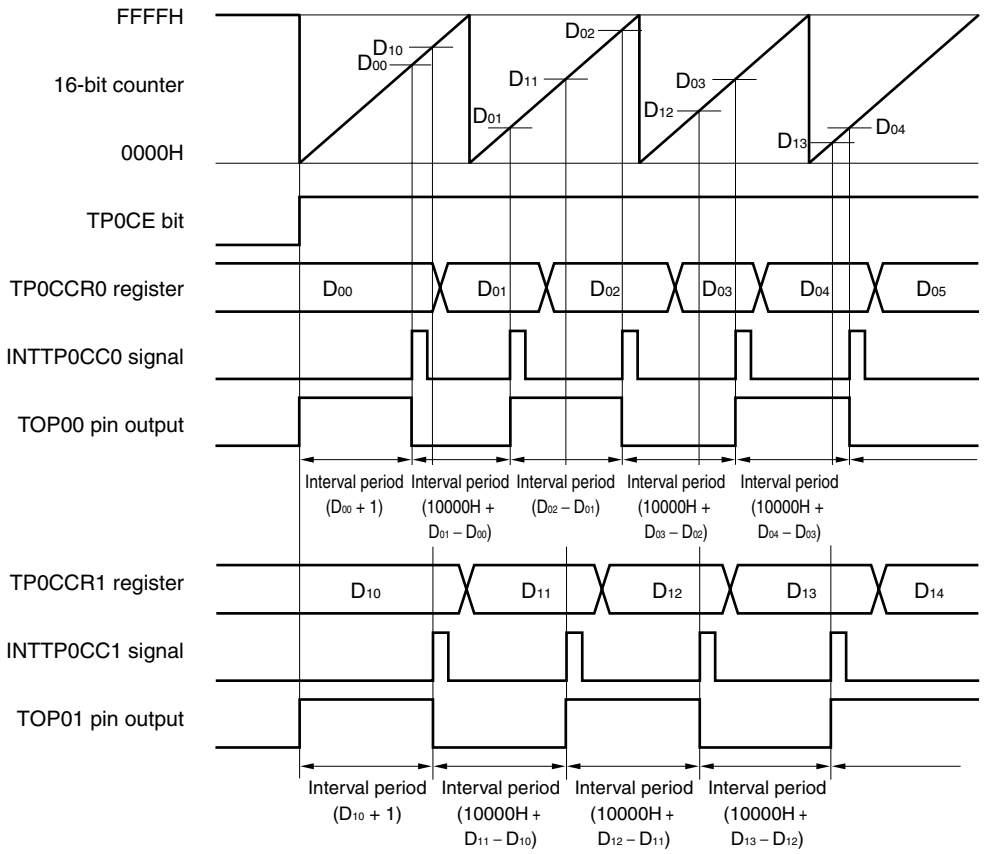
Figure 7-33. Software Processing Flow in Free-Running Timer Mode (Capture Function) (2/2)



(2) Operation timing in free-running timer mode

(a) Interval operation with compare register

When 16-bit timer/event counter P is used as an interval timer with the TP0CCRa register used as a compare register, software processing is necessary for setting a comparison value to generate the next interrupt request signal each time the INTTP0CCa signal has been detected.



When performing an interval operation in the free-running timer mode, two intervals can be set with one channel.

To perform the interval operation, the value of the corresponding TP0CCRa register must be re-set in the interrupt servicing that is executed when the INTTP0CCa signal is detected.

The set value for re-setting the TP0CCRa register can be calculated by the following expression, where "D_a" is the interval period.

Compare register default value: $D_a - 1$

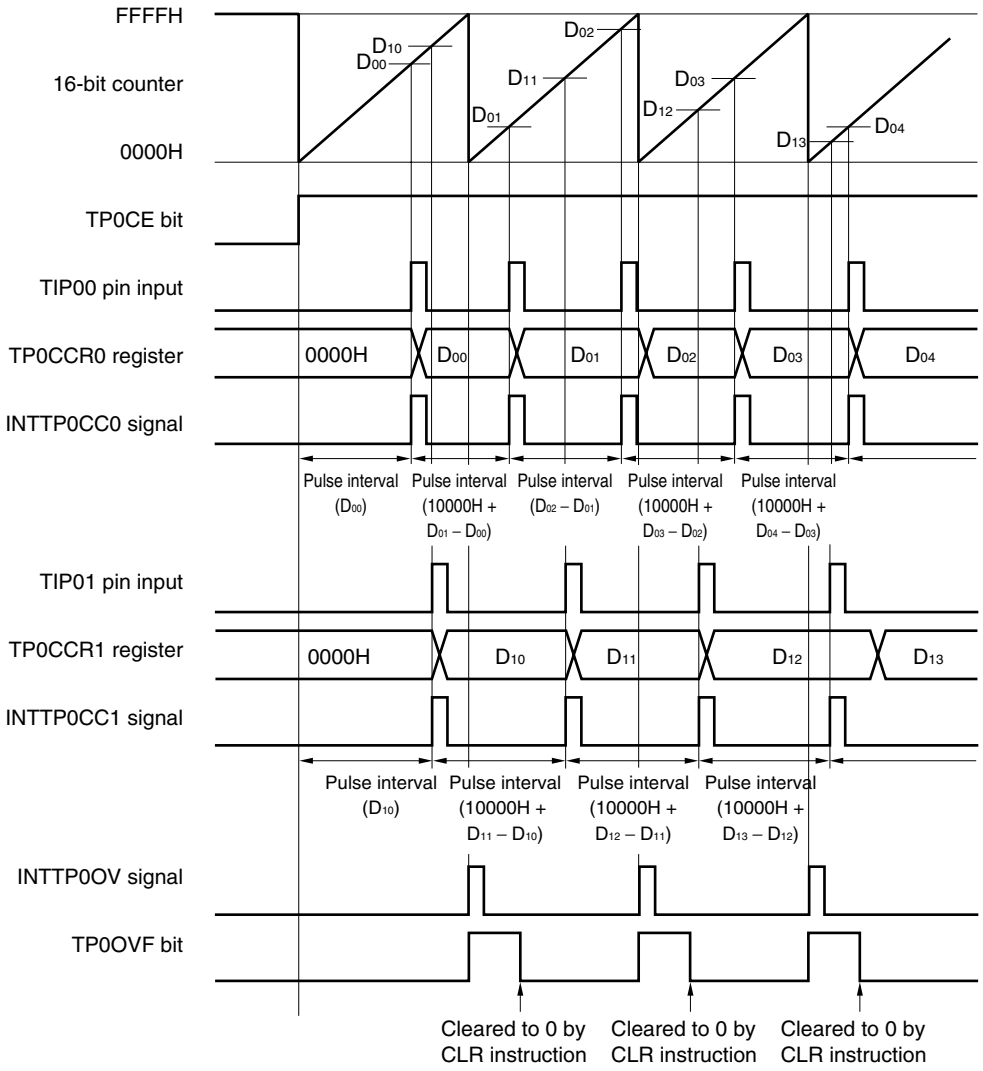
Value set to compare register second and subsequent time: Previous set value + D_a

(If the calculation result is greater than FFFFH, subtract 10000H from the result and set this value to the register.)

Remark a = 0, 1

(b) Pulse width measurement with capture register

When pulse width measurement is performed with the TP0CCRa register used as a capture register, software processing is necessary for reading the capture register each time the INTTP0CCa signal has been detected and for calculating an interval.



When executing pulse width measurement in the free-running timer mode, two pulse widths can be measured with one channel.

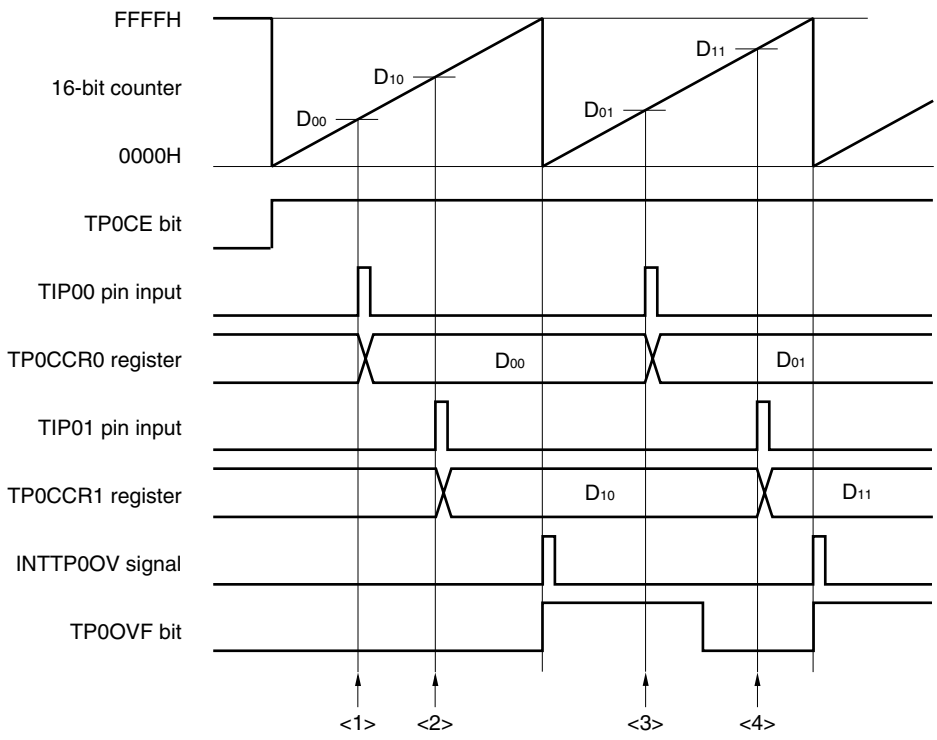
To measure a pulse width, the pulse width can be calculated by reading the value of the TP0CCRa register in synchronization with the INTTP0CCa signal, and calculating the difference between the read value and the previously read value.

Remark a = 0, 1

(c) Processing of overflow when two capture registers are used

Care must be exercised in processing the overflow flag when two capture registers are used. First, an example of incorrect processing is shown below.

Example of incorrect processing when two capture registers are used



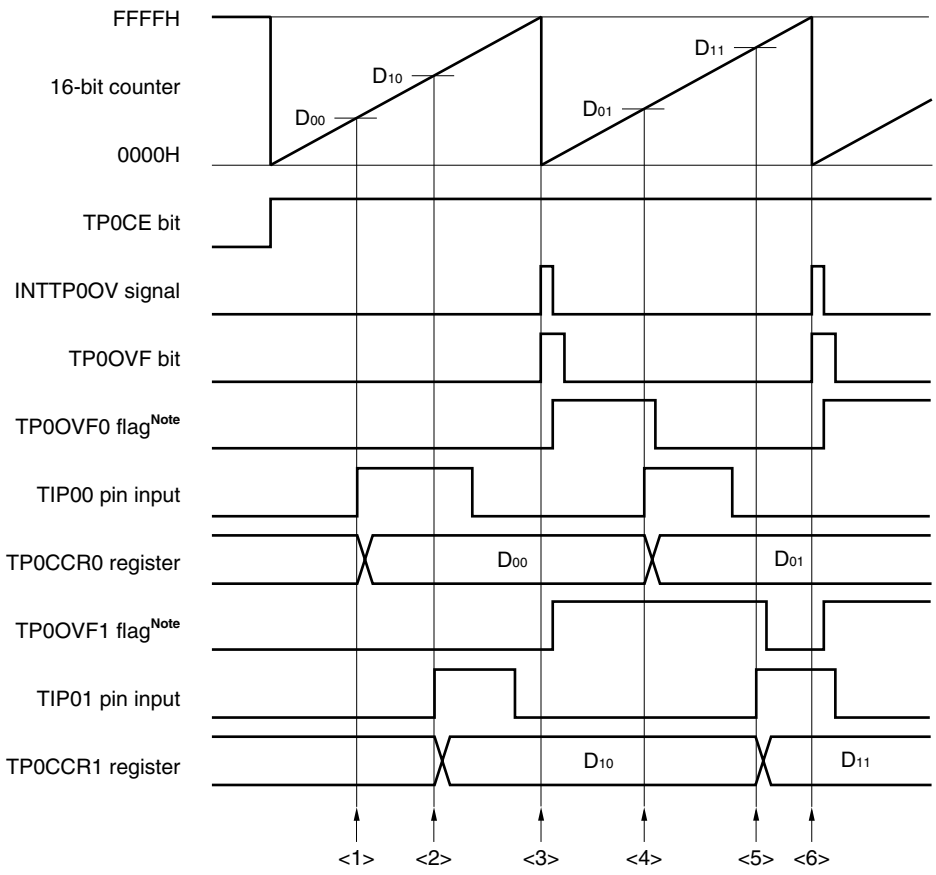
The following problem may occur when two pulse widths are measured in the free-running timer mode.

<1> Read the TP0CCR0 register (setting of the default value of the TIP00 pin input).
<2> Read the TP0CCR1 register (setting of the default value of the TIP01 pin input).
<3> Read the TP0CCR0 register.
Read the overflow flag. If the overflow flag is 1, clear it to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).
<4> Read the TP0CCR1 register.
Read the overflow flag. Because the flag is cleared in <3>, 0 is read.
Because the overflow flag is 0, the pulse width can be calculated by (D_{11} − D_{10}) (incorrect).

When two capture registers are used, and if the overflow flag is cleared to 0 by one capture register, the other capture register may not obtain the correct pulse width.
Use software when using two capture registers. An example of how to use software is shown below.

(1/2)

Example when two capture registers are used (using overflow interrupt)



Note The TP0OVF0 and TP0OVF1 flags are set on the internal RAM by software.

<1> Read the TP0CCR0 register (setting of the default value of the TIP00 pin input).

<2> Read the TP0CCR1 register (setting of the default value of the TIP01 pin input).

<3> An overflow occurs. Set the TP0OVF0 and TP0OVF1 flags to 1 in the overflow interrupt servicing, and clear the overflow flag to 0.

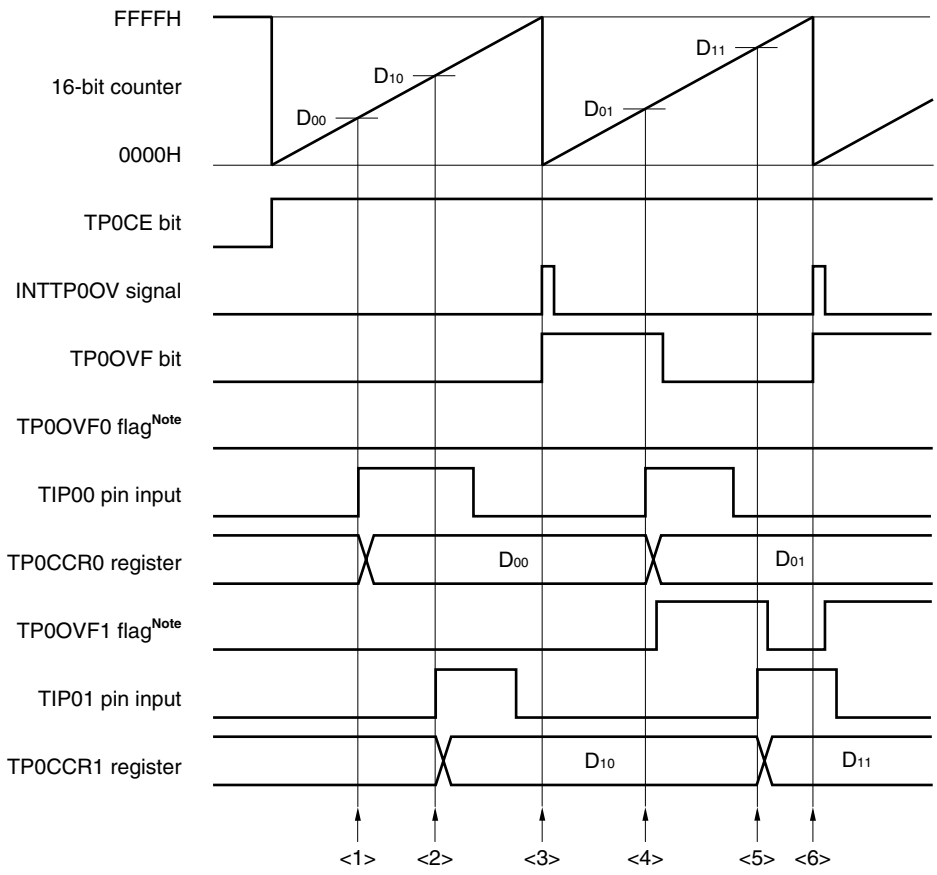
<4> Read the TP0CCR0 register.
Read the TP0OVF0 flag. If the TP0OVF0 flag is 1, clear it to 0.
Because the TP0OVF0 flag is 1, the pulse width can be calculated by (10000H + D_{01} – D_{00}).

<5> Read the TP0CCR1 register.
Read the TP0OVF1 flag. If the TP0OVF1 flag is 1, clear it to 0 (the TP0OVF0 flag is cleared in <4>, and the TP0OVF1 flag remains 1).
Because the TP0OVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} – D_{10}) (correct).

<6> Same as <3>

(2/2)

Example when two capture registers are used (without using overflow interrupt)



Note The TP0OVF0 and TP0OVF1 flags are set on the internal RAM by software.

<1> Read the TP0CCR0 register (setting of the default value of the TIP00 pin input).

<2> Read the TP0CCR1 register (setting of the default value of the TIP01 pin input).

<3> An overflow occurs. Nothing is done by software.

<4> Read the TP0CCR0 register.

Read the overflow flag. If the overflow flag is 1, set only the TP0OVF1 flag to 1, and clear the overflow flag to 0.

Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} – D_{00}).

<5> Read the TP0CCR1 register.

Read the overflow flag. Because the overflow flag is cleared in <4>, 0 is read.

Read the TP0OVF1 flag. If the TP0OVF1 flag is 1, clear it to 0.

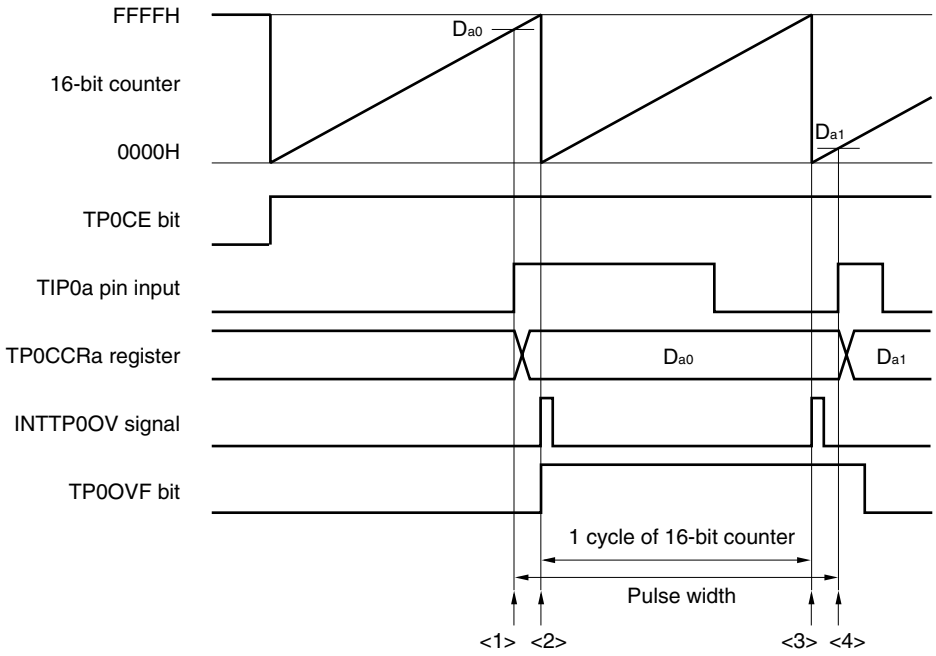
Because the TP0OVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} – D_{10}) (correct).

<6> Same as <3>

(d) Processing of overflow if capture trigger interval is long

If the pulse width is greater than one cycle of the 16-bit counter, care must be exercised because an overflow may occur more than once from the first capture trigger to the next. First, an example of incorrect processing is shown below.

Example of incorrect processing when capture trigger interval is long



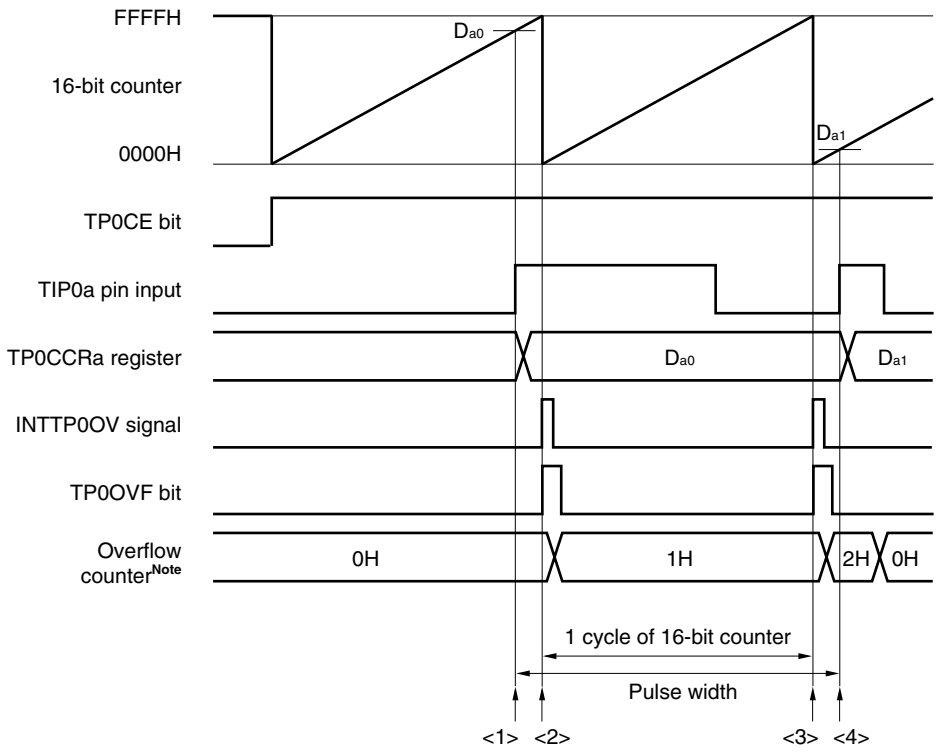
The following problem may occur when long pulse width is measured in the free-running timer mode.

<1> Read the TP0CCRa register (setting of the default value of the TIP0a pin input).
<2> An overflow occurs. Nothing is done by software.
<3> An overflow occurs a second time. Nothing is done by software.
<4> Read the TP0CCRa register.
Read the overflow flag. If the overflow flag is 1, clear it to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{a1} – D_{a0}) (incorrect).
Actually, the pulse width must be (20000H + D_{a1} – D_{a0}) because an overflow occurs twice.

If an overflow occurs twice or more when the capture trigger interval is long, the correct pulse width may not be obtained.

If the capture trigger interval is long, slow the count clock to lengthen one cycle of the 16-bit counter, or use software. An example of how to use software is shown next.

Example when capture trigger interval is long



Note The overflow counter is set arbitrarily by software on the internal RAM.

<1> Read the TP0CCRa register (setting of the default value of the TIP0a pin input).

<2> An overflow occurs. Increment the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

<3> An overflow occurs a second time. Increment (+1) the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

<4> Read the TP0CCRa register.

Read the overflow counter.

→ When the overflow counter is “N”, the pulse width can be calculated by ($N \times 10000H + D_{a1} - D_{a0}$).

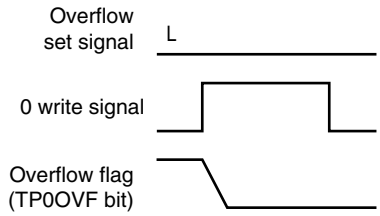
In this example, the pulse width is ($20000H + D_{a1} - D_{a0}$) because an overflow occurs twice.

Clear the overflow counter (0H).

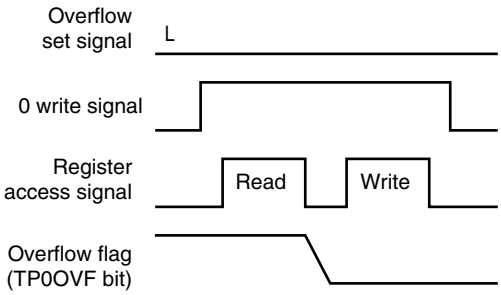
(e) Clearing overflow flag

The overflow flag can be cleared to 0 by clearing the TP0OVF bit to 0 with the CLR instruction and by writing 8-bit data (bit 0 is 0) to the TP0OPT0 register. To accurately detect an overflow, read the TP0OVF bit when it is 1, and then clear the overflow flag by using a bit manipulation instruction.

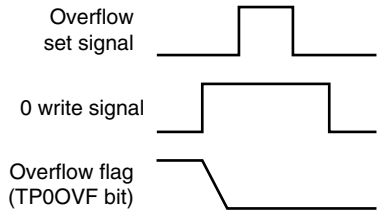
(i) Operation to write 0 (without conflict with setting)



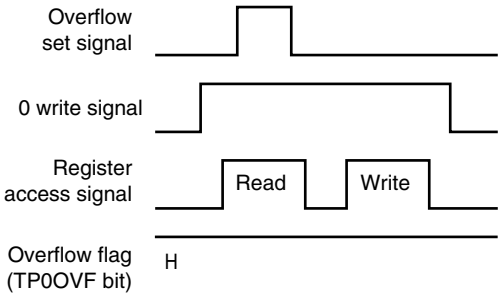
(iii) Operation to clear to 0 (without conflict with setting)



(ii) Operation to write 0 (conflict with setting)



(iv) Operation to clear to 0 (conflict with setting)



To clear the overflow flag to 0, read the overflow flag to check if it is set to 1, and clear it with the CLR instruction. If 0 is written to the overflow flag without checking if the flag is 1, the set information of overflow may be erased by writing 0 ((ii) in the above chart). Therefore, software may judge that no overflow has occurred even when an overflow actually has occurred.

If execution of the CLR instruction conflicts with occurrence of an overflow when the overflow flag is cleared to 0 with the CLR instruction, the overflow flag remains set even after execution of the clear instruction.

7.5.7 Pulse width measurement mode (TP0MD2 to TP0MD0 bits = 110)

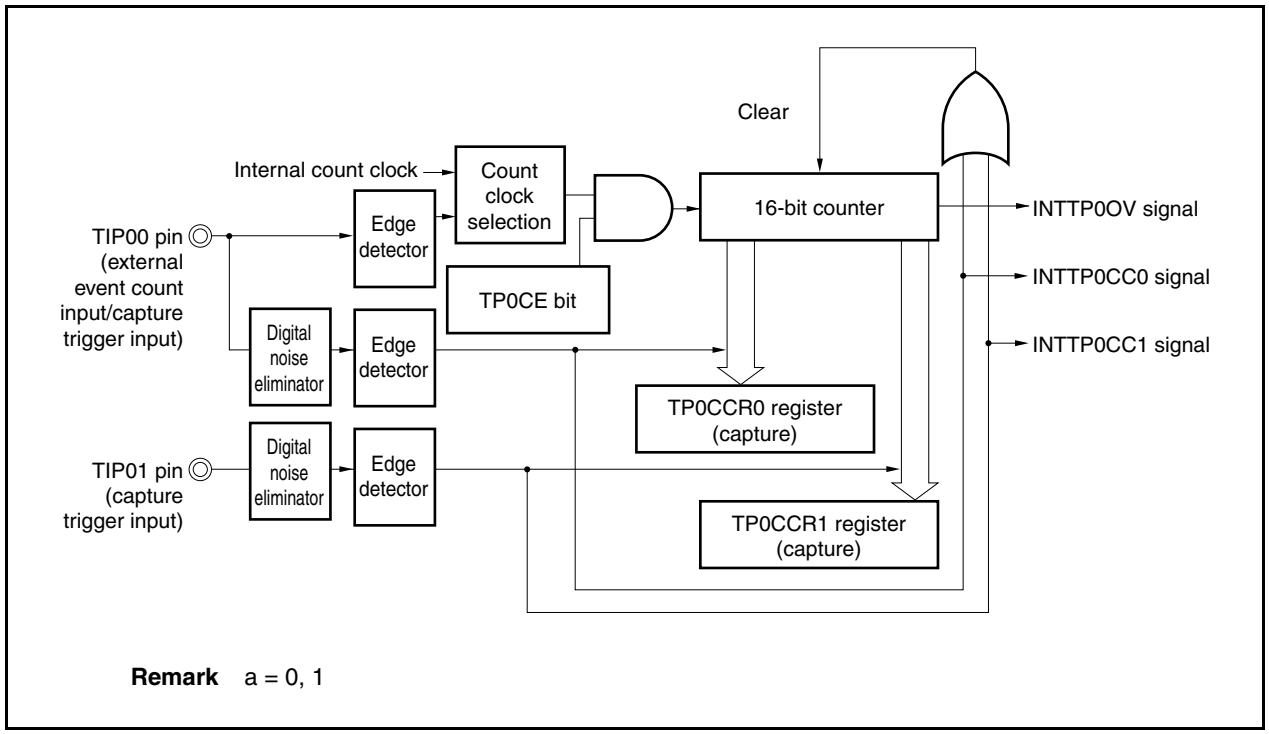
In the pulse width measurement mode, 16-bit timer/event counter P starts counting when the TP0CTL0.TP0CE bit is set to 1. Each time the valid edge input to the TIP0a pin has been detected, the count value of the 16-bit counter is stored in the TP0CCRa register, and the 16-bit counter is cleared to 0000H.

The interval of the valid edge can be measured by reading the TP0CCRa register after a capture interrupt request signal (INTTP0CCa) occurs.

Select either the TIP00 or TIP01 pin as the capture trigger input pin. Specify “No edge detected” by using the TP0IOC1 register for the unused pins.

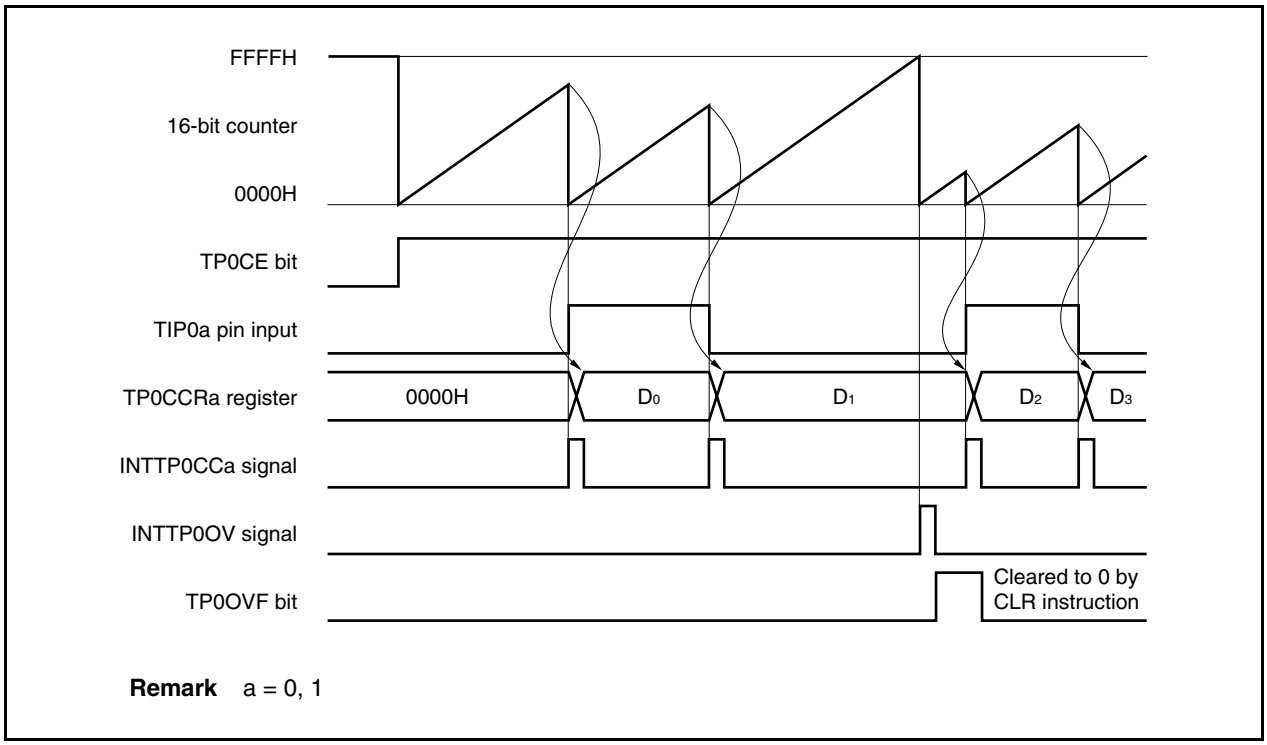
When an external clock is used as the count clock, measure the pulse width of the TIP01 pin because the external clock is fixed to the TIP00 pin. At this time, clear the TP0IOC1.TP0IS1 and TP0IOC1.TP0IS0 bits to 00 (capture trigger input (TIP00 pin): No edge detected).

Figure 7-34. Configuration in Pulse Width Measurement Mode



Remark a = 0, 1

Figure 7-35. Basic Timing in Pulse Width Measurement Mode



Remark a = 0, 1

When the TP0CE bit is set to 1, the 16-bit counter starts counting. When the valid edge input to the TIP0a pin is later detected, the count value of the 16-bit counter is stored in the TP0CCRa register, the 16-bit counter is cleared to 0000H, and a capture interrupt request signal (INTTP0CCa) is generated.

The pulse width is calculated as follows.

Pulse width = Captured value × Count clock cycle

If the valid edge is not input to the TIP0a pin even when the 16-bit counter counted up to FFFFH, an overflow interrupt request signal (INTTP0OV) is generated at the next count clock, and the counter is cleared to 0000H and continues counting. At this time, the overflow flag (TP0OPT0.TP0OVF bit) is also set to 1. Clear the overflow flag to 0 by executing the CLR instruction via software.

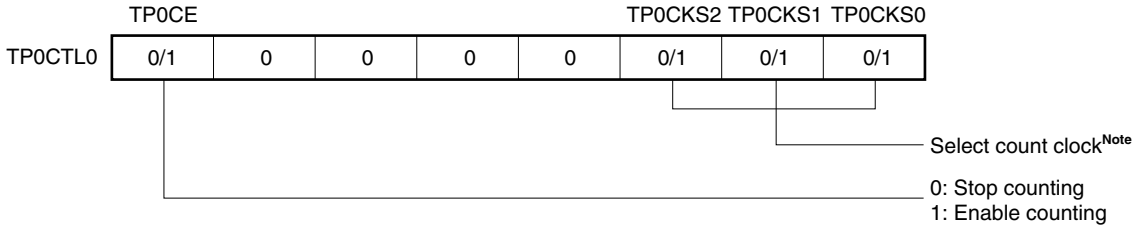
If the overflow flag is set to 1, the pulse width can be calculated as follows.

Pulse width = (10000H × TP0OVF bit set (1) count + Captured value) × Count clock cycle

Remark a = 0, 1

Figure 7-36. Register Setting in Pulse Width Measurement Mode (1/2)

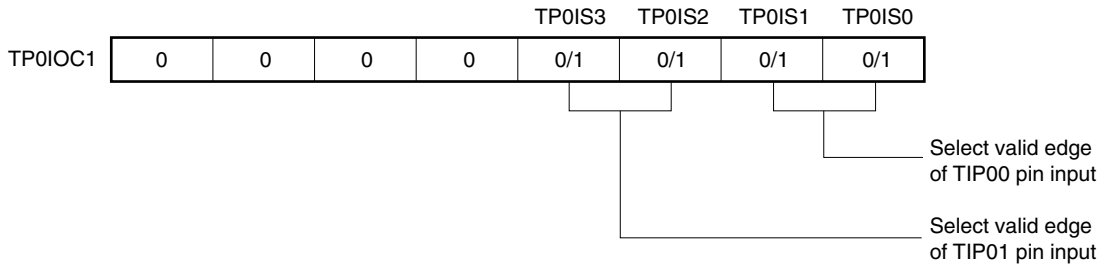
(a) TMP0 control register 0 (TP0CTL0)



Note Setting is invalid when the TP0EEE bit = 1.

(b) TMP0 control register 1 (TP0CTL1)

(c) TMP0 I/O control register 1 (TP0IOC1)



(d) TMP0 I/O control register 2 (TP0IOC2)

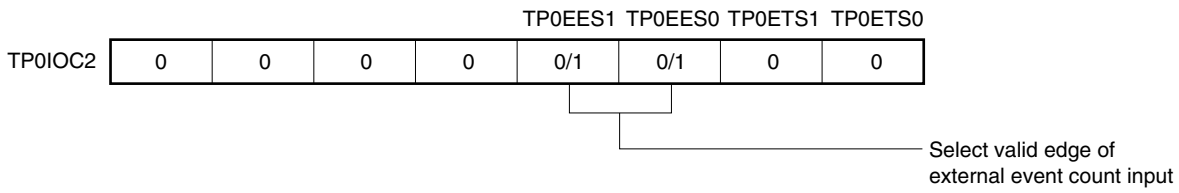


Figure 7-36. Register Setting in Pulse Width Measurement Mode (2/2)

(e) TMP0 option register 0 (TP0OPT0)

			TP0CCS1	TP0CCS0				TP0OVF
TP0OPT0	0	0	0	0	0	0	0	0/1

Overflow flag

(f) TMP0 counter read buffer register (TP0CNT)

The value of the 16-bit counter can be read by reading the TP0CNT register.

(g) TMP0 capture/compare registers 0 and 1 (TP0CCR0 and TP0CCR1)

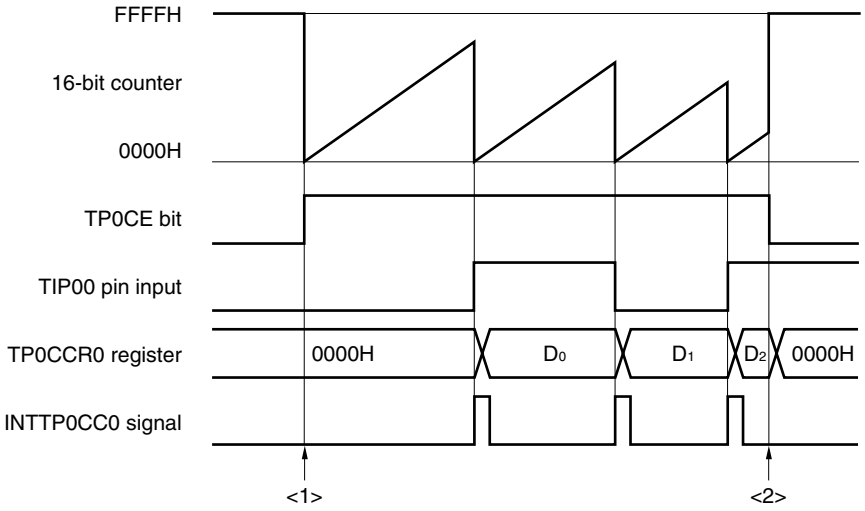
These registers store the count value of the 16-bit counter when the valid edge input to the TIP0a pin is detected.

Remarks 1. TMP0 I/O control register 0 (TP0IOC0) is not used in the pulse width measurement mode.

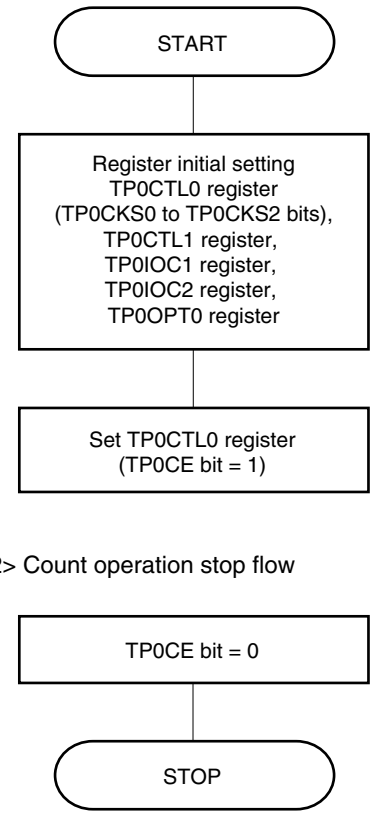
2. a = 0, 1

(1) Operation flow in pulse width measurement mode

Figure 7-37. Software Processing Flow in Pulse Width Measurement Mode



<1> Count operation start flow



Initial setting of these registers is performed before setting the TP0CE bit to 1.

The TP0CKS0 to TP0CKS2 bits can be set at the same time when counting has been started (TP0CE bit = 1).

<2> Count operation stop flow

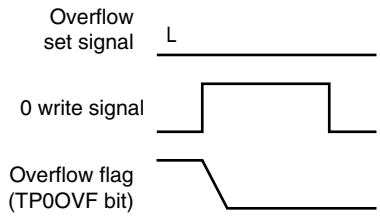
The counter is initialized and counting is stopped by clearing the TP0CE bit to 0.

(2) Operation timing in pulse width measurement mode

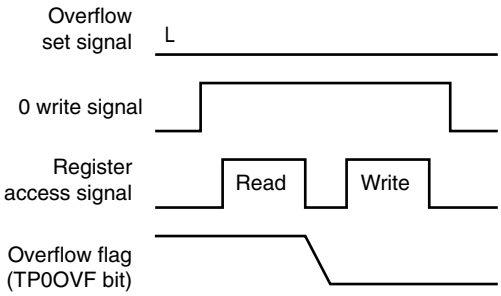
(a) Clearing overflow flag

The overflow flag can be cleared to 0 by clearing the TP0OVF bit to 0 with the CLR instruction and by writing 8-bit data (bit 0 is 0) to the TP0OPT0 register. To accurately detect an overflow, read the TP0OVF bit when it is 1, and then clear the overflow flag by using a bit manipulation instruction.

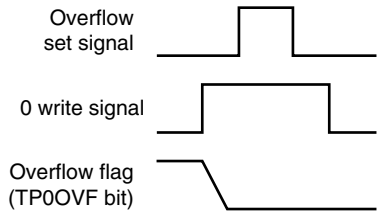
(i) Operation to write 0 (without conflict with setting)



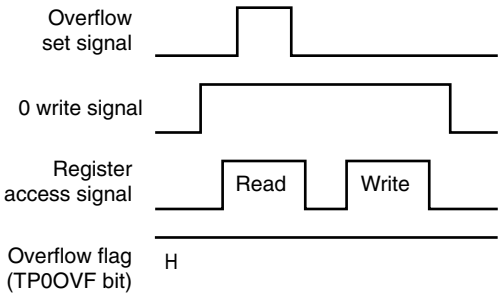
(iii) Operation to clear to 0 (without conflict with setting)



(ii) Operation to write 0 (conflict with setting)



(iv) Operation to clear to 0 (conflict with setting)



To clear the overflow flag to 0, read the overflow flag to check if it is set to 1, and clear it with the CLR instruction. If 0 is written to the overflow flag without checking if the flag is 1, the set information of overflow may be erased by writing 0 ((ii) in the above chart). Therefore, software may judge that no overflow has occurred even when an overflow actually has occurred.

If execution of the CLR instruction conflicts with occurrence of an overflow when the overflow flag is cleared to 0 with the CLR instruction, the overflow flag remains set even after execution of the clear instruction.

7.5.8 Timer output operations

The following table shows the operations and output levels of the TOP00 and TOP01 pins.

Table 7-4. Timer Output Control in Each Mode

Operation Mode	TOP01 Pin	TOP00 Pin
Interval timer mode	Square wave output	
External event count mode	Square wave output	–
External trigger pulse output mode	External trigger pulse output	Square wave output
One-shot pulse output mode	One-shot pulse output	
PWM output mode	PWM output	
Free-running timer mode	Square wave output (only when compare function is used)	
Pulse width measurement mode	–	

Table 7-5. Truth Table of TOP00 and TOP01 Pins Under Control of Timer Output Control Bits

TP0IOC0.TP0OLa Bit	TP0IOC0.TP0OEa Bit	TP0CTL0.TP0CE Bit	Level of TOP0a Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark a = 0, 1

7.6 Eliminating Noise on Capture Trigger Input Pin (TIP0a)

The TIP0a pin has a digital noise eliminator.

However, this circuit is valid only when the pin is used as a capture trigger input pin; it is invalid when the pin is used as an external event count input pin or external trigger input pin.

Digital noise can be eliminated by specifying the alternate function of the TIP0a pin using the PMC3, PFC3, and PFCE3 registers.

The number of times of sampling can be selected from three or two by using the PaNFC.PaNFSTS bit. The sampling clock can be selected from fxx, fxx/2, fxx/4, fxx/16, fxx/32, or fxx/64, by using the PaNFC.PaNFC2 to PaNFC.PaNFC0 bits.

(1) TIP0a noise elimination control register (PaNFC)

This register is used to select the sampling clock and the number of times of sampling for eliminating digital noise.

This register can be read or written in 8-bit or 1-bit units.

Reset input clears this register to 00H.

After reset: 00H R/W Address: P0NFC FFFFFB00H, P1NFC FFFFFB04H

	7	6	5	4	3	2	1	0
PaNFC (a = 0, 1)	0	PaNFSTS	0	0	0	PaNFC2	PaNFC1	PaNFC0

PaNFSTS	Setting of number of times of sampling for eliminating digital noise
0	Number of times of sampling = 3
1	Number of times of sampling = 2

PaNFC2	PaNFC1	PaNFC0	Sampling clock selection
0	0	0	fxx
0	0	1	fxx/2
0	1	0	fxx/4
0	1	1	fxx/16
1	0	0	fxx/32
1	0	1	fxx/64
Other than above			Setting prohibited

Cautions 1. Enable starting the 16-bit counter of TMP0 (TP0CTL.TP0CE bit = 1) after the lapse of the sampling clock period × number of times of sampling.

2. Be sure to clear bits 7, 5 to 3 to "0".

<Setting procedure>

<1> Select the number of times of sampling and the sampling clock by using the PaNFC register.
<2> Select the alternate function (of the TIP0a pin) by using the PMC3, PFC3, and PFCE3 registers.
<3> Set the operating mode of TMP0 (such as the capture mode or the valid edge of the capture trigger).
<4> Enable the TMP0 count operation.

<Noise elimination width>

The digital noise elimination width (t_{WTIPa}) is as follows, where T is the sampling clock period and M is the number of times of sampling.

- $t_{WTIPa} < (M - 1)T$: Accurately eliminated as noise
- $(M - 1)T \leq t_{WTIPa} < MT$: Eliminated as noise or detected as valid edge
- $t_{WTIPa} \geq MT$: Accurately detected as valid edge

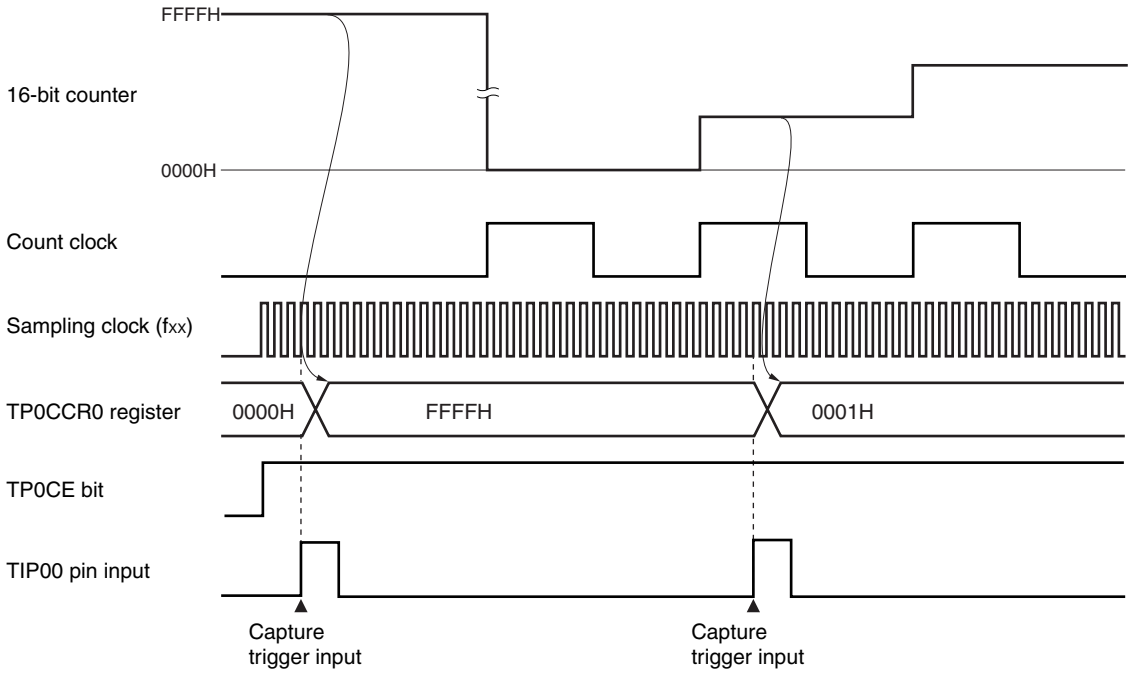
Therefore, a pulse width of MT or longer must be input so that the valid edge of the capture trigger input can be accurately detected.

7.7 Cautions

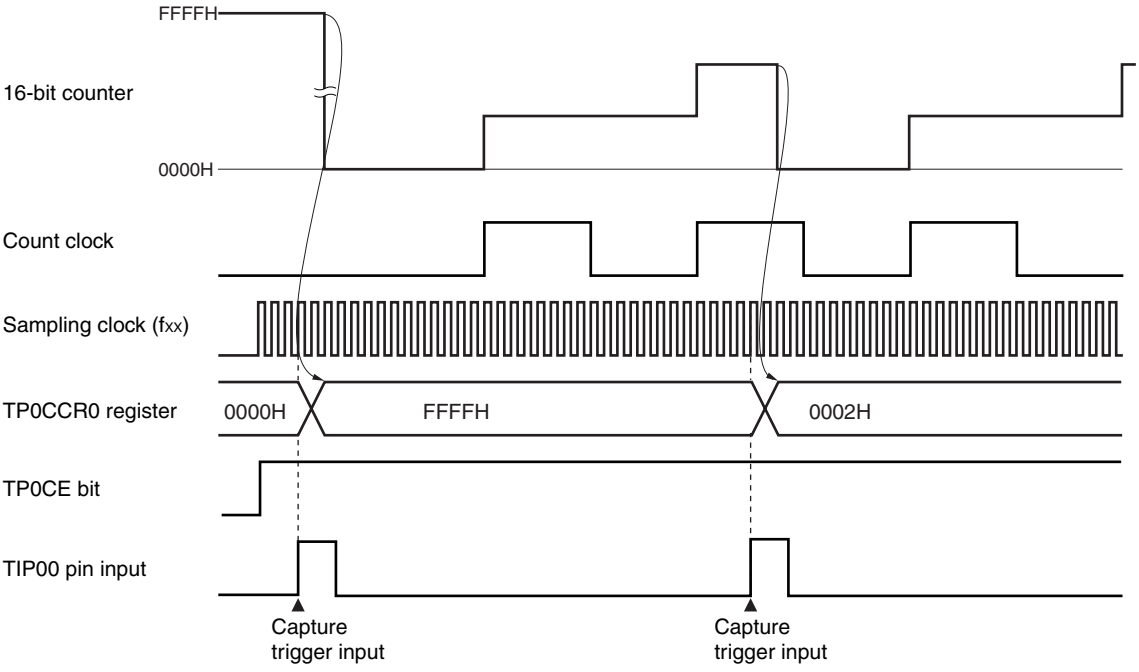
(1) Capture operation

When the capture operation is used and fxx/8, fxx/16, fxx/32, fxx/64, fxx/128, or the external event counter (TP0CLT1.TP0EEE bit = 1) is selected as the count clock, FFFFH, not 0000H, may be captured in the TP0CCRn register if the capture trigger is input immediately after the TP0CE bit is set to 1.

(a) Free-running timer mode



(b) Pulse width measurement mode



CHAPTER 8 16-BIT TIMER/EVENT COUNTER 0

In the V850ES/KG2, four channels of 16-bit timer/event counter 0 are provided.

8.1 Functions

16-bit timer/event counter 0n has the following functions (n = 0 to 3).

(1) Interval timer

16-bit timer/event counter 0n generates an interrupt request at the preset time interval.

(2) Square-wave output

16-bit timer/event counter 0n can output a square wave with any selected frequency.

(3) External event counter

16-bit timer/event counter 0n can measure the number of pulses of an externally input signal.

(4) One-shot pulse output

16-bit timer/event counter 0n can output a one-shot pulse whose output pulse width can be set freely.

(5) PPG output

16-bit timer/event counter 0n can output a rectangular wave whose frequency and output pulse width can be set freely.

(6) Pulse width measurement

16-bit timer/event counter 0n can measure the pulse width of an externally input signal.

8.2 Configuration

16-bit timer/event counter 0n includes the following hardware.

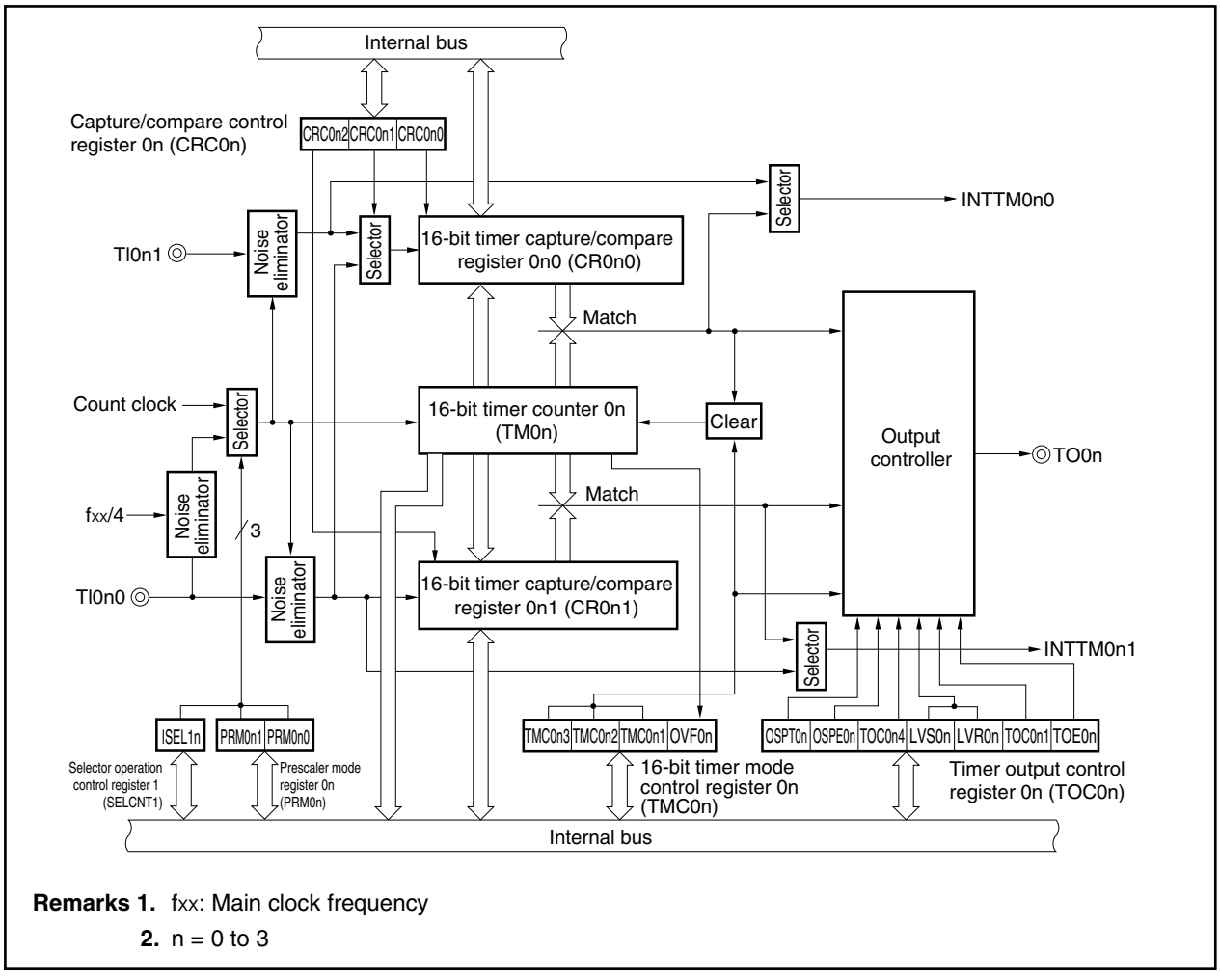
Table 8-1. Configuration of 16-Bit Timer/Event Counter 0n

Item	Configuration
Time/counter	16-bit timer counter 0n (TM0n)
Register	16-bit timer capture/compare registers: 16-bit × 2 (CR0n0, CR0n1)
Timer input	2 (TI0n0, TI0n1 pins)
Timer output	1 (TO0n pin), output controller
Control registers[Note]	16-bit timer mode control register 0n (TMC0n) Capture/compare control register 0n (CRC0n) 16-bit timer output control register 0n (TOC0n) Prescaler mode register 0n (PRM0n) Selector operation control register 1 (SELCNT1)

Note To use the TI0n0, TI0n1, and TO0n pin functions, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

The block diagram is shown below.

Figure 8-1. Block Diagram of 16-Bit Timer/Event Counter 0n



Remarks 1. fxx: Main clock frequency

2. n = 0 to 3

(1) 16-bit timer counter 0n (TM0n)

The TM0n register is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

After reset: 0000H R Address: TM00 FFFFF600H, TM01 FFFFF610H, TM02 FFFFF620H, TM03 FFFFF630H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM0n																

(n = 0 to 3)

The count value of the TM0n register can be read by reading the TM0n register when the values of the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are other than 00. The value of the TM0n register is 0000H if it is read when the TMC0n3 and TMC0n2 bits are 00.

The count value is reset to 0000H in the following cases.

- At reset signal generation
- If the TMC0n3 and TMC0n2 bits are cleared to 00
- If the valid edge of the TI0n0 pin is input in the mode in which the clear & start occurs when inputting the valid edge to the TI0n0 pin
- If the TM0n register and the CR0n0 register match in the mode in which the clear & start occurs when the TM0n register and the CR0n0 register match
- The TOC0n.OSPT0n bit is set to 1 in one-shot pulse output mode or the valid edge is input to the TI0n0 pin

Remark n = 0 to 3

(2) 16-bit timer capture/compare register 0n0 (CR0n0), 16-bit timer capture/compare register 0n1 (CR0n1)

The CR0n0 and CR0n1 registers are 16-bit registers that are used with a capture function or comparison function selected by using the CRC0n register.

Change of the value of the CR0n0 register while the timer is operating (TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = other than 00) is prohibited.

The value of the CR0n1 register can be changed during operation if the value has been set in a specific way. For details, see **8.5.1 Rewriting CR0n0 register during TM0n operation**.

These registers can be read or written in 16-bit units.

Reset sets these registers to 0000H.

(a) 16-bit timer capture/compare register 0n0 (CR0n0)

After reset: 0000H R/W Address: CR000 FFFFF602H, CR010 FFFFF612H, CR020 FFFFF622H, CR030 FFFFF632H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR0n0																

(n = 0 to 3)

(i) When the CR0n0 register is used as a compare register

The value set in the CR0n0 register is constantly compared with the TM0n register count value, and an interrupt request signal (INTTM0n0) is generated if they match. The value is held until the CR0n0 register is rewritten.

(ii) When the CR0n0 register is used as a capture register

The count value of the TM0n register is captured to the CR0n0 register when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI0n0 pin or the valid edge of the TI0n1 pin can be selected by using the CRC0n or PRM0n register.

(b) 16-bit timer capture/compare register 0n1 (CR0n1)

After reset: 0000H R/W Address: CR001 FFFFF604H, CR011 FFFFF614H, CR021 FFFFF624H, CR031 FFFFF634H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR0n1																

(n = 0 to 3)

(i) When using the CR0n1 register as a compare register

The value set to the CR0n1 register and the count value of the TM0n register are always compared and when these values match, an interrupt request signal (INTTM0n1) is generated.

(ii) When using the CR0n1 register as a capture register

The TM0n register count value is captured to the CR0n1 register by inputting a capture trigger.

The valid edge of the TI0n0 pin can be selected as the capture trigger. The valid edge of the TI0n0 pin is set with the PRM0n register.

Cautions 1. When the P33, P35, P92, and P94 pins are used as the valid edges of TI000, TI010, TI020, and TI030, and the timer output function is used, set the P34, P32, P30, and P31 pins as the timer output pins (TO00 to TO03).

2. If clearing of the TMC0n3 and TMC0n2 bits to 00 and input of the capture trigger conflict, then the captured data is undefined.

3. To change the mode from the capture mode to the comparison mode, first clear the TMC0n3 and TMC0n2 bits to 00, and then change the setting.

A value that has been once captured remains stored in the CR0n0 and CR0n1 registers unless the device is reset. If the mode has been changed to the comparison mode, be sure to set a comparison value.

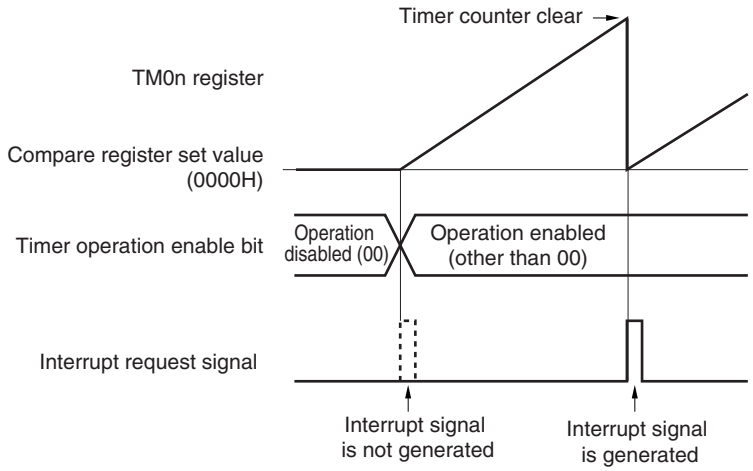
(c) Setting range when used as compare register

When the CR0n0 or CR0n1 register is used as a compare register, set it as shown below.

Operation	CR0n0 Register	CR0n1 Register
• Operation as interval timer • Operation as square-wave output • Operation as external event counter	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM0n1).
• Operation in the clear & start mode entered by TI0n0 pin valid edge input • Operation as free-running timer	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
• Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M ≤ N
• Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM0n register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI0n0 pin valid edge (when clear & start mode is entered by TI0n0 pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM0n and CR0n0 (CR0n0 = other than 0000H, CR0n1 = 0000H))



Remarks 1. N: CR0n0 register set value
M: CR0n1 register set value

2. For details of operation enable bits (TMC0n.TMC0n3, TMC0n.TMC0n2 bits), refer to **8.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

Table 8-2. Capture Operation of CR0n0 and CR0n1 Registers

External Input Signal / Capture Operation	TI0n0 Pin Input		TI0n1 Pin Input	
Capture operation of CR0n0 register	CRC0n1 bit = 1 TI0n0 pin input (reverse phase)	Set values of ESn01 and ESn00 Position of edge to be captured	CRC0n1 bit = 0 TI0n1 pin input	Set values of ESn11 and ESn10 Position of edge to be captured
		01: Rising		01: Rising
		00: Falling		00: Falling
		11: Both edges (cannot be captured)		11: Both edges
	Interrupt signal	INTTM0n0 signal is not generated even if value is captured.	Interrupt signal	INTTM0n0 signal is generated each time value is captured.
Capture operation of CR0n1 register	TI0n0 pin input[Note]	Set values of ESn01 and ESn00 Position of edge to be captured		
		01: Rising		
		00: Falling		
		11: Both edges		
	Interrupt signal	INTTM0n1 signal is generated each time value is captured.		

Note The capture operation of the CR0n1 register is not affected by the setting of the CRC0n1 bit.

Caution To capture the count value of the TM0n register to the CR0n0 register by using the phase reverse to that input to the TI0n0 pin, the interrupt request signal (INTTM0n0) is not generated after the value has been captured. If the valid edge is detected on the TI0n1 pin during this operation, the capture operation is not performed but the INTTM0n0 signal is generated as an external interrupt signal. To not use the external interrupt, mask the INTTM0n0 signal.

Remarks 1. CRC0n1: See **8.3 (2) Capture/compare control register 0n (CRC0n)**.
ESn11, ESn10, ESn01, ESn00: See **8.3 (4) Prescaler mode register 0n (PRM0n)**.

2. n = 0 to 3

8.3 Registers

Registers used to control 16-bit timer/event counter 0n are shown below.

- 16-bit timer mode control register 0n (TMC0n)
- Capture/compare control register 0n (CRC0n)
- 16-bit timer output control register 0n (TOC0n)
- Prescaler mode register 0n (PRM0n)
- Selector operation control register 1 (SELCNT1)

Remark To use the TI0n0, TI0n1, and TO0n pin functions, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

(1) 16-bit timer mode control register 0n (TMC0n)

TMC0n is an 8-bit register that sets the 16-bit timer/event counter 0n operation mode, the TM0n register clear mode, and output timing, and detects an overflow.

Rewriting TMC0n is prohibited during operation (when the TMC0n3 and TMC0n2 bits = other than 00). However, it can be changed when the TMC0n3 and TMC0n2 bits are cleared to 00 (stopping operation) and when the OVF0n bit is cleared to 0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Cautions 1. 16-bit timer/event counter 0n starts operation at the moment TMC0n2 and TMC0n3 are set to values other than 00 (operation stop mode), respectively. Set TMC0n2 and TMC0n3 to 00 to stop the operation.

2. Do not access the TMC0n register when the main clock is stopped and the subclock is operating.
For details, refer to 3.4.8 (1) (b).

Remark n = 0 to 3

After reset: 00H R/W Address: TMC00 FFFFF606H, TMC01 FFFFF616H, TMC02 FFFFF626H
TMC03 FFFFF636H

	7	6	5	4	3	2	1	<0>
TMC0n	0	0	0	0	TMC0n3	TMC0n2	TMC0n1	OVF0n

(n = 0 to 3)

TMC0n3	TMC0n2	Enable operation of 16-bit timer/event counter 0n
0	0	Disables TM0n operation. Stops supplying operating clock. Clears 16-bit timer counter (TM0n).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI0n0 pin valid edge input[Note 1]
1	1	Clear & start mode entered upon a match between TM0n and CR0n0

TMC0n1[Note 2]	Condition to reverse timer output (TO0n)
0	• Match between TM0n and CR0n0 or match between TM0n and CR0n1
1	• Match between TM0n and CR0n0 or match between TM0n and CR0n1 • Trigger input of TI0n0 pin valid edge

OVF0n	TM0n register overflow flag
Clear (0)	Clears OVF0n to 0 or TMC0n.TMC0n3 and TMC0n.TMC0n2 = 00
Set (1)	Overflow occurs.
OVF0n is set to 1 when the value of TM0n changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI0n0 pin valid edge input, and clear & start mode entered upon a match between TM0n and CR0n0). It can also be set to 1 by writing 1 to the OVF0n bit.	

Notes 1. The TI0n0 pin valid edge is set by the PRM0n register.

2. Be sure to clear the TMC0m1 bit to 0 when the TO0m pin and TI0m0 pin are used alternately (m = 0 to 3).

(2) Capture/compare control register 0n (CRC0n)

The CRC0n register is the register that controls the operation of the CR0n0 and CR0n1 registers.

Changing the value of the CRC0n register is prohibited during operation (when the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = other than 00).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: CRC00 FFFFF608H, CRC01 FFFFF618H, CRC02 FFFFF628H CRC03 FFFFF638H

	7	6	5	4	3	2	1	0
CRC0n	0	0	0	0	0	CRC0n2	CRC0n1	CRC0n0

(n = 0 to 3)

CRC0n2	CR0n1 register operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC0n1	CR0n0 register capture trigger selection
0	Captures on valid edge of TI0n1 pin
1	Captures on valid edge of TI0n0 pin by reverse phase[Note]
The valid edge of the TI0n1 and TI0n0 pin is set by the PRM0n register. If PRM0n.ESn01 and PRM0n.ESn00 are set to 11 (both edges) when CRC0n1 is 1, the valid edge of the TI0n0 pin cannot be detected.	

CRC0n0	CR0n0 register operating mode selection
0	Operates as compare register
1	Operates as capture register
If TMC0n3 and TMC0n2 are set to 11 (clear & start mode entered upon a match between TM0n and CR0n0), be sure to set the CRC0n0 bit to 0.	

Note When the valid edge is detected from the TI0n1 pin, the capture operation is not performed but the INTTM0n0 signal is generated as an external interrupt signal.

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by the PRM0n or SELCNT1 register.

(3) 16-bit timer output control register 0n (TOC0n)

The TOC0n register is an 8-bit register that controls the TO0n pin output.

The TOC0n register can be rewritten while only the OSPT0n bit is operating (when the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = other than 00). Rewriting the other bits is prohibited during operation.

However, TOC0n4 can be rewritten during timer operation as a means to rewrite the CR0n1 register (see **8.5.1 Rewriting CR0n1 register during TM0n operation**).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Caution Be sure to set the TOC0n register using the following procedure.

<1> Set the TOC0n4 and TOC0n1 bits to 1.

<2> Set only the TOE0n bit to 1.

<3> Set either the LVS0n bit or LVR0n bit to 1.

(1/2)

After reset: 00H R/W Address: TOC00 FFFFF609H, TOC01 FFFFF619H, TOC02 FFFFF629H, TOC03 FFFFF639H

TOC0n (n = 0 to 3)

7	<6>	<5>	4	<3>	<2>	1	<0>
0	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n

OSPT0n	One-shot pulse output trigger via software
0	–
1	One-shot pulse output
The value of this bit is always “0” when it is read. If it is set to 1, TM0n is cleared and started.	

OSPE0n	One-shot pulse output operation control
0	Successive pulse output
1	One-shot pulse output
One-shot pulse output operates correctly in the free-running timer mode or clear & start mode entered by TI0n0 pin valid edge input. The one-shot pulse cannot be output in the clear & start mode entered upon a match between the TM0n and CR0n0 registers.	

TOC0n4	TO0n pin output control on match between CR0n1 and TM0n registers
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM0n1) is generated even when the TOC0n4 bit = 0.	

(2/2)

LVS0n	LVR0n	Setting of TO0n pin output status
0	0	No change
0	1	Initial value of TO0n pin output is low level (TO0n pin output is cleared to 0).
1	0	Initial value of TO0n pin output is high level (TO0n pin output is set to 1).
1	1	Setting prohibited

- The LVS0n and LVR0n bits can be used to set the initial value of the output level of the TO0n pin. If the initial value does not have to be set, leave the LVS0n and LVR0n bits as 00n.
- Be sure to set the LVS0n and LVR0n bits when TOE0n = 1.
  The LVS0n, LVR0n, and TOE0n bits being simultaneously set to 1 is prohibited.
- The LVS0n and LVR0n bits are trigger bits. By setting these bits to 1, the initial value of the output level of the TO0n pin can be set. Even if these bits are cleared to 0, output of the TO0n pin is not affected.
- The values of the LVS0n and LVR0n bits are always 0 when they are read.
- For how to set the LVS0n and LVR0n bits, see **8.5.2 Setting LVS0n and LVR0n bits**.

TOC0n1	TO0n pin output control on match between CR0n0 and TM0n registers
0	Disables inversion operation
1	Enables inversion operation

The interrupt signal (INTTM0n0) is generated even when the TOC0n1 bit = 0.

TOE0n	TO0n pin output control
0	Disables output (TO0n pin output fixed to low level)
1	Enables output

(4) Prescaler mode register 0n (PRM0n)

The PRM0n register is the register that sets the TM0n register count clock and TI0n0 and TI0n1 pin input valid edges. The PRM0n1 and PRM0n0 bits are set in combination with the SELCNT1.ISEL1n bit. Refer to **8.3 (6) Count clock setting for 16-bit timer/event counter 0n** for details.

Rewriting the PRM0n register is prohibited during operation (when the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = other than 00).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Cautions 1. Do not apply the following setting when setting the PRM0n1 and PRM0n0 bits to 11 (to specify the valid edge of the TI0n0 pin as a count clock).

- **Clear & start mode entered by the TI0n0 pin valid edge**
- **Setting the TI0n0 pin as a capture trigger**

2. If the operation of the 16-bit timer/event counter 0n is enabled when the TI0n0 or TI0n1 pin is at high level and when the valid edge of the TI0n0 or TI0n1 pin is specified to be the rising edge or both edges, the high level of the TI0n0 or TI0n1 pin is detected as a rising edge. Note this when the TI0n0 or TI0n1 pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and is then enabled again.

3. When the P33, P35, P92, and P94 pins are used as the valid edges of TI000, TI010, TI020, and TI030, and the timer output function is used, set the P34, P32, P30, and P31 pins as the timer output pins (TO00 to TO03).

After reset: 00H R/W Address: PRM00 FFFFF607H, PRM01 FFFFF617H, PRM02 FFFFF627H, PRM03 FFFFF637H

PRM0n (n = 0 to 3)

7	6	5	4	3	2	1	0
ESn11	ESn10	ESn01	ESn00	0	0	PRM0n1	PRM0n0

ESn11	ESn10	TI0n1 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ESn01	ESn00	TI0n0 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

(5) Selector operation control register 1 (SELCNT1)

The SELCNT1 register sets the count clock of 16-bit timer/event counter 0n.

The SELCNT1 register is set in combination with the PRM0n.PRMn01 and PRM0n.PRMn00 bits. Refer to **8.3 (6) Count clock setting for 16-bit timer/event counter 0n** for details.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF30AH

	7	6	5	4	3	2	1	0
SELCNT1	0	0	0	0	ISEL13	ISEL12	ISEL11	ISEL10

(6) Count clock setting for 16-bit timer/event counter 0n

The count clock for 16-bit timer/event counter 0n is set by using the PRM0n.PRM0n1, PRM0n.PRM0n0, and SELCNT1.ISEL1n bits in combination.

(a) Count clock for 16-bit timer/event counters 00 and 02

SELCNT1 Register	PRM0n Register		Selection of Count Clock[Note 1]			
ISEL1n Bit	PRM0n1 Bit	PRM0n0 Bit	Count Clock	f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
0	0	0	$f_{XX}/2$	100 ns	125 ns	200 ns
0	0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	0	$f_{XX}/8$	400 ns	500 ns	800 ns
0	1	1	Valid edge of TI0n0[Note 2]	–	–	–
1	0	0	$f_{XX}/32$	1.6 μs	2.0 μs	3.2 μs
1	0	1	$f_{XX}/64$	3.2 μs	4.0 μs	6.4 μs
1	1	0	$f_{XX}/128$	6.4 μs	8.0 μs	12.8 μs
1	1	1	Setting prohibited			

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions:

V_{DD} = REGC = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 4.0 to 5.5 V, REGC = 10 μF: Count clock ≤ 5 MHz

V_{DD} = REGC = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark n = 0 or 2

(b) Count clock for 16-bit timer/event counter 01

SELCNT1 Register	PRM01 Register		Selection of Count Clock[Note 1]			
ISEL11 Bit	PRM011 Bit	PRM010 Bit	Count Clock	f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
0	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	0	INTWT	–	–	–
0	1	1	Valid edge of TI010[Note 2]	–	–	–
1	0	0	$f_{XX}/2$	100 ns	125 ns	200 ns
1	0	1	$f_{XX}/8$	400 ns	500 ns	800 ns
1	1	0	$f_{XX}/16$	800 ns	1.0 μs	1.6 μs
1	1	1	Setting prohibited			

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions:

V_{DD} = REGC = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 4.0 to 5.5 V, REGC = 10 μF: Count clock ≤ 5 MHz

V_{DD} = REGC = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

(c) Count clock for 16-bit timer/event counter 03

SELCNT1 Register	PRM03 Register		Selection of Count Clock[Note 1]			
ISEL13 Bit	PRM031 Bit	PRM030 Bit	Count Clock	f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
0	0	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	0	1	$f_{XX}/16$	800 ns	1.0 μs	1.6 μs
0	1	0	$f_{XX}/512$	25.6 μs	32.0 μs	51.2 μs
0	1	1	Valid edge of TI030[Note 2]	–	–	–
1	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
1	0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
1	1	0	$f_{XX}/8$	400 ns	500 ns	800 ns
1	1	1	Setting prohibited			

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions:

V_{DD} = REGC = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 4.0 to 5.5 V, REGC = 10 μF: Count clock ≤ 5 MHz

V_{DD} = REGC = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

8.4 Operation

8.4.1 Interval timer operation

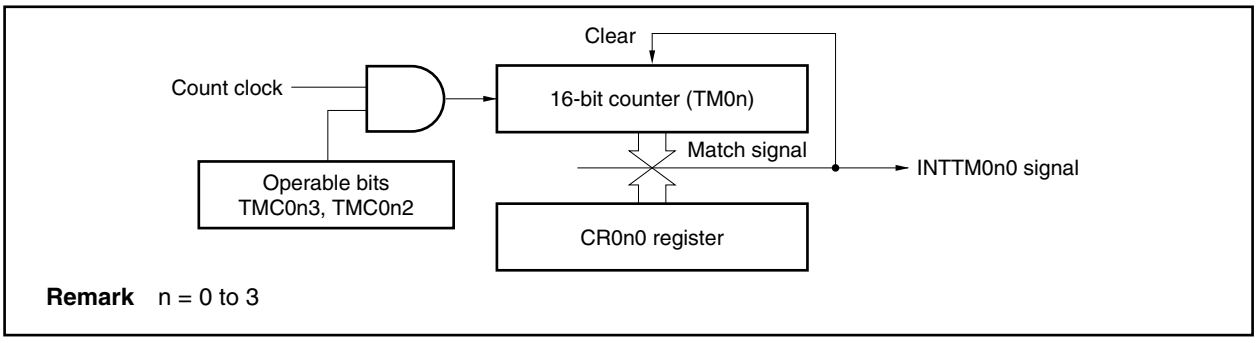
If the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 11 (clear & start mode entered upon a match between the TM0n register and the CR0n0 register), the count operation is started in synchronization with the count clock.

When the value of the TM0n register later matches the value of the CR0n0 register, the TM0n register is cleared to 0000H and a match interrupt signal (INTTM0n0) is generated. This INTTM0n0 signal enables the TM0n register to operate as an interval timer.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

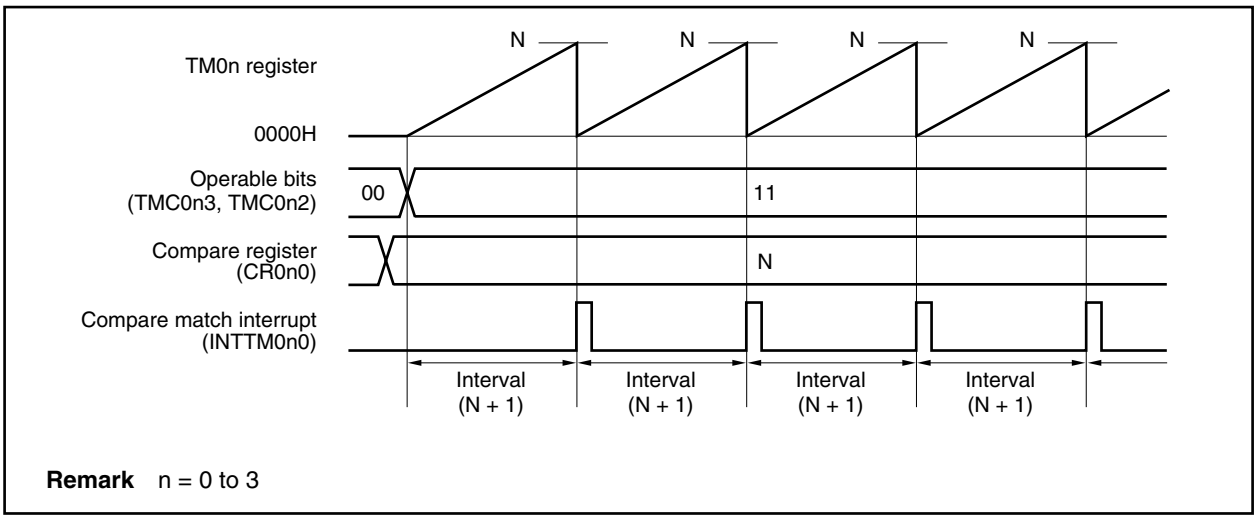
2. For enabling the INTTM0n0 interrupt, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

Figure 8-2. Block Diagram of Interval Timer Operation



Remark n = 0 to 3

Figure 8-3. Basic Timing Example of Interval Timer Operation



Remark n = 0 to 3

Figure 8-4. Example of Register Settings for Interval Timer Operation

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	1	0	0

Clears and starts on match between TM0n and CR0n0.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR0n0 used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)

	ESn11	ESn10	ESn01	ESn00			PRM0n1	PRM0n0		ISEL1n
PRM0n	0	0	0	0	0	0	0/1	0/1	SELCNT1	0/1

Selects count clock.

(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

If M is set to the CR0n0 register, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

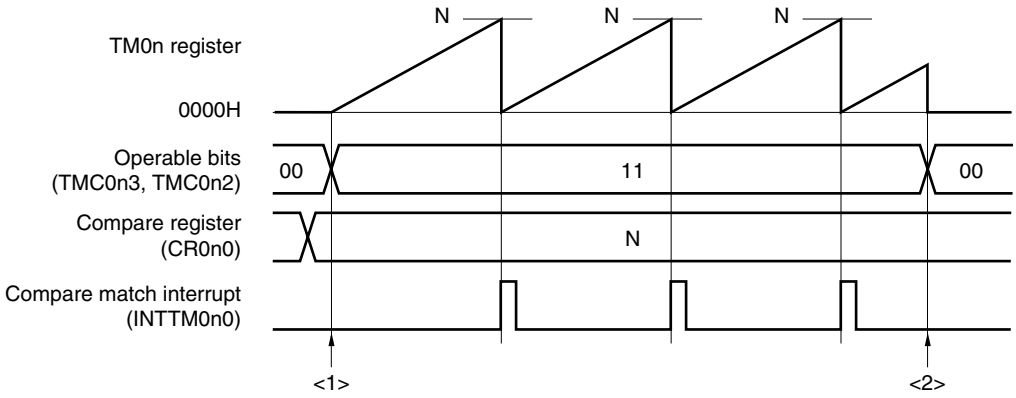
Setting the CR0n0 register to 0000H is prohibited.

(g) 16-bit capture/compare register 0n1 (CR0n1)

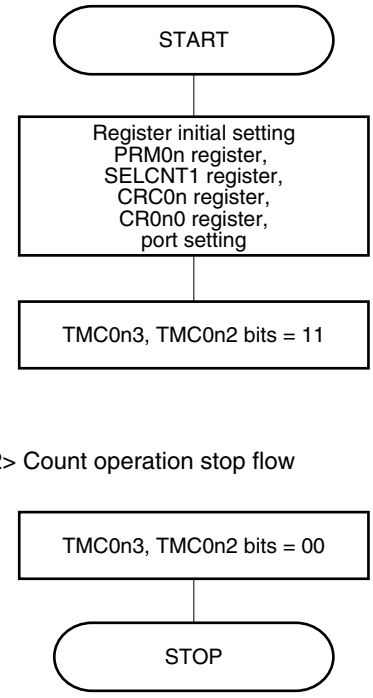
Usually, the CR0n1 register is not used for the interval timer function. However, a compare match interrupt (INTTM0n1) is generated when the set value of the CR0n1 register matches the value of the TM0n register. Therefore, mask the interrupt request by using the interrupt mask flag (TM0MKn1).

Remark n = 0 to 3

Figure 8-5. Example of Software Processing for Interval Timer Function



<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC0n3 and TMC0n2 bits to 11.

Starts count operation

<2> Count operation stop flow

The counter is initialized and counting is stopped by clearing the TMC0n3 and TMC0n2 bits to 00.

Remark n = 0 to 3

8.4.2 Square wave output operation

When 16-bit timer/event counter 0n operates as an interval timer (see **8.4.1**), a square wave can be output from the TO0n pin by setting the TOC0n register to 03H.

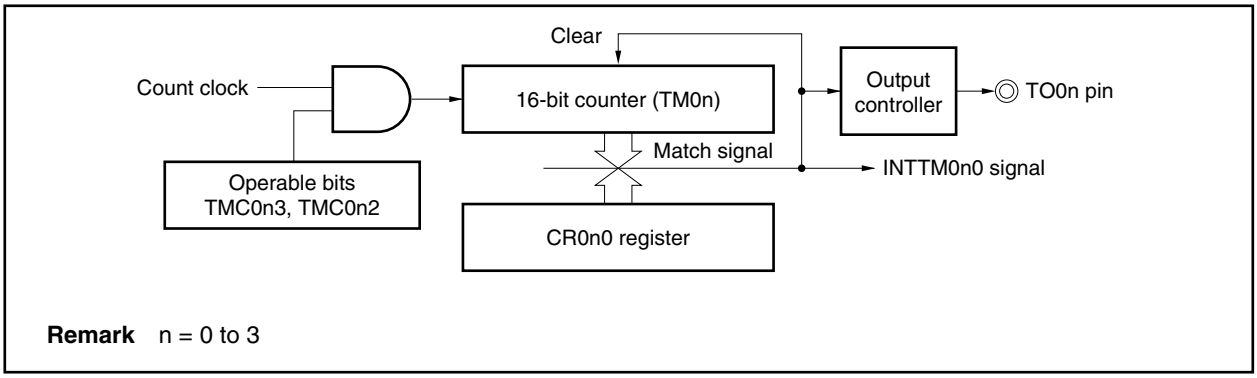
When the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 11 (count clear & start mode entered upon a match between the TM0n register and the CR0n0 register), the counting operation is started in synchronization with the count clock.

When the value of the TM0n register later matches the value of the CR0n0 register, the TM0n register is cleared to 0000H, an interrupt signal (INTTM0n0) is generated, and output of the TO0n pin is inverted. This TO0n pin output that is inverted at fixed intervals enables TO0n to output a square wave.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

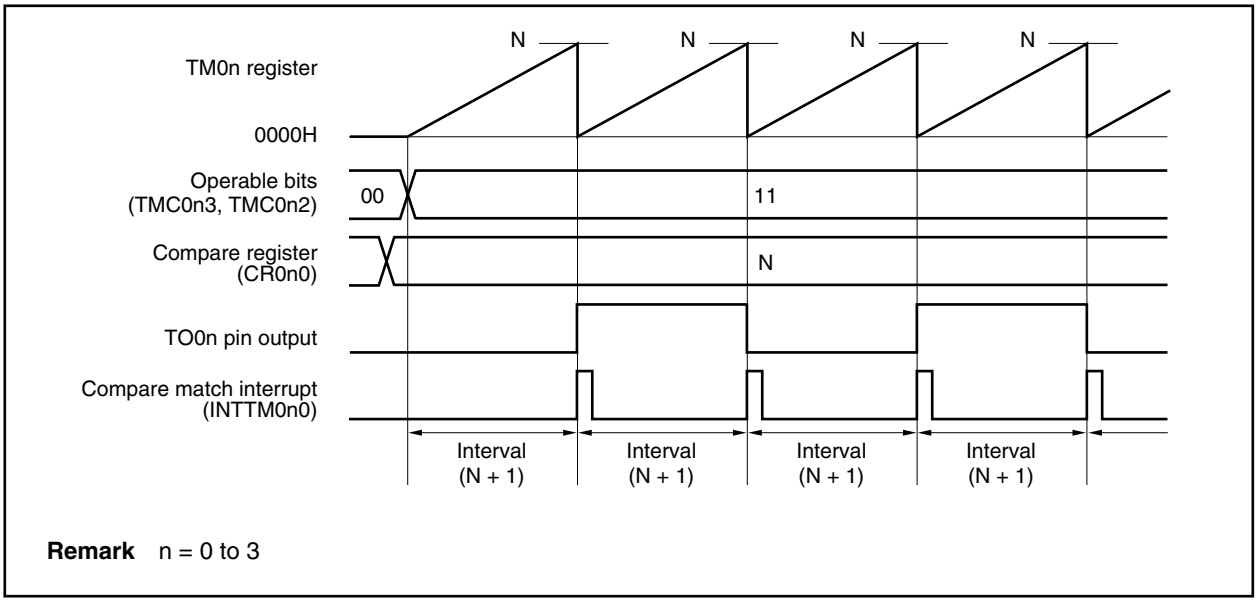
2. For enabling the INTTM0n0 interrupt, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

Figure 8-6. Block Diagram of Square Wave Output Operation



Remark n = 0 to 3

Figure 8-7. Basic Timing Example of Square Wave Output Operation



Remark n = 0 to 3

Figure 8-8. Example of Register Settings for Square Wave Output Operation

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	1	0	0

Clears and starts on match between TM0n and CR0n0.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR0n0 used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0/1	0/1	1	1

Enables TO0n pin output.

Inverts TO0n pin output on match between TM0n and CR0n0.

Specifies the initial value of TO0n output F/F.

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)

	ESn11	ESn10	ESn01	ESn00			PRM0n1	PRM0n0		ISEL1n
PRM0n	0	0	0	0	0	0	0/1	0/1	SELCNT1	0/1

Selects count clock.

(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

If M is set to the CR0n0 register, the square wave frequency is as follows.

$1 / [2 \times (M + 1) \times \text{Count clock cycle}]$

Setting the CR0n0 register to 0000H is prohibited.

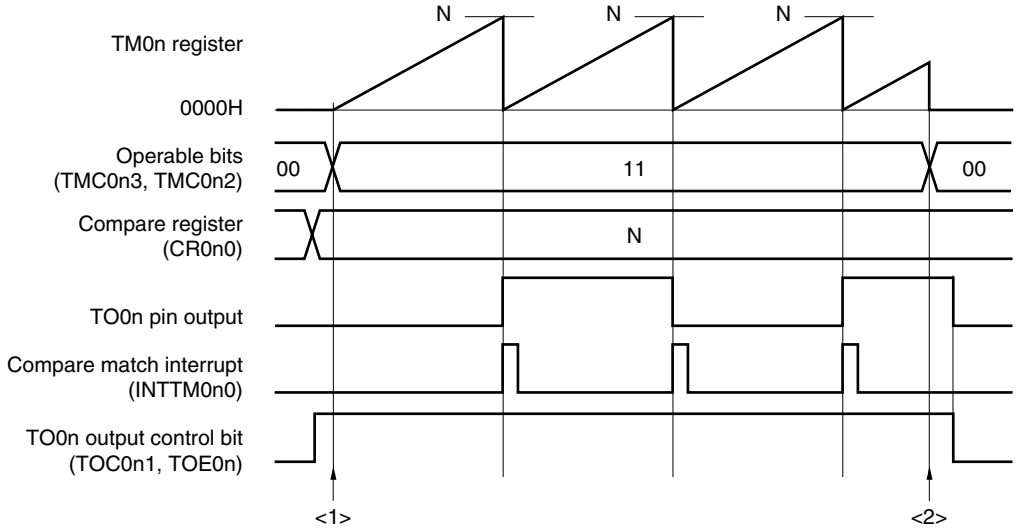
(g) 16-bit capture/compare register 0n1 (CR0n1)

Usually, the CR0n1 register is not used for the square wave output function. However, a compare match interrupt (INTTM0n1) is generated when the set value of the CR0n1 register matches the value of the TM0n register.

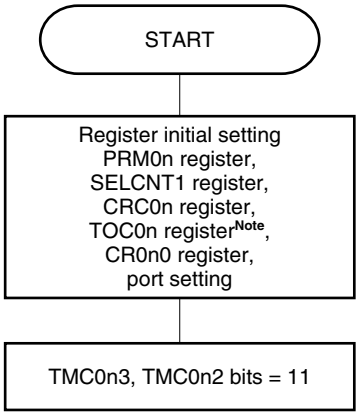
Therefore, mask the interrupt request by using the interrupt mask flag (TM0MKn1).

Remark n = 0 to 3

Figure 8-9. Example of Software Processing for Square Wave Output Function



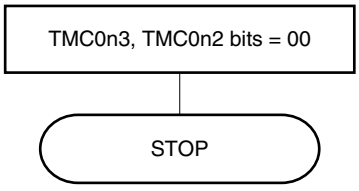
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC0n3 and TMC0n2 bits to 11.

Starts count operation.

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC0n3 and TMC0n2 bits to 00.

Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0 to 3

8.4.3 External event counter operation

When the PRM0n.PRM0n1 and PRM0n.PRM0n0 bits are set to 11 (for counting up with the valid edge of the TI0n0 pin) and the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 11, the valid edge of an external event input is counted, and a match interrupt signal indicating matching between the TM0n register and the CR0n0 register (INTTM0n0) is generated.

To input the external event, the TI0n0 pin is used. Therefore, the timer/event counter cannot be used as an external event counter in the clear & start mode entered by the TI0n0 pin valid edge input (when the TMC0n3 and TMC0n2 bits = 10).

The INTTM0n0 signal is generated with the following timing.

- Timing of generation of INTTM0n0 signal (second time or later)
  = Number of times of detection of valid edge of external event × (Set value of the CR0n0 register + 1)

However, the first match interrupt immediately after the timer/event counter has started operating is generated with the following timing.

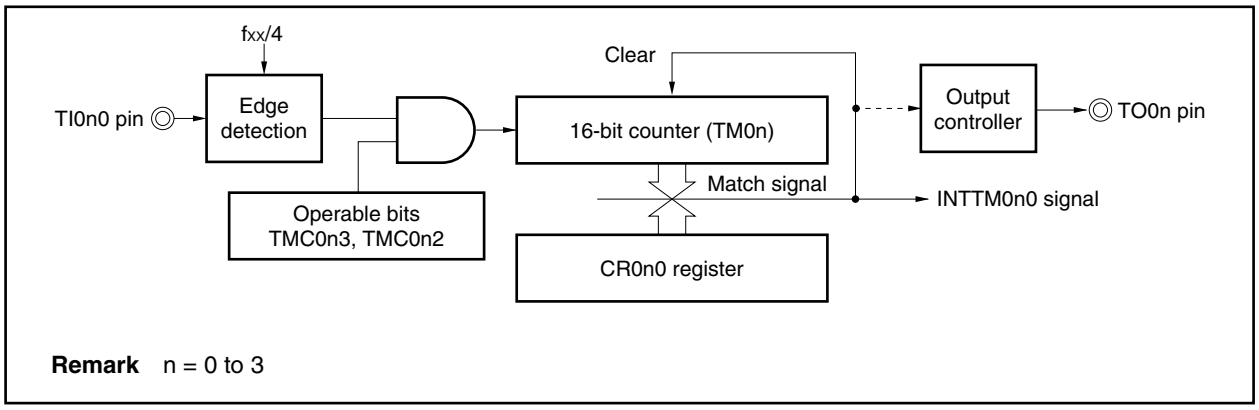
- Number of times of detection of valid edge of external event input × (Set value of the CR0n0 register + 2)

To detect the valid edge, the signal input to the TI0n0 pin is sampled during the clock cycle of f_{PRS}. The valid edge is not detected until it is detected two times in a row. Therefore, a noise with a short pulse width can be eliminated.

Remarks 1. For the alternate-function pin (TI0n0) settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For enabling the INTTM0n0 interrupt, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

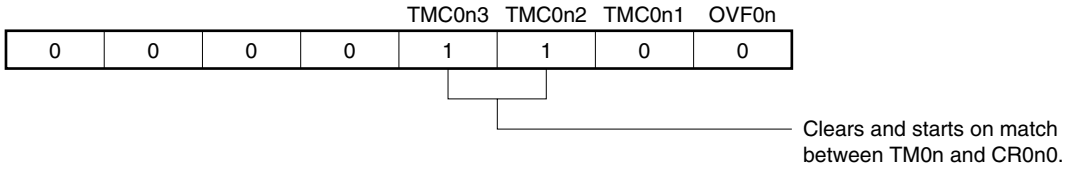
Figure 8-10. Block Diagram of External Event Counter Operation



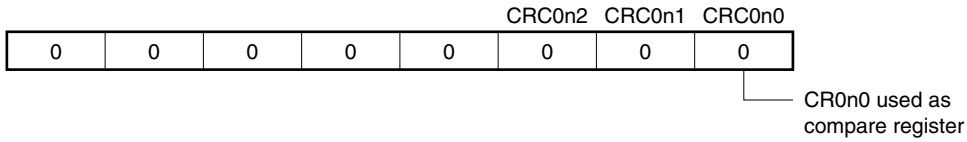
Remark n = 0 to 3

Figure 8-11. Example of Register Settings in External Event Counter Mode

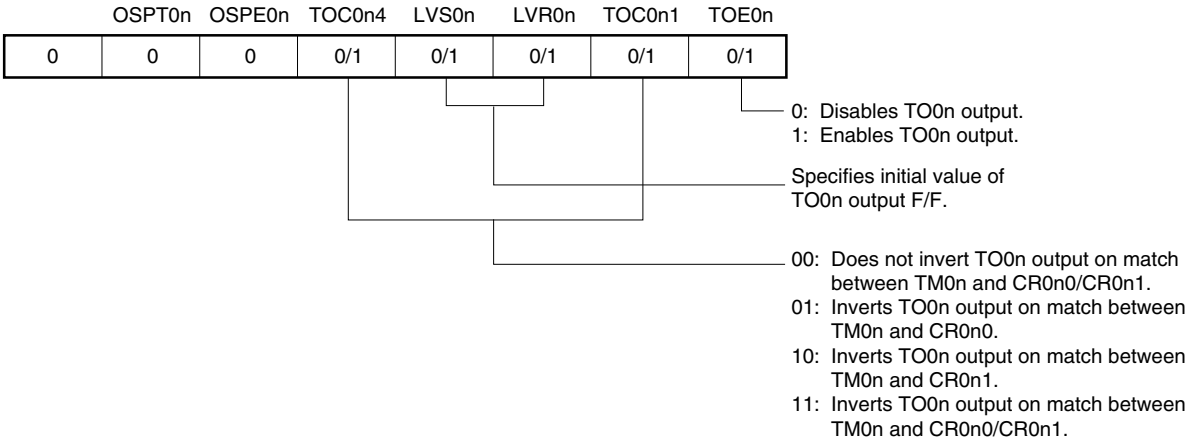
(a) 16-bit timer mode control register 0n (TMC0n)



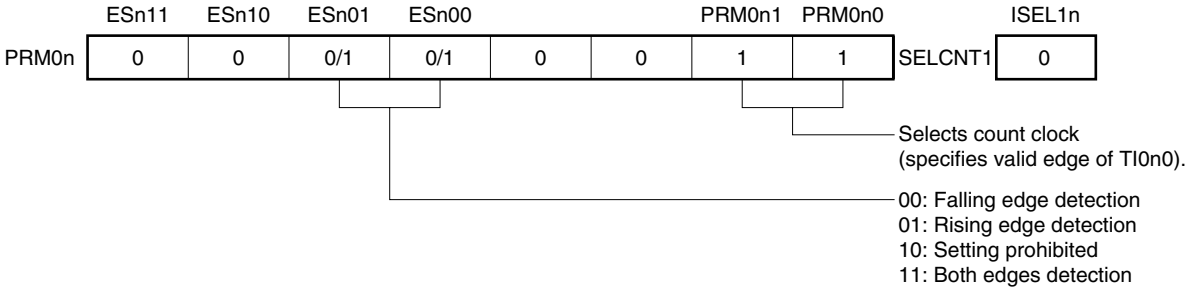
(b) Capture/compare control register 0n (CRC0n)



(c) 16-bit timer output control register 0n (TOC0n)



(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)



(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

If M is set to the CR0n0 register, the interrupt signal (INTTM0n0) is generated when the number of external events reaches (M + 1).

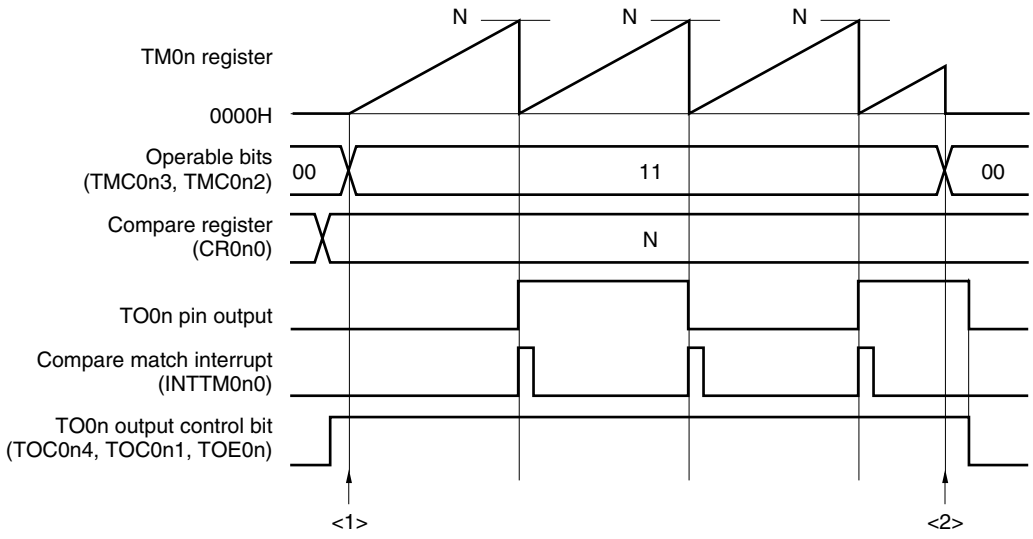
Setting the CR0n0 register to 0000H is prohibited.

(g) 16-bit capture/compare register 0n1 (CR0n1)

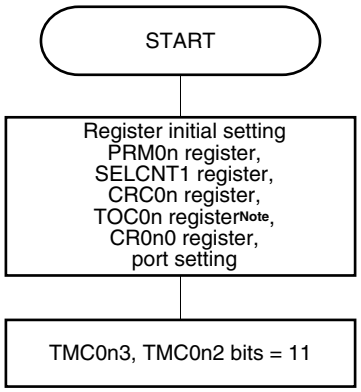
When this register's value matches the count value of the TM0n register, an interrupt signal (INTTM0n1) is generated. The count value of the TM0n register is not cleared.

Remark n = 0 to 3

Figure 8-12. Example of Software Processing in External Event Counter Mode



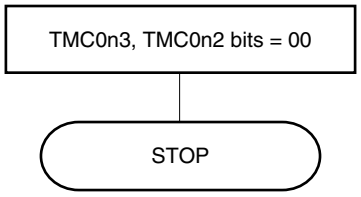
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC0n3 and TMC0n2 bits to 11.

Starts count operation.

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC0n3 and TMC0n2 bits to 00.

Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0 to 3

8.4.4 Operation in clear & start mode entered by TI0n0 pin valid edge input

When the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 10 (clear & start mode entered by the TI0n0 pin valid edge input) and the count clock (set by the PRM0n, SELCNT1 registers) is supplied to the timer/event counter, the TM0n register starts counting up. When the valid edge of the TI0n0 pin is detected during the counting operation, the TM0n register is cleared to 0000H and starts counting up again. If the valid edge of the TI0n0 pin is not detected, the TM0n register overflows and continues counting.

The valid edge of the TI0n0 pin is a cause to clear the TM0n register. Starting the counter is not controlled immediately after the start of the operation.

The CR0n0 and CR0n1 registers are used as compare registers and capture registers.

(a) When the CR0n0 and CR0n1 registers are used as compare registers

Signals INTTM0n0 and INTTM0n1 are generated when the value of the TM0n register matches the value of the CR0n0 and CR0n1 registers.

(b) When the CR0n0 and CR0n1 registers are used as capture registers

The count value of the TM0n register is captured to the CR0n0 register and the INTTM0n0 signal is generated when the valid edge is input to the TI0n1 pin (or when the phase reverse to that of the valid edge is input to the TI0n0 pin).

When the valid edge is input to the TI0n0 pin, the count value of the TM0n register is captured to the CR0n1 register and the INTTM0n1 signal is generated. As soon as the count value has been captured, the counter is cleared to 0000H.

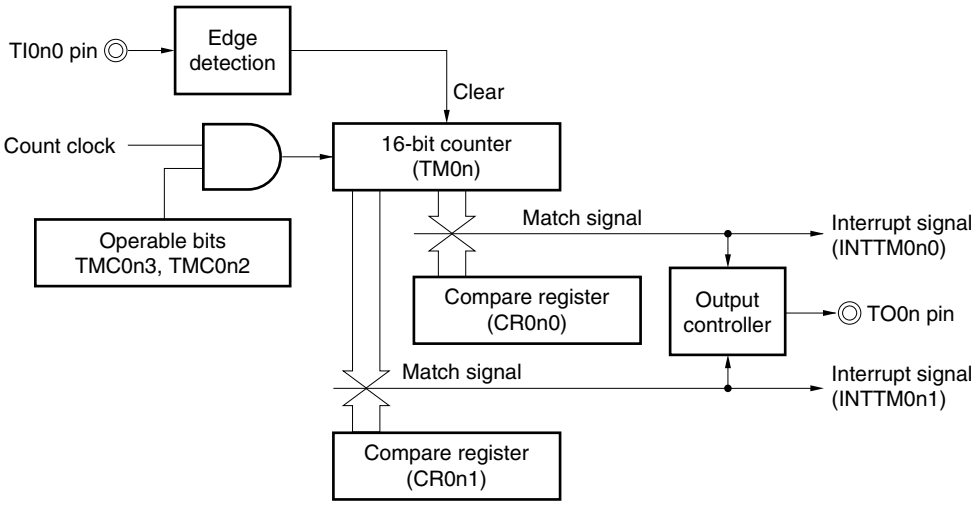
Caution Do not set the count clock as the valid edge of the TI0n0 pin (RPM0n.PRM0n1 and RPM0n.PRM0n0 bits = 11). When the PRM0n1 and PRM0n0 bits = 11, the TM0n register is cleared.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For enabling the INTTM0n0 interrupt, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

(1) Operation in clear & start mode entered by TI0n0 pin valid edge input (CR0n0 register: compare register, CR0n1 register: compare register)

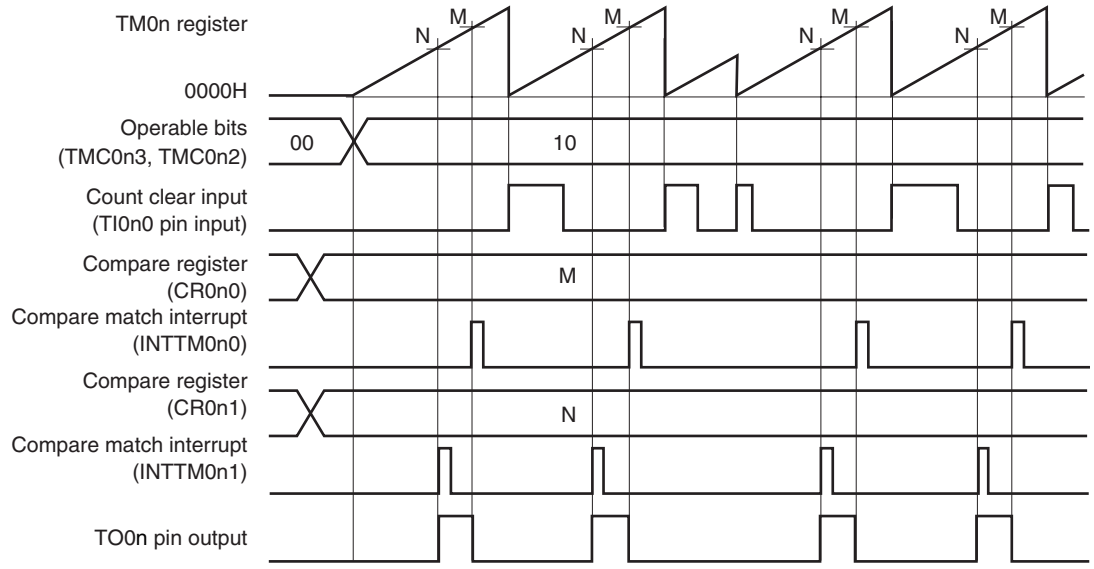
Figure 8-13. Block Diagram of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 register: Compare Register, CR0n1 register: Compare Register)



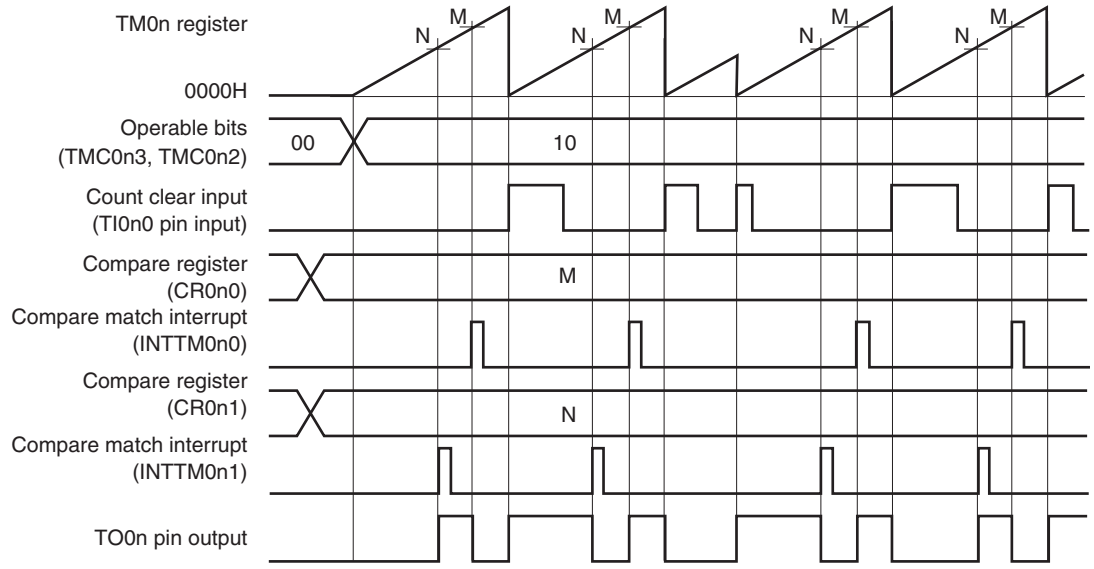
Remark n = 0 to 3

Figure 8-14. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Compare Register, CR0n1 Register: Compare Register)

(a) TOC0n = 13H, PRM0n = 10H, CRC0n = 00H, TMC0n = 08H



(b) TOC0n = 13H, PRM0n = 10H, CRC0n, = 00H, TMC0n = 0AH



(a) and (b) differ as follows depending on the setting of the TMC0n register (TMC0n1 bit).

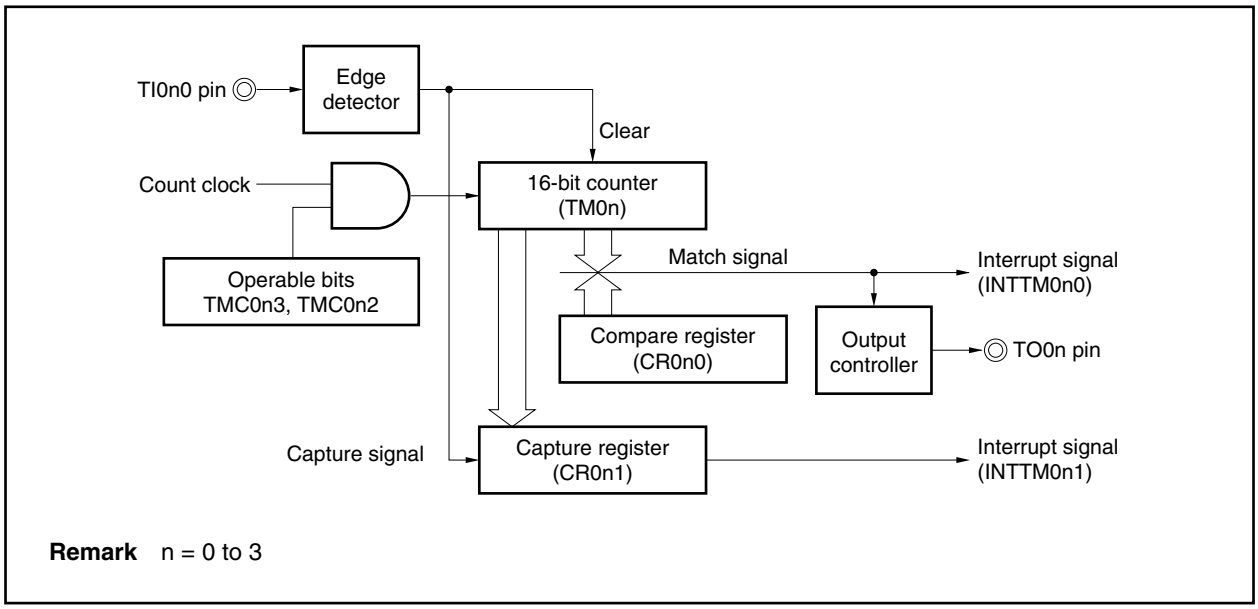
(a) The output level of the TO0n pin is inverted when the TM0n register matches a compare register.

(b) The output level of the TO0n pin is inverted when the TM0n register matches a compare register or when the valid edge of the TI0n0 pin is detected.

Remark n = 0 to 3

(2) Operation in clear & start mode entered by TI0n0 pin valid edge input (CR0n0 register: compare register, CR0n1 register: capture register)

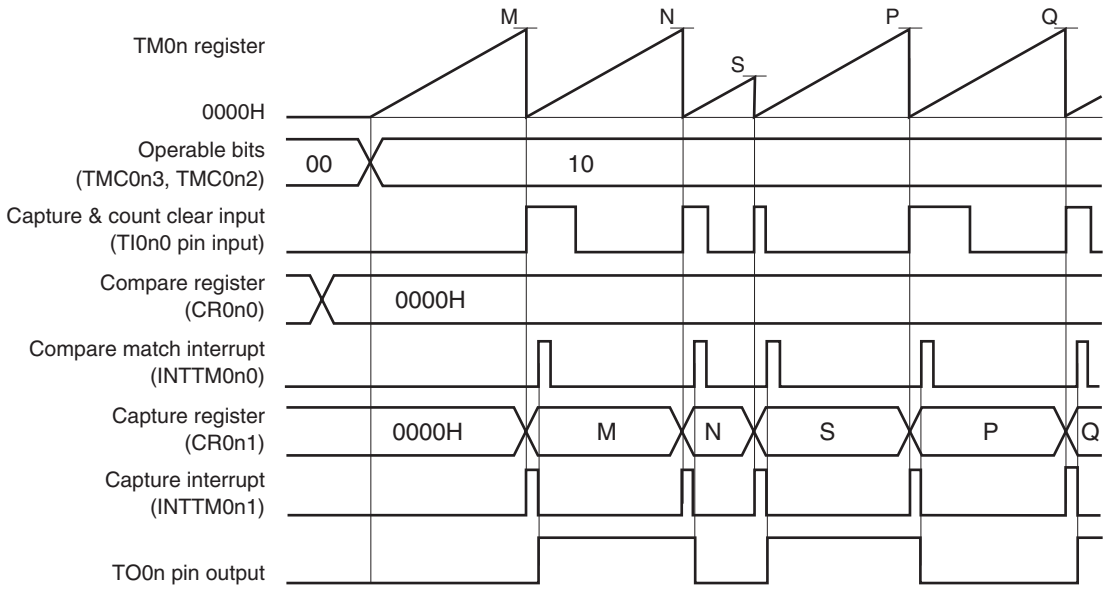
Figure 8-15. Block Diagram of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Compare Register, CR0n1 Register: Capture Register)



Remark n = 0 to 3

Figure 8-16. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Compare Register, CR0n1 Register: Capture Register) (1/2)

(a) TOC0n = 13H, PRM0n = 10H, CRC0n, = 04H, TMC0n = 08H, CR0n0 = 0000H



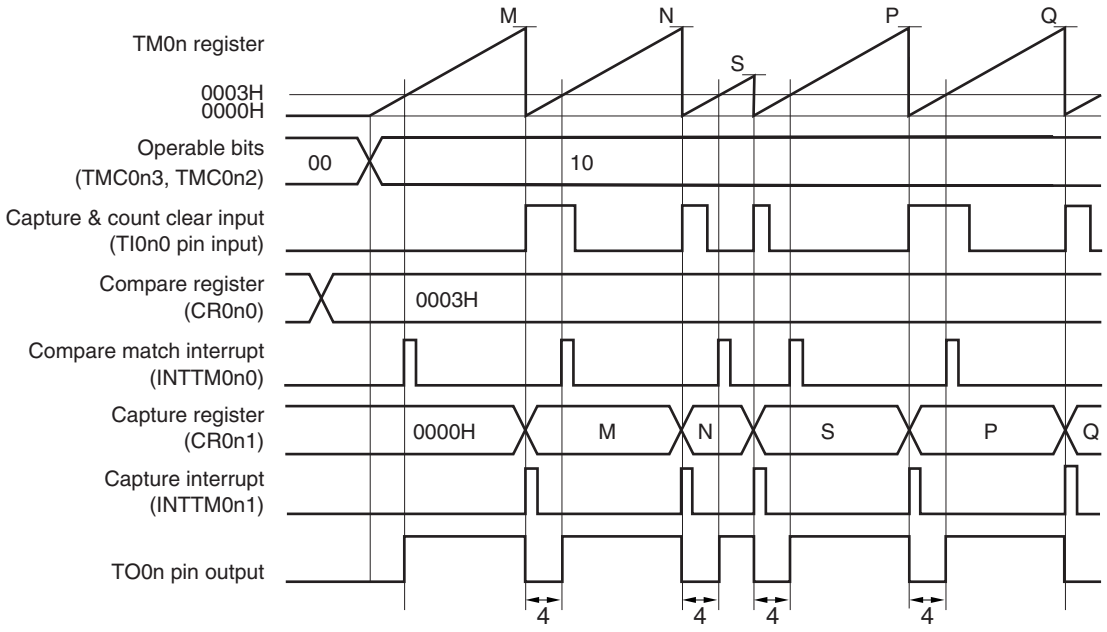
This is an application example where the output level of the TO0n pin is inverted when the count value has been captured & cleared.

The count value is captured to the CR0n1 register and the TM0n register is cleared (to 0000H) when the valid edge of the TI0n0 pin is detected. When the count value of the TM0n register is 0000H, a compare match interrupt signal (INTTM0n0) is generated, and the output level of the TO0n pin is inverted.

Remark n = 0 to 3

Figure 8-16. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Compare Register, CR0n1 Register: Capture Register) (2/2)

(b) TOC0n = 13H, PRM0n = 10H, CRC0n = 04H, TMC0n = 0AH, CR0n0 = 0003H



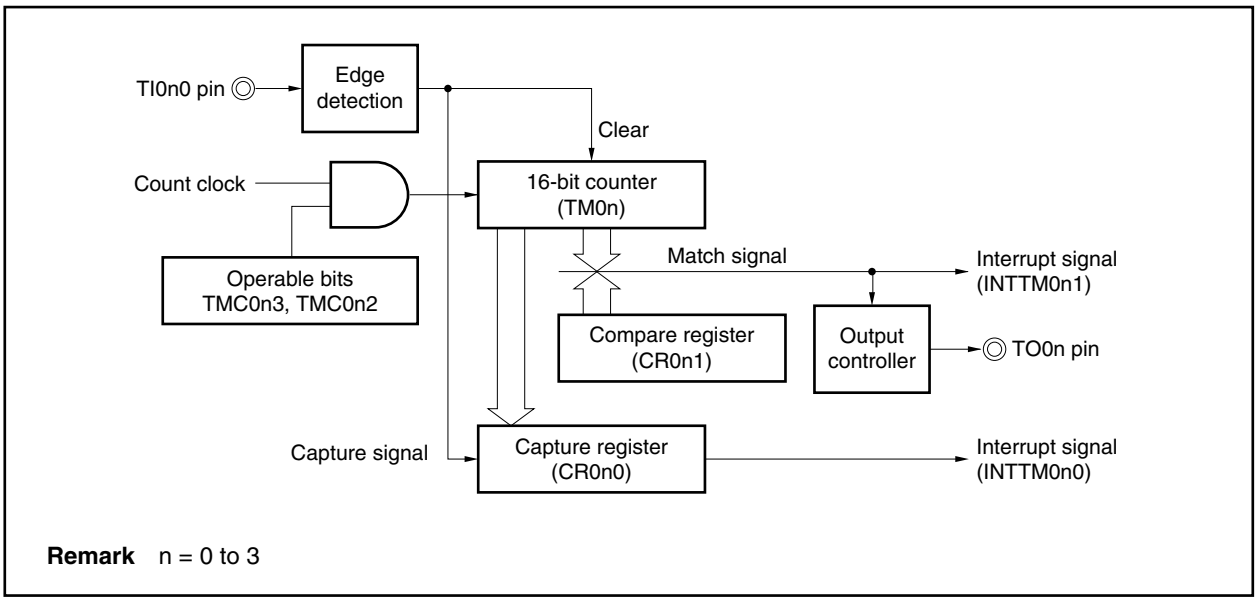
This is an application example where the width set to the CR0n0 register (4 clocks in this example) is to be output from the TO0n pin when the count value has been captured & cleared.

The count value is captured to the CR0n1 register, a capture interrupt signal (INTTM0n1) is generated, the TM0n register is cleared (to 0000H), and the output level of the TO0n pin is inverted when the valid edge of the TI0n0 pin is detected. When the count value of the TM0n register is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM0n0) is generated and the output level of the TO0n pin is inverted.

Remark n = 0 to 3

(3) Operation in clear & start mode entered by TI0n0 pin valid edge input (CR0n0 register: capture register, CR0n1 register: compare register)

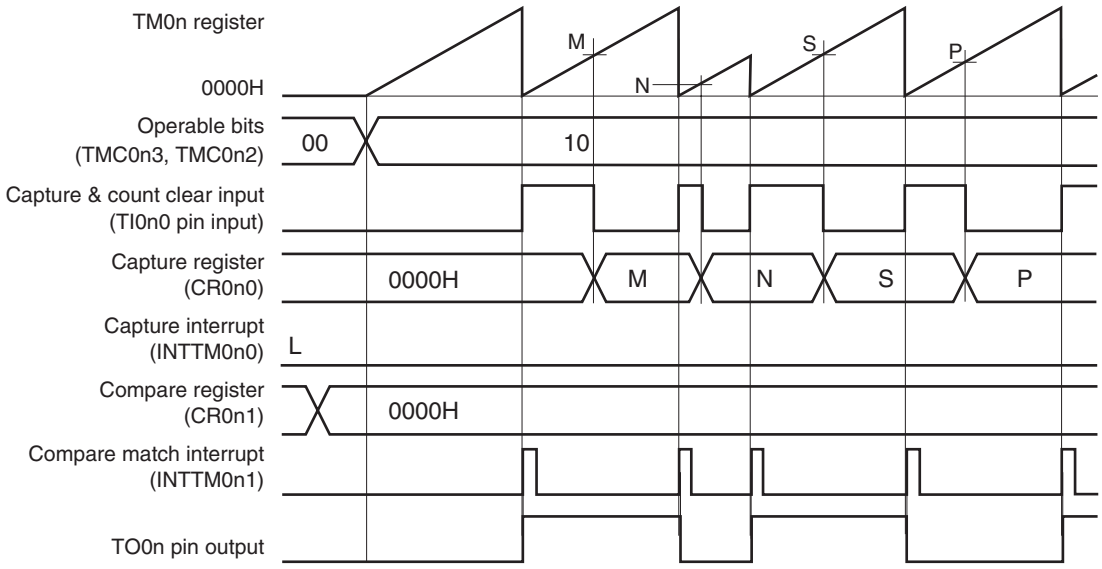
Figure 8-17. Block Diagram of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Compare Register)



Remark n = 0 to 3

Figure 8-18. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Compare Register) (1/2)

(a) TOC0n = 13H, PRM0n = 10H, CRC0n = 03H, TMC0n = 08H, CR0n1 = 0000H



This is an application example where the output level of the TO0n pin is to be inverted when the count value has been captured & cleared.

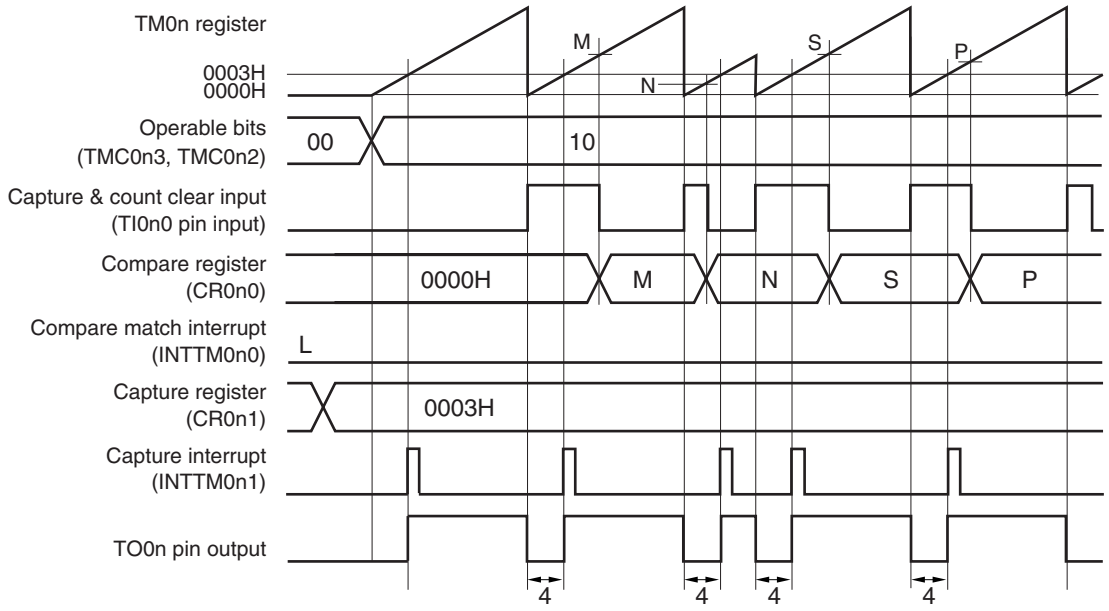
The TM0n register is cleared at the rising edge detection of the TI0n0 pin and it is captured to the CR0n0 register at the falling edge detection of the TI0n0 pin.

When the CRC0n.CRC0n1 bit is set to 1, the count value of the TM0n register is captured to CR0n0 in the phase reverse to that of the signal input to the TI0n0 pin, but the capture interrupt signal (INTTM0n0) is not generated. However, the INTTM0n0 signal is generated when the valid edge of the TI0n1 pin is detected. Mask the INTTM0n0 signal when it is not used.

Remark n = 0 to 3

Figure 8-18. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Compare Register) (2/2)

(b) TOC0n = 13H, PRM0n = 10H, CRC0n = 03H, TMC0n = 0AH, CR0n1 = 0003H



This is an application example where the width set to the CR0n1 register (4 clocks in this example) is to be output from the TO0n pin when the count value has been captured & cleared.

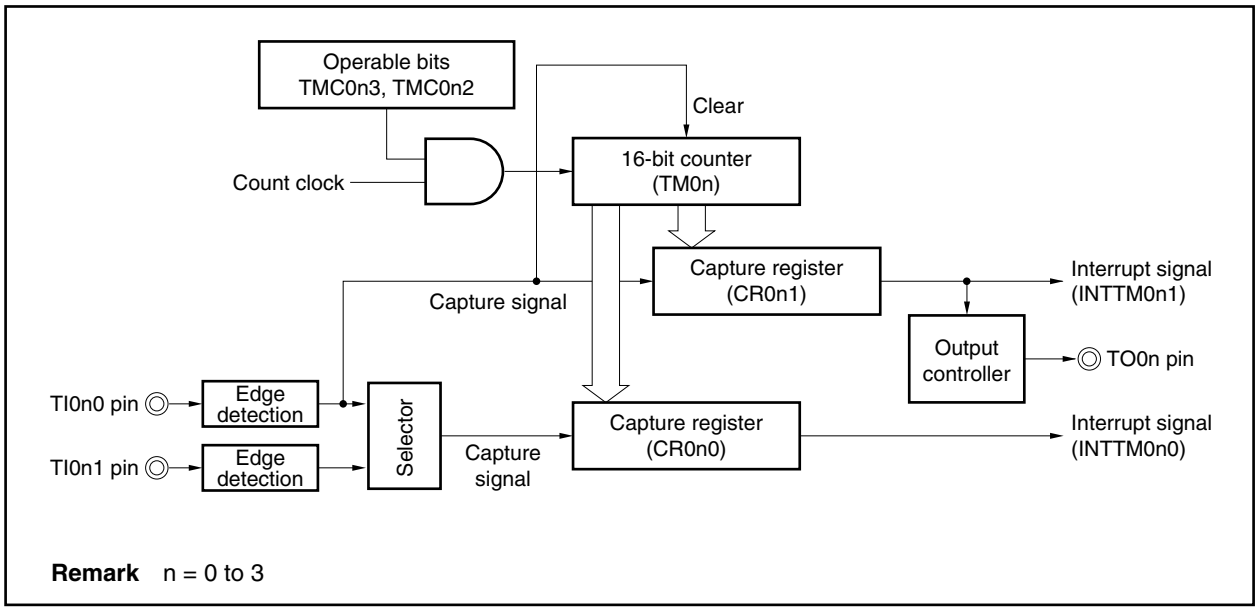
The TM0n register is cleared (to 0000H) at the rising edge detection of the TI0n0 pin and captured to the CR0n0 register at the falling edge detection of the TI0n0 pin. The output level of the TO0n pin is inverted when the TM0n register is cleared (to 0000H) because the rising edge of the TI0n0 pin has been detected or when the value of the TM0n register matches that of a compare register (CR0n1).

When the CRC0n.CRC0n1 bit is 1, the count value of the TM0n register is captured to the CR0n0 register in the phase reverse to that of the input signal of the TI0n0 pin, but the capture interrupt signal (INTTM0n0) is not generated. However, the INTTM0n0 interrupt is generated when the valid edge of the TI0n1 pin is detected. Mask the INTTM0n0 signal when it is not used.

Remark n = 0 to 3

(4) Operation in clear & start mode entered by TI0n0 pin valid edge input (CR0n0 register: capture register, CR0n1 register: capture register)

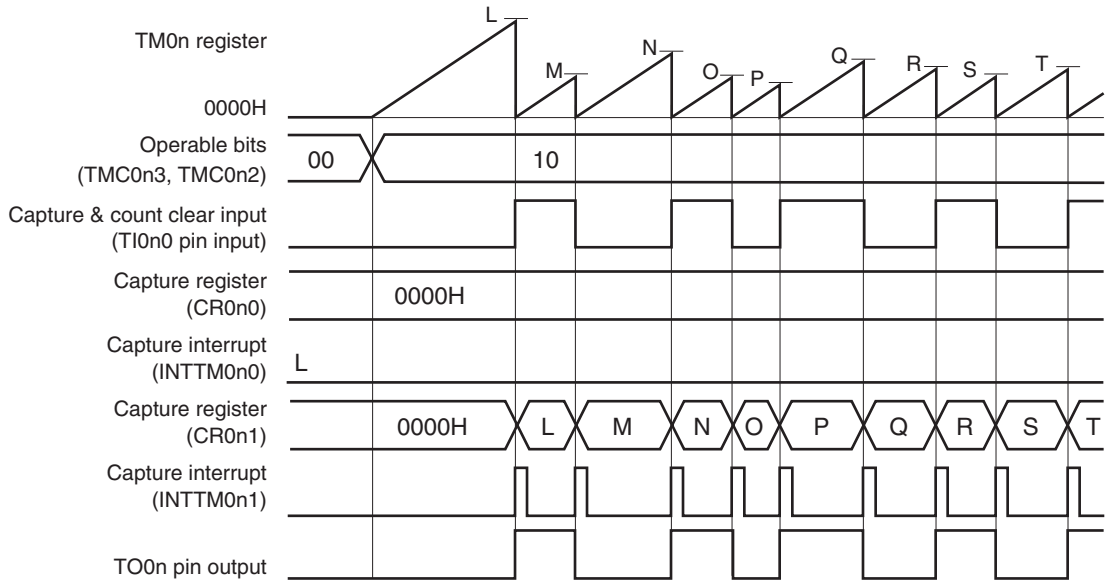
Figure 8-19. Block Diagram of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Capture Register)



Remark n = 0 to 3

Figure 8-20. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Capture Register) (1/3)

(a) TOC0n = 13H, PRM0n = 30H, CRC0n = 05H, TMC0n = 0AH

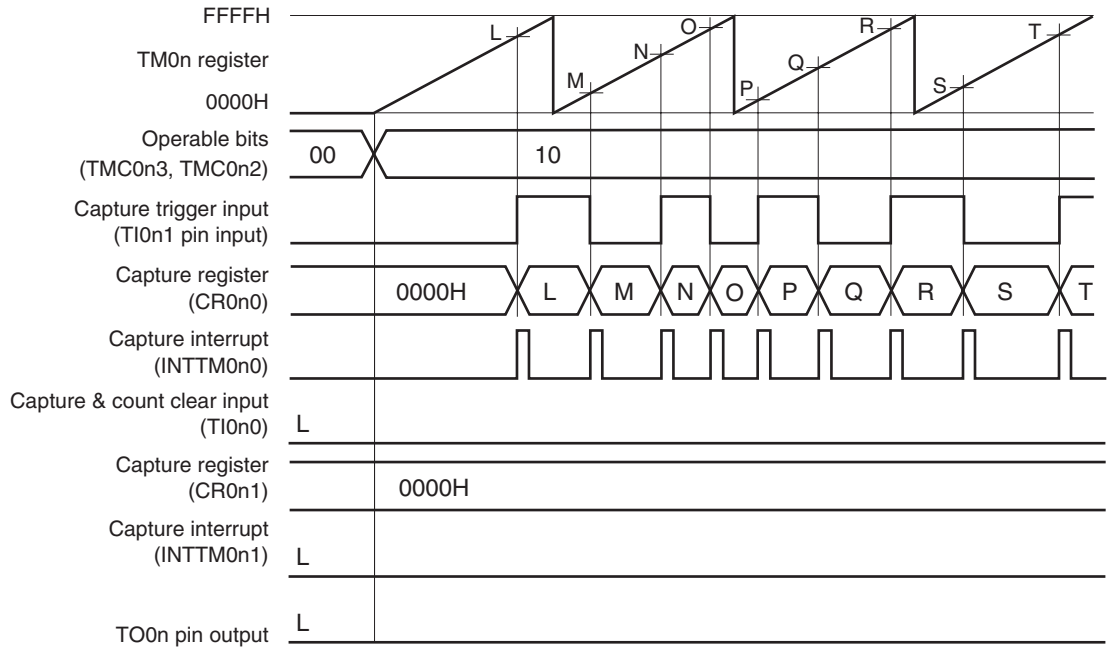


This is an application example where the count value is captured to the CR0n1 register, the TM0n register is cleared, and the TO0n pin output is inverted when the rising or falling edge of the TI0n0 pin is detected.
When the edge of the TI0n1 pin is detected, an interrupt signal (INTTM0n0) is generated. Mask the INTTM0n0 signal when it is not used.

Remark n = 0 to 3

Figure 8-20. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Capture Register) (2/3)

(b) TOC0n = 13H, PRM0n = C0H, CRC0n = 05H, TMC0n = 0AH

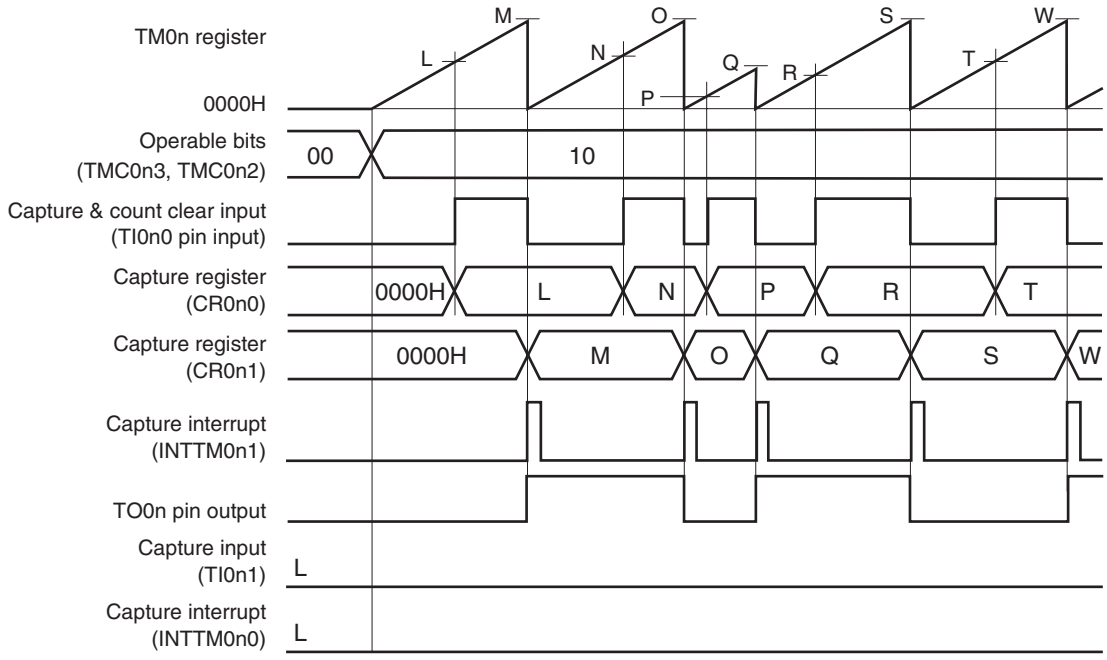


This is a timing example where an edge is not input to the TI0n0 pin, in an application where the count value is captured to the CR0n0 register when the rising or falling edge of the TI0n1 pin is detected.
Because the TO0n0 pin does not detect any edges, the TO0n pin output is not inverted and remains low level.

Remark n = 0 to 3

Figure 8-20. Timing Example of Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (CR0n0 Register: Capture Register, CR0n1 Register: Capture Register) (3/3)

(c) TOC0n = 13H, PRM0n = 00H, CRC0n = 07H, TMC0n = 0AH



This is an application example where the pulse width of the signal input to the TI0n0 pin is measured.
By setting the CRC0n register, the count value can be captured to the CR0n0 register in the phase reverse to the falling edge of the TI0n0 pin (i.e., rising edge) and to the CR0n1 register at the falling edge of the TI0n0 pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR0n1 register value] – [CR0n0 register value] × [Count clock cycle]
- Low-level width = [CR0n0 register value] × [Count clock cycle]

If the reverse phase of the TI0n0 pin is selected as a trigger to capture the count value to the CR0n0 register, the INTTM0n0 signal is not generated. Read the values of the CR0n0 and CR0n1 registers to measure the pulse width immediately after the INTTM0n1 signal is generated.
However, if the valid edge specified by the PRM0n.ESn11 and PRM0n.ESn10 bits is input to the TI0n1 pin, the count value is not captured but the INTTM0n0 signal is generated. To measure the pulse width of the TI0n0 pin, mask the INTTM0n0 signal when it is not used.

Remark n = 0 to 3

Figure 8-21. Example of Register Settings in Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	1	0	0/1	0

- TMC0n1: 0: Inverts TO0n output on match between CR0n0 and CR0n1. 1: Inverts TO0n output on match between CR0n0 and CR0n1 and valid edge of TI0n0 pin.
- TMC0n2: Clears and starts at valid edge input of TI0n0 pin.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0/1	0/1	0/1

- CRC0n0: 0: CR0n0 used as compare register 1: CR0n0 used as capture register
- CRC0n1: 0: TI0n1 pin is used as capture trigger of CR0n0. 1: Reverse phase of TI0n0 pin is used as capture trigger of CR0n0.
- CRC0n2: 0: CR0n1 used as compare register 1: CR0n1 used as capture register

(c) 16-bit timer output control register 0n (TOC0n)

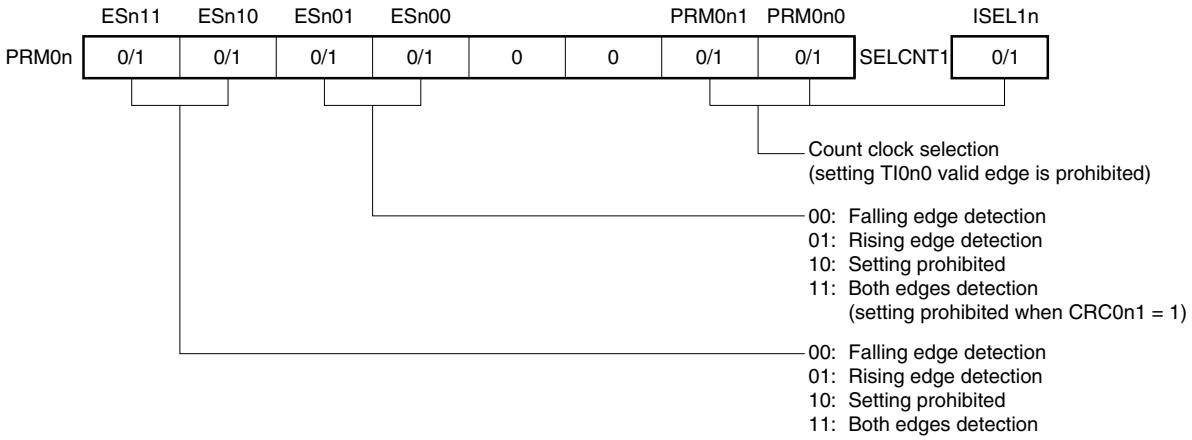
	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0/1	0/1	0/1	0/1	0/1

- TOE0n: 0: Disables TO0n output 1: Enables TO0n output
- LVR0n: Specifies initial value of TO0n output F/F
- TOC0n1: 00: Does not invert TO0n output on match between TM0n and CR0n0/CR0n1. 01: Inverts TO0n output on match between TM0n and CR0n0. 10: Inverts TO0n output on match between TM0n and CR0n1. 11: Inverts TO0n output on match between TM0n and CR0n0/CR0n1.

Remark n = 0 to 3

Figure 8-21. Example of Register Settings in Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input (2/2)

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)



(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

When this register is used as a compare register and when its value matches the count value of the TM0n register, an interrupt signal (INTTM0n0) is generated. The count value of the TM0n register is not cleared.

To use this register as a capture register, select either the TI0n0 or TI0n1 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of the TM0n register is stored in the CR0n0 register.

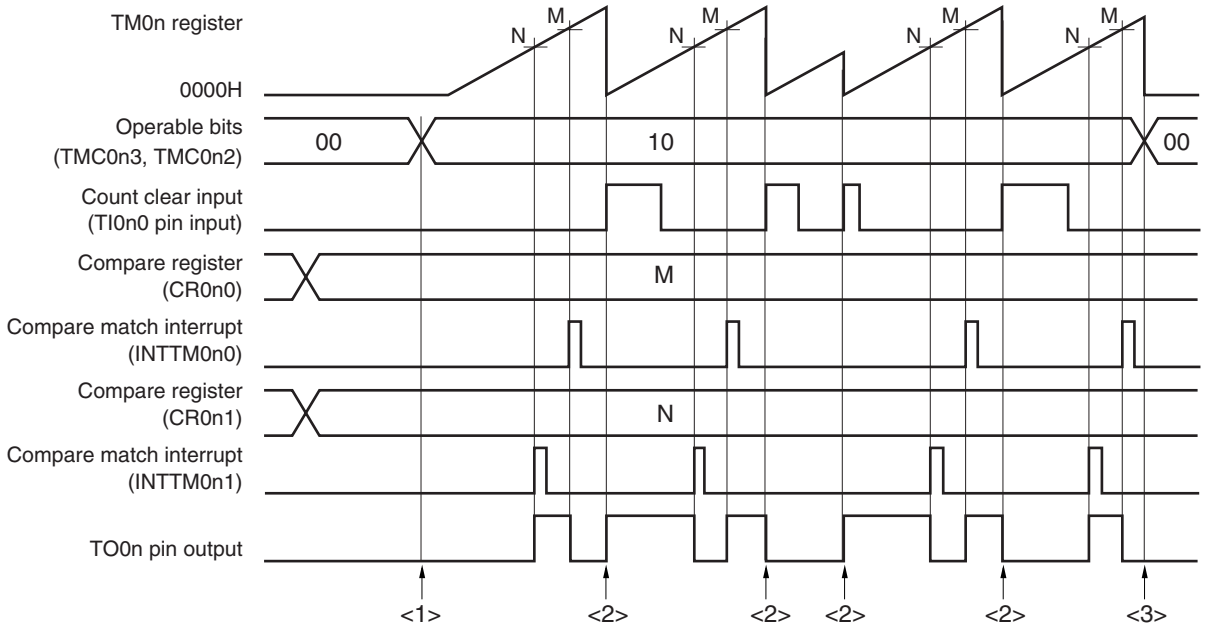
(g) 16-bit capture/compare register 0n1 (CR0n1)

When this register is used as a compare register and when its value matches the count value of the TM0n register, an interrupt signal (INTTM0n1) is generated. The count value of the TM0n register is not cleared.

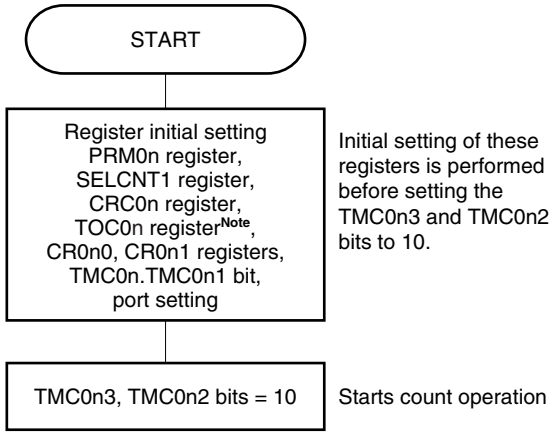
When this register is used as a capture register, the TI0n0 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of the TM0n register is stored in the CR0n1 register.

Remark n = 0 to 3

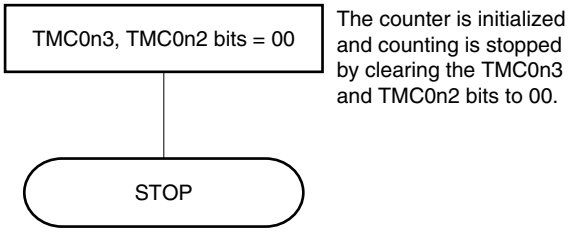
Figure 8-22. Example of Software Processing in Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input



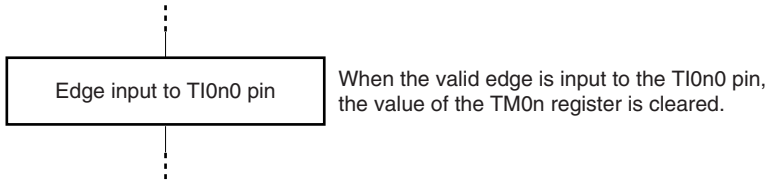
<1> Count operation start flow



<3> Count operation stop flow



<2> TM0n register clear & start flow



Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0 to 3

8.4.5 Free-running timer operation

When the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 01 (free-running timer mode), 16-bit timer/event counter 0n continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (TMC0n.OVF0n bit) is set to 1 at the next clock, and the TM0n register is cleared (to 0000H) and continues counting. Clear the OVF0n bit to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

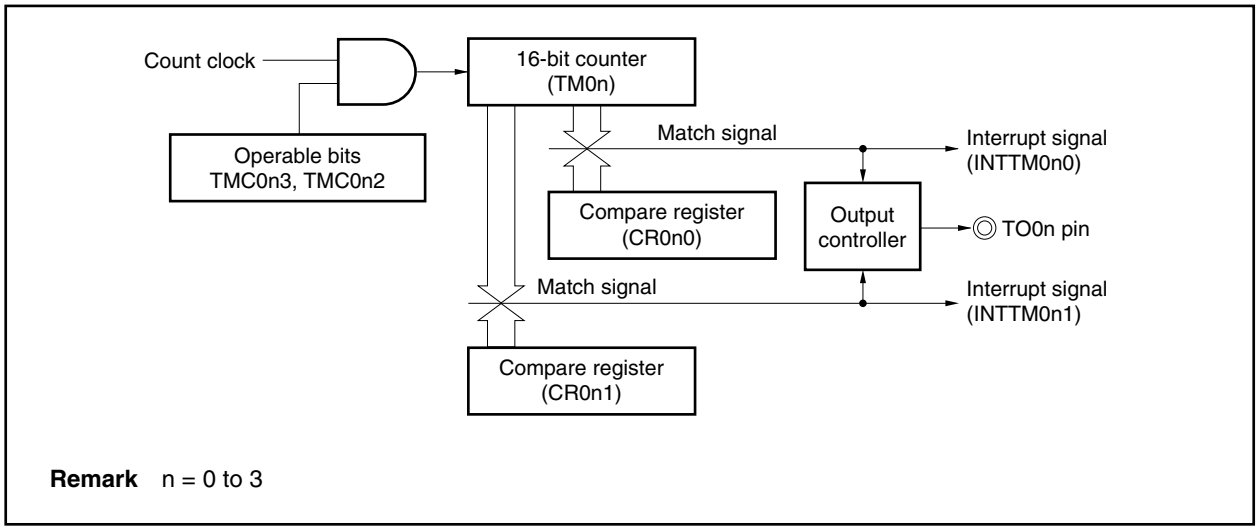
- Both the CR0n0 and CR0n1 registers are used as compare registers.
- Either the CR0n0 register or CR0n1 register is used as a compare register and the other is used as a capture register.
- Both the CR0n0 and CR0n1 registers are used as capture registers.

Remarks 1. For the alternate-function pin (TO0n) settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For enabling the INTTM0n0 and INTTM0n1 interrupts, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

(1) Free-running timer mode operation (CR0n0 register: compare register, CR0n1 register: compare register)

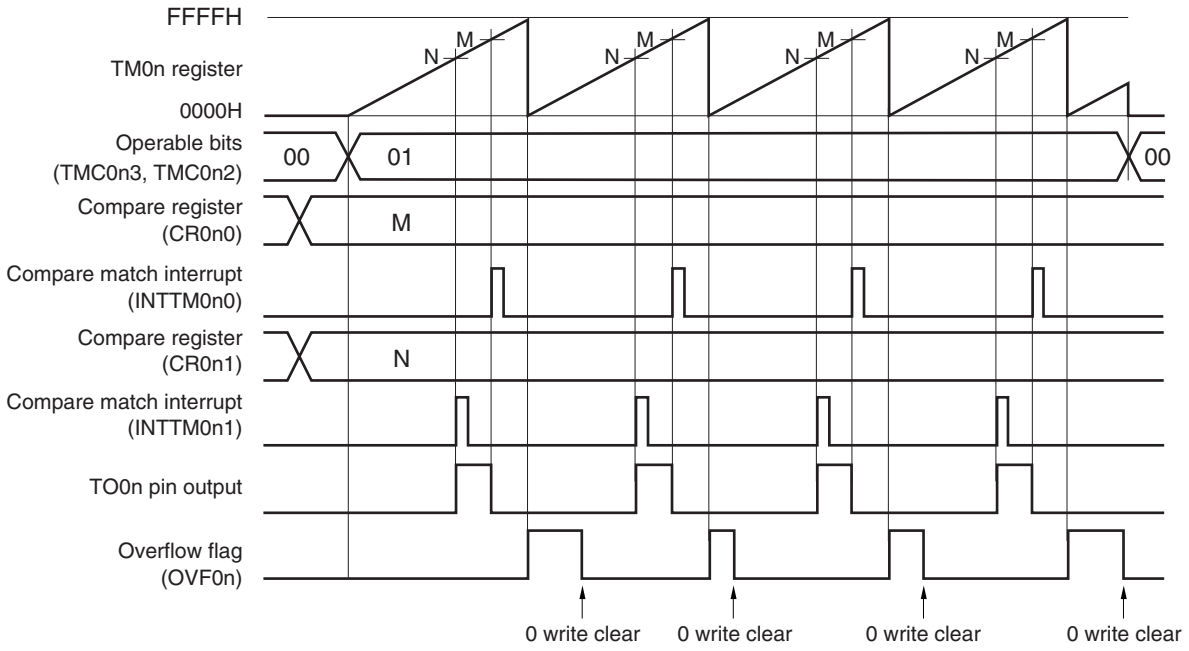
Figure 8-23. Block Diagram of Free-Running Timer Mode (CR0n0 Register: Compare Register, CR0n1 Register: Compare Register)



Remark n = 0 to 3

Figure 8-24. Timing Example of Free-Running Timer Mode
(CR0n0 Register: Compare Register, CR0n1 Register: Compare Register)

• TOC0n = 13H, PRM0n = 00H, CRC0n = 00H, TMC0n = 04H

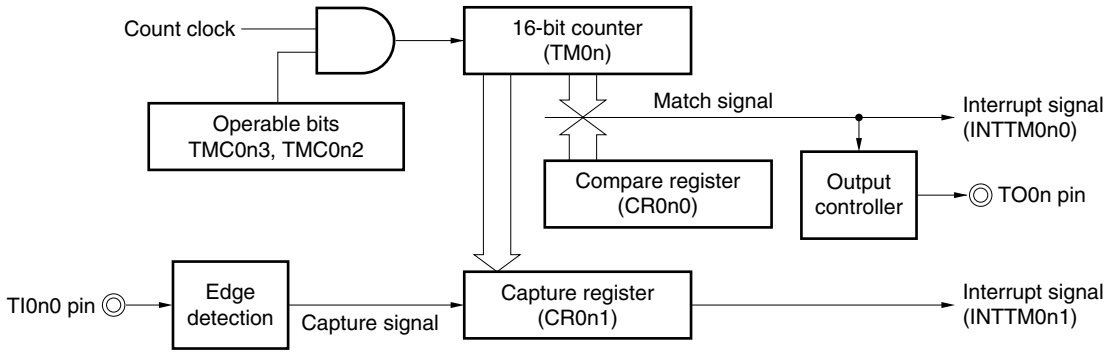


This is an application example where two compare registers are used in the free-running timer mode.
The output level of the TO0n pin is reversed each time the count value of the TM0n register matches the set values of the CR0n0 and CR0n1 registers. When the count value matches the register value, the INTTM0n0 or INTTM0n1 signal is generated.

Remark n = 0 to 3

(2) Free-running timer mode operation
(CR0n0 register: compare register, CR0n1 register: capture register)

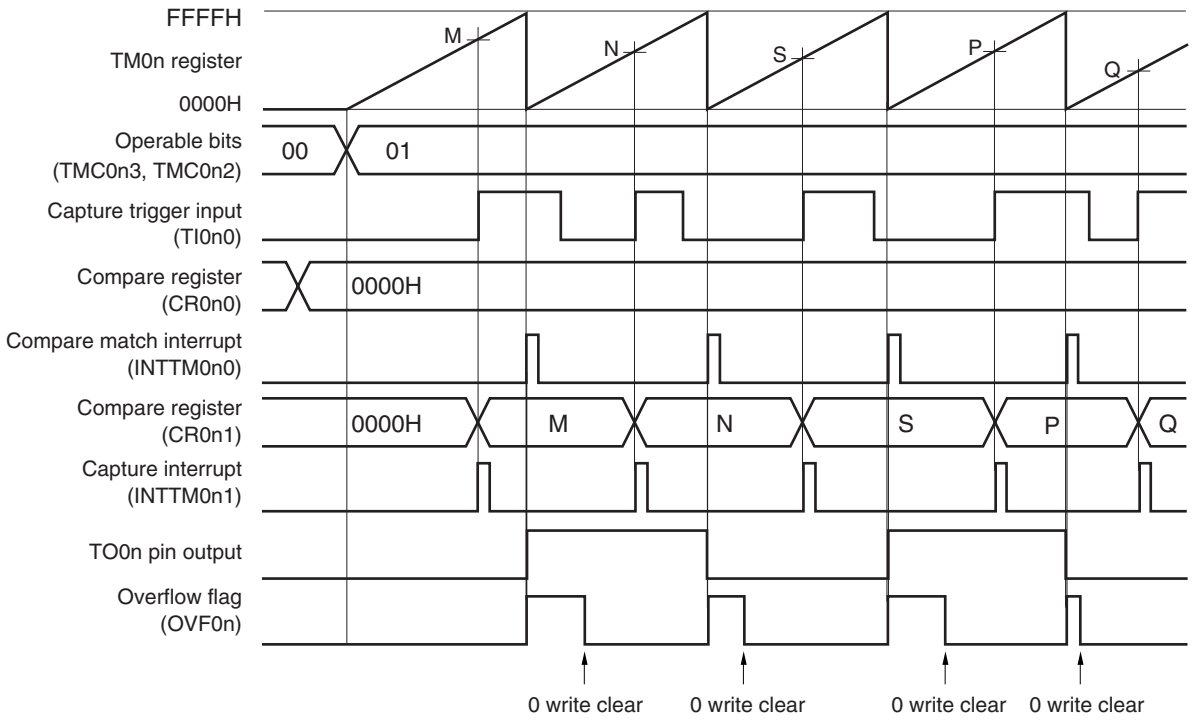
Figure 8-25. Block Diagram of Free-Running Timer Mode
(CR0n0 Register: Compare Register, CR0n1 Register: Capture Register)



Remark n = 0 to 3

Figure 8-26. Timing Example of Free-Running Timer Mode
(CR0n0 Register: Compare Register, CR0n1 Register: Capture Register)

• **TOC0n = 13H, PRM0n = 10H, CRC0n = 04H, TMC0n = 04H**



This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

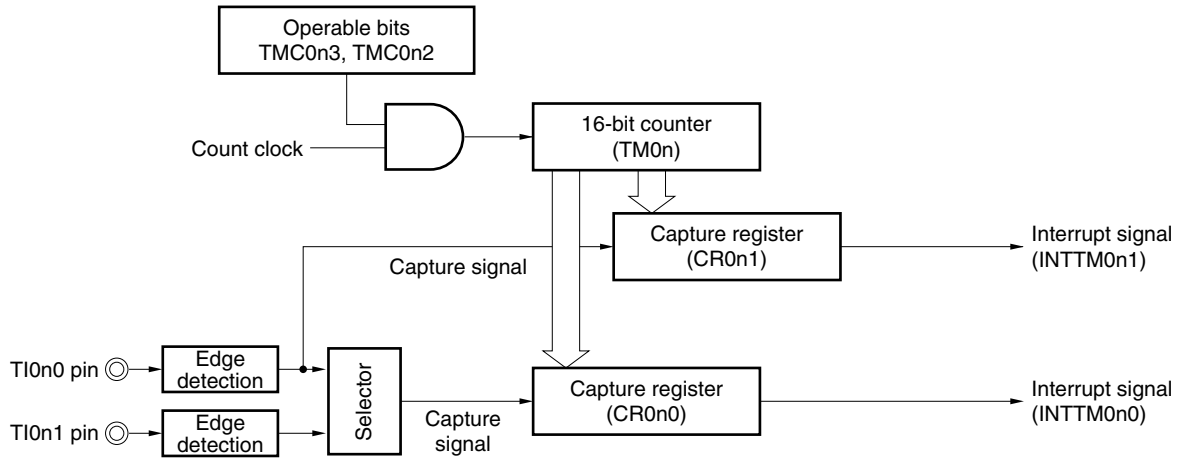
In this example, the INTTM0n0 signal is generated and the output level of the TO0n pin is reversed each time the count value of the TM0n register matches the set value of the CR0n0 register (compare register). In addition, the INTTM0n1 signal is generated and the count value of the TM0n register is captured to the CR0n1 register each time the valid edge of the TI0n0 pin is detected.

Remark n = 0 to 3

(3) Free-running timer mode operation

(CR0n0 register: capture register, CR0n1 register: capture register)

Figure 8-27. Block Diagram of Free-Running Timer Mode
(CR0n0 Register: Capture Register, CR0n1 Register: Capture Register)



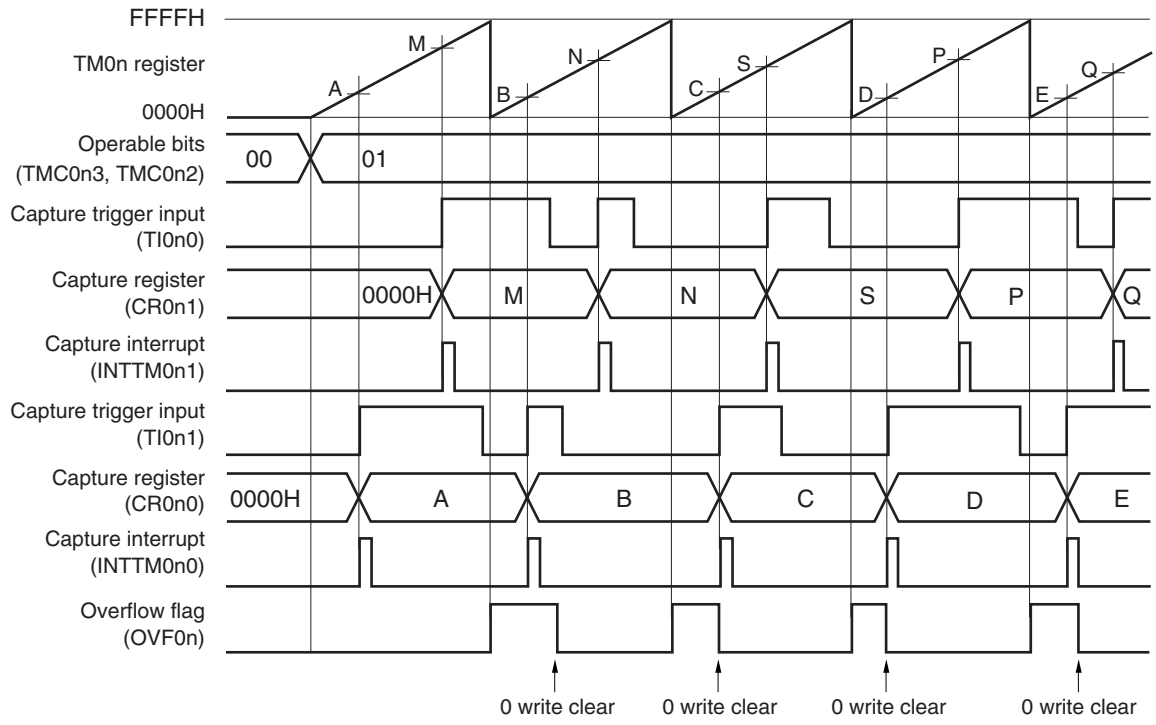
Remarks 1. If both the CR0n0 and CR0n1 registers are used as capture registers in the free-running timer mode, the output level of the TO0n pin is not inverted.

However, it can be inverted each time the valid edge of the TI0n0 pin is detected if the TMC0n.TMC0n1 bit is set to 1.

2. n = 0 to 5

Figure 8-28. Timing Example of Free-Running Timer Mode
(CR0n0 Register: Capture Register, CR0n1 Register: Capture Register) (1/2)

(a) TOC0n = 13H, PRM0n = 0 to 50H, CRC0n = 05H, TMC0n = 04H

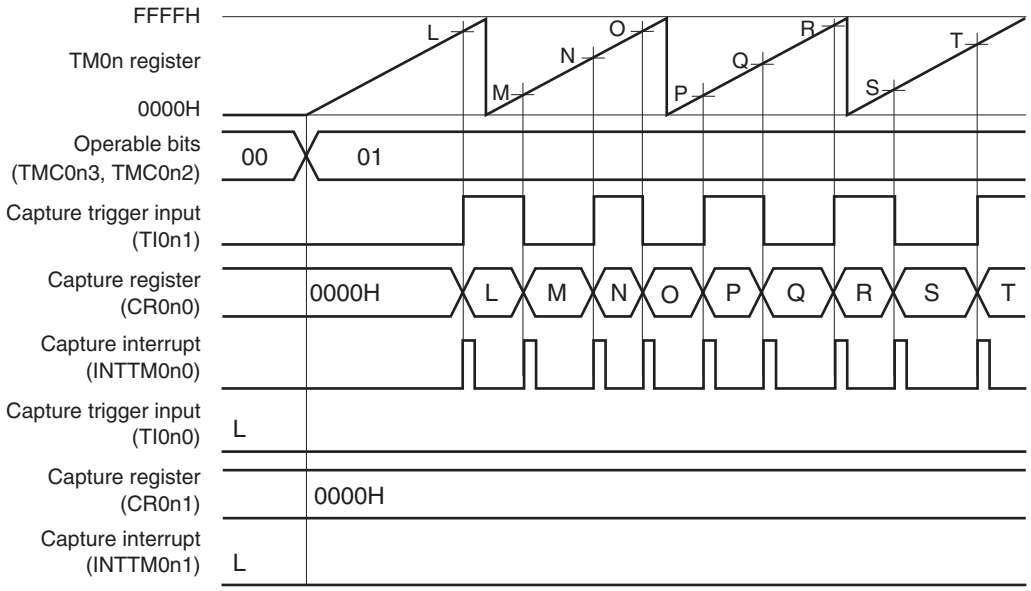


This is an application example where the count values that have been captured at the valid edges of separate capture trigger signals are stored in separate capture registers in the free-running timer mode.
The count value is captured to the CR0n1 register when the valid edge of the TI0n0 pin input is detected and to the CR0n0 register when the valid edge of the TI0n1 pin input is detected.

Remark n = 0 to 3

Figure 8-28. Timing Example of Free-Running Timer Mode (CR0n0 Register: Capture Register, CR0n1 Register: Capture Register) (2/2)

(b) TOC0n = 13H, PRM0n = C0H, CRC0n = 05H, TMC0n = 04H



This is an application example where both the edges of the TI0n1 pin are detected and the count value is captured to the CR0n0 register in the free-running timer mode.

When both the CR0n0 and CR0n1 registers are used as capture registers and when the valid edge of only the TI0n1 pin is to be detected, the count value cannot be captured to the CR0n1 register.

Remark n = 0 to 3

Figure 8-29. Example of Register Settings in Free-Running Timer Mode (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	0	1	0/1	0

- 0: Inverts TO0n pin output on match between CR0n0 and CR0n1.
- 1: Inverts TO0n pin output on match between CR0n0 and CR0n1 and valid edge of TI0n0 pin.

Free-running timer mode

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0/1	0/1	0/1

- 0: CR0n0 used as compare register
- 1: CR0n0 used as capture register

- 0: TI0n1 pin is used as capture trigger of CR0n0.
- 1: Reverse phase of TI0n0 pin is used as capture trigger of CR0n0.

- 0: CR0n1 used as compare register
- 1: CR0n1 used as capture register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0/1	0/1	0/1	0/1	0/1

- 0: Disables TO0n output
- 1: Enables TO0n output

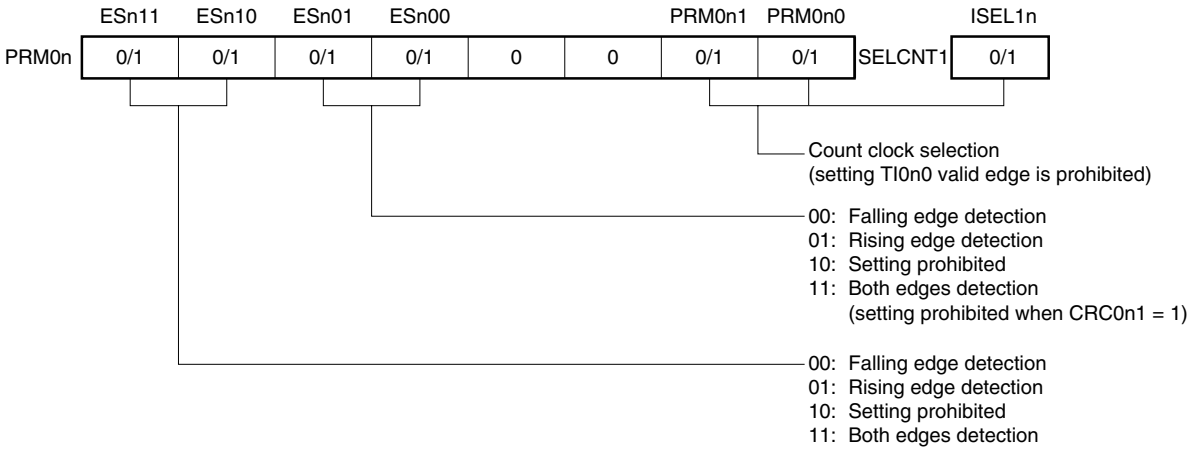
Specifies initial value of TO0n output F/F

- 00: Does not invert TO0n output on match between TM0n and CR0n0/CR0n1.
- 01: Inverts TO0n output on match between TM0n and CR0n0.
- 10: Inverts TO0n output on match between TM0n and CR0n1.
- 11: Inverts TO0n output on match between TM0n and CR0n0/CR0n1.

Remark n = 0 to 3

Figure 8-29. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)



(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

When this register is used as a compare register and when its value matches the count value of the TM0n register, an interrupt signal (INTTM0n0) is generated. The count value of the TM0n register is not cleared.

To use this register as a capture register, select either the TI0n0 or TI0n1 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of the TM0n register is stored in the CR0n0 register.

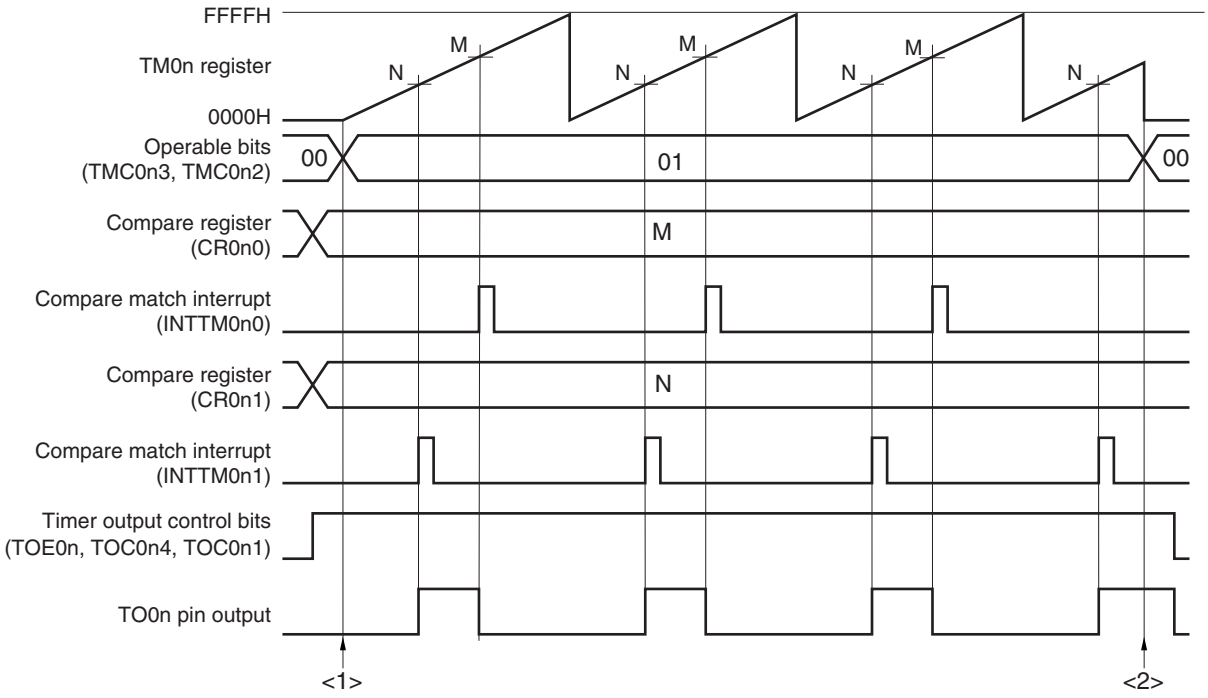
(g) 16-bit capture/compare register 0n1 (CR0n1)

When this register is used as a compare register and when its value matches the count value of the TM0n register, an interrupt signal (INTTM0n1) is generated. The count value of the TM0n register is not cleared.

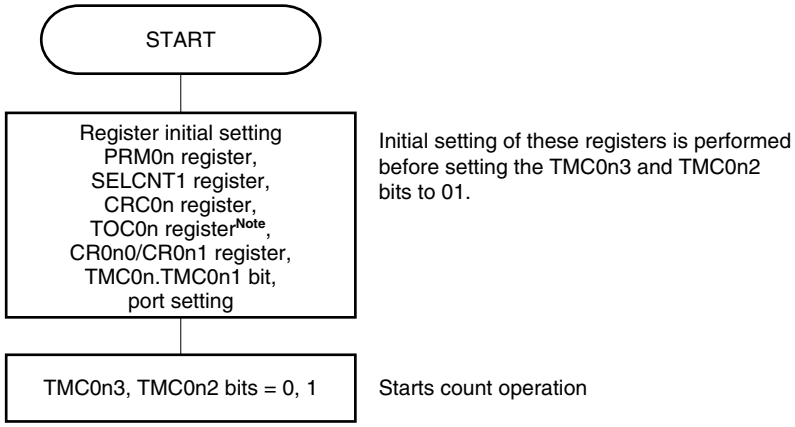
When this register is used as a capture register, the TI0n0 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of the TM0n register is stored in the CR0n1 register.

Remark n = 0 to 3

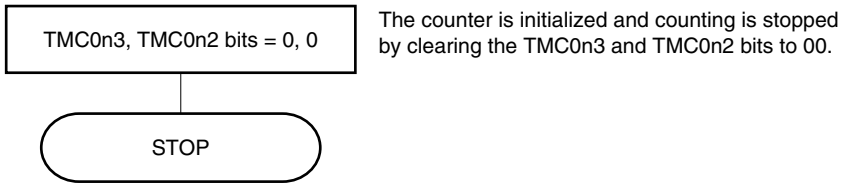
Figure 8-30. Example of Software Processing in Free-Running Timer Mode



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0 to 3

8.4.6 PPG output operation

A rectangular wave having a pulse width set in advance by the CR0n1 register is output from the TO0n pin as a PPG (Programmable Pulse Generator) signal during a cycle set by the CR0n0 register when the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits are set to 11 (clear & start upon a match between the TM0n register and the CR0n0 register).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

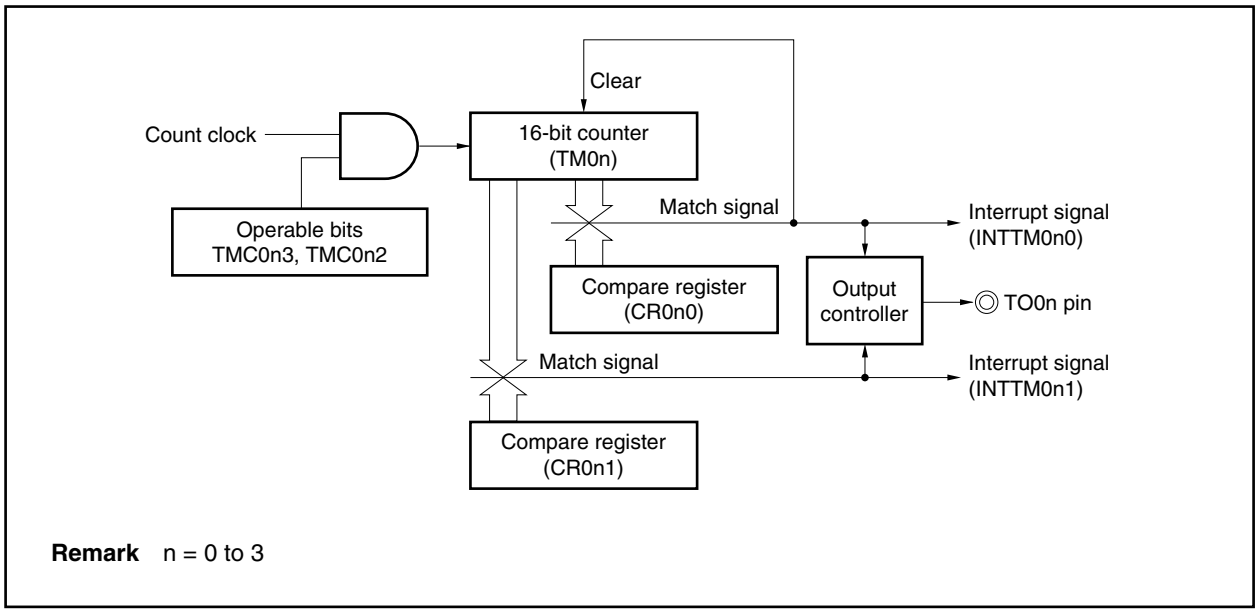
- Pulse cycle = (Set value of the CR0n0 register + 1) × Count clock cycle
- Duty = (Set value of the CR0n1 register + 1) / (Set value of the CR0n0 register + 1)

Caution To change the duty factor (value of the CR0n1 register) during operation, see 8.5.1 Rewriting CR0n1 register during TM0n operation.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For enabling the INTTM0n0 and INTTM0n1 interrupts, refer to **CHAPTER 21 INTERRUPT/ EXCEPTION PROCESSING FUNCTION**.

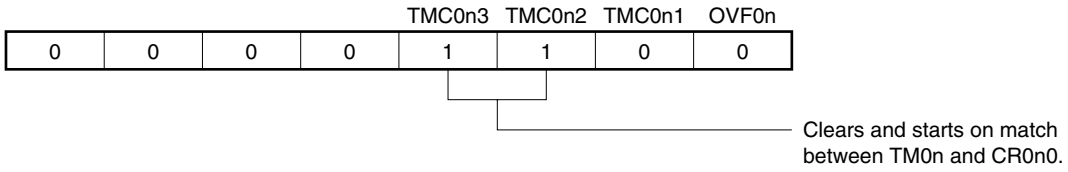
Figure 8-31. Block Diagram of PPG Output Operation



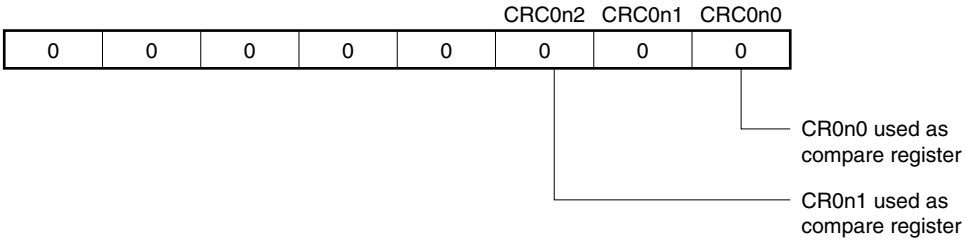
Remark n = 0 to 3

Figure 8-32. Example of Register Settings for PPG Output Operation

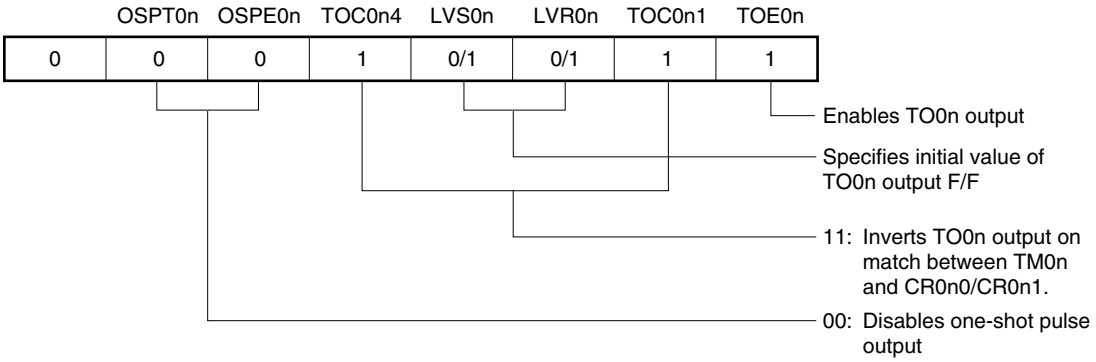
(a) 16-bit timer mode control register 0n (TMC0n)



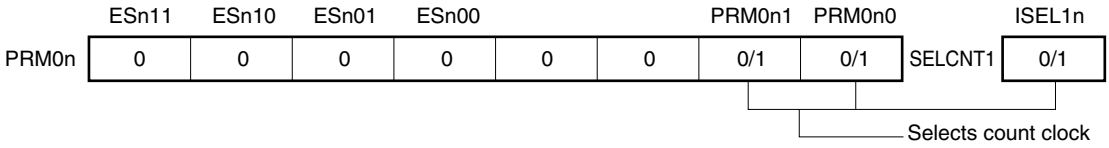
(b) Capture/compare control register 0n (CRC0n)



(c) 16-bit timer output control register 0n (TOC0n)



(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)



(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

An interrupt signal (INTTM0n0) is generated when the value of this register matches the count value of the TM0n register.

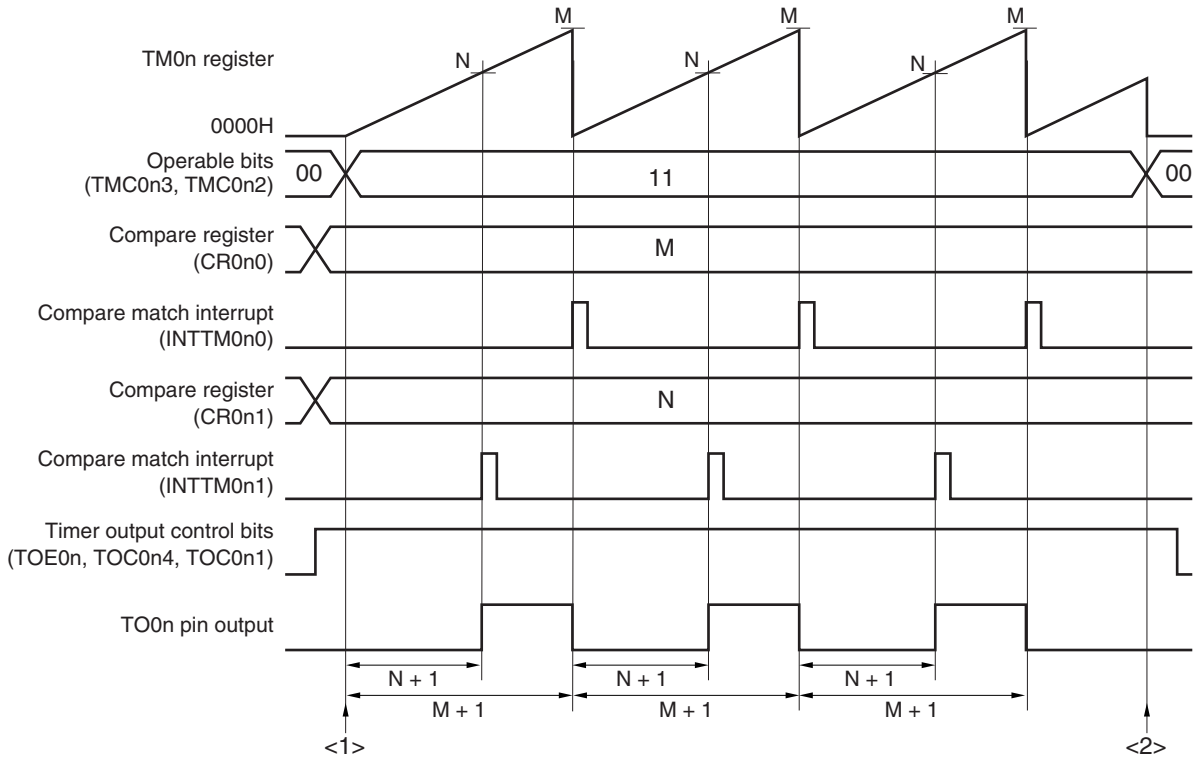
(g) 16-bit capture/compare register 0n1 (CR0n1)

An interrupt signal (INTTM0n1) is generated when the value of this register matches the count value of the TM0n register.

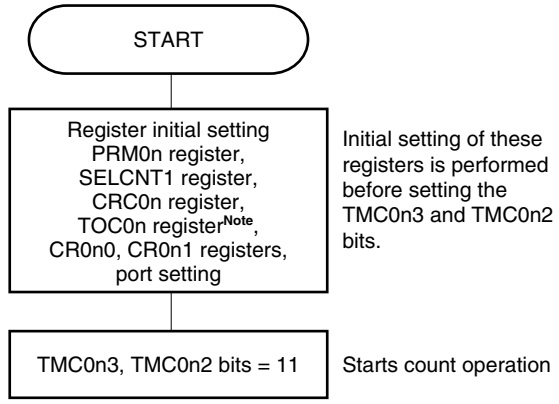
Caution Set values to the CR0n0 and CR0n1 registers such that the condition 0000H ≤ CR0n1 < CR0n0 ≤ FFFFH is satisfied.

Remark n = 0 to 3

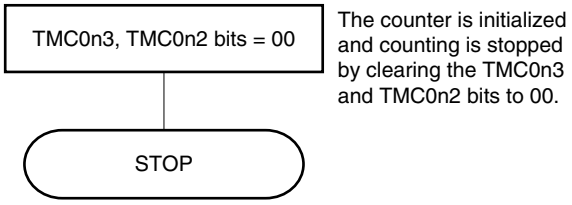
Figure 8-33. Example of Software Processing for PPG Output Operation



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remarks 1. PPG pulse cycle = (M + 1) × Count clock cycle
PPG duty = (N + 1)/(M + 1)

2. n = 0 to 3

8.4.7 One-shot pulse output operation

A one-shot pulse can be output by setting the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits to 01 (free-running timer mode) or to 10 (clear & start mode entered by the TI0n0 pin valid edge) and setting the TOC0n.OSPE0n bit to 1.

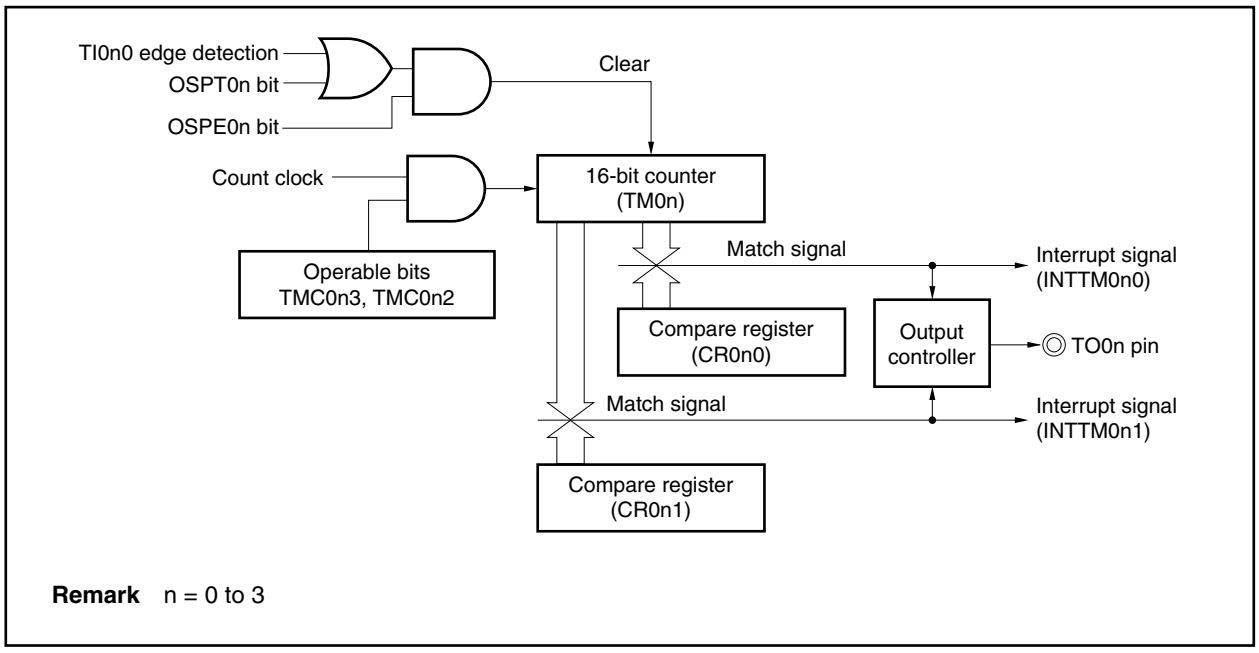
When the TOC0n.OSPT0n is set to 1 or when the valid edge is input to the TI0n0 pin during timer operation, clearing & starting of the TM0n register is triggered, and a pulse of the difference between the values of the CR0n0 and CR0n1 registers is output only once from the TO0n pin.

Caution Do not input the trigger again (setting OSPT0n to 1 or detecting the valid edge of the TI0n0 pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For enabling the INTTM0n0 and INTTM0n1 interrupts, refer to **CHAPTER 21 INTERRUPT/ EXCEPTION PROCESSING FUNCTION**.

Figure 8-34. Block Diagram of One-Shot Pulse Output Operation



Remark n = 0 to 3

Figure 8-35. Example of Register Settings for One-Shot Pulse Output Operation (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	0/1	0/1	0	0

01: Free running timer mode
10: Clear and start mode by valid edge of TI0n0 pin.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	0	0	0

CR0n0 used as compare register

CR0n1 used as compare register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0/1	1	1	0/1	0/1	1	1

Enables TO0n pin output

Specifies initial value of TO0n pin output

Inverts TO0n output on match between TM0n and CR0n0/CR0n1.

Enables one-shot pulse output

Software trigger is generated by writing 1 to this bit (operation is not affected even if 0 is written to it).

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)

	ESn11	ESn10	ESn01	ESn00			PRM0n1	PRM0n0		ISEL1n
PRM0n	0	0	0	0	0	0	0/1	0/1	SELCNT1	0/1

Selects count clock

Remark n = 0 to 3

Figure 8-35. Example of Register Settings for One-Shot Pulse Output Operation (2/2)

(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

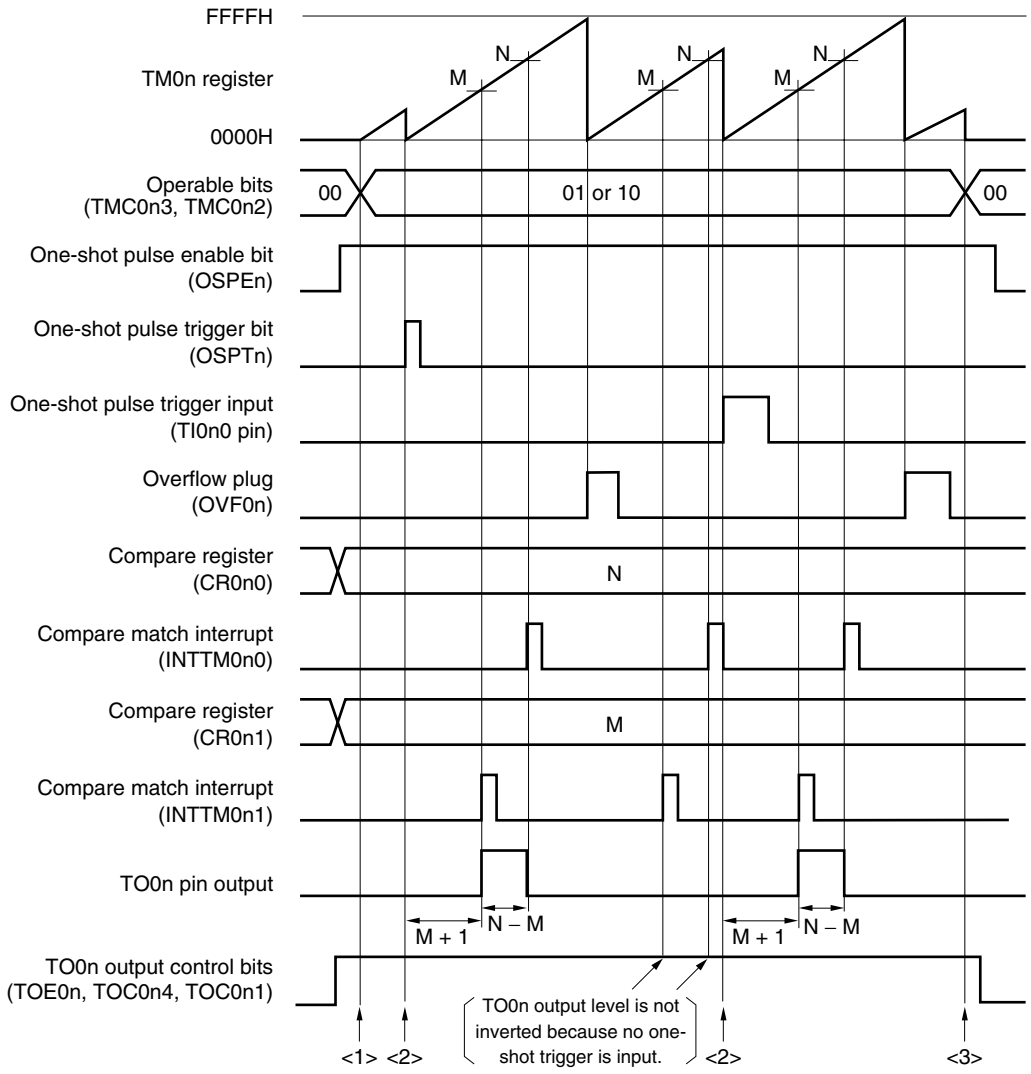
This register is used as a compare register when a one-shot pulse is output. When the value of the TM0n register matches that of the CR0n0 register, an interrupt signal (INTTM0n0) is generated and the output level of the TO0n pin is inverted.

(g) 16-bit capture/compare register 0n1 (CR0n1)

This register is used as a compare register when a one-shot pulse is output. When the value of the TM0n register matches that of the CR0n1 register, an interrupt signal (INTTM0n1) is generated and the output level of the TO0n pin is inverted.

Remark n = 0 to 3

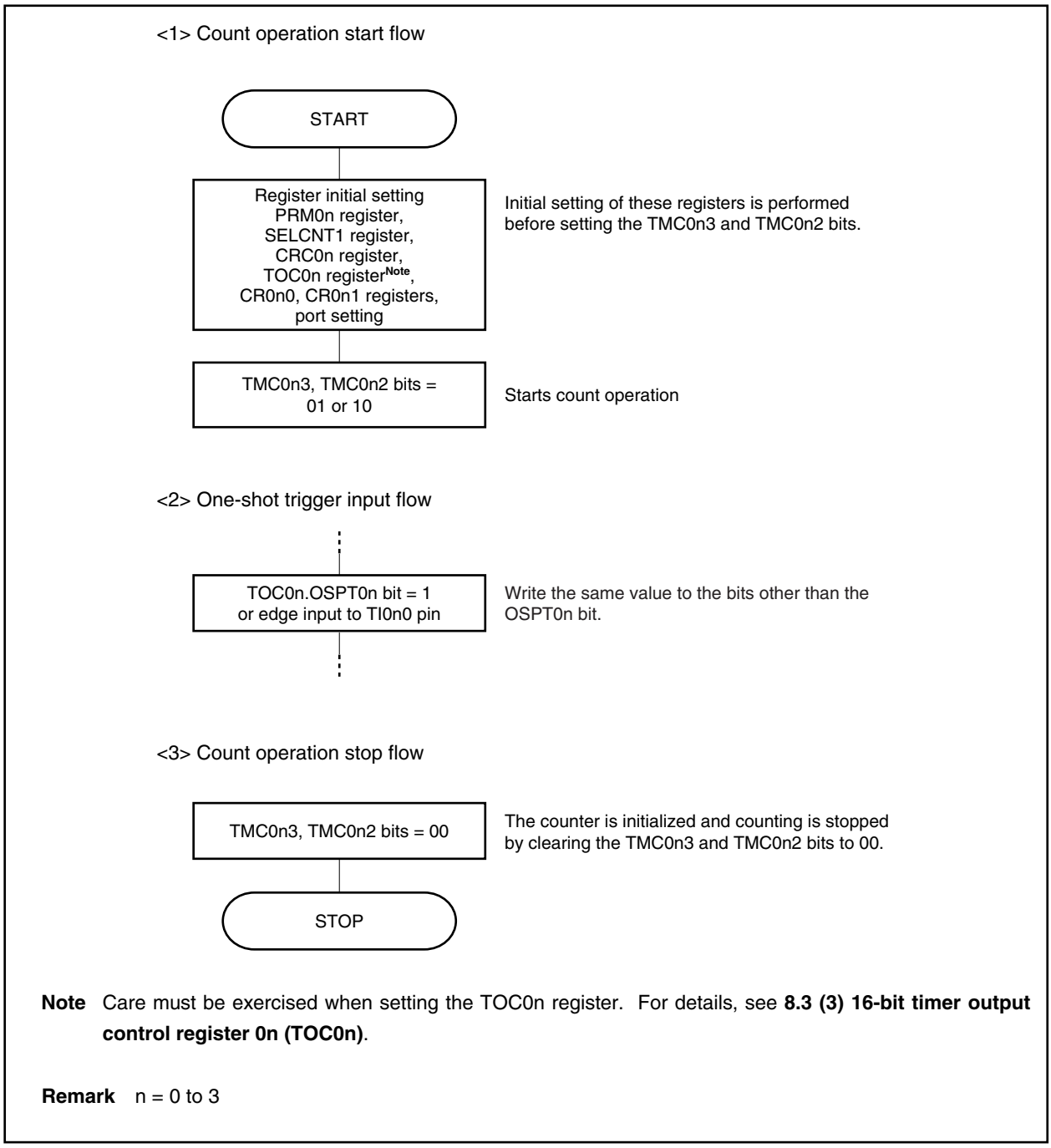
Figure 8-36. Example of Software Processing for One-Shot Pulse Output Operation (1/2)



- Time from when the one-shot pulse trigger is input until the one-shot pulse is output
  = (M + 1) × Count clock cycle
- One-shot pulse output active level width
  = (N – M) × Count clock cycle

Remark n = 0 to 3

Figure 8-36. Example of Software Processing for One-Shot Pulse Output Operation (2/2)



Note Care must be exercised when setting the TOC0n register. For details, see **8.3 (3) 16-bit timer output control register 0n (TOC0n)**.

Remark n = 0 to 3

8.4.8 Pulse width measurement operation

The TM0n register can be used to measure the pulse width of the signal input to the TI0n0 and TI0n1 pins.

Measurement can be accomplished by operating the 16-bit timer/event counter 0n in the free-running timer mode or by restarting the timer in synchronization with the signal input to the TI0n0 pin.

When an interrupt is generated, read the value of the valid capture register and measure the pulse width. Check the TMC0n.OVF0n flag. If it is set (to 1), clear it to 0 by software.

Figure 8-37. Block Diagram of Pulse Width Measurement (Free-Running Timer Mode)

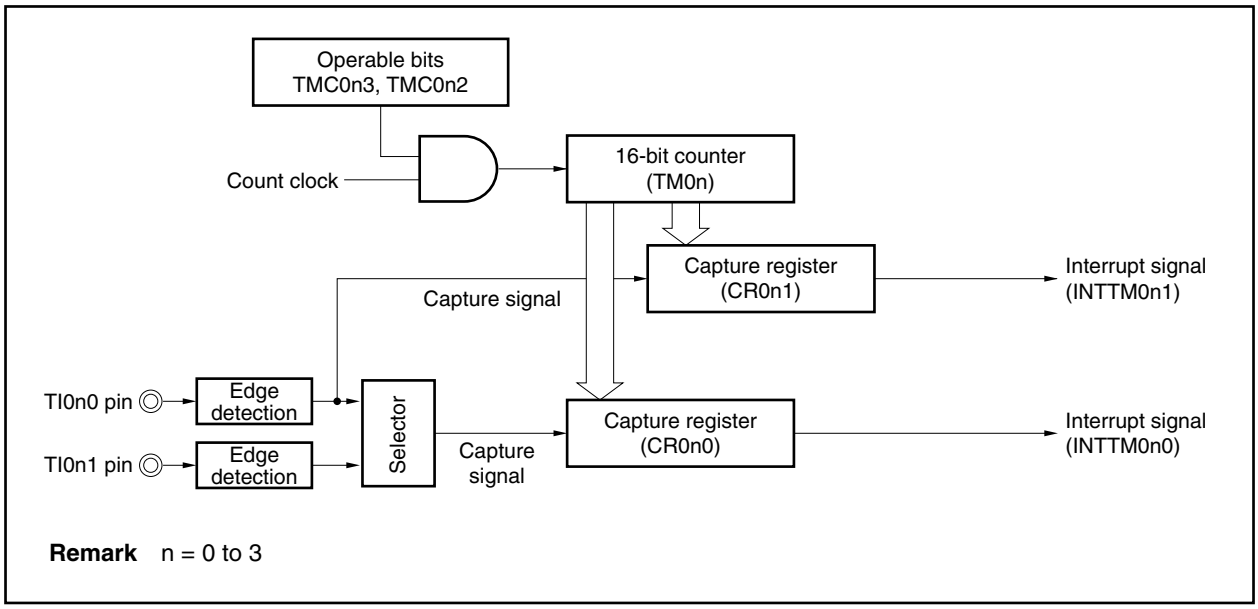
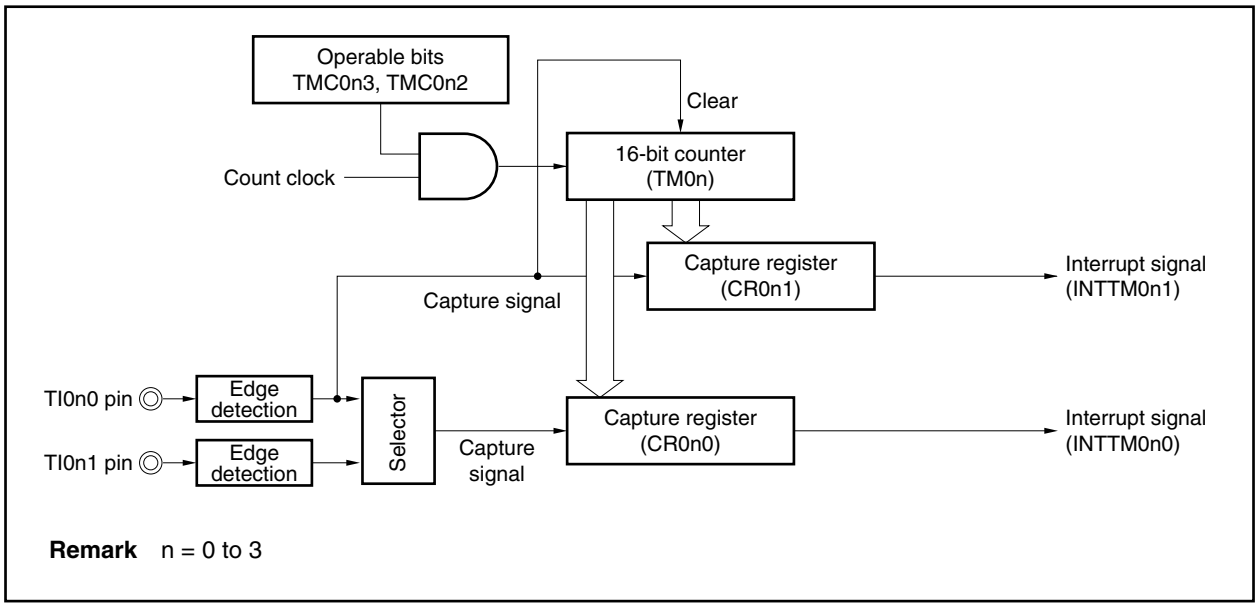


Figure 8-38. Block Diagram of Pulse Width Measurement (Clear & Start Mode Entered by TI0n0 Pin Valid Edge Input)



A pulse width can be measured in the following three ways.

- Measuring the pulse width by using two input signals of the TI0n0 and TI0n1 pins (free-running timer mode)
- Measuring the pulse width by using one input signal of the TI0n0 pin (free-running timer mode)
- Measuring the pulse width by using one input signal of the TI0n0 pin (clear & start mode entered by the TI0n0 pin valid edge input)

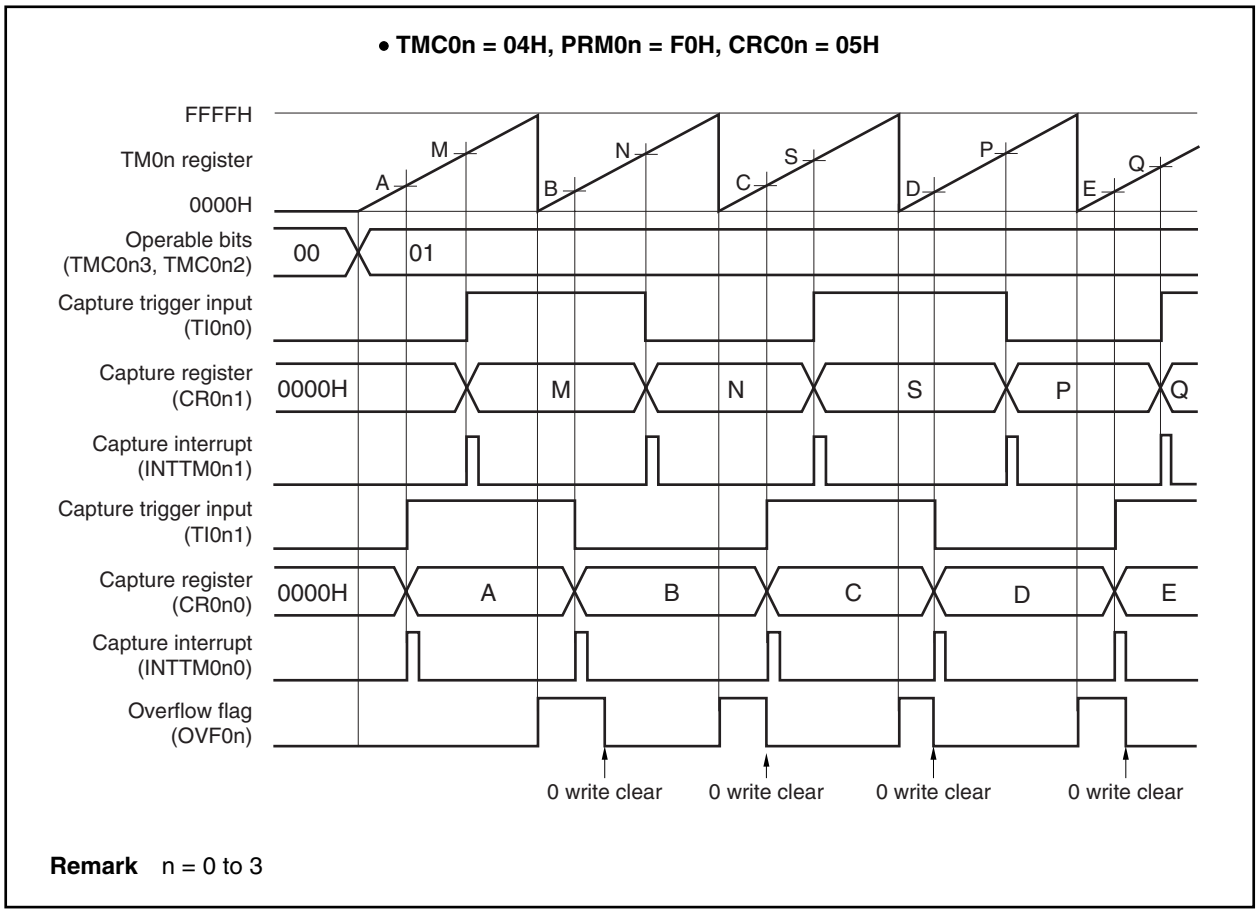
(1) Measuring the pulse width by using two input signals of the TI0n0 and TI0n1 pins (free-running timer mode)

Set the free-running timer mode (the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = 01). When the valid edge of the TI0n0 pin is detected, the count value of the TM0n register is captured to the CR0n1 register. When the valid edge of the TI0n1 pin is detected, the count value of the TM0n register is captured to the CR0n0 register. Specify detection of both the edges of the TI0n0 and TI0n1 pins.

By this measurement method, the previous count value is subtracted from the count value captured by the edge of each input signal. Therefore, save the previously captured value to a separate register in advance.

If an overflow occurs, the value becomes negative if the previously captured value is simply subtracted from the current captured value and, therefore, a borrow occurs (the PSW.CY bit is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear the TMC0n.OVF0n bit to 0.

Figure 8-39. Timing Example of Pulse Width Measurement (1)



Remark n = 0 to 3

(2) Measuring the pulse width by using one input signal of the TI0n0 pin (free-running timer mode)

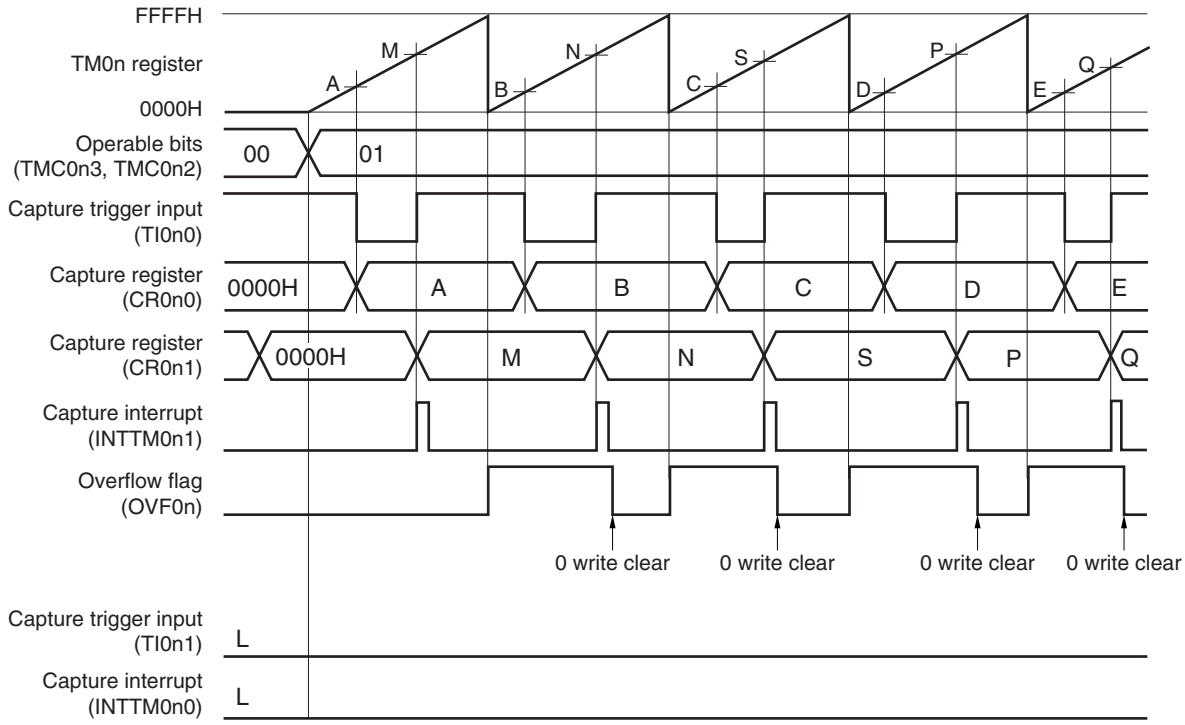
Set the free-running timer mode (the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = 01). The count value of the TM0n register is captured to the CR0n0 register in the phase reverse to the valid edge detected on the TI0n0 pin. When the valid edge of the TI0n0 pin is detected, the count value of the TM0n register is captured to the CR0n1 register.

By this measurement method, values are stored in separate capture registers when a width from one edge to another is measured. Therefore, the capture values do not have to be saved. By subtracting the value of one capture register from that of another, a high-level width, low-level width, and cycle are calculated.

If an overflow occurs, the value becomes negative if one captured value is simply subtracted from another and, therefore, a borrow occurs (the PSW.CY bit is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear the TMC0n.OVF0n bit to 0.

Figure 8-40. Timing Example of Pulse Width Measurement (2)

• TMC0n = 04H, PRM0n = 10H, CRC0n = 07H



Remark n = 0 to 3

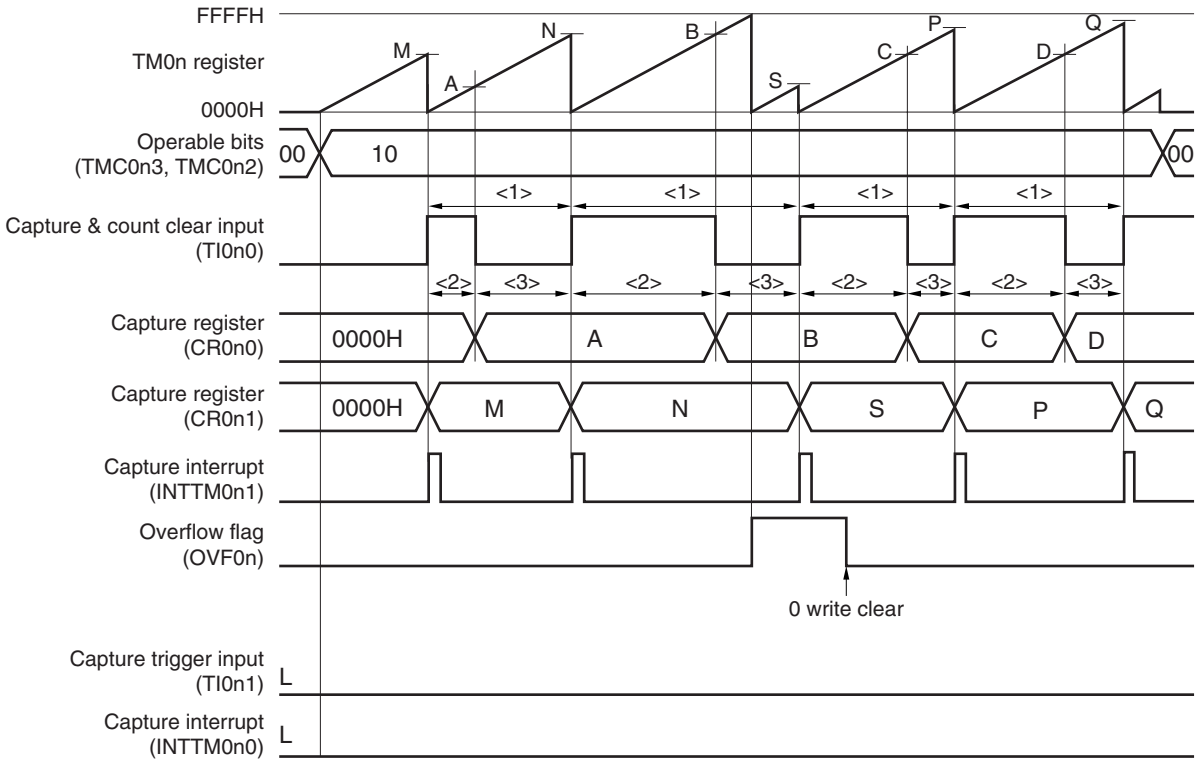
(3) Measuring the pulse width by using one input signal of the TI0n0 pin (clear & start mode entered by the TI0n0 pin valid edge input)

Set the clear & start mode entered by the TI0n0 pin valid edge (the TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = 10). The count value of the TM0n register is captured to the CR0n0 register in the phase reverse to the valid edge of the TI0n0 pin, and the count value of the TM0n register is captured to the CR0n1 register and the TM0n register is cleared (0000H) when the valid edge of the TI0n0 pin is detected. Therefore, a cycle is stored in the CR0n1 register if the TM0n register does not overflow.

If an overflow occurs, take the value that results from adding 10000H to the value stored in the CR0n1 register as a cycle. Clear the TMC0n.OVF0n bit to 0.

Figure 8-41. Timing Example of Pulse Width Measurement (3)

• TMC0n = 08H, PRM0n = 10H, CRC0n = 07H



<1> Pulse cycle = (10000H × Number of times OVF0n bit is set to 1 + Captured value of the CR0n1 register) × Count clock cycle

<2> High-level pulse width = (10000H × Number of times OVF0n bit is set to 1 + Captured value of the CR0n0 register) × Count clock cycle

<3> Low-level pulse width = (Pulse cycle − High-level pulse width)

Remark n = 0 to 3

Figure 8-42. Example of Register Settings for Pulse Width Measurement (1/2)

(a) 16-bit timer mode control register 0n (TMC0n)

				TMC0n3	TMC0n2	TMC0n1	OVF0n
0	0	0	0	0/1	0/1	0	0

01: Free running timer mode
10: Clear and start mode entered by valid edge of TI0n0 pin.

(b) Capture/compare control register 0n (CRC0n)

					CRC0n2	CRC0n1	CRC0n0
0	0	0	0	0	1	0/1	1

1: CR0n0 used as capture register

0: TI0n1 pin is used as capture trigger of CR0n0.
1: Reverse phase of TI0n0 pin is used as capture trigger of CR0n0.

1: CR0n1 used as capture register

(c) 16-bit timer output control register 0n (TOC0n)

	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n
0	0	0	0	0	0	0	0

(d) Prescaler mode register 0n (PRM0n), selector operation control register 1 (SELCNT1)

	ESn11	ESn10	ESn01	ESn00			PRM0n1	PRM0n0		ISEL1n
PRM0n	0/1	0/1	0/1	0/1	0	0	0/1	0/1	SELCNT1	0/1

Selects count clock
(setting valid edge of TI0n0 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection
(setting when CRC0n1 = 1 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection

Remark n = 0 to 3

Figure 8-42. Example of Register Settings for Pulse Width Measurement (2/2)

(e) 16-bit timer counter 0n (TM0n)

By reading the TM0n register, the count value can be read.

(f) 16-bit capture/compare register 0n0 (CR0n0)

This register is used as a capture register. Either the TI0n0 or TI0n1 pin is selected as a capture trigger. When a specified edge of the capture trigger is detected, the count value of the TM0n register is stored in the CR0n0 register.

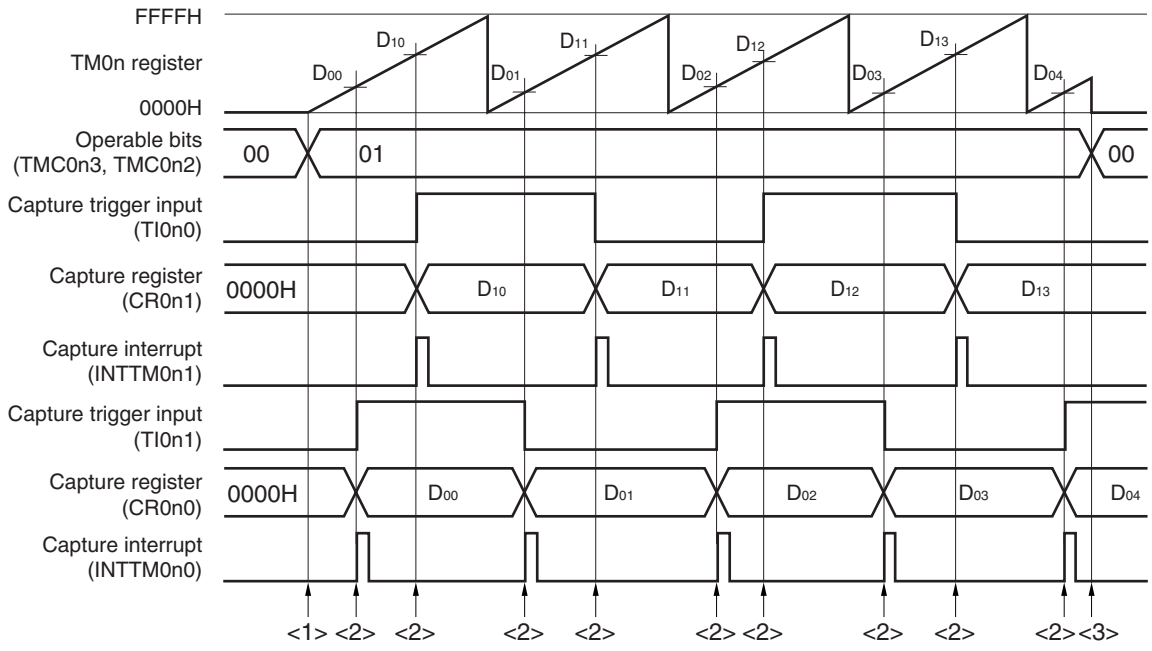
(g) 16-bit capture/compare register 0n1 (CR0n1)

This register is used as a capture register. The signal input to the TI0n0 pin is used as a capture trigger. When the capture trigger is detected, the count value of the TM0n register is stored in the CR0n1 register.

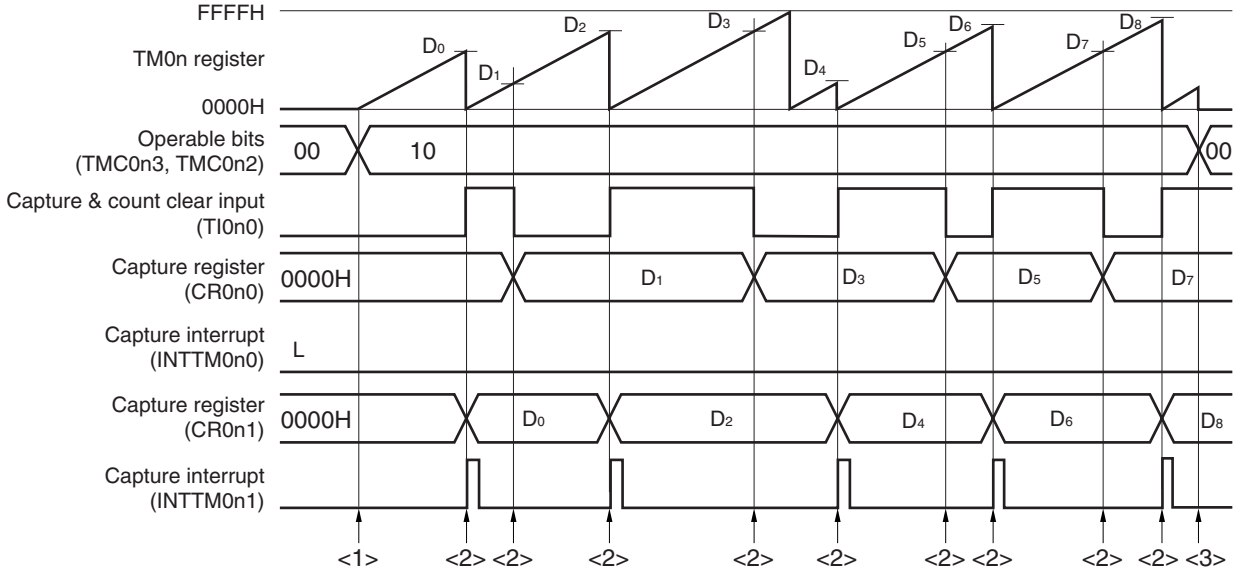
Remark n = 0 to 3

Figure 8-43. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode

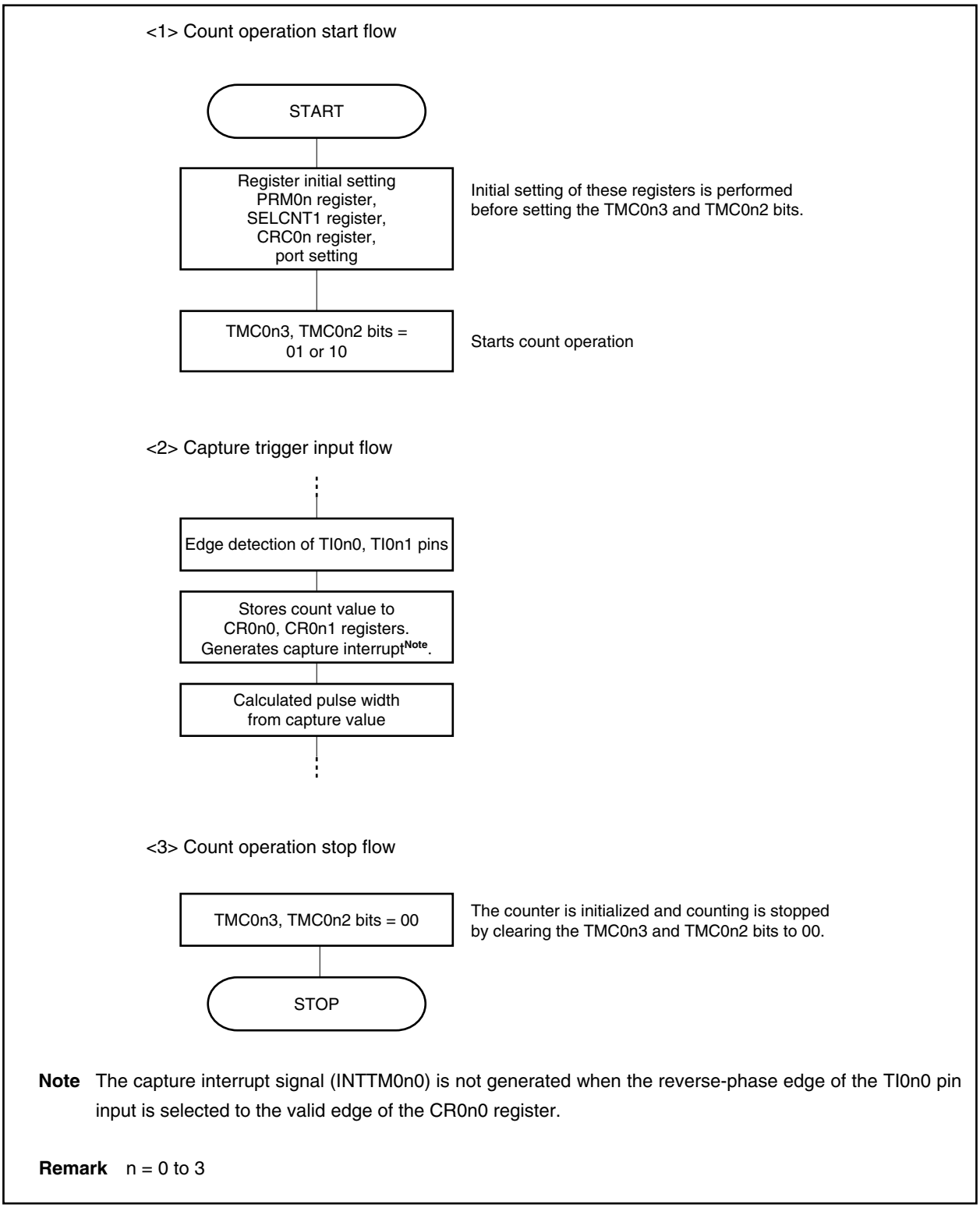


(b) Example of clear & start mode entered by TI0n0 pin valid edge



Remark n = 0 to 3

Figure 8-43. Example of Software Processing for Pulse Width Measurement (2/2)



Note The capture interrupt signal (INTTM0n0) is not generated when the reverse-phase edge of the TI0n0 pin input is selected to the valid edge of the CR0n0 register.

Remark n = 0 to 3

8.5 Special Use of TM0n

8.5.1 Rewriting CR0n1 register during TM0n operation

In principle, rewriting the CR0n0 and CR0n1 registers of the V850ES/KG2 when they are used as compare registers is prohibited while the TM0n register is operating (TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = other than 00).

However, the value of the CR0n1 register can be changed, even while the TM0n register is operating, using the following procedure if the CR0n1 register is used for PPG output and the duty factor is changed (change the value of the CR0n1 register immediately after its value matches the value of the TM0n register. If the value of the CR0n1 register is changed immediately before its value matches the TM0n register, an unexpected operation may be performed).

Procedure for changing value of the CR0n1 register

<1> Disable interrupt INTTM0n1 (TM0ICn0.TM0MKn1 bit = 1).
<2> Disable reversal of the timer output when the value of the TM0n register matches that of the CR0n1 register (TOC0n.TOC0n4 bit = 0).
<3> Change the value of the CR0n1 register.
<4> Wait for one cycle of the count clock of the TM0n register.
<5> Enable reversal of the timer output when the value of the TM0n register matches that of the CR0n1 register (TOC0n.TOC0n4 bit = 1).
<6> Clear the interrupt flag of INTTM0n1 to 0 (TM0ICn0.TM0IFn1 bit = 0).
<7> Enable interrupt INTTM0n1 (TM0ICn0.TM0MKn1 bit = 0).

Remark For the TM0ICn0 register, see **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

8.5.2 Setting LVS0n and LVR0n bits

(1) Usage of the LVS0n and LVR0n bits

The TOC0n.LVS0n and TOC0n.LVR0n bits are used to set the default value of the TO0n pin output and to invert the timer output without enabling the timer operation (TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = 00). Clear the LVS0n and LVR0n bits to 00 (default value: low-level output) when software control is unnecessary.

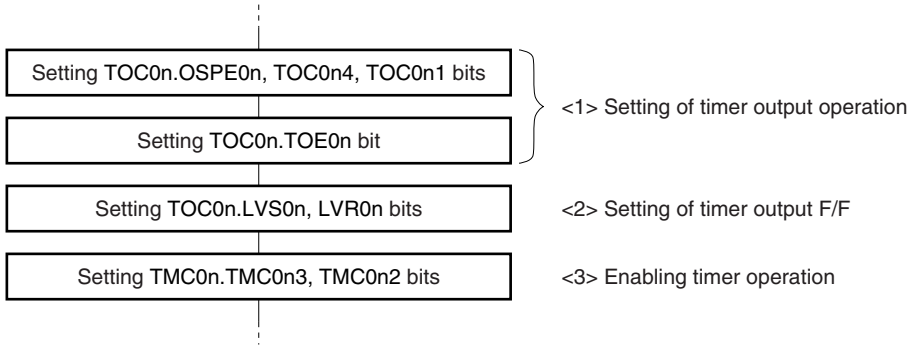
LVS0n Bit	LVR0n Bit	Timer Output Status
0	0	Not changed (low-level output)
0	1	Cleared (low-level output)
1	0	Set (high-level output)
1	1	Setting prohibited

Remark n = 0 to 3

(2) Setting the LVS0n and LVR0n bits

Set the LVS0n and LVR0n bits using the following procedure.

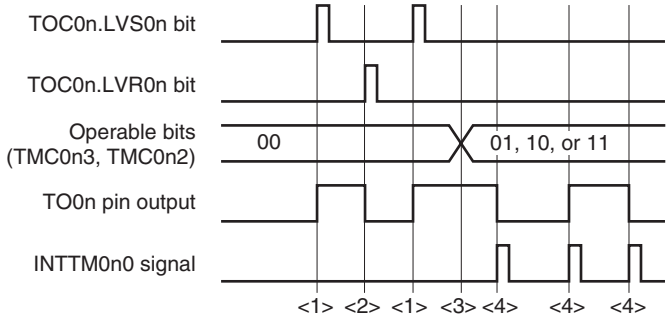
Figure 8-44. Example of Flow for Setting LVS0n and LVR0n Bits



Caution Be sure to set the LVS0n and LVR0n bits following steps <1>, <2>, and <3> above. Step <2> can be performed after <1> and before <3>.

Remark n = 0 to 3

Figure 8-45. Timing Example of LVR0n and LVS0n Bits



<1> The TO0n pin output goes high when the LVS0n and LVR0n bits = 10.

<2> The TO0n pin output goes low when the LVS0n and LVR0n bits = 01 (the pin output remains unchanged from the high level even if the LVS0n and LVR0n bits are cleared to 00).

<3> The timer starts operating when the TMC0n3 and TMC0n2 bits are set to 01, 10, or 11. Because the LVS0n and LVR0n bits were set to 10 before the operation was started, the TO0n pin output starts from the high level. After the timer starts operating, setting the LVS0n and LVR0n bits is prohibited until the TMC0n3 and TMC0n2 bits = 00 (disabling the timer operation).

<4> The output level of the TO0n pin is inverted each time an interrupt signal (INTTM0n0) is generated.

Remark n = 0 to 3

8.6 Cautions

(1) Alternate functions of TI0n0/TO0n pins

Channel	Pin	Alternate function	Remarks
TM00	TI000	P33/TO00/TIP00/TOP00	Shares the pin with TO00.
	TI001	P34/TO00/TIP01/TOP01	Shares the pin with TO00.
	TO00	P33/TI000/TIP00/TOP00	Assigned to two pins, P33 and P34.
		P34/TI001/TIP01/TOP01	
TM01	TI010	P35/TO01	Shares the pin with TO01.
	TI011	P50/KR0/RTP00	–
	TO01	P32/ASCK0/ADTRG	Assigned to two pins, P32 and P35.
		P35/TI010	
TM02	TI020	P92/A2/TO02	Shares the pin with TO02.
	TI021	P93/A3	–
	TO02	P30/TXD0	Assigned to two pins, P30 and P92.
		P92/TI020/A2	
TM03	TI030	P94/A4/TO03	Shares the pin with TO03.
	TI031	P95/A5	–
	TO03	P31/RXD0/INTP7	Assigned to two pins, P31 and P94.
		P94/TI030/A4	

(a) For TM00

- To perform the one-shot pulse output with detecting the valid edge of the TI000 pin as a trigger, use the output of the TO00 pin that functions alternately as P34.
  When using the output of the TO00 pin that functions alternately as P33, the TI000 pin that functions alternately as P33 cannot be used.
  When using only a software trigger (setting (1) TOC00.OSPT00 bit) as the start trigger for the one-shot pulse output, either of the P33 and P34 pins can be used as the TO00 pin output.
- To perform the TO00 pin output inversion operation by detecting the valid edge of the TI000 pin input, use the output of the TO00 pin that functions alternately as P34.
  When using the output of the TO00 pin that functions alternately as P33, the TI000 pin that functions alternately as P33 cannot be used. Therefore, the TO00 pin output inversion operation by detecting the valid edge of the TI000 pin input cannot be performed. When using the TO00 pin that functions alternately as P33, clear the TMC00.TMC001 bit to 0.

(b) For TM01

- To perform the one-shot pulse output with detecting the valid edge of the TI010 pin as a trigger, use the output of the TO01 pin that functions alternately as P32.
  When using the output of the TO01 pin that functions alternately as P35, the TI010 pin that functions alternately as P35 cannot be used.
  When using only a software trigger (setting (1) TOC01.OSPT01 bit) as the start trigger for the one-shot pulse output, either of the P32 and P35 pins can be used as the TO01 pin output.
- To perform the TO01 pin output inversion operation by detecting the valid edge of the TI010 pin input, use the output of the TO01 pin that functions alternately as P32.
  When using the output of the TO01 pin that functions alternately as P35, the TI010 pin that functions alternately as P35 cannot be used. Therefore, the TO01 pin output inversion operation by detecting the valid edge of the TI010 pin input cannot be performed. When using the TO01 pin that functions alternately as P35, clear the TMC01.TMC011 bit to 0.

(c) For TM02

- To perform the one-shot pulse output, use the output of the TO02 pin that functions alternately as P30. The output of the TO02 pin that functions alternately as P92 cannot be used for one-shot pulse output not only when using the detection of the TI020 pin valid edge as a trigger but also when using only the software trigger (setting (1) TOC02.OSPT02 bit) as a start trigger.
- To perform the TO02 pin output inversion operation by detecting the valid edge of the TI020 pin input, use the output of the TO02 pin that functions alternately as P30.
  When using the output of the TO02 pin that functions alternately as P92, the TI020 pin that functions alternately as P92 cannot be used. Therefore, the TO02 pin output inversion operation by detecting the valid edge of the TI020 pin input cannot be performed. When using the TO02 pin that functions alternately as P92, clear the TMC02.TMC021 bit to 0.

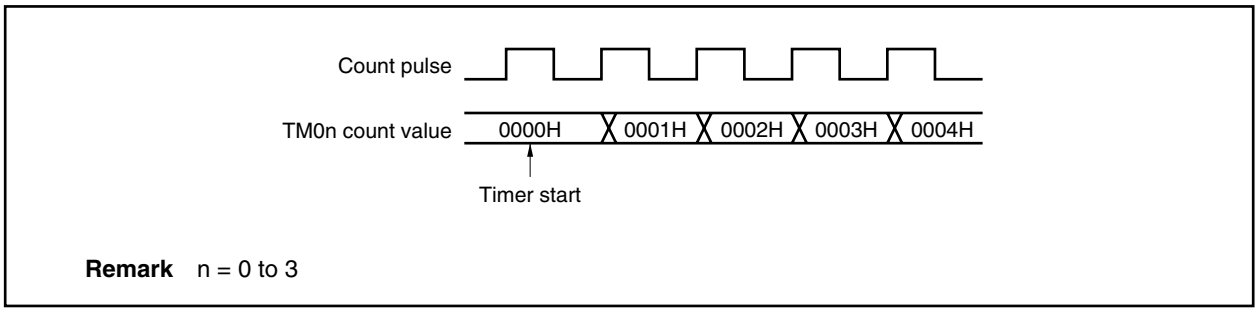
(d) For TM03

- To perform the one-shot pulse output, use the output of the TO03 pin that functions alternately as P31. The output of the TO03 pin that functions alternately as P94 cannot be used for one-shot pulse output not only when using the detection of the TI030 pin valid edge as a trigger but also when using only the software trigger (setting (1) TOC03.OSPT03 bit) as a start trigger.
- To perform the TO03 pin output inversion operation by detecting the valid edge of the TI030 pin input, use the output of the TO03 pin that functions alternately as P31.
  When using the output of the TO03 pin that functions alternately as P94, the TI030 pin that functions alternately as P94 cannot be used. Therefore, the TO03 pin output inversion operation by detecting the valid edge of the TI030 pin input cannot be performed. When using the TO03 pin that functions alternately as P94, clear the TMC03.TMC031 bit to 0.

(2) Error on starting timer

An error of up to 1 clock occurs before the match signal is generated after the timer has been started. This is because the count of the TM0n register is started asynchronously to the count pulse.

Figure 8-46. Count Start Timing of TM0n Register



Remark n = 0 to 3

(3) Setting CR0n0 and CR0n1 registers (in the mode in which clear & start occurs upon match between TM0n register and CR0n0 register)

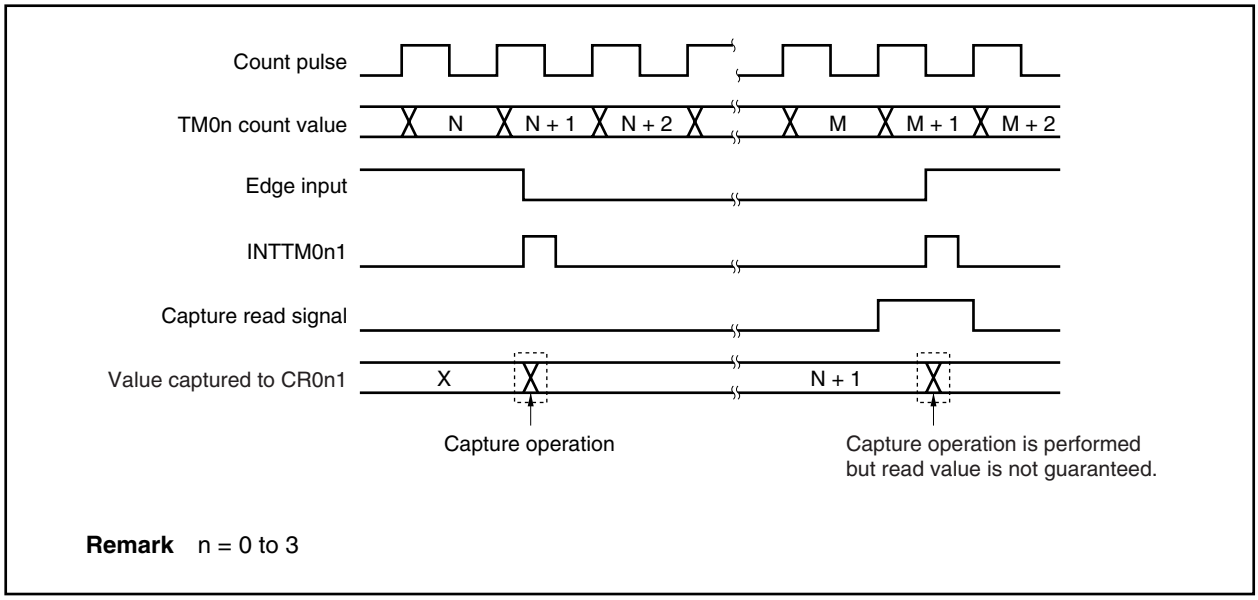
Set the CR0n0 and CR0n1 registers to a value other than 0000H (when using these registers as external event counters, one-pulse count operation is not possible).

Remark n = 0 to 3

(4) Data hold timing of capture register

(a) If the valid edge of the TI0n1/TI0n0 pin is input while the CR0n0/CR0n1 register is read, the CR0n0/CR0n1 register performs capture operation, but the read value at this time is not guaranteed. However, the interrupt request signal (INTTM0n0/INTTM0n1) is generated as a result of detection of the valid edge.

Figure 8-47. Data Hold Timing of Capture Register



Remark n = 0 to 3

(b) The values of the CR0n0 and CR0n1 registers are not guaranteed after 16-bit timer/event counter 0n has stopped.

(5) Setting valid edge

Set the valid edge of the TI0n0 pin while the timer operation is stopped (TMC0n.TMC0n3 and TMC0n.TMC0n2 bits = 00). Set the valid edge by using the PRM0n.ESn00 and PRM0n.ESn01 bits.

(6) Re-triggering one-shot pulse

Make sure that the trigger is not generated while an active level is being output in the one-shot pulse output mode. Be sure to input the next trigger after the current active level is output.

Remark n = 0 to 3

(7) Operation of OVF0n flag

(a) Setting of OVF0n flag

The TMC0n.OVF0n flag is set to 1 in the following case in addition to when the TM0n register overflows.

Select the mode in which clear & start occurs upon match between the TM0n register and the CR0n0 register.

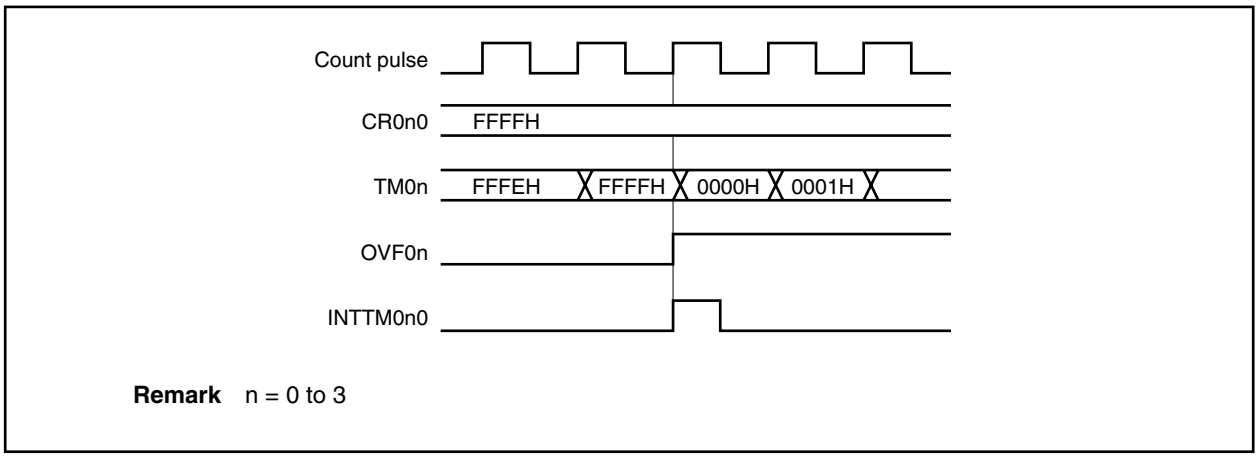
↓

Set the CR0n0 register to FFFFH

↓

When the TM0n register is cleared from FFFFH to 0000H upon match with the CR0n0 register

Figure 8-48. Operation Timing of OVF0n Flag



Remark n = 0 to 3

(b) Clearing of OVF0n flag

After the TM0n register overflows, clearing OVF0n flag is invalid and set (1) again even if the OVF0n flag is cleared (0) before the next count clock is counted (before TM0n register becomes 0001H).

Remark n = 0 to 3

(8) One-shot pulse output

One-shot pulse output operates normally in either the free-running timer mode or the mode in which clear & start occurs on the valid edge of the TI0n0 pin. In the mode in which clear & start occurs upon match between the TM0n register and the CR0n0 register, one-shot pulse output is not possible.

Remark n = 0 to 3

(9) Capture operation

(a) If valid edge of TI0n0 pin is specified for count clock

If the valid edge of the TI0n0 pin is specified for the count clock, the capture register that specified the TI0n0 pin as the trigger does not operate normally.

(b) To ensure that signals input from TI0n1 and TI0n0 pins are correctly captured

To accurately capture the count value, the pulse input to the TI0n0 and TI0n1 pins as a capture trigger must be wider than two count clocks selected by the PRM0n and SELCNT1 registers.

(c) Interrupt signal generation

Although a capture operation is performed at the falling edge of the count clock, an interrupt request signal (INTTM0n0, INTTM0n1) is generated at the rising edge of the next count clock.

(d) Note when CRC0n.CRC0n1 bit is set to 1

When the count value of the TM0n register is captured to the CR0n0 register in the phase reverse to the signal input to the TI0n0 pin, the interrupt signal (INTTM0n0) is not generated after the count value is captured. If the valid edge is detected on the TI0n1 pin during this operation, the capture operation is not performed but the INTTM0n0 signal is generated as an external interrupt signal. Mask the INTTM0n0 signal when the external interrupt is not used.

Remark n = 0 to 3

(10) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 0n is enabled after reset and while the TI0n0 or TI0n1 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI0n0 or TI0n1 pin, then the high level of the TI0n0 or TI0n1 pin is detected as the rising edge. Note this when the TI0n0 or TI0n1 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for noise elimination

The sampling clock for noise elimination differs depending on whether the valid edge of TI0n0 is used for the count clock or as a capture trigger. In the former case, sampling is performed using $f_{XX}/4$, and in the latter case, sampling is performed using the count clock selected by the PRM0n and SELCNT1 registers.

When the signal input to the TI0n0 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated.

Remarks 1. f_{XX}: Main clock frequency

2. n = 0 to 3

CHAPTER 9 8-BIT TIMER/EVENT COUNTER 5

In the V850ES/KG2, two channels of 8-bit timer/event counter 5 are provided.

9.1 Functions

8-bit timer/event counter 5n has the following two modes (n = 0, 1).

- Mode using 8-bit timer/event counter alone (individual mode)
- Mode using cascade connection (16-bit resolution: cascade connection mode)

These two modes are described below.

(1) Mode using 8-bit timer/event counter alone (individual mode)

8-bit timer/event counter 5n operates as an 8-bit timer/event counter.
The following functions can be used.

- Interval timer
- External event counter
- Square-wave output
- PWM output

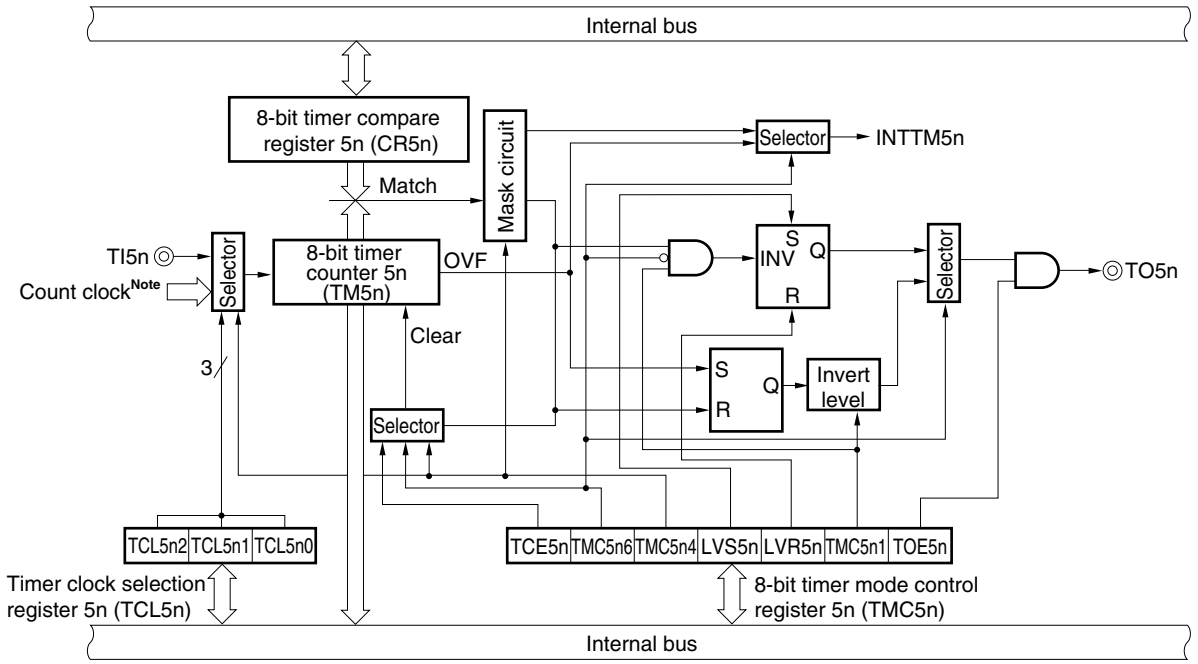
(2) Mode using cascade connection (16-bit resolution: cascade connection mode)

8-bit timer/event counter 5n operates as a 16-bit timer/event counter by connecting the TM5n register in cascade. The following functions can be used.

- Interval timer with 16-bit resolution
- External event counter with 16-bit resolution
- Square-wave output with 16-bit resolution

The block diagram of 8-bit timer/event counter 5n is shown next.

Figure 9-1. Block Diagram of 8-Bit Timer/Event Counter 5n



Note The count clock is set by the TCL5n register.

Remark n = 0, 1

9.2 Configuration

8-bit timer/event counter 5n includes the following hardware.

Table 9-1. Configuration of 8-Bit Timer/Event Counter 5n

Item	Configuration
Timer registers	8-bit timer counter 5n (TM5n) 16-bit timer counter 5 (TM5): Only when using cascade connection
Registers	8-bit timer compare register 5n (CR5n) 16-bit timer compare register 5 (CR5): Only when using cascade connection
Timer output	1 (TO5n pin)
Control registers Note	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) 16-bit timer mode control register 5 (TMC5): Only when using cascade connection

Note When using the functions of the TI5n and TO5n pins, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

Remark n = 0, 1

(1) 8-bit timer counter 5n (TM5n)

The TM5n register is an 8-bit read-only register that counts the count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

Through cascade connection, the TM5n registers can be used as a 16-bit timer.

When using the TM50 register and the TM51 register in cascade as a 16-bit timer, these registers can be read only in 16-bit units. Therefore, read these registers twice and compare the values, taking into consideration that the reading occurs during a count change.

After reset: 00H R Address: TM50 FFFFF5C0H, TM51 FFFFF5C1H

	7	6	5	4	3	2	1	0
TM5n								

(n = 0, 1)

The count value is reset to 00H in the following cases.

<1> Reset

<2> When the TMC5n.TCE5n bit is cleared (0)

<3> The TM5n register and CR5n register match in the mode in which clear & start occurs on a match between the TM5n register and the CR5n register

Caution When connected in cascade, these registers become 0000H even when the TCE50 bit in the lowest timer (TM50) is cleared.

Remark n = 0, 1

(2) 8-bit timer compare register 5n (CR5n)

The CR5n register can be read and written in 8-bit units.

In a mode other than the PWM mode, the value set to the CR5n register is always compared to the count value of the TM5n register, and if the two values match, an interrupt request signal (INTTM5n) is generated.

In the PWM mode, TM5n register overflow causes the TO5n pin output to change to the active level, and when the values of the TM5n register and the CR5n register match, the TO5n pin output changes to the inactive level.

The value of the CR5n register can be set in the range of 00H to FFH.

When using the TM50 register and TM51 register in cascade as a 16-bit timer, the CR50 register and CR51 register operate as 16-bit timer compare register 5 (CR5). The counter value and register value are compared in 16-bit lengths, and if they match, an interrupt request signal (INTTM50) is generated.

After reset: 00H R/W Address: CR50 FFFFF5C2H, CR51 FFFFF5C3H

	7	6	5	4	3	2	1	0
CR5n								

(n = 0, 1)

Cautions 1. In the mode in which clear & start occurs upon a match of the TM5n register and CR5n register (TMC5n.TMC5n6 bit = 0), do not write a different value to the CR5n register during the count operation.

2. In the PWM mode, set the CR5n register rewrite interval to three or more count clocks (clock selected with the TCL5n register).

3. Before changing the value of the CR5n register when using a cascade connection, be sure to stop the timer operation.

Remark n = 0, 1

9.3 Registers

The following two registers are used to control 8-bit timer/event counter 5n.

- Timer clock selection register 5n (TCL5n)
- 8-bit timer mode control register 5n (TMC5n)

Remark To use the functions of the TI5n and TO5n pins, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

(1) Timer clock selection register 5n (TCL5n)

The TCL5n register sets the count clock of 8-bit timer/event counter 5n and the valid edge of the TI5n pin input.

The TCL5n register can be read or written in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TCL50 FFFFF5C4H, TCL51 FFFFF5C5H

	7	6	5	4	3	2	1	0
TCL5n	0	0	0	0	0	TCL5n2	TCL5n1	TCL5n0

(n = 0, 1)

TCL5n2	TCL5n1	TCL5n0	Count clock selection[Note]		
			Clock	f_{XX}	
				20 MHz	10 MHz
0	0	0	Falling edge of TI5n	–	–
0	0	1	Rising edge of TI5n	–	–
0	1	0	f_{XX}	Setting prohibited	100 ns
0	1	1	$f_{XX}/2$	100 ns	200 ns
1	0	0	$f_{XX}/4$	200 ns	0.4 μs
1	0	1	$f_{XX}/64$	3.2 μs	6.4 μs
1	1	0	$f_{XX}/256$	12.8 μs	25.6 μs
1	1	1	INTTM010	–	–

Note When the internal clock is selected, set so as to satisfy the following conditions.

REGC = V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: Count clock ≤ 5 MHz

REGC = V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

Caution Before overwriting the TCL5n register with different data, stop the timer operation.

Remark When the TM5n register is connected in cascade, the TCL51 register settings are invalid.

(2) 8-bit timer mode control register 5n (TMC5n)

The TMC5n register performs the following six settings.

- Controls counting by the TM5n register
- Selects the operation mode of the TM5n register
- Selects the individual mode or cascade connection mode
- Sets the status of the timer output flip-flop
- Controls the timer output flip-flop or selects the active level in the PWM (free-running timer) mode
- Controls timer output

The TMC5n register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TMC50 FFFFF5C6H, TMC51 FFFFF5C7H

TMC5n (n = 0, 1)

<7>	6	5	4	<3>	<2>	1	<0>
TCE5n	TMC5n6	0	TMC514[Note]	LVS5n	LVR5n	TMC5n1	TOE5n

TCE5n	Control of count operation of 8-bit timer/event counter 5n
0	Counting is disabled after the counter is cleared to 0 (counter disabled)
1	Start count operation

TMC5n6	Selection of operation mode of 8-bit timer/event counter 5n
0	Mode in which clear & start occurs on match between TM5n register and CR5n register
1	PWM (free-running timer) mode

TMC514	Selection of individual mode or cascade connection mode for 8-bit timer/event counter 51
0	Individual mode
1	Cascade connection mode (connected with 8-bit timer/event counter 50)

LVS5n	LVR5n	Setting of status of timer output F/F
0	0	Unchanged
0	1	Reset timer output F/F to 0
1	0	Set timer output F/F to 1
1	1	Setting prohibited

TMC5n1	Other than PWM (free-running timer) mode (TMC5n6 bit = 0)	PWM (free-running timer) mode (TMC5n6 bit = 1)
	Controls timer F/F	Selects active level
0	Disable inversion operation	High active
1	Enable inversion operation	Low active

TOE5n	Timer output control
0	Disable output (TO5n pin is low level)
1	Enable output

Note Bit 4 of the TMC50 register is fixed to 0.

Cautions 1. Because the TO51 and TI51 pins are alternate functions of the same pin, only one can be used at one time.

2. The LVS5n and LVR5n bit settings are valid in modes other than the PWM mode.

3. Do not set <1> to <4> below at the same time. Set as follows.

<1> Set the TMC5n1, TMC5n6, and TMC514[Note] bits: Setting of operation mode

<2> Set the TOE5n bit for timer output enable: Timer output enable

<3> Set the LVS5n and LVR5n bits (Caution 2): Setting of timer output F/F

<4> Set the TCE5n bit

Remarks 1. In the PWM mode, the PWM output is set to the inactive level by the TCE5n bit = 0.

2. When the LVS5n and LVR5n bits are read, 0 is read.

3. The values of the TMC5n6, LVS5n, LVR5n, TMC5n1, and TOE5n bits are reflected to the TO5n output regardless of the TCE5n bit value.

9.4 Operation

9.4.1 Operation as interval timer

8-bit timer/event counter 5n operates as an interval timer that repeatedly generates interrupts at the interval of the count value preset in the CR5n register. If the count value in the TM5n register matches the value set in the CR5n register, the value of the TM5n register is cleared to 00H and counting is continued, and at the same time, an interrupt request signal (INTTM5n) is generated.

Setting method

<1> Set each register.
- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation and selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register (TMC5n register = 0000xx00B, ×: don't care).

<2> When the TMC5n.TCE5n bit is set to 1, the count operation starts.

<3> When the values of the TM5n register and CR5n register match, the INTTM5n signal is generated (TM5n register is cleared to 00H).

<4> Then, the INTTM5n signal is repeatedly generated at the same interval. To stop counting, set the TCE5n bit = 0.

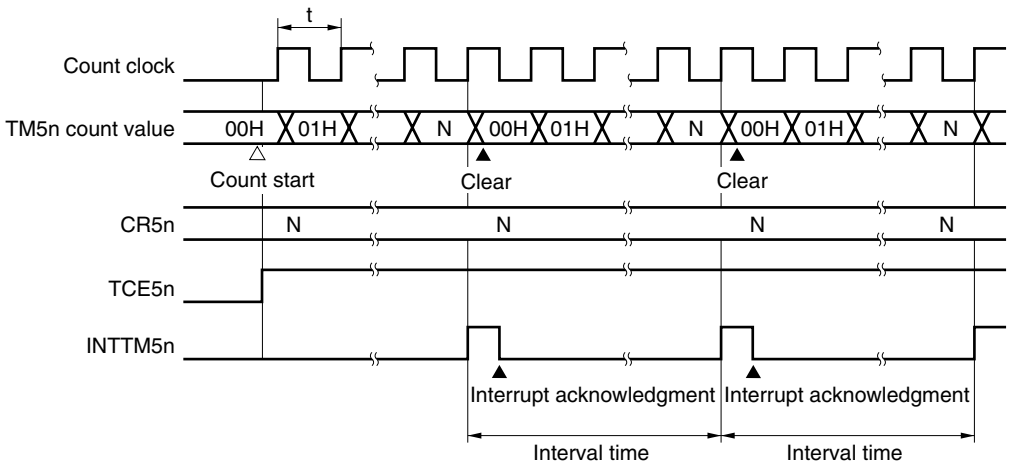
Interval time = (N + 1) × t: N = 00H to FFH

Caution During interval timer operation, do not rewrite the value of the CR5n register.

Remark n = 0, 1

Figure 9-2. Timing of Interval Timer Operation (1/2)

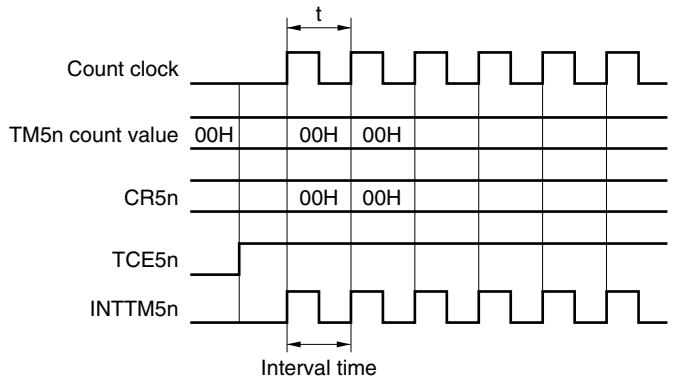
Basic operation



Remark n = 0, 1

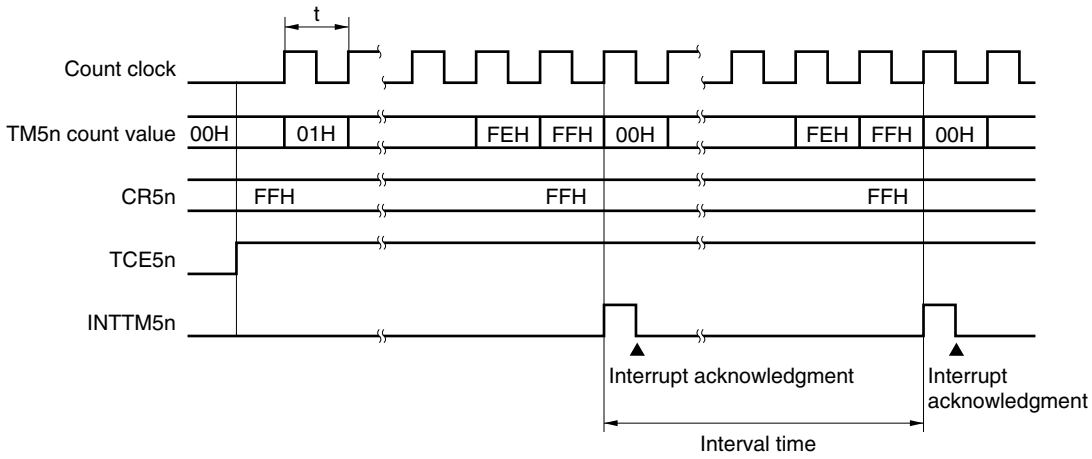
Figure 9-2. Timing of Interval Timer Operation (2/2)

When CR5n register = 00H



Remark n = 0, 1

When CR5n register = FFH



Remark n = 0, 1

9.4.2 Operation as external event counter

The external event counter counts the number of clock pulses input to the TI5n pin from an external source by using the TM5n register.

Each time the valid edge specified by the TCL5n register is input to the TI5n pin, the TM5n register is incremented. Either the rising edge or the falling edge can be specified as the valid edge.

When the count value of the TM5n register matches the value of the CR5n register, the TM5n register is cleared to 00H and an interrupt request signal (INTTM5n) is generated.

Setting method

<1> Set each register.

- TCL5n register: Selects the TI5n pin input edge.
  Falling edge of TI5n pin → TLC5n register = 00H
  Rising edge of TI5n pin → TCL5n register = 01H
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register, disables timer output F/F inversion operation, and disables timer output.
  (TMC5n register = 0000xx00B, ×: don't care)
- For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TMC5n.TCE5n bit is set to 1, the counter counts the number of pulses input from the TI5n pin.

<3> When the values of the TM5n register and CR5n register match, the INTTM5n signal is generated (TM5n register is cleared to 00H).

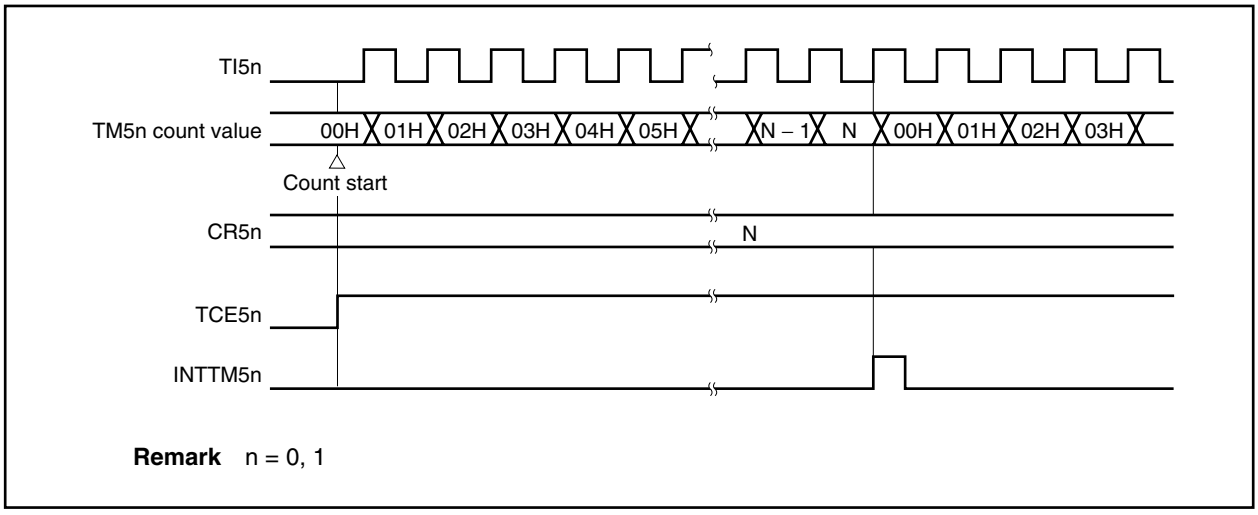
<4> Then, the INTTM5n signal is generated each time the values of the TM5n register and CR5n register match.

INTTM5n signal is generated when the valid edge of TI5n pin is input N + 1 times: N = 00H to FFH

Caution During external event counter operation, do not rewrite the value of the CR5n register.

Remark n = 0, 1

Figure 9-3. Timing of External Event Counter Operation (with Rising Edge Specified)



Remark n = 0, 1

9.4.3 Square-wave output operation

A square wave with any frequency can be output at an interval determined by the value preset in the CR5n register.

By setting the TMC5n.TOE5n bit to 1, the output status of the TO5n pin is inverted at an interval determined by the count value preset in the CR5n register. In this way, a square wave of any frequency can be output (duty = 50%) (n = 0, 1).

Setting method

<1> Set each register.

- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register, sets initial value of timer output, enables timer output F/F inversion operation, and enables timer output.
  (TMC5n register = 00001011B or 00000111B)
- For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TMC5n.TCE5n bit is set to 1, counting starts.

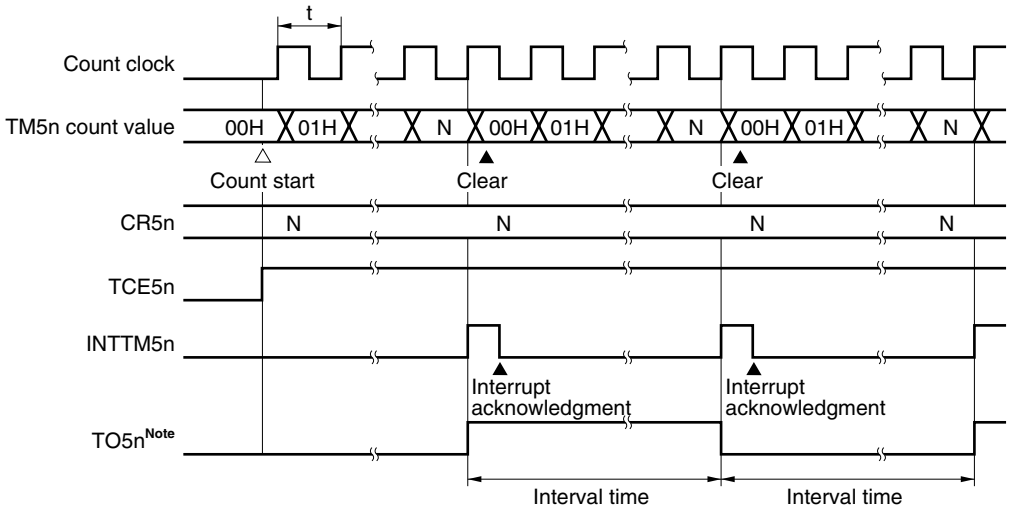
<3> When the values of the TM5n register and CR5n register match, the timer output F/F is inverted. Moreover, the INTTM5n signal is generated and the TM5n register is cleared to 00H.

<4> Then, the timer output F/F is inverted during the same interval and a square wave is output from the TO5n pin.

Frequency = 1/2t(N + 1): N = 00H to FFH

Caution Do not rewrite the value of the CR5n register during square-wave output.

Figure 9-4. Timing of Square-Wave Output Operation



Note The initial value of the TO5n pin output can be set using the TMC5n.LVS5n and TMC5n.LVR5n bits.

Remark n = 0, 1

9.4.4 8-bit PWM output operation

By setting the TMC5n.TMC5n6 bit to 1, 8-bit timer/event counter 5n performs PWM output.

Pulses with a duty factor determined by the value set in the CR5n register are output from the TO5n pin.

Set the width of the active level of the PWM pulse in the CR5n register. The active level can be selected using the TMC5n.TMC5n1 bit.

The count clock can be selected using the TCL5n register.

PWM output can be enabled/disabled by the TMC5n.TOE5n bit.

Caution The CR5n register rewrite interval must be three or more operation clocks (set by the TCL5n register).

Use method

<1> Set each register.

- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects PWM mode, and leave timer output F/F unchanged, sets active level, and enables timer output.
  (TMC5n register = 01000001B or 01000011B)
- For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TMC5n.TCE5n bit is set to 1, counting starts.

PWM output operation

<1> When counting starts, PWM output (output from the TO5n pin) outputs the inactive level until an overflow occurs.

<2> When an overflow occurs, the active level set by setting method <1> is output. The active level is output until the value of the CR5n register and the count value of the TM5n register match. An interrupt request signal (INTTM5n) is generated.

<3> When the value of the CR5n register and the count value of the TM5n register match, the inactive level is output and continues to be output until an overflow occurs again.

<4> Then, steps <2> and <3> are repeated until counting is stopped.

<5> When counting is stopped by clearing TCE5n bit to 0, PWM output becomes inactive.

Cycle = 256t, active level width = Nt, duty = N/256: N = 00H to FFH

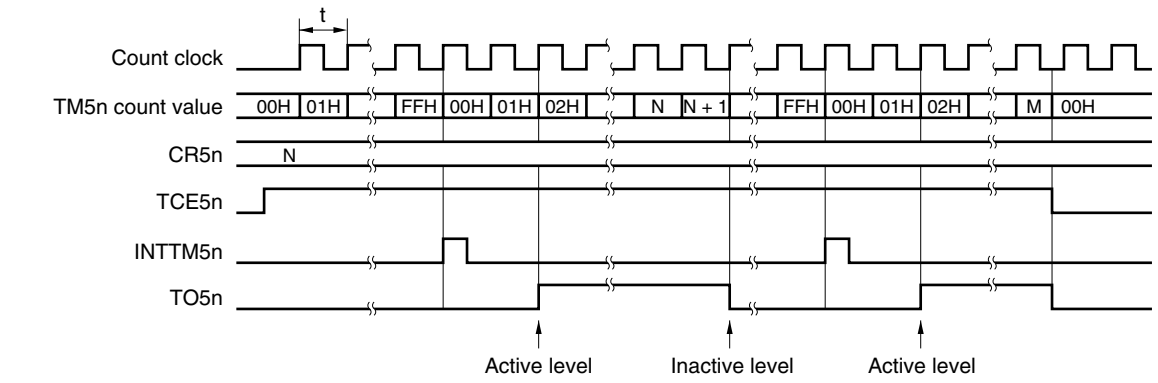
Remarks 1. n = 0, 1

2. For the detailed timing, refer to **Figure 9-5 Timing of PWM Output Operation** and **Figure 9-6 Timing of Operation Based on CR5n Register Transitions**.

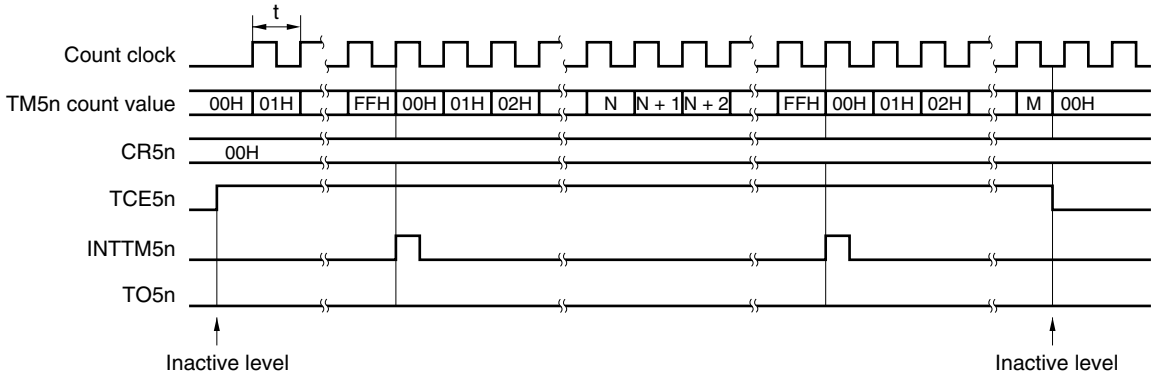
(a) Basic operation of PWM output

Figure 9-5. Timing of PWM Output Operation

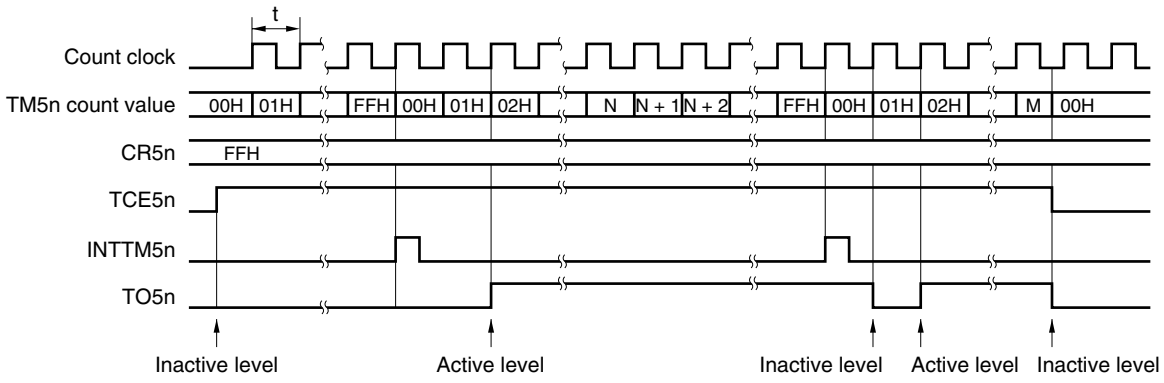
Basic operation (active level = H)



When CR5n register = 00H



When CR5n register = FFH



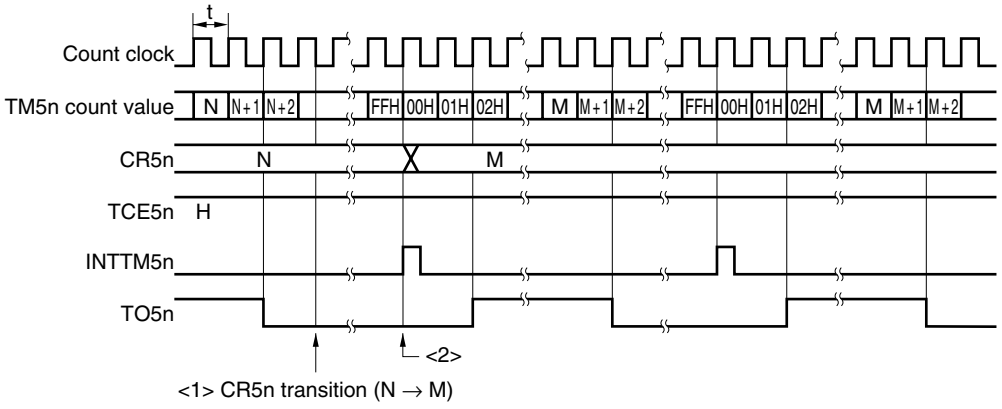
Remark n = 0, 1

(b) Operation based on CR5n register transitions

Figure 9-6. Timing of Operation Based on CR5n Register Transitions

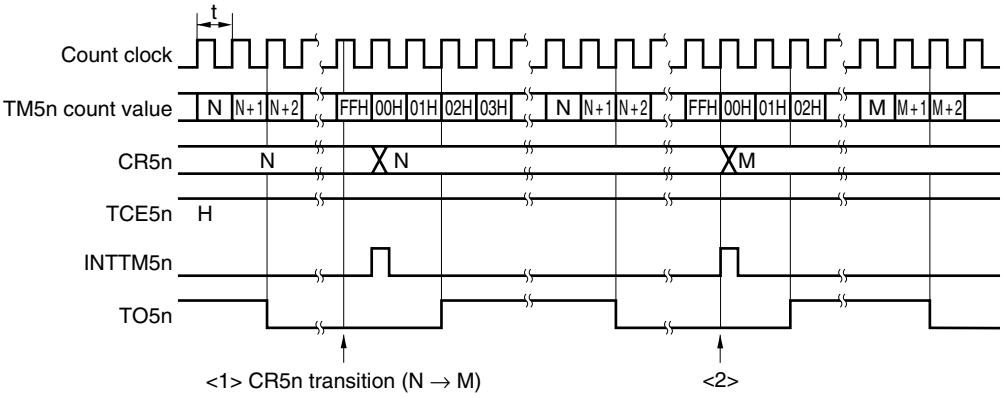
When the value of the CR5n register changes from N to M before the rising edge of the FFH clock

→ The value of the CR5n register is transferred at the overflow that occurs immediately after.



When the value of the CR5n register changes from N to M after the rising edge of the FFH clock

→ The value of the CR5n register is transferred at the second overflow.



Caution In the case of reload from the CR5n register between <1> and <2>, the value that is actually used differs (Read value: M; Actual value of CR5n register: N).

Remark n = 0, 1

9.4.5 Operation as interval timer (16 bits)

The 16-bit resolution timer/event counter mode is selected by setting the TMC51.TMC514 bit to 1.

8-bit timer/event counter 5n operates as an interval timer by repeatedly generating interrupts using the count value preset in 16-bit timer compare register 5 (CR5) as the interval.

Setting method

<1> Set each register.

- TCL50 register: Selects the count clock (t)
  (The TCL51 register does not need to be set in cascade connection)
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TMC51 register: Selects the mode in which clear & start occurs on a match between TM5 register and CR5 register (×: don't care)

  (TMC50 register = 0000xx00B
  TMC51 register = 0001xx00B)

<2> Set the TMC51.TCE51 bit to 1. Then set the TMC50.TCE50 bit to 1 to start the count operation.

<3> When the values of the TM5 register and CR5 register connected in cascade match, the INTTM50 signal is generated (the TM5 register is cleared to 0000H).

<4> The INTTM50 signal is then generated repeatedly at the same interval.

Interval time = (N + 1) × t: N = 0000H to FFFFH

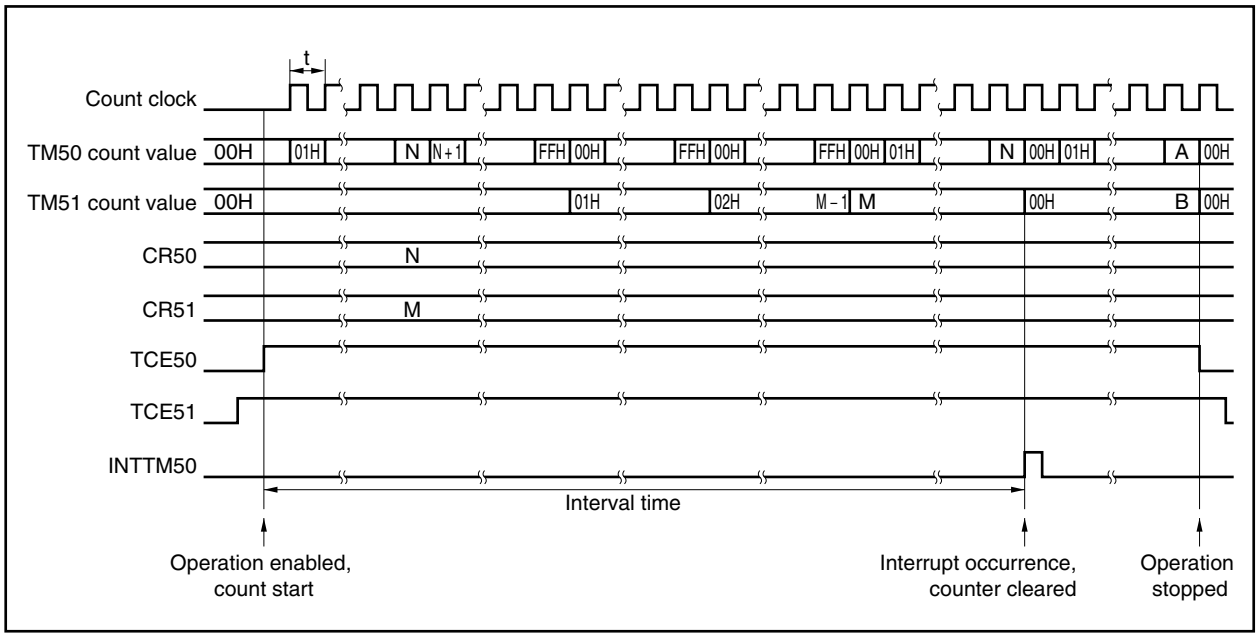
Cautions 1. To write using 8-bit access during cascade connection, set the TCE51 bit to 1 at operation start and then set the TCE50 bit to 1. When operation is stopped, clear the TCE50 bit to 0 and then clear the TCE51 bit to 0.

2. During cascade connection, TI50 input, TO50 output, and the INTTM50 signal are used. Do not use TI51 input, TO51 output, and the INTTM51 signal; mask them instead (for details, refer to CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION). Clear the LVS51, LVR51, TMC511, and TOE51 bits to 0.

3. Do not change the value of the CR5 register during timer operation.

Figure 9-7 shows a timing example of the cascade connection mode with 16-bit resolution.

Figure 9-7. Cascade Connection Mode with 16-Bit Resolution



9.4.6 Operation as external event counter (16 bits)

The 16-bit resolution timer/event counter mode is selected by setting the TMC51.TMC514 bit to 1.

The external event counter counts the number of clock pulses input to the TI50 pin from an external source using 16-bit timer counter 5 (TM5).

Setting method

<1> Set each register.

- TCL50 register: Selects the TI50 pin input edge.
  (The TCL51 register does not have to be set during cascade connection.)
  Falling edge of TI50 pin → TCL50 register = 00H
  Rising edge of TI50 pin → TCL50 register = 01H
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TMC51 registers: Stops count operation, selects the clear & stop mode entered on a match between the TM5 register and CR5 register, disables timer output F/F inversion, and disables timer output.
  (×: don't care)
  (TMC50 register = 0000xx00B
  TMC51 register = 0001xx00B)
- For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions.**

<2> Set the TMC51.TCE51 bit to 1. Then set the TMC50.TCE50 bit to 1 and count the number of pulses input from the TI50 pin.

<3> When the values of the TM5 register and CR5 register connected in cascade match, the INTTM50 signal is generated (the TM5 register is cleared to 0000H).

<4> The INTTM50 signal is then generated each time the values of the TM5 register and CR5 register match.

INTTM50 signal is generated when the valid edge of TI50 pin is input N + 1 times: N = 0000H to FFFFH

Cautions 1. During external event counter operation, do not rewrite the value of the CR5n register.

2. To write using 8-bit access during cascade connection, set the TCE51 bit to 1 and then set the TCE50 bit to 1. When operation is stopped, clear the TCE50 bit to 0 and then clear the TCE51 bit to 0 (n = 0, 1).

3. During cascade connection, TI50 input and the INTTM50 signal are used. Do not use TI51 input, TO51 output, and the INTTM51 signal; mask them instead (for details, refer to CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION). Clear the LVS51, LVR51, TMC511, and TOE51 bits to 0.

4. Do not change the value of the CR5 register during external event counter operation.

9.4.7 Square-wave output operation (16-bit resolution)

The 16-bit resolution timer/event counter mode is selected by setting the TMC51.TMC514 bit to 1.

8-bit timer/event counter 5n outputs a square wave of any frequency using the interval preset in 16-bit timer compare register 5 (CR5).

Setting method

<1> Set each register.

- TCL50 register: Selects the count clock (t)
  (The TCL51 register does not have to be set in cascade connection)
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TCM51 registers: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5 register and CR5 register.

LVS50	LVR50	Timer Output F/F Status Settings
1	0	High-level output
0	1	Low-level output

Enables timer output F/F inversion, and enables timer output.
(TMC50 register = 00001011B or 00000111B
TMC51 register = 00010000B)

- For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions.**

<2> Set the TMC51.TCE51 bit to 1. Then set the TMC50.TCE50 bit to 1 to start the count operation.

<3> When the values of the TM5 register and the CR5 register connected in cascade match, the TO50 timer output F/F is inverted. Moreover, the INTTM50 signal is generated and the TM5 register is cleared to 0000H.

<4> Then, the timer output F/F is inverted during the same interval and a square wave is output from the TO50 pin.

Frequency = 1/2t(N + 1): N = 0000H to FFFFH

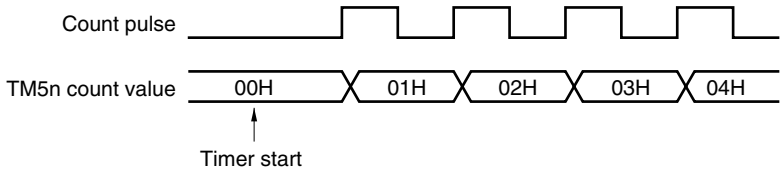
Caution Do not write a different value to the CR5 register during operation.

9.4.8 Cautions

(1) Error on starting timer

An error of up to 1 clock occurs before the match signal is generated after the timer has been started. This is because the TM5n register is started asynchronously to the count pulse.

Figure 9-8. Count Start Timing of TM5n Register



Remark n = 0, 1

CHAPTER 10 8-BIT TIMER H

In the V850ES/KG2, two channels of 8-bit timer H are provided.

10.1 Functions

8-bit timer Hn has the following functions (n = 0, 1).

- Interval timer
- Square ware output
- PWM output
- Carrier generator

10.2 Configuration

8-bit timer Hn includes the following hardware.

Table 10-1. Configuration of 8-Bit Timer Hn

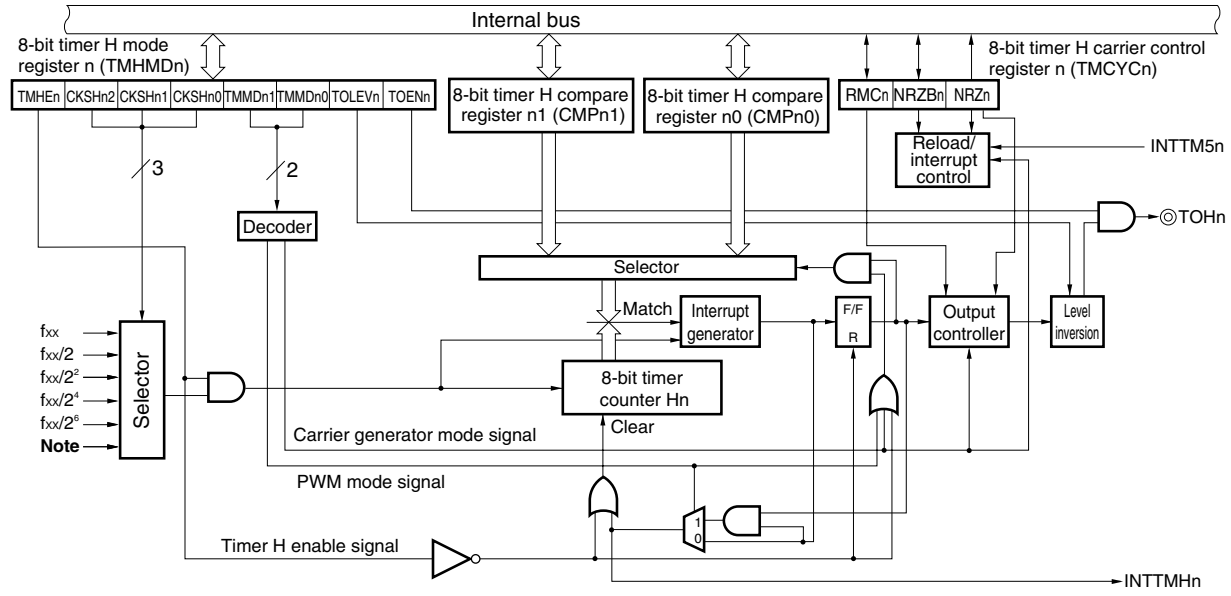
Item	Configuration
Timer registers	8-bit timer counter Hn: 1 each
Register	8-bit timer H compare register n0 (CMPn0): 1 each 8-bit timer H compare register n1 (CMPn1): 1 each
Timer outputs	TOHn, output controller
Control registers[Note]	8-bit timer H mode register n (TMHMDn) 8-bit timer H carrier control register n (TMCYCn)

Note To use the TOHn pin function, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

Remark n = 0, 1

The block diagram is shown below.

Figure 10-1. Block Diagram of 8-Bit Timer Hn



Note $f_{XX}/2^{10}$ when n = 0, f_{XT} when n = 1

Remark n = 0, 1

(1) 8-bit timer H compare register n0 (CMPn0)

This register can be read or written in 8-bit units. This register is used in all of the timer operation modes.

This register constantly compares the value set to the CMPn0 register with the count value of 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn) and inverts the output level of the TOHn pin.

Rewrite the value of the CMPn0 register while the timer is stopped (TMHMDn.TMHEn bit = 0).

Reset sets this register to 00H.

After reset: 00H R/W Address: CMP00 FFFFF582H, CMP10 FFFFF592H

	7	6	5	4	3	2	1	0
CMPn0								

(n = 0, 1)

Caution Rewriting the CMPn0 register during timer count operation is prohibited.

(2) 8-bit timer H compare register n1 (CMPn1)

This register can be read or written in 8-bit units.

This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to the CMPn1 register with the count value of 8-bit timer counter Hn and, when the two values match, inverts the output level of the TOHn pin. No interrupt request signal is generated.

In the carrier generator mode, the CMPn1 register always compares the value set to the CMPn1 register with the count value of 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn). At the same time, the count value is cleared.

The CMPn1 register can be rewritten during timer count operation.

If the value of the CMPn1 register is rewritten while the timer is operating, the new value is latched and transferred to the CMPn1 register when the count value of the timer matches the old value of the CMPn1 register, and then the value of the CMPn1 register is changed to the new value. If matching of the count value and the CMPn1 register value and writing a value to the CMPn1 register conflict, the value of the CMPn1 register is not changed.

Reset sets this register to 00H.

After reset: 00H R/W Address: CMP01 FFFFF583H, CMP11 FFFFF593H

	7	6	5	4	3	2	1	0
CMPn1								

(n = 0, 1)

The CMPn1 register can be rewritten during timer count operation.

In the carrier generator mode, after the CMPn1 register is set, if the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, an interrupt request signal (INTTMHn) is generated. At the same time, the value of 8-bit timer counter Hn is cleared to 00H.

If the set value of the CMPn1 register is rewritten during timer operation, the reload timing is when the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match. If the transfer timing and write to the CMPn1 register from the CPU conflict, transfer is not performed.

Caution In the PWM output mode and carrier generator mode, be sure to set the CMPn1 register when starting the timer count operation (TMHMDn.TMHEn bit = 1) after the timer count operation was stopped (TMHEn bit = 0) (be sure to set again even if setting the same value to the CMPn1 register).

10.3 Registers

The registers that control 8-bit timer Hn are as follows.

- 8-bit timer H mode register n (TMHMDn)
- 8-bit timer H carrier control register n (TMCYCn)

Remarks 1. To use the TOHn pin function, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. n = 0, 1

(1) 8-bit timer H mode register n (TMHMDn)

The TMHMDn register controls the mode of 8-bit timer Hn.

TMHMDn register can be read or written in 8-bit or 1-bit units.

Reset sets TMHMDn to 00H.

Remark n = 0, 1

(a) 8-bit timer H mode register 0 (TMHMD0)

After reset: 00H R/W Address: FFFFF580H

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKSH02	CKSH01	CKSH00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	8-bit timer H0 operation enable
0	Stop timer count operation (8-bit timer counter H0 = 00H)
1	Enable timer count operation (Counting starts when clock is input)

CKSH02	CKSH01	CKSH00	Selection of count clock			
			Count clock[Note]	f_{XX} = 20 MHz	f_{XX} = 16.0 MHz	f_{XX} = 10.0 MHz
0	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	1	$f_{XX}/16$	800 ns	1 μs	1.6 μs
1	0	0	$f_{XX}/64$	1.6 μs	4 μs	6.4 μs
1	0	1	$f_{XX}/1024$	51.2 μs	64 μs	102.4 μs
Other than above			Setting prohibited			

TMMD01	TMMD00	8-bit timer H0 operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV0	Timer output level control (default)
0	Low level
1	High level

TOEN0	Timer output control
0	Disable output
1	Enable output

Note Set so as to satisfy the following conditions.

REGC = V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: Count clock ≤ 5 MHz

REGC = V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

Cautions 1. When the TMHE0 bit = 1, setting bits other than those of the TMHMD0 register is prohibited.

2. In the PWM output mode and carrier generator mode, be sure to set the CMP01 register when starting the timer count operation (TMHE0 bit = 1) after the timer count operation was stopped (TMHE0 bit = 0) (be sure to set again even if setting the same value to the CMP01 register).

3. When using the carrier generator mode, set 8-bit timer H0 count clock frequency to six times 8-bit timer/event counter 50 count clock frequency or higher.

(b) 8-bit timer H mode register 1 (TMHMD1)

After reset: 00H R/W Address: FFFFF590H

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKSH12	CKSH11	CKSH10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	8-bit timer H1 operation enable
0	Stop timer count operation (8-bit timer counter H1 = 00H)
1	Enable timer count operation (Counting starts when clock is input)

CKSH12	CKSH11	CKSH10	Selection of count clock			
			Count clock[Note]	f_{XX} = 20.0 MHz	f_{XX} = 16.0 MHz	f_{XX} = 10.0 MHz
0	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	1	$f_{XX}/16$	800 ns	1 μs	1.6 μs
1	0	0	$f_{XX}/64$	1.6 μs	4 μs	6.4 μs
1	0	1	f_{XT} (subclock)			
Other than above			Setting prohibited			

TMMD11	TMMD10	8-bit timer H1 operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (default)
0	Low level
1	High level

TOEN1	Timer output control
0	Disable output
1	Enable output

Note Set so as to satisfy the following conditions.

REGC = V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: Count clock ≤ 5 MHz

REGC = V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

Cautions 1. When the TMHE1 bit = 1, setting bits other than those of the TMHMD1 register is prohibited.

2. In the PWM output mode and carrier generator mode, be sure to set the CMP11 register when starting the timer count operation (TMHE1 bit = 1) after the timer count operation was stopped (TMHE1 bit = 0) (be sure to set again even if setting the same value to the CMP11 register).

3. When using the carrier generator mode, set 8-bit timer H1 count clock frequency to six times 8-bit timer/event counter 51 count clock frequency or higher.

(2) 8-bit timer H carrier control register n (TMCYCn)

This register controls the 8-bit timer Hn remote control output and carrier pulse output status.

TMCYCn register can be read or written in 8-bit or 1-bit units. The NRZn bit is a read-only bit.

Reset sets TMCYCn to 00H.

Remark n = 0, 1

After reset: 00H R/W Address: TMCYC0 FFFFF581H, TMCYC1 FFFFF591H

	7	6	5	4	3	2	1	<0>
TMCYCn	0	0	0	0	0	RMCn	NRZBn	NRZn

(n = 0, 1)

RMCn	NRZBn	Remote control output
0	0	Low-level output
0	1	High-level output
1	0	Low-level output
1	1	Carrier pulse output

NRZn	Carrier pulse output status flag
0	Carrier output disabled status (low-level status)
1	Carrier output enable status

10.4 Operation

10.4.1 Operation as interval timer/square wave output

When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, an interrupt request signal (INTTMHn) is generated and 8-bit timer counter Hn is cleared to 00H.

The CMPn1 register cannot be used in the interval timer mode. Even if the CMPn1 register is set, this has no effect on the timer output because matches between 8-bit timer counter Hn and the CMPn1 register are not detected.

A square wave of the desired frequency (duty = 50%) is output from the TOHn pin, by setting the TMHMDn.TOENn bit to 1.

Remarks 1. For the alternate-function pin (TOHn) settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

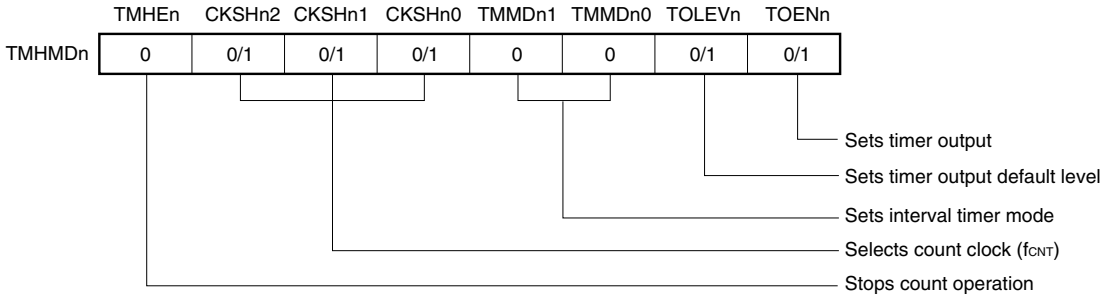
2. For INTTMHn interrupt enable, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

Setting

<1> Set each register.

Figure 10-2. Register Settings in Interval Timer Mode

(i) 8-bit timer H mode register n (TMHMDn) settings



(ii) CMPn0 register settings

The interval time is as follows if N is set as a comparison value.

- Interval time = (N + 1)/f_{CNT}

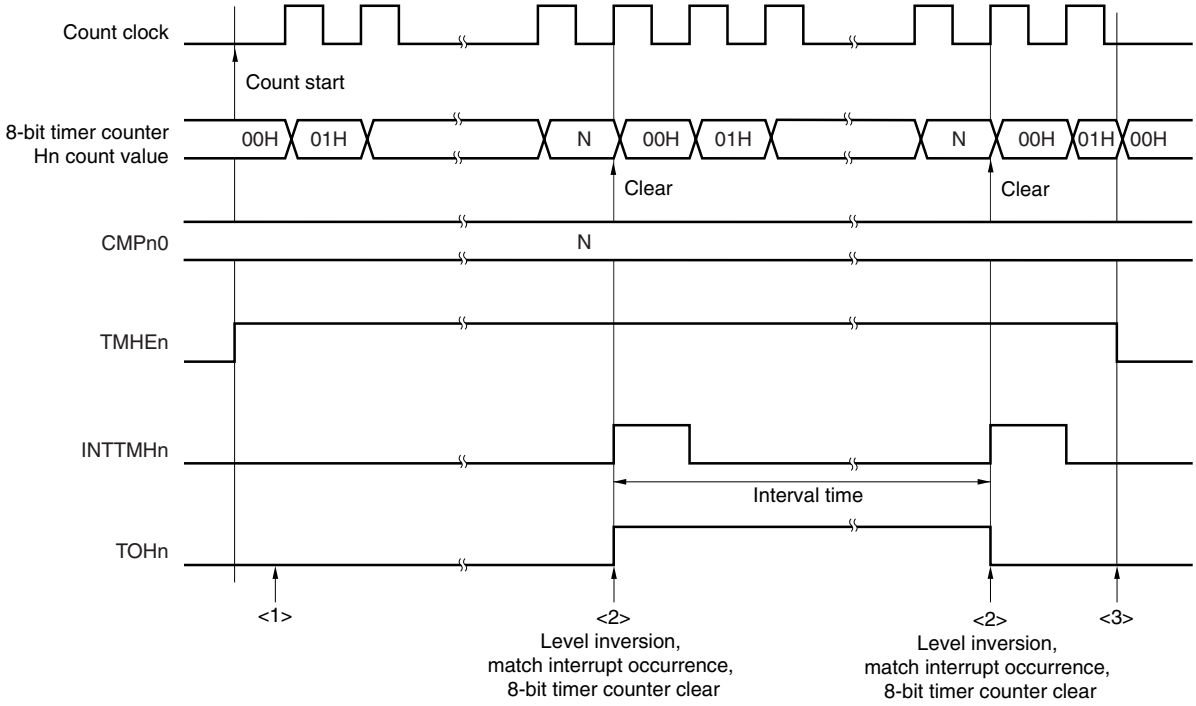
<2> When the TMHEn bit is set to 1, counting starts.

<3> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the INTTMHn signal is generated and 8-bit timer counter Hn is cleared to 00H.

<4> Then, the INTTMHn signal is generated in the same interval. To stop the count operation, clear the TMHEn bit to 0.

Figure 10-3. Timing of Interval Timer/Square Wave Output Operation (1/2)

Basic operation (operation when 01H ≤ CMPn0 ≤ FEH)



<1> When the TMHEn bit is set to 1, the count operation is enabled. The count clock starts counting no more than one clock after operation has been enabled.

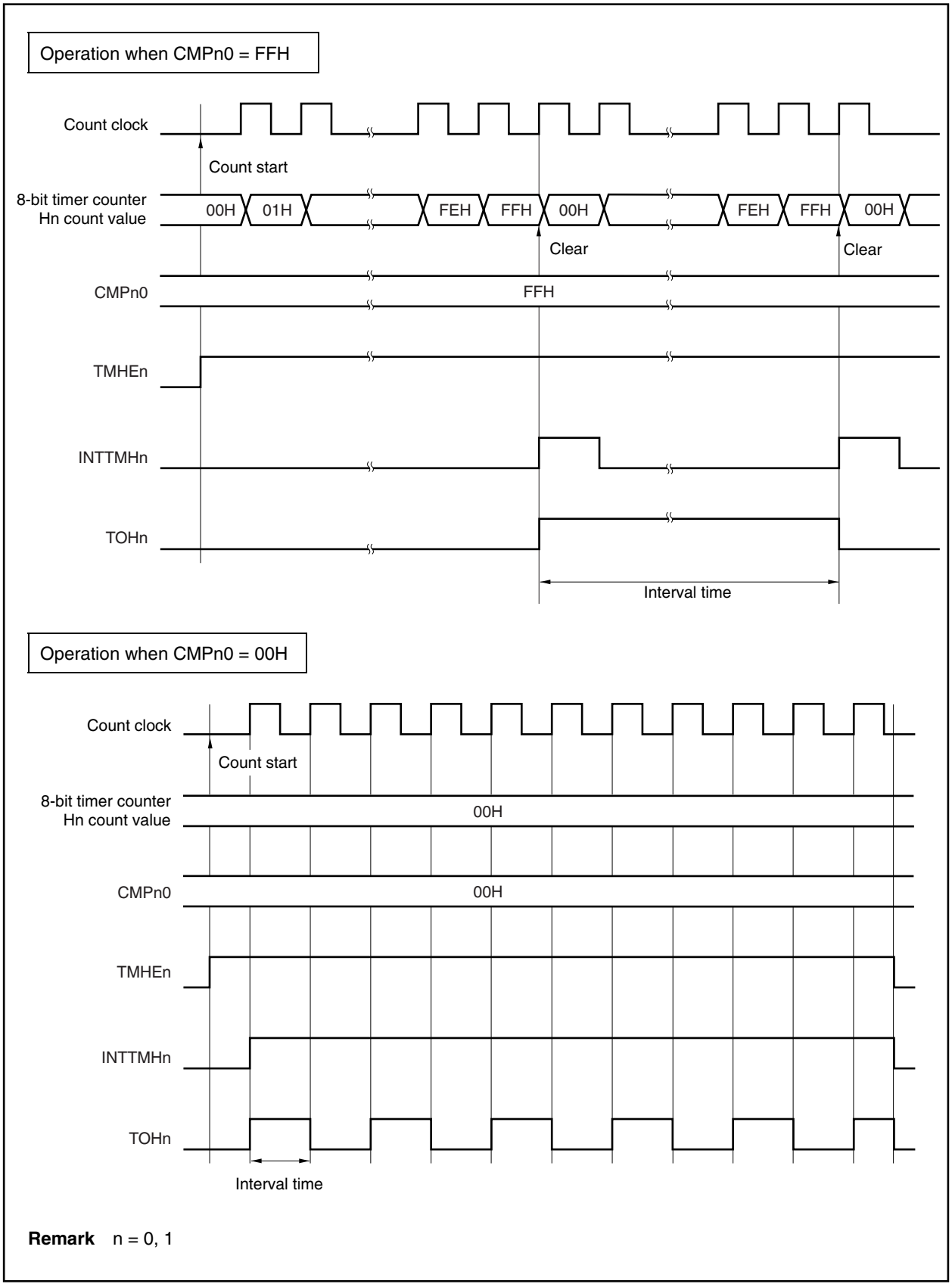
<2> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the value of 8-bit timer counter Hn is cleared, the TOHn output level is inverted, and the INTTMHn signal is output at the rising edge of the count clock.

<3> The INTTMHn signal and TOHn output are set to the default level when the TMHEn bit is cleared to 0 during 8-bit timer Hn operation. If the level is already at the default level before the TMHMDn.TMHEn bit is cleared to 0, that level is maintained.

Remarks 1. n = 0, 1

2. 01H ≤ N ≤ FEH

Figure 10-3. Timing of Interval Timer/Square Wave Output Operation (2/2)



Remark n = 0, 1

10.4.2 PWM output mode operation

In the PWM output mode, a pulse of any duty and cycle can be output.

The CMPn0 register controls the timer output (TOHn) cycle. Rewriting the CMPn0 register during timer operation is prohibited.

The CMPn1 register controls the timer output (TOHn) duty. The CMPn1 register can be rewritten during timer operation.

The operation in the PWM output mode is as follows.

After timer counting starts, when the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the TOHn output level is inverted and 8-bit timer counter Hn is cleared to 00H. When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the TOHn output level is inverted.

Remarks 1. For the alternate-function pin (TOHn) settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

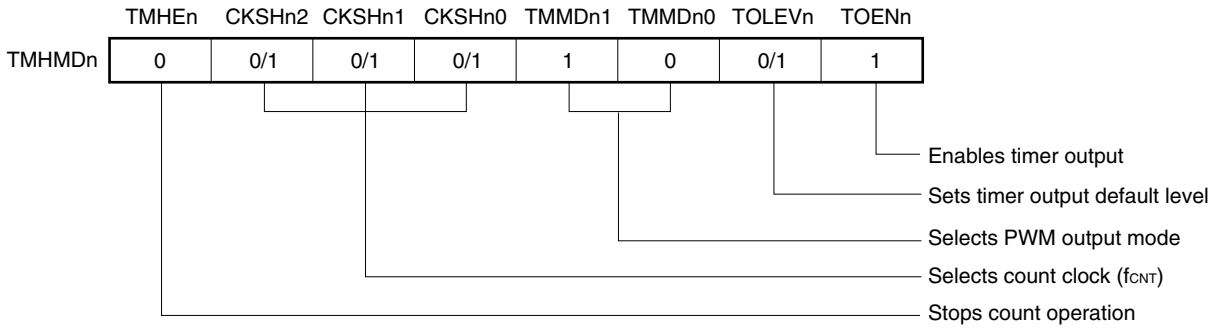
2. For INTTMHn interrupt enable, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

Setting

<1> Set each register.

Figure 10-4. Register Settings in PWM Output Mode

(i) 8-bit timer H mode register n (TMHMDn) settings



(ii) CMPn0 register setting

- Compare value (N): Sets cycle

(ii) CMPn1 register setting

- Compare value (M): Sets duty

Remarks 1. n = 0, 1

2. 00H ≤ CMPn1 (M) < CMPn0 (N) ≤ FFH

<2> When the TMHEn bit is set to 1, counting starts.

<3> After the count operation is enabled, the first compare register to be compared is the CMPn0 register. When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, and the TOHn output level is inverted. At the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register.

<4> When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the TOHn output level is inverted, and at the same time the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. At this time, 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<5> A pulse of any duty can be obtained through the repetition of steps <3> and <4> above.

<6> To stop the count operation, clear the TMHEn bit to 0.

Designating the set value of the CMPn0 register as (N), the set value of the CMPn1 register as (M), and the count clock frequency as f_{CNT}, the PWM pulse output cycle and duty are as follows.

PWM pulse output cycle = (N + 1)/f_{CNT}
Duty = inactive width: Active width = (M + 1) : (N + 1)

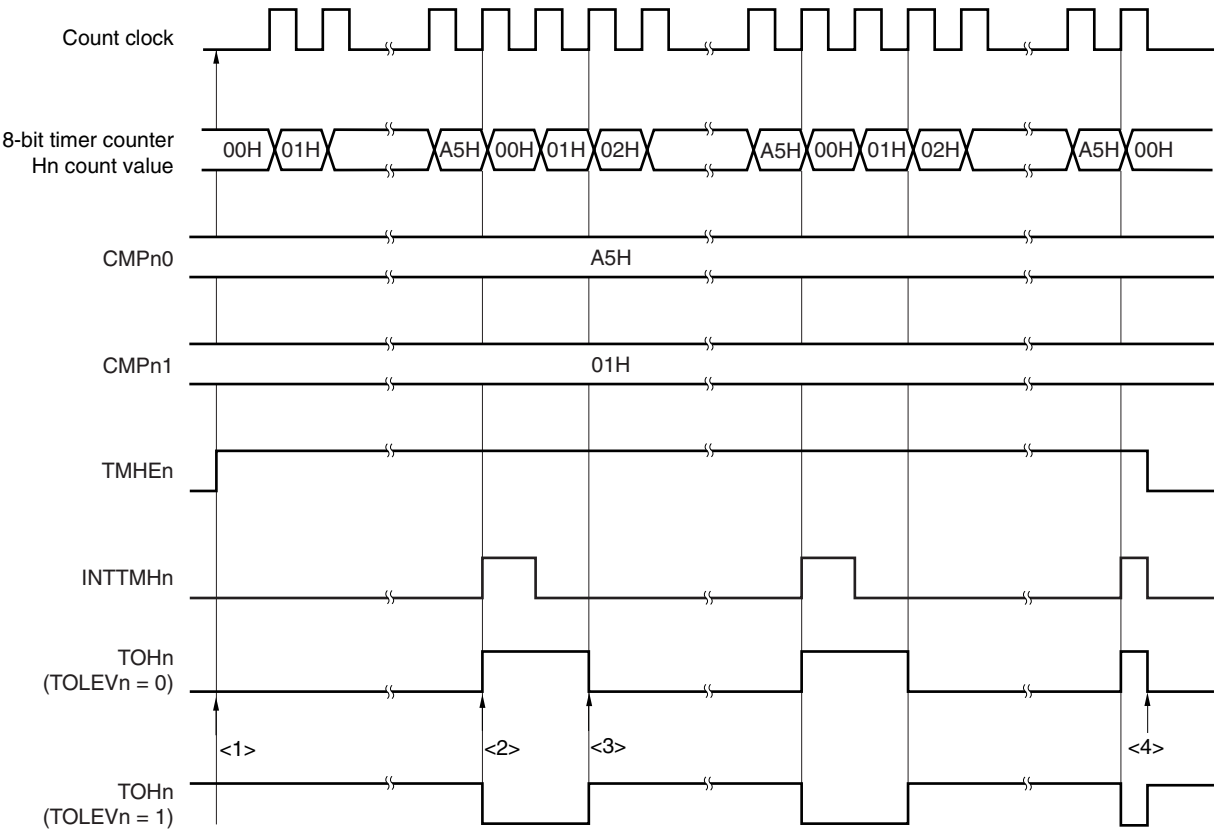
Cautions 1. The set value of the CMPn1 register can be changed while the timer counter is operating. However, this takes a duration of at least three operating clocks (signal selected by the CKSHn2 to CKSHn0 bits of the TMHMDn register) from when the value of the CMPn1 register is changed until the value is transferred to the register.

2. Be sure to set the CMPn1 register when starting the timer count operation (TMHEn bit = 1) after the timer count operation was stopped (TMHEn bit = 0) (be sure to set again even if setting the same value to the CMPn1 register).

3. Make sure that the CMPn1 register set value (M) and CMPn0 register set value (N) are within the following range.
00H ≤ CMPn1 (M) < CMPn0 (N) ≤ FFH

Figure 10-5. Operation Timing in PWM Output Mode (1/4)

Basic operation



<1> When the TMHEn bit is set to 1, counting starts. At this time TOHn output remains the default level.

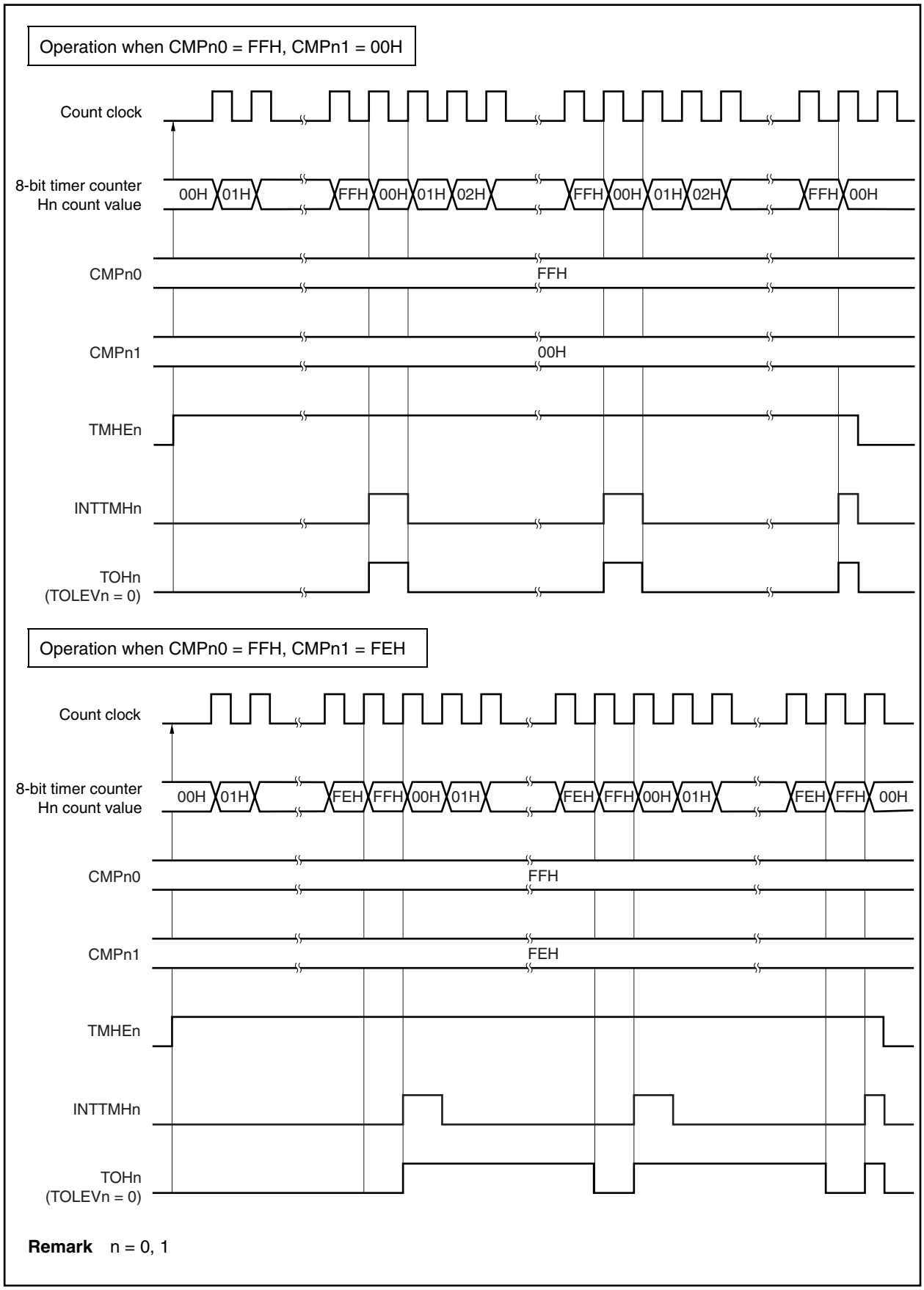
<2> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the TOHn output level is inverted, 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

<3> When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the TOHn output level is inverted. At this time, the value of 8-bit timer counter Hn is not cleared and the INTTMHn signal is not output.

<4> When the TMHEn bit is cleared to 0 during 8-bit timer Hn operation, the INTTMHn signal and TOHn output are set to the default level.

Remark n = 0, 1

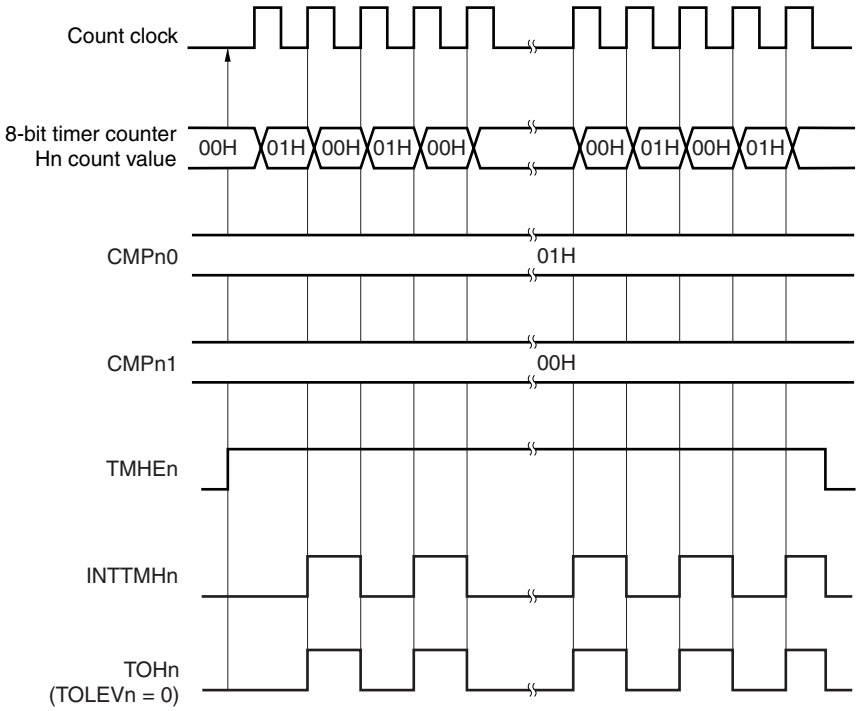
Figure 10-5. Operation Timing in PWM Output Mode (2/4)



Remark n = 0, 1

Figure 10-5. Operation Timing in PWM Output Mode (3/4)

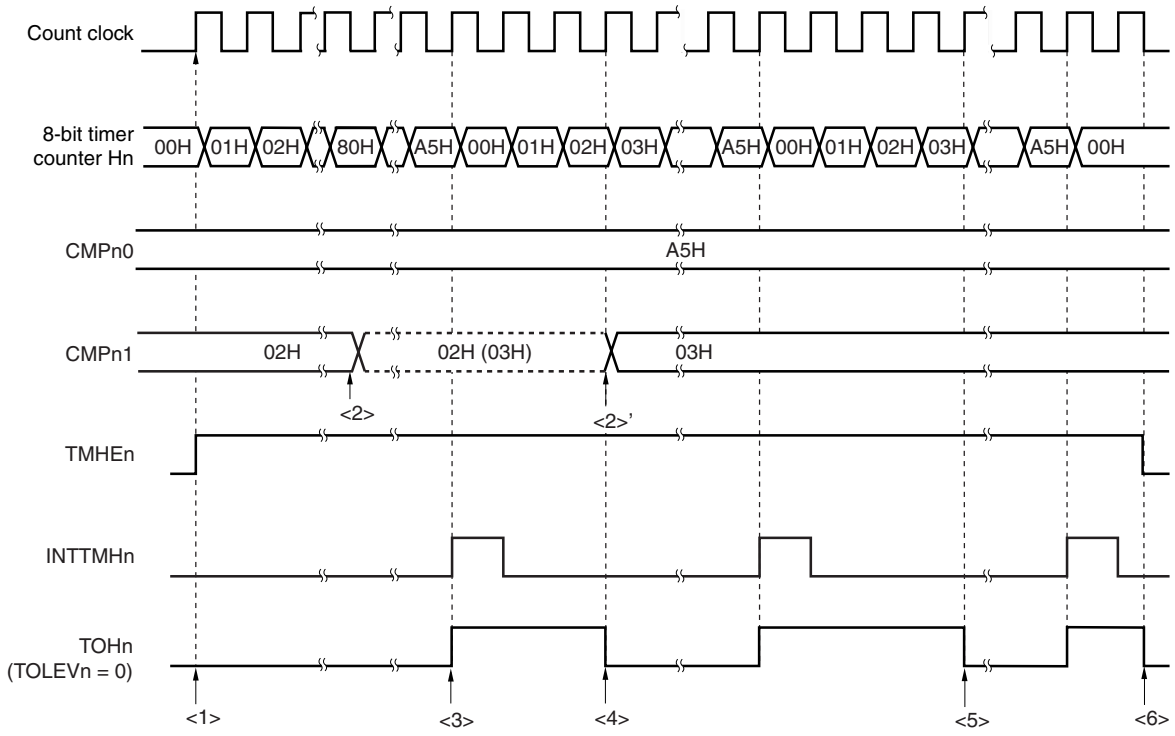
Operation when CMPn0 = 01H, CMPn1 = 00H



Remark n = 0, 1

Figure 10-5. Operation Timing in PWM Output Mode (4/4)

Operation by changing CMPn1 (CMPn1 = 02H → 03H, CMPn0 = A5H)



<1> When the TMHEn bit is set to 1, counting starts. At this time, the TOHn output remains the default level.

<2> The set value of the CMPn1 register can be changed during count operation. This operation is asynchronous to the count clock.

<3> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, 8-bit timer counter Hn is cleared, the TOHn output level is inverted, and the INTTMHn signal is generated.

<4> Even if the value of the CMPn1 register is changed, that value is latched and not transferred to the register. When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register prior to the change match, the changed value is transferred to the CMPn1 register and the value of the CMPn1 register is changed (<2>').

However, three or more count clocks are required from the time the value of the CMPn1 register is changed until it is transferred to the register. Even if a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the count value of 8-bit timer counter Hn matches the changed set value of the CMPn1 register, the TOHn output level is inverted. 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> When the TMHEn bit is cleared to 0 during 8-bit timer Hn operation, the INTTMHn signal and TOHn output are set to the default level.

10.4.3 Carrier generator mode operation

The carrier clock generated by 8-bit timer Hn is output using the cycle set with 8-bit timer/event counter 5n.

In the carrier generator mode, 8-bit timer/event counter 5n is used to control the extent to which the carrier pulse of 8-bit timer Hn is output, and the carrier pulse is output from the TOHn output.

Remarks 1. For the alternate-function pin (TOHn) settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. For INTTMHn interrupt enable, refer to **CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

(1) Carrier generation

In the carrier generator mode, the CMPn0 register generates a waveform with the low-level width of the carrier pulse and the CMPn1 register generates a waveform with the high-level width of the carrier pulse.

During 8-bit timer Hn operation, the CMPn1 register can be rewritten, but rewriting of the CMPn0 register is prohibited.

(2) Carrier output control

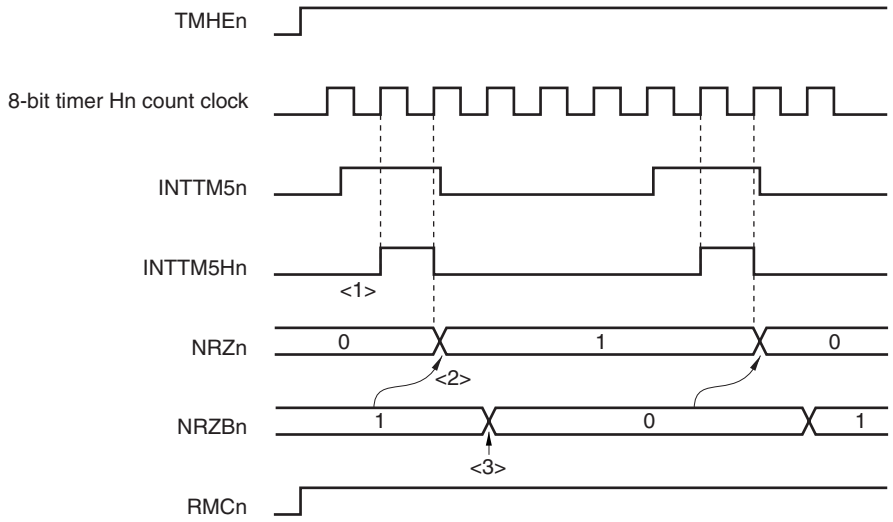
Carrier output control is performed with the interrupt request signal (INTTM5n) of 8-bit timer/event counter 5n and the TMCYCn.NRZBn and TMCYCn.RMCn bits. The output relationships are as follows.

RMCn Bit	NRZBn Bit	Output
0	0	Low level output
0	1	High level output
1	0	Low level output
1	1	Carrier pulse output

Remark n = 0, 1

To control carrier pulse output during count operation, the TMCYCn.NRZn and TMCYCn.NRZBn bits have a master and slave bit configuration. The NRZn bit is read-only while the NRZBn bit can be read and written. The INTTM5n signal is synchronized with the 8-bit timer Hn clock and output as the INTTM5Hn signal. The INTTM5Hn signal becomes the data transfer signal of the NRZn bit and the value of the NRZBn bit is transferred to the NRZn bit. The transfer timing from the NRZBn bit to the NRZn bit is as follows.

Figure 10-6. Transfer Timing



<1> The INTTM5n signal is synchronized with the count clock of 8-bit timer Hn and is output as the INTTM5Hn signal.

<2> The value of the NRZBn bit is transferred to the NRZn bit at the second clock from the rising edge of the INTTM5Hn signal.

<3> Write the next value to the NRZBn bit in the interrupt servicing programming that has been started by the INTTM5Hn interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR5n register.

Cautions 1. Do not rewrite the NRZBn bit again until at least the second clock after it has been rewritten, or else transfer from the NRZBn bit to the NRZn bit is not guaranteed.

2. When using 8-bit timer/event counter 5n in the carrier generator mode, an interrupt occurs at the timing of <1>. An interrupt occurs at a different timing when it is used in other than the carrier generator mode.

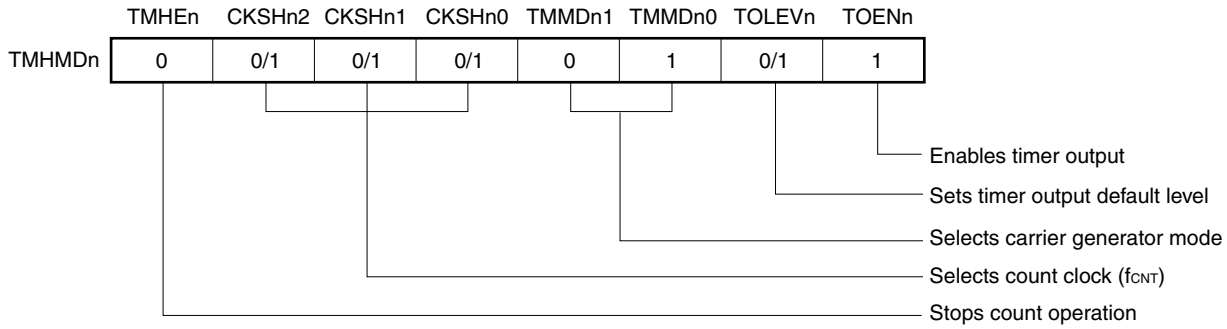
Remark n = 0, 1

Setting

<1> Set each register.

Figure 10-7. Register Settings in Carrier Generator Mode

- 8-bit timer H mode register n (TMHMDn)



- CMPn0 register: Compare value
- CMPn1 register: Compare value
- TMCYCn register: RMCn = 1 ... Remote control output enable bit
  NRZBn = 0/1 ... Carrier output enable bit
- TCL5n, TMC5n registers: Refer to **9.3 Registers**.

Remark n = 0, 1

<2> When the TMHEn bit is set to 1, 8-bit timer Hn count operation starts.

<3> When the TMC5n.TCE5n bit is set to 1, 8-bit timer/event counter 5n count operation starts.

<4> After the count operation is enabled, the first compare register to be compared is the CMPn0 register. When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the INTTMHn signal is generated, 8-bit timer counter Hn is cleared, and at the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register.

<5> When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the INTTMHn signal is generated, 8-bit timer counter Hn is cleared, and at the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register.

<6> The carrier clock is obtained through the repetition of steps <4> and <5> above.

<7> The INTTM5n signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal. This signal becomes the data transfer signal of the NRZBn bit and the value of the NRZBn bit is transferred to the NRZn bit.

<8> Write the next value to the NRZBn bit in the interrupt servicing programming that has been started by the INTTM5Hn interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR5n register.

<9> When the NRZn bit becomes high level, the carrier clock is output from the TOHn pin.

<10> Any carrier clock can be obtained through the repetition of the above steps. To stop the count operation, clear the TMHEn bit to 0.

Designating the set value of the CMPn0 register as (N), the set value of the CMPn1 register as (M), and the count clock frequency as f_{CNT}, the carrier clock output cycle and duty are as follows.

Carrier clock output cycle = (N + M + 2)/f_{CNT}
Duty = High level width: Carrier clock output width = (M + 1) : (N + M + 2)

Cautions 1. Be sure to set the CMPn1 register when starting the timer count operation (TMHEn bit = 1) after the timer count operation was stopped (TMHEn bit = 0) (be sure to set again even if setting the same value to the CMPn1 register).

2. Set the values of the CMPn0 and CMPn1 registers in the range of 01H to FFH.

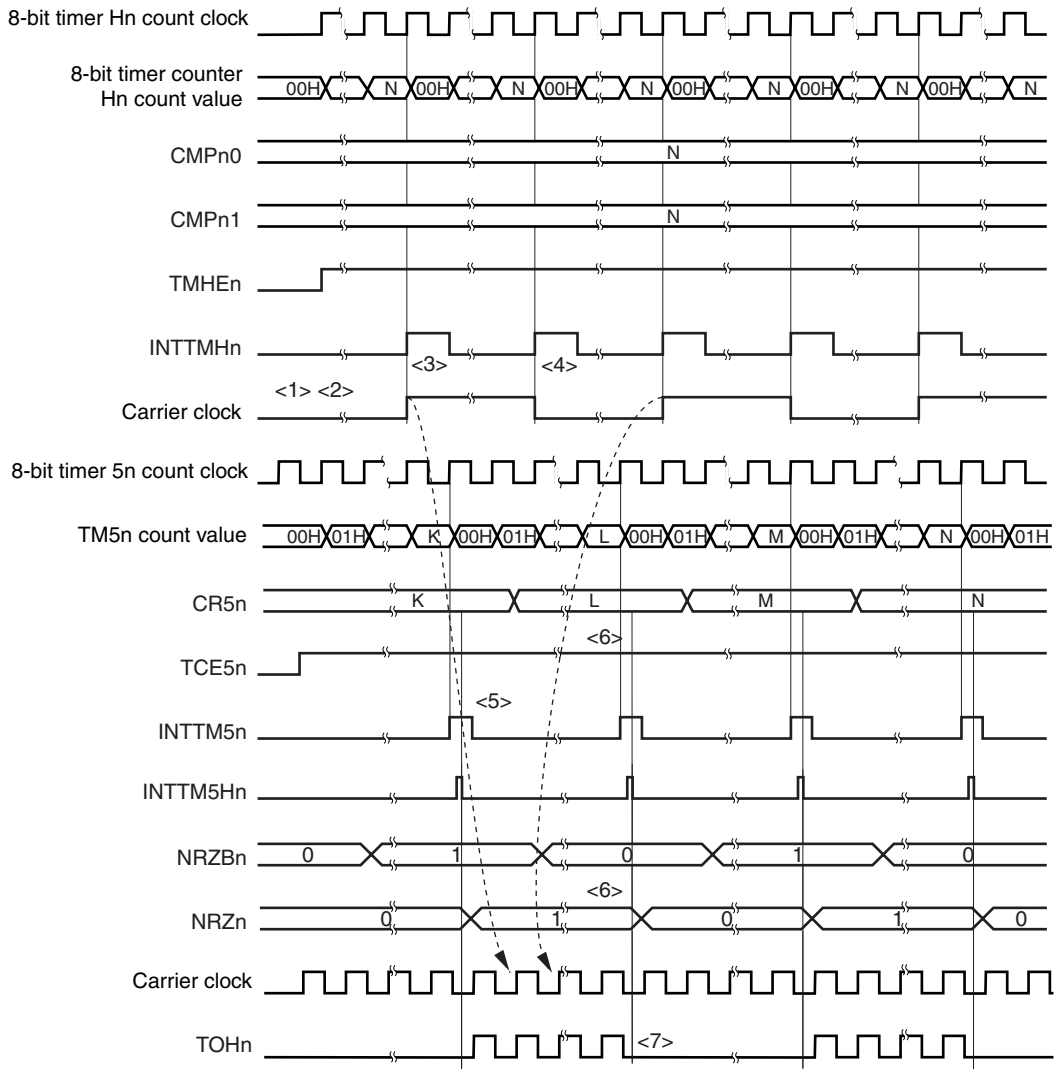
3. In the carrier generator mode, three operating clocks (signal selected by the TMHMDn.CKSHn0 to TMHMDn.CKSHn2 bits) are required for actual transfer of the new value to the register after the CMPn1 register has been rewritten.

4. Be sure to perform the TMCYCn.RMCn bit setting before the start of the count operation.

5. When using the carrier generator mode, set the 8-bit timer Hn count clock frequency to six times the 8-bit timer/event counter 5n count clock frequency or higher.

Figure 10-8. Carrier Generator Mode (1/3)

Operation when the CMPn0 register = N, the CMPn1 register = N is set



<1> When the TMHEn bit = 0 and the TCE5n bit = 0, the operation of 8-bit timer Hn is stopped.

<2> When the TMHEn bit is set to 1, 8-bit timer Hn starts counting. The carrier clock remains the default level.

<3> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the first INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register. 8-bit timer counter Hn is cleared to 00H.

<4> When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. 8-bit timer counter Hn is cleared to 00H. A carrier clock with a duty of 50% is generated through the repetition of steps <3> and <4>.

<5> The INTTM5n signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal.

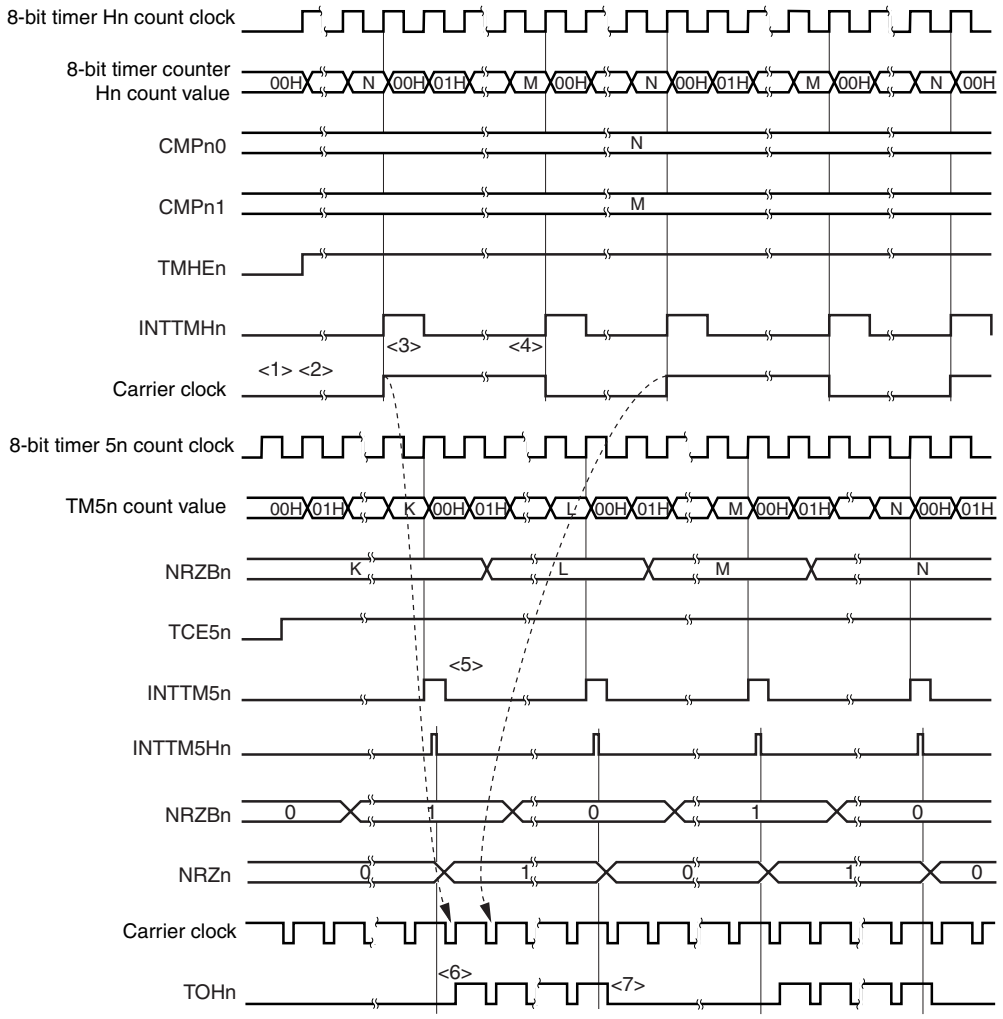
<6> The INTTM5Hn signal becomes the data transfer signal of the NRZBn bit, and the value of the NRZBn bit is transferred to the NRZn bit.

<7> The TOHn output is made low level by clearing the NRZn bit = 0.

Remark n = 0, 1

Figure 10-8. Carrier Generator Mode (2/3)

Operation when the CMPn0 register = N, the CMPn1 register = M is set



<1> When the TMHEn bit = 0 and the TCE5n bit = 0, the operation of 8-bit timer Hn is stopped.

<2> When the TMHEn bit is set to 1, 8-bit timer Hn starts counting. The carrier clock remains the default level at this time.

<3> When the count value of 8-bit timer counter Hn and the set value of the CMPn0 register match, the first INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register. 8-bit timer counter Hn is cleared to 00H.

<4> When the count value of 8-bit timer counter Hn and the set value of the CMPn1 register match, the INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. 8-bit timer counter Hn is cleared to 00H. A carrier clock with a fixed duty (other than 50%) is generated through the repetition of steps <3> and <4>.

<5> The INTTM5n signal is generated. This signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal.

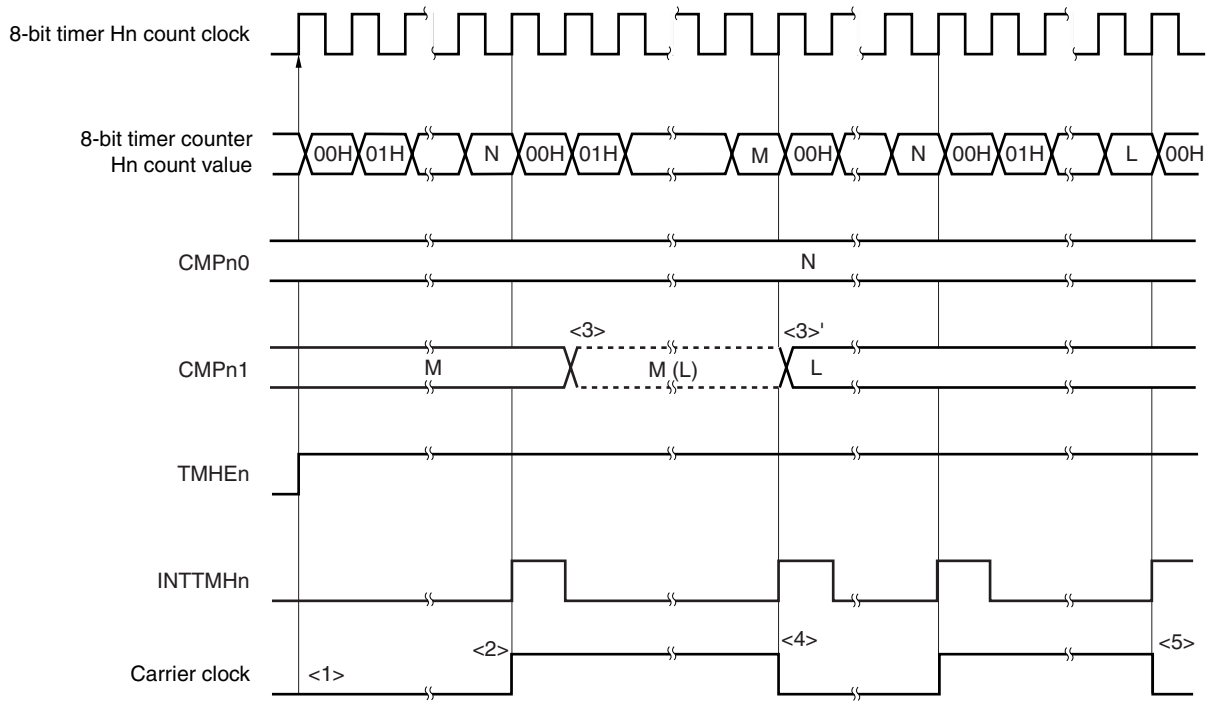
<6> The carrier is output from the rising edge of the first carrier clock by setting the NRZn bit = 1.

<7> By setting the NRZn bit = 0, the TOHn output is also maintained high level while the carrier clock is high level, and does not change to low level (the high level width of the carrier waveform is guaranteed through steps <6> and <7>).

Remark n = 0, 1

Figure 10-8. Carrier Generator Mode (3/3)

Operation based on the CMPn1 register transitions



<1> When the TMHEn bit is set to 1, counting starts. The carrier clock remains the default level at this time.

<2> When the count value of the 8-bit timer counter Hn matches the value of the CMPn0 register, the INTTMHn signal is output, the carrier signal is inverted, and the 8-bit timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter Hn is changed from the CMPn0 register to the CMPn1 register.

<3> The CMPn1 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer Hn is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter Hn matches the value (M) of the CMPn1 register before the change, the CMPn1 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMPn1 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter Hn and the value (M) of the CMPn1 register match, the INTTMHn signal is output, the carrier signal is inverted, and 8-bit timer counter Hn is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter Hn is changed from the CMPn1 register to the CMPn0 register.

<5> The timing at which the count value of 8-bit timer counter Hn and the value of the CMPn1 register match again is the changed value (L).

Remark n = 0, 1

CHAPTER 11 INTERVAL TIMER, WATCH TIMER

The V850ES/KG2 includes interval timer BRG and a watch timer. Interval timer BRG can also be used as the source clock of the watch timer. The watch timer can also be used as interval timer WT.

Two interval timer channels and one watch timer channel can be used at the same time.

11.1 Interval Timer BRG

11.1.1 Functions

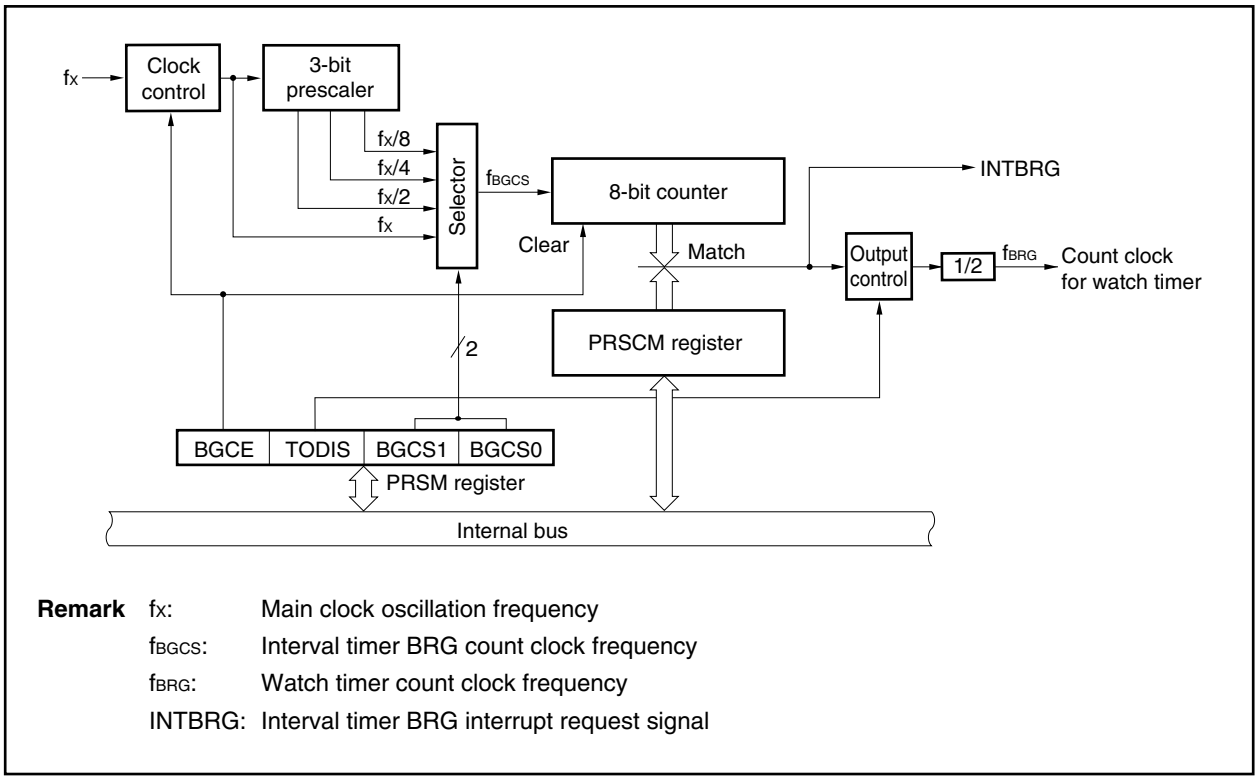
Interval timer BRG has the following functions.

- Interval timer BRG: An interrupt request signal (INTBRG) is generated at a specified interval.
- Generation of count clock for watch timer: When the main clock is used as the count clock for the watch timer, a count clock (f_{BRG}) is generated.

11.1.2 Configuration

The following shows the block diagram of interval timer BRG.

Figure 11-1. Block Diagram of Interval Timer BRG



Remark fx: Main clock oscillation frequency
f_{BGCS}: Interval timer BRG count clock frequency
f_{BRG}: Watch timer count clock frequency
INTBRG: Interval timer BRG interrupt request signal

(1) Clock control

The clock control controls supply/stop of the operation clock of interval timer BRG.

(2) 3-bit prescaler

The 3-bit prescaler divides f_X to generate $f_X/2$, $f_X/4$, and $f_X/8$.

(3) Selector

The selector selects the count clock (f_{BGCS}) for interval timer BRG from f_X, $f_X/2$, $f_X/4$, and $f_X/8$.

(4) 8-bit counter

The 8-bit counter counts the count clock (f_{BGCS}).

(5) Output control

The output control controls supply of the count clock (f_{BRG}) for the watch timer.

(6) PRSCM register

The PRSCM register is an 8-bit compare register that sets the interval time.

(7) PRSM register

The PRSM register controls the operation of interval timer BRG, the selector, and clock supply to the watch timer.

11.1.3 Registers

Interval timer BRG includes the following registers.

(1) Interval timer BRG mode register (PRSM)

PRSM controls the operation of interval timer BRG, selection of count clock, and clock supply to the watch timer.

This register can be read or written in 8-bit or 1-bit units.

Reset sets PRSM to 00H.

After reset: 00H R/W Address: FFFFF8B0H

	7	6	5	<4>	3	2	1	0
PRSM	0	0	0	BGCE	0	TODIS	BGCS1	BGCS0

BGCE	Control of interval timer operation
0	Operation stopped, 8-bit counter cleared to 01H
1	Operate

TODIS	Control of clock supply for watch timer
0	Clock for watch timer supplied
1	Clock for watch timer not supplied

BGCS1	BGCS0	Selection of input clock (f_{BGCS})[Note]			
			10 MHz	5 MHz	4 MHz
0	0	fx	100 ns	200 ns	250 ns
0	1	fx/2	200 ns	400 ns	500 ns
1	0	fx/4	400 ns	800 ns	1 μs
1	1	fx/8	800 ns	1.6 μs	2 μs

Note Set these bits so that the following conditions are satisfied.

V_{DD} = 4.0 to 5.5 V: $f_{BGCS} \leq$ 10 MHz

V_{DD} = 2.7 to 4.0 V: $f_{BGCS} \leq$ 5 MHz

Cautions 1. Do not change the values of the TODIS, BGCS1, and BGCS0 bits while interval timer BRG is operating (BGCE bit = 1). Set the TODIS, BGCS1, and BGCS0 bits before setting (1) the BGCE bit.

2. When the BGCE bit is cleared (to 0), the 8-bit counter is cleared.

(2) Interval timer BRG compare register (PRSCM)

PRSCM is an 8-bit compare register.

This register can be read or written in 8-bit units.

Reset sets PRSCM to 00H.

After reset: 00H R/W Address: FFFFF8B1H

	7	6	5	4	3	2	1	0
PRSCM	PRSCM7	PRSCM6	PRSCM5	PRSCM4	PRSCM3	PRSCM2	PRSCM1	PRSCM0

Caution Do not rewrite the PRSCM register while interval timer BRG is operating (PRSM.BGCE bit = 1). Set the PRSCM register before setting (1) the BGCE bit.

11.1.4 Operation

(1) Operation of interval timer BRG

Set the count clock by using the BGCS1 and BGCS0 bits of PRSM and the 8-bit compare value by using the PRSCM register.

When the PRSM.BGCE bit is set (1), interval timer BRG starts operating.

Each time the count value of the 8-bit counter and the set value in the PRSCM register match, an interrupt request signal (INTBRG) is generated. At the same time, the 8-bit counter is cleared to 00H and counting is continued.

The interval time can be obtained from the following equation.

Interval time = $2^m \times N/fx$

Remark m: Division value (set values of BGCS1 and BGCS0 bits) = 0 to 3
N: Set value in PRSCM register = 1 to 256 (when the set value in the PRSCM register is 00H, N = 256)
fx: Main clock oscillation frequency

(2) Count clock supply for watch timer

Set the count clock by using the BGCS1 and BGCS0 bits of PRSM and the 8-bit compare value by using the PRSCM register, so that the count clock frequency (f_{BRG}) of the watch timer is 32.768 kHz. Clear (0) the PRSM.TODIS bit at the same time.

When the PRSM.BGCE bit is set (1), f_{BRG} is supplied to the watch timer.

f_{BRG} is obtained from the following equation.

$f_{BRG} = fx/(2^{m+1} \times N)$

To set f_{BRG} to 32.768 kHz, perform the following calculation to set the BGCS1 and BGCS0 bits and the PRSCM register.

<1> Set N = fx/65,536 (round off the decimal) to set m = 0.
<2> If N is even, N = N/2 and m = m + 1
<3> Repeat step <2> until N is even or m = 3
<4> Set N to the PRSCM register and m to the BGCS1 and BGCS0 bits.

Example: When fx = 4.00 MHz

<1> N = 4,000,000/65,536 = 61 (round off the decimal), m = 0
<2>, <3> Since N is odd, the values remain as N = 61, m = 0
<4> The set value in the PRSCM register: 3DH (61), the set values in the BGCS1 and BGCS0 bits: 00

Remark m: Divided value (set value in the BGCS1 and BGCS0 bits) = 0 to 3
N: Set value in PRSCM register = 1 to 256 (when the set value in the PRSCM register is 00H, N = 256)
fx: Main clock oscillation frequency

11.2 Watch Timer

11.2.1 Functions

The watch timer has the following functions.

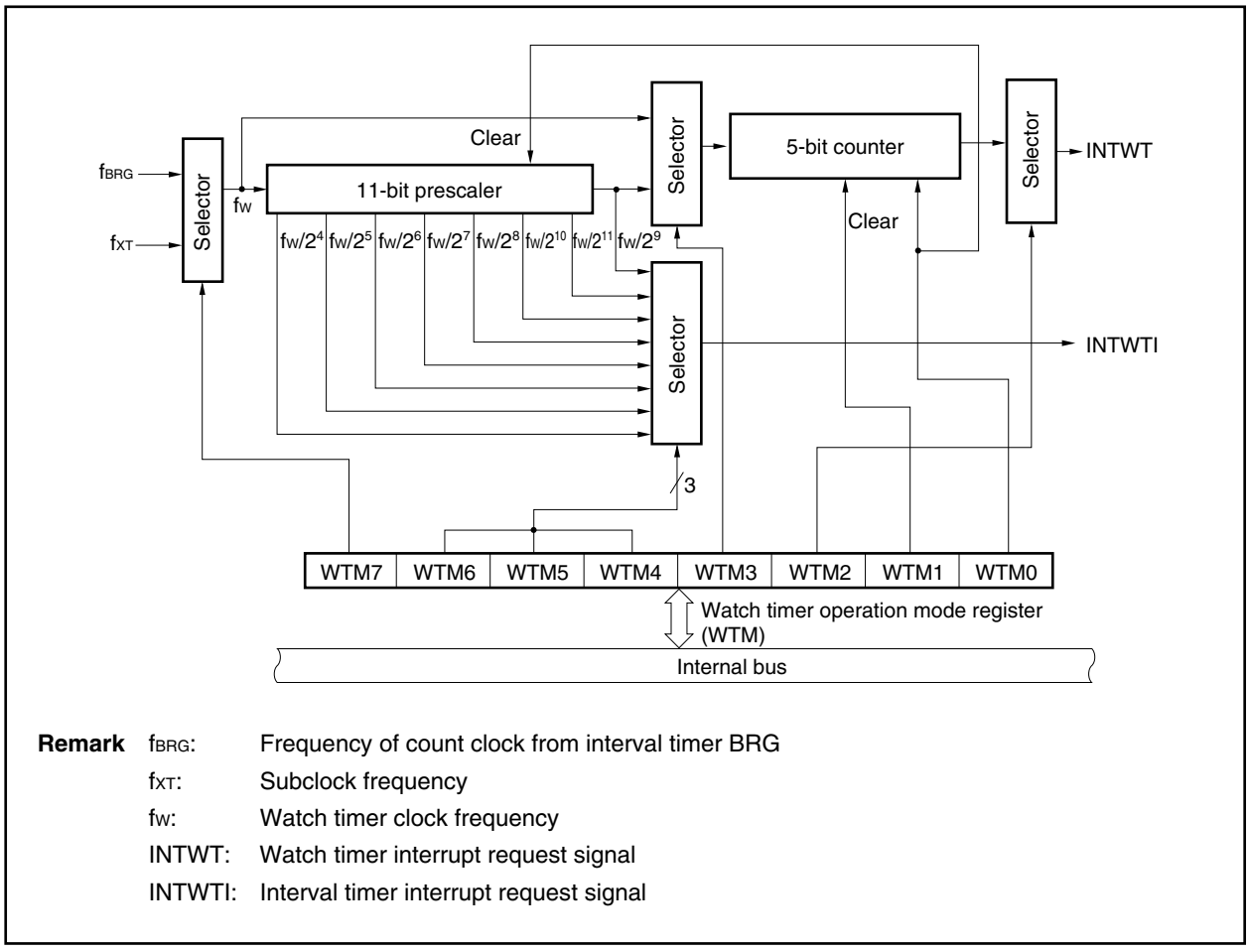
- Watch timer: An interrupt request signal (INTWT) is generated at time intervals of 0.5 or 0.25 seconds by using the main clock or subclock.
- Interval timer: An interrupt request signal (INTWTI) is generated at the preset time interval.

The watch timer and interval timer functions can be used at the same time.

11.2.2 Configuration

The following shows the block diagram of the watch timer.

Figure 11-2. Block Diagram of Watch Timer



Remark f_{BRG}: Frequency of count clock from interval timer BRG
f_{XT}: Subclock frequency
f_W: Watch timer clock frequency
INTWT: Watch timer interrupt request signal
INTWTI: Interval timer interrupt request signal

(1) 11-bit prescaler

The 11-bit prescaler generates a clock of $f_W/2^4$ to $f_W/2^{11}$ by dividing f_W.

(2) 5-bit counter

The 5-bit counter generates the watch timer interrupt request signal (INTWT) at intervals of $2^4/f_W$, $2^5/f_W$, $2^{13}/f_W$, or $2^{14}/f_W$ by counting f_W or $f_W/2^9$.

(3) Selectors

The watch timer has the following four selectors.

- Selector that selects the main clock (the clock from interval timer BRG (f_{BRG})) or the subclock (f_{XT}) as the clock for the watch timer.
- Selector that selects f_W or $f_W/2^9$ as the count clock frequency of the 5-bit counter
- Selector that selects $2^4/f_W$ or $2^{13}/f_W$, or $2^5/f_W$ or $2^{14}/f_W$ as the INTWT signal generation time interval.
- Selector that selects the generation time interval of the interval timer WT interrupt request signal (INTWTI) from $2^4/f_W$ to $2^{11}/f_W$.

(4) 8-bit counter

The 8-bit counter counts the count clock (f_{BGCS}).

(5) WTM register

The WTM register is an 8-bit register that controls the operation of the watch timer/interval timer WT and sets the interval of interrupt request signal generation.

11.2.3 Registers

The watch timer includes the following register.

(1) Watch timer operation mode register (WTM)

This register enables or disables the count clock and operation of the watch timer, sets the interval time of the 11-bit prescaler, controls the operation of the 5-bit counter, and sets the timer of watch timer interrupt request signal (INTWT) generation.

The WTM register can be read or written in 8-bit or 1-bit units.

Reset sets WTM to 00H.

After reset: 00H R/W Address: FFFFF680H

	7	6	5	4	3	2	<1>	<0>
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	WTM6	WTM5	WTM4	Selection of interval timer interrupt (INTWTI) time
0	0	0	0	2^4/fw (488 μs: fw = fXT)
0	0	0	1	2^5/fw (977 μs: fw = fXT)
0	0	1	0	2^6/fw (1.95 ms: fw = fXT)
0	0	1	1	2^7/fw (3.91 ms: fw = fXT)
0	1	0	0	2^8/fw (7.81 ms: fw = fXT)
0	1	0	1	2^9/fw (15.6 ms: fw = fXT)
0	1	1	0	2^{10}/fw (31.3 ms: fw = fXT)
0	1	1	1	2^{11}/fw (62.5 ms: fw = fXT)
1	0	0	0	2^4/fw (488 μs: fw = fBRG)
1	0	0	1	2^5/fw (977 μs: fw = fBRG)
1	0	1	0	2^6/fw (1.95 ms: fw = fBRG)
1	0	1	1	2^7/fw (3.91 ms: fw = fBRG)
1	1	0	0	2^8/fw (7.81 ms: fw = fBRG)
1	1	0	1	2^9/fw (15.6 ms: fw = fBRG)
1	1	1	0	2^{10}/fw (31.3 ms: fw = fBRG)
1	1	1	1	2^{11}/fw (62.5 ms: fw = fBRG)

WTM7	WTM3	WTM2	Selection of watch timer interrupt (INTWT) time
0	0	0	2^{14}/fw (0.5 s: fw = fXT)
0	0	1	2^{13}/fw (0.25 s: fw = fXT)
0	1	0	2^5/fw (977 μs: fw = fXT)
0	1	1	2^4/fw (488 μs: fw = fXT)
1	0	0	2^{14}/fw (0.5 s: fw = fBRG)
1	0	1	2^{13}/fw (0.25 s: fw = fBRG)
1	1	0	2^5/fw (977 μs: fw = fBRG)
1	1	1	2^4/fw (488 μs: fw = fBRG)

WTM1	Control of 5-bit counter operation
0	Clear after operation stops
1	Start

WTM0	Watch timer operation enable
0	Stop operation (clear both prescaler and 5-bit counter)
1	Enable operation

Caution Rewrite the WTM2 to WTM7 bits while both the WTM0 and WTM1 bits are 0.

Remarks 1. fw: Watch timer clock frequency

2. Values in parentheses apply when fw = 32.768 kHz

11.2.4 Operation

(1) Operation as watch timer

The watch timer generates an interrupt request at fixed time intervals. The watch timer operates using time intervals of 0.25 or 0.5 seconds with the subclock (32.768 kHz).

The count operation starts when the WTM.WTM0 and WTM.WTM1 bits are set to 11. When these bits are cleared to 00, the 10-bit prescaler and 5-bit counter are cleared and the count operation stops.

The 5-bit counter can be cleared to synchronize the time by clearing the WTM1 bit to 0 when the watch timer and interval timer WT operate simultaneously. At this time, an error of up to 15.6 ms may occur in the watch timer, but interval timer WT is not affected.

(2) Operation as interval timer

The watch timer can also be used as an interval timer that repeatedly generates an interrupt request signal (INTWTI) at intervals specified by a count value set in advance.

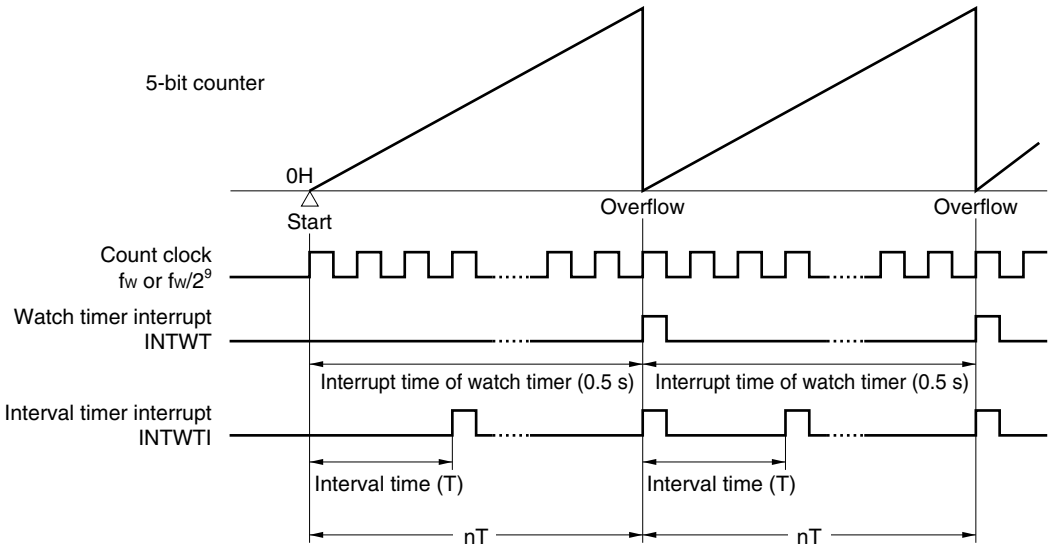
The interval time can be selected by the WTM.WTM4 to WTM.WTM7 bits.

Table 11-1. Interval Time of Interval Timer

WTM7	WTM6	WTM5	WTM4	Interval Time	
0	0	0	0	$2^4 \times 1/f_W$	488 μs (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	0	1	$2^5 \times 1/f_W$	977 μs (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	1	0	$2^6 \times 1/f_W$	1.95 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	1	1	$2^7 \times 1/f_W$	3.91 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	0	0	$2^8 \times 1/f_W$	7.81 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	0	1	$2^9 \times 1/f_W$	15.6 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	1	0	$2^{10} \times 1/f_W$	31.3 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	1	1	$2^{11} \times 1/f_W$	62.5 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
1	0	0	0	$2^4 \times 1/f_W$	488 μs (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	0	1	$2^5 \times 1/f_W$	977 μs (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	1	0	$2^6 \times 1/f_W$	1.95 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	1	1	$2^7 \times 1/f_W$	3.91 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	0	0	$2^8 \times 1/f_W$	7.81 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	0	1	$2^9 \times 1/f_W$	15.6 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	1	0	$2^{10} \times 1/f_W$	31.3 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	1	1	$2^{11} \times 1/f_W$	62.5 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)

Remark f_W: Watch timer clock frequency

Figure 11-3. Operation Timing of Watch Timer/Interval Timer



Remarks 1. Assuming that the interrupt time of the watch timer is set to 0.5 seconds.

2. fw: Watch timer clock frequency

Values in parentheses apply when count clock fw = 32.768 kHz.

n: Number of interval timer WT operations

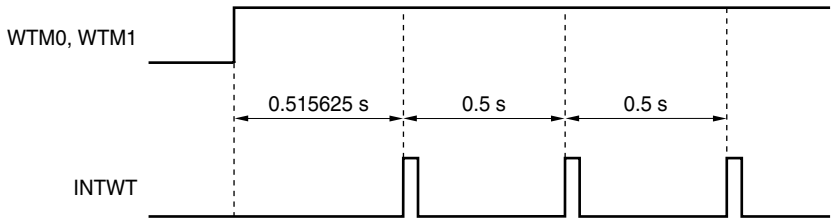
11.3 Cautions

(1) Operation as watch timer

Some time is required before the first watch timer interrupt request (INTWT) is generated after operation is enabled (WTM.WTM1 and WTM.WTM0 bits = 11).

Figure 11-4. Example of Generation of Watch Timer Interrupt Request (INTWT) (When Interrupt Period = 0.5 s)

It takes 0.515625 (max.) seconds for the first INTWT to be generated ($2^9 \times 1/32768 = 0.015625$ (max.) s longer). INTWT is then generated every 0.5 seconds.



(2) When watch timer and interval timer BRG operate simultaneously

When using the subclock as the count clock for the watch timer, the interval time of interval timer BRG can be set to any value. Changing the interval time does not affect the watch timer (before changing the interval time, stop operation).

When using the main clock as the count clock for the watch timer, set the interval time of interval timer BRG to approximately 65.536 kHz. Do not change this value.

(3) When interval timer BRG and interval timer WT operate simultaneously

When using the subclock as the count clock for interval timer WT, the interval times of interval timers BRG and WT can be set to any values. They can also be changed later (before changing the value, stop operation).

When using the main clock as the count clock for interval timer WT, the interval time of interval timer BRG can be set to any value, but cannot be changed later (it can be changed only when interval timer WT stops operation). The interval time of interval timer WT can be set to $\times 2^5$ to $\times 2^{12}$ of the set value of interval timer BRG. It can also be changed later.

(4) When watch timer and interval timer WT operate simultaneously

The interval time of interval timer WT can be set to a value between 488 μs and 62.5 ms. It cannot be changed later.

Do not stop interval timer WT (clear (0) the WTM.WTM0 bit) while the watch timer is operating. If the WTM0 bit is set (1) after it had been cleared (0), the watch timer will have a discrepancy of up to 0.5 or 0.25 seconds.

(5) When watch timer, interval timer BRG, and interval timer WT operate simultaneously

When using the subclock as the count clock for the watch timer, the interval times of interval timers BRG and WT can be set to any values. The interval time of interval timer BRG can be changed later (before changing the value, stop operation).

When using the main clock as the count clock for the watch timer, set the interval time of interval timer BRG to approximately 65.536 kHz. It cannot be changed later. The interval time of interval timer WT can be set to a value between 488 μs and 62.5 ms. It cannot be changed later.

Do not stop interval timer BRG (clear (0) the PRSM.BGCE bit) or interval timer WT (clear (0) the WTM.WTM0 bit) while the watch timer is operating.

CHAPTER 12 WATCHDOG TIMER FUNCTIONS

12.1 Watchdog Timer 1

12.1.1 Functions

Watchdog timer 1 has the following operation modes.

- Watchdog timer
- Interval timer

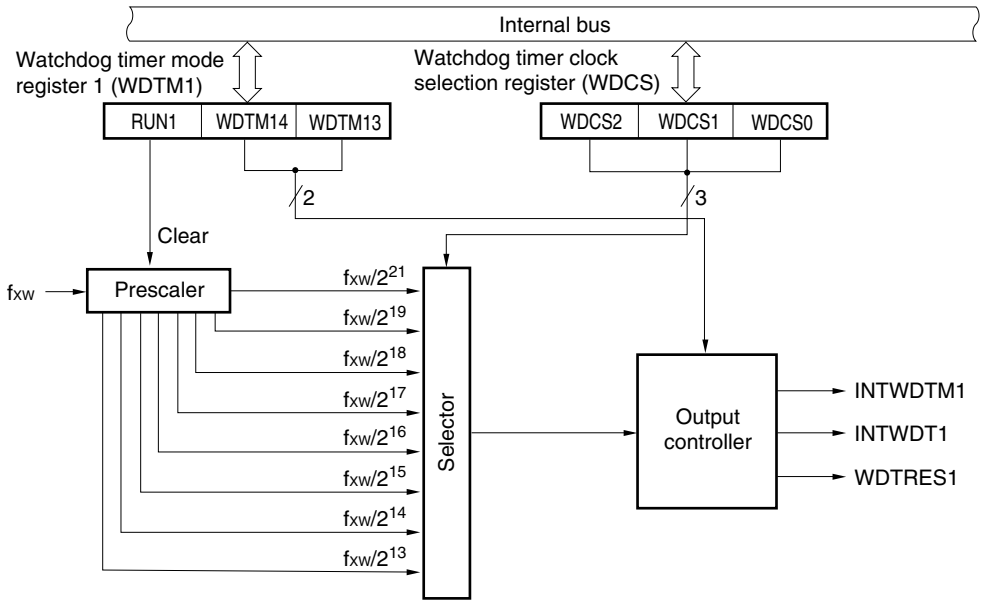
The following functions are realized from the above-listed operation modes.

- Generation of non-maskable interrupt request signal (INTWDT1) upon overflow of watchdog timer 1[Note]
- Generation of system reset signal (WDTRES1) upon overflow of watchdog timer 1
- Generation of maskable interrupt request signal (INTWDTM1) upon overflow of interval timer

Note For non-maskable interrupt servicing due to non-maskable interrupt request signal (INTWDT1, INTWDT2), refer to **21.10 Cautions**.

Remark Select whether to use watchdog timer 1 in the watchdog timer 1 mode or the interval timer mode with the WDTM1 register.

Figure 12-1. Block Diagram of Watchdog Timer 1



Remark INTWDTM1: Request signal for maskable interrupt through watchdog timer 1 overflow
INTWDT1: Request signal for non-maskable interrupt through watchdog timer 1 overflow
WDTRES1: Reset signal through watchdog timer 1 overflow
$f_{XW} = f_X$: Watchdog timer 1 clock frequency

12.1.2 Configuration

Watchdog timer 1 includes the following hardware.

Table 12-1. Configuration of Watchdog Timer 1

Item	Configuration
Control register	Watchdog timer clock selection register (WDCS) Watchdog timer mode register 1 (WDTM1)

12.1.3 Registers

The registers that control watchdog timer 1 are as follows.

- Watchdog timer clock selection register (WDCS)
- Watchdog timer mode register 1 (WDTM1)

(1) Watchdog timer clock selection register (WDCS)

This register sets the overflow time of watchdog timer 1 and the interval timer.

The WDCS register can be read or written in 8-bit or 1-bit units.

Reset sets WDCS to 00H.

After reset: 00H R/W Address: FFFFF6C1H

	7	6	5	4	3	2	1	0
WDCS	0	0	0	0	0	WDCS2	WDCS1	WDCS0

WDCS2	WDCS1	WDCS0	Overflow time of watchdog timer 1/interval timer			
				f_{XW}		
				4 MHz	5 MHz	10 MHz
0	0	0	$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
0	0	1	$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.638 ms
0	1	0	$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
0	1	1	$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
1	0	0	$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
1	0	1	$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.2 ms
1	1	0	$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
1	1	1	$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

(2) Watchdog timer mode register 1 (WDTM1)

This register sets the watchdog timer 1 operation mode and enables/disables count operations.

This register is a special register that can be written only in a special sequence (refer to **3.4.7 Special registers**).

The WDTM1 register can be read or written in 8-bit or 1-bit units.

Reset sets WDTM1 to 00H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the WDTM1 register.
For details, refer to 3.4.8 (1) (b).

After reset: 00H R/W Address: FFFFF6C2H

	<7>	6	5	4	3	2	1	0
WDTM1	RUN1	0	0	WDTM14	WDTM13	0	0	0

RUN1	Selection of operation mode of watchdog timer 1[Note 1]
0	Stop counting
1	Clear counter and start counting

WDTM14	WDTM13	Selection of operation mode of watchdog timer 1[Note 2]
0	0	Interval timer mode (Upon overflow, maskable interrupt INTWDTM1 is generated.)
0	1	
1	0	Watchdog timer mode 1[Note 3] (Upon overflow, non-maskable interrupt INTWDT1 is generated.)
1	1	Watchdog timer mode 2 (Upon overflow, reset operation WDTRES1 is started.)

Notes 1. Once the RUN1 bit is set (to 1), it cannot be cleared (to 0) by software.
Therefore, when counting is started, it cannot be stopped except reset.

2. Once the WDTM13 and WDTM14 bits are set (to 1), they cannot be cleared (to 0) by software and can be cleared only by reset.

3. For non-maskable interrupt servicing due to non-maskable interrupt request signal (INTWDT1), refer to **21.10 Cautions**.

12.1.4 Operation

(1) Operation as watchdog timer 1

Watchdog timer 1 operation to detect a program loop is selected by setting the WDTM1.WDTM14 bit to 1.

The count clock (program loop detection time interval) of watchdog timer 1 can be selected using the WDCS.WDCS0 to WDCS.WDCS2 bits. The count operation is started by setting the WDTM1.RUN1 bit to 1. When, after the count operation is started, the RUN1 bit is again set to 1 within the set program loop detection time interval, watchdog timer 1 is cleared and the count operation starts again.

If the program loop detection time is exceeded without RUN1 bit being set to 1, reset signal (WDTRES1) through the value of the WDTM1.WDTM13 bit or a non-maskable interrupt request signal (INTWDT1) is generated.

The count operation of watchdog timer 1 stops in the STOP mode and IDLE mode. Set the RUN1 bit to 1 before the STOP mode or IDLE mode is entered in order to clear watchdog timer 1.

Because watchdog timer 1 operates in the HALT mode, make sure that an overflow will not occur during HALT.

Cautions 1. When the subclock is selected for the CPU clock, the count operation of watchdog timer 1 is stopped (the value of watchdog timer 1 is maintained).

2. For non-maskable interrupt servicing due to the INTWDT1 signal, refer to 21.10 Cautions.

Table 12-2. Program Loop Detection Time of Watchdog Timer 1

Clock	Program Loop Detection Time		
	f_{XW} = 4 MHz	f_{XW} = 5 MHz	f_{XW} = 10 MHz
$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.683 ms
$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.21 ms
$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

(2) Operation as interval timer

Watchdog timer 1 can be made to operate as an interval timer that repeatedly generates interrupts using the count value set in advance as the interval, by clearing the WDTM1.WDTM14 bit to 0.

When watchdog timer 1 operates as an interval timer, the interrupt mask flag (WDTMK) and priority specification flags (WDTPR0 to WDTPR2) of the WDTIC register are valid and maskable interrupt request signals (INTWDTM1) can be generated. The default priority of the INTWDTM1 signal is set to the highest level among the maskable interrupt request signals.

The interval timer continues to operate in the HALT mode, but it stops operating in the STOP mode and the IDLE mode.

Cautions 1. Once the WDTM14 bit is set to 1 (thereby selecting the watchdog timer 1 mode), the interval timer mode is not entered as long as reset is not performed.

2. When the subclock is selected for the CPU clock, the count operation of the watchdog timer 1 stops (the value of the watchdog timer is maintained).

Table 12-3. Interval Time of Interval Timer

Clock	Interval Time		
	f_{XW} = 4 MHz	f_{XW} = 5 MHz	f_{XW} = 10 MHz
$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.638 ms
$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.21 ms
$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

12.2 Watchdog Timer 2

12.2.1 Functions

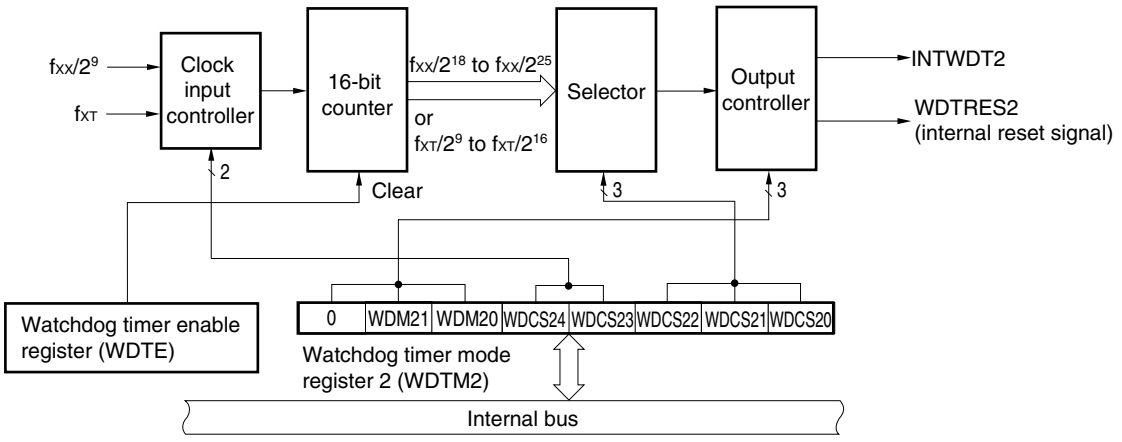
Watchdog timer 2 has the following functions.

- Default start watchdog timer[Note 1]
  → Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDTRES2 signal)
  → Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2 signal)[Note 2]
- Input selectable from main clock and subclock as the source clock

Notes 1. Watchdog timer 2 automatically starts in the reset mode following reset release.
When watchdog timer 2 is not used, either stop its operation before reset is executed through this function, or clear once watchdog timer 2 and stop it within the next interval time.
Also, write to the WDTM2 register for verification purposes only once, even if the default settings (reset mode, interval time: $f_{XX}/2^{25}$) need not be changed.

2. For non-maskable interrupt servicing due to a non-maskable interrupt request signal (INTWDT2), refer to **21.10 Cautions**.

Figure 12-2. Block Diagram of Watchdog Timer 2



Remark f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
INTWDT2: Non-maskable interrupt request signal through watchdog timer 2
WDTRES2: Watchdog timer 2 reset signal

12.2.2 Configuration

Watchdog timer 2 includes the following hardware.

Table 12-4. Configuration of Watchdog Timer 2

Item	Configuration
Control register	Watchdog timer mode register 2 (WDTM2) Watchdog timer enable register (WDTE)

12.2.3 Registers

(1) Watchdog timer mode register 2 (WDTM2)

This register sets the overflow time and operation clock of watchdog timer 2.

The WDTM2 register can be read or written in 8-bit units. This register can be read any number of times, but it can be written only once following reset release.

Reset sets WDTM2 to 67H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the WDTM2 register.
For details, refer to 3.4.8 (1) (b).

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4	3	2	1	0
WDTM2	0	WDM21	WDM20	WDCS24	WDCS23	WDCS22	WDCS21	WDCS20

WDM21	WDM20	Selection of operation mode of watchdog timer 2
0	0	Stops operation
0	1	Non-maskable interrupt request mode (generation of INTWDT2)
1	–	Reset mode (generation of WDTRES2)

Cautions 1. To stop the operation of watchdog timer 2, write "1FH" to the WDTM2 register.
2. For details about bits WDCS0 to WDCS4, refer to Table 12-5 Watchdog Timer 2 Clock Selection.
3. If the WDTM2 register is written twice after a reset, an overflow signal is forcibly output.
4. To intentionally generate an overflow signal, write data to the WDTM2 register only twice, or write a value other than "ACH" to the WDTE register only once.

Table 12-5. Watchdog Timer 2 Clock Selection

WDCS24	WDCS23	WDCS22	WDCS21	WDCS20	Selected Clock	f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
0	0	0	0	0	$2^{18}/f_{XX}$	13.1 ms	16.4 ms	26.2 ms
0	0	0	0	1	$2^{19}/f_{XX}$	26.2 ms	32.8 ms	52.4 ms
0	0	0	1	0	$2^{20}/f_{XX}$	52.4 ms	65.5 ms	104.9 ms
0	0	0	1	1	$2^{21}/f_{XX}$	104.9 ms	131.1 ms	209.7 ms
0	0	1	0	0	$2^{22}/f_{XX}$	209.7 ms	262.1 ms	419.4 ms
0	0	1	0	1	$2^{23}/f_{XX}$	419.4 ms	524.3 ms	838.9 ms
0	0	1	1	0	$2^{24}/f_{XX}$	838.9 ms	1048.6 ms	1677.7 ms
0	0	1	1	1	$2^{25}/f_{XX}$	1677.7 ms	2097.2 ms	3355.4 ms
0	1	0	0	0	$2^{9}/f_{XT}$	15.625 ms (f_{XT} = 32.768 kHz)		
0	1	0	0	1	$2^{10}/f_{XT}$	31.25 ms (f_{XT} = 32.768 kHz)		
0	1	0	1	0	$2^{11}/f_{XT}$	62.5 ms (f_{XT} = 32.768 kHz)		
0	1	0	1	1	$2^{12}/f_{XT}$	125 ms (f_{XT} = 32.768 kHz)		
0	1	1	0	0	$2^{13}/f_{XT}$	250 ms (f_{XT} = 32.768 kHz)		
0	1	1	0	1	$2^{14}/f_{XT}$	500 ms (f_{XT} = 32.768 kHz)		
0	1	1	1	0	$2^{15}/f_{XT}$	1000 ms (f_{XT} = 32.768 kHz)		
0	1	1	1	1	$2^{16}/f_{XT}$	2000 ms (f_{XT} = 32.768 kHz)		
1	×	×	×	×	Operation stopped			

(2) Watchdog timer enable register (WDTE)

The counter of watchdog timer 2 is cleared and counting restarted by writing “ACH” to the WDTE register.

The WDTE register can be read or written in 8-bit units.

Reset sets WDTE to 9AH.

After reset: 9AH R/W Address: FFFFF6D1H

	7	6	5	4	3	2	1	0
WDTE								

Cautions 1. When a value other than “ACH” is written to the WDTE register, an overflow signal is forcibly output.

2. When a 1-bit memory manipulation instruction is executed for the WDTE register, an overflow signal is forcibly output.

3. The read value of the WDTE register is always “9AH” (value that differs from written value “ACH”).

4. To intentionally generate an overflow signal, write a value other than “ACH” to the WDTE register only once, or write data to the WDTM2 register only twice.

12.2.4 Operation

Watchdog timer 2 automatically starts in the reset mode following reset release.

The WDTM2 register can be written to only once following reset through byte access. To use watchdog timer 2, write the operation mode and the interval time to the WDTM2 register using 8-bit memory manipulation instructions. After this is done, the operation of watchdog timer 2 cannot be stopped.

The watchdog timer 2 program loop detection time interval can be selected by the WDTM2.WDCS24 to WDTM2.WDCS20 bits. Writing ACH to the WDTE register clears the counter of watchdog timer 2 and starts the count operation again. After the count operation starts, write ACH to the WDTE register within the set program loop detection time interval.

If the program loop detection time is exceeded without ACH being written to the WDTE register, a reset signal (WDTRES2) or non-maskable interrupt request signal (INTWDT2) is generated depending on the set value of the WDTM2.WDM21 and WDTM2.WDM20 bits.

To not use watchdog timer 2, write 1FH to the WDTM2 register.

For non-maskable interrupt servicing when the non-maskable interrupt request mode is set, refer to **21.10 Cautions**.

If the main clock is selected as the source clock of watchdog timer 2, the watchdog timer stops operation in the IDLE/STOP mode. Therefore, clear watchdog timer 2 by writing ACH to the WDTE register before the IDLE/STOP mode is set.

Because watchdog timer 2 operates in the HALT mode or when the subclock is selected as its source clock in the IDLE/STOP mode, exercise care that the timer does not overflow in the HALT mode.

13.1 Function

The real-time output function (RTO) transfers preset data to the RTBL0 and RTBH0 registers, and then transfers this data with hardware to an external device via the real-time output latches, upon occurrence of a timer interrupt. The pins through which the data is output to an external device constitute a port called a real-time output port.

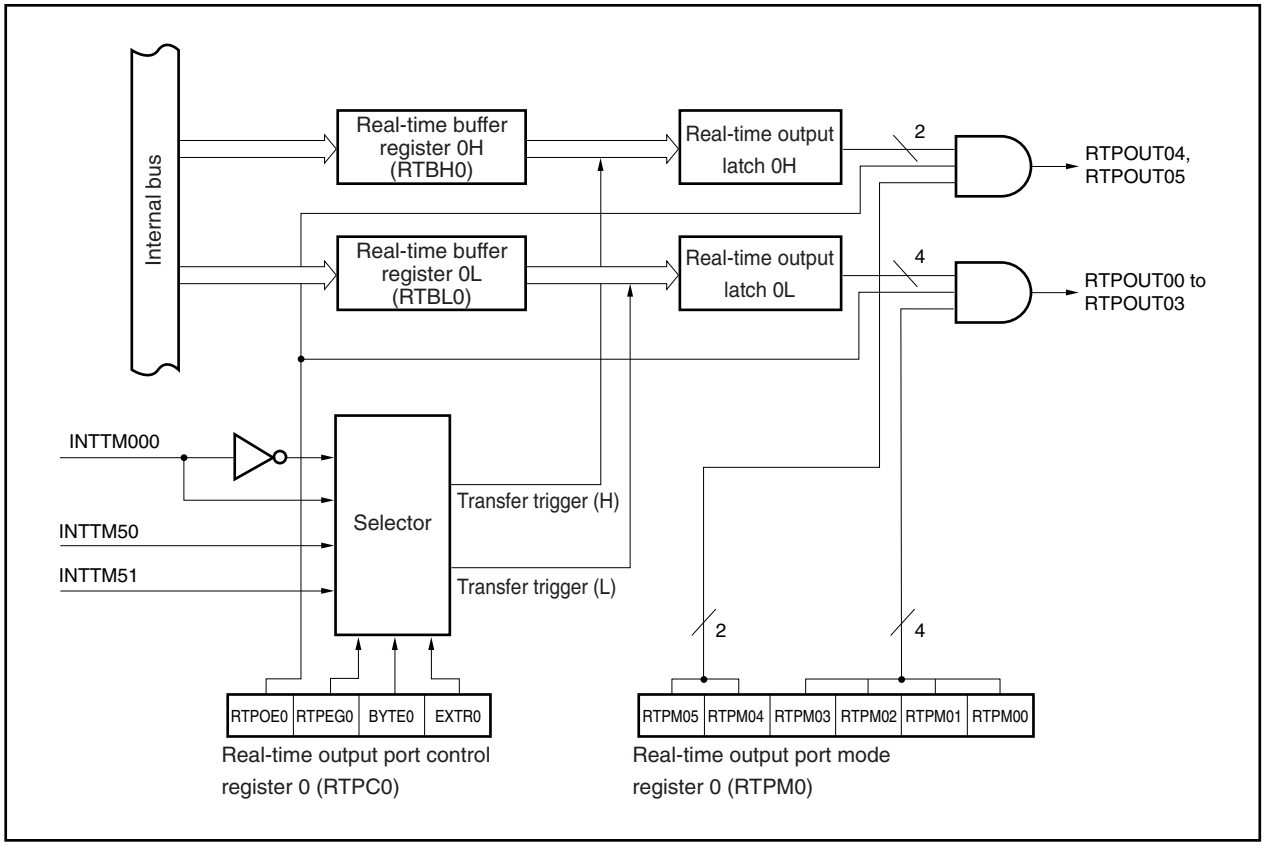
Because RTO can output signal without jitter, it is suitable for controlling a stepping motor.

In the V850ES/KG2, a 6-bit real-time output port channel is provided.

The real-time output port can be set in the port mode or real-time output port mode in 1-bit units.

The block diagram of RTO is shown below.

Figure 13-1. Block Diagram of RTO



13.2 Configuration

RTO includes the following hardware.

Table 13-1. Configuration of RTO

Item	Configuration
Registers	Real-time output buffer register 0 (RTBL0, RTBH0)
Control registers	Real-time output port mode register 0 (RTPM0) Real-time output port control register 0 (RTPC0)

(1) Real-time output buffer register 0 (RTBL0, RTBH0)

RTBL0 and RTBH0 are 4-bit registers that hold output data in advance.

These registers are mapped to independent addresses in the peripheral I/O register area.

They can be read or written in 8-bit or 1-bit units.

If an operation mode of 4 bits × 1 channel or 2 bits × 1 channel is specified (RTPC0.BYTE0 bit = 0), data can be individually set to the RTBL0 and RTBH0 registers. The data of both these registers can be read at once by specifying the address of either of these registers.

If an operation mode of 6 bits × 1 channel is specified (BYTE0 bit = 1), 8-bit data can be set to both the RTBL0 and RTBH0 registers by writing the data to either of these registers. Moreover, the data of both these registers can be read at once by specifying the address of either of these registers.

Table 13-2 shows the operation when the RTBL0 and RTBH0 registers are manipulated.

After reset: 00H R/W Address: RTBL0 FFFFF6E0H, RTBH0 FFFFF6E2H

	7	6	5	4	3	2	1	0
RTBL0					RTBL03	RTBL02	RTBL01	RTBL00
RTBH0	0	0	RTBH05	RTBH04				

Cautions 1. When writing to bits 6 and 7 of the RTBH0 register, always write 0.

2. When the main clock is stopped and the CPU is operating on the subclock, do not access the RTBL0 and RTBH0 registers using an access method that causes a wait. For details, refer to 3.4.8 (1) (b).

Table 13-2. Operation During Manipulation of RTBL0 and RTBH0 Registers

Operation Mode	Register to Be Manipulated	Read		Write[Note]	
		Higher 4 bits	Lower 4 bits	Higher 4 bits	Lower 4 bits
4 bits × 1 channel, 2 bits × 1 channel	RTBL0	RTBH0	RTBL0	Invalid	RTBL0
	RTBH0	RTBH0	RTBL0	RTBH0	Invalid
6 bits × 1 channel	RTBL0	RTBH0	RTBL0	RTBH0	RTBL0
	RTBH0	RTBH0	RTBL0	RTBH0	RTBL0

Note After setting the real-time output port, set output data to the RTBL0 and RTBH0 registers by the time a real-time output trigger is generated.

13.3 Registers

RTO is controlled using the following two types of registers.

- Real-time output port mode register 0 (RTPM0)
- Real-time output port control register 0 (RTPC0)

(1) Real-time output port mode register 0 (RTPM0)

This register selects the real-time output port mode or port mode in 1-bit units.

The RTPM0 register can be read or written in 8-bit or 1-bit units.

Reset sets RTPM0 to 00H.

After reset: 00H R/W Address: FFFFF6E4H

	7	6	5	4	3	2	1	0
RTPM0	0	0	RTPM05	RTPM04	RTPM03	RTPM02	RTPM01	RTPM00

RTPM0m	Control of real-time output port (m = 0 to 5)
0	Real-time output disabled
1	Real-time output enabled

Cautions 1. To reflect real-time output signals (RTPOUT00 to RTPOUT05) to the pins (RTP00 to RTP05), set them to the real-time output port with the PMC5 and PFC5 registers.

2. By enabling real-time output operation (RTPC0.RTPOE0 bit = 1), the bits specified as real-time output enabled perform real-time output, and the bits specified as real-time output disabled output 0.

3. If real-time output is disabled (RTPOE0 bit = 0), real-time output signals (RTPOUT00 to RTPOUT05) all output 0, regardless of the RTPM0 register setting.

(2) Real-time output port control register 0 (RTPC0)

This register sets the operation mode and output trigger of the real-time output port.

The relationship between the operation mode and output trigger of the real-time output port is as shown in Table 13-3.

The RTPC0 register can be read or written in 8-bit or 1-bit units.

Reset sets RTPC0 to 00H.

After reset: 00H R/W Address: FFFFF6E5H

	<7>	6	5	4	3	2	1	0
RTPC0	RTPOE0	RTPEG0	BYTE0	EXTR0[Note 1]	0	0	0	0

RTPOE0	Control of real-time output operation
0	Disables operation[Note 2]
1	Enables operation

RTPEG0	Valid edge of INTTM000 signal
0	Falling edge[Note 3]
1	Rising edge

BYTE0	Specification of channel configuration for real-time output
0	4 bits × 1 channel, 2 bits × 1 channel
1	6 bits × 1 channel

Notes 1. For the EXTR0 bit, refer to **Table 13-3**.

2. When real-time output operation is disabled (RTPOE0 bit = 0), real-time output signals (RTPOUT00 to RTPOUT05) all output 0.

3. The INTTM000 signal is output for 1 clock of the count clock selected with 16-bit timer/event counter 00.

Caution Perform the settings for the RTPEG0, BYTE0, and EXTR0 bits only when the RTPOE0 bit = 0.

Table 13-3. Operation Modes and Output Triggers of Real-Time Output Port

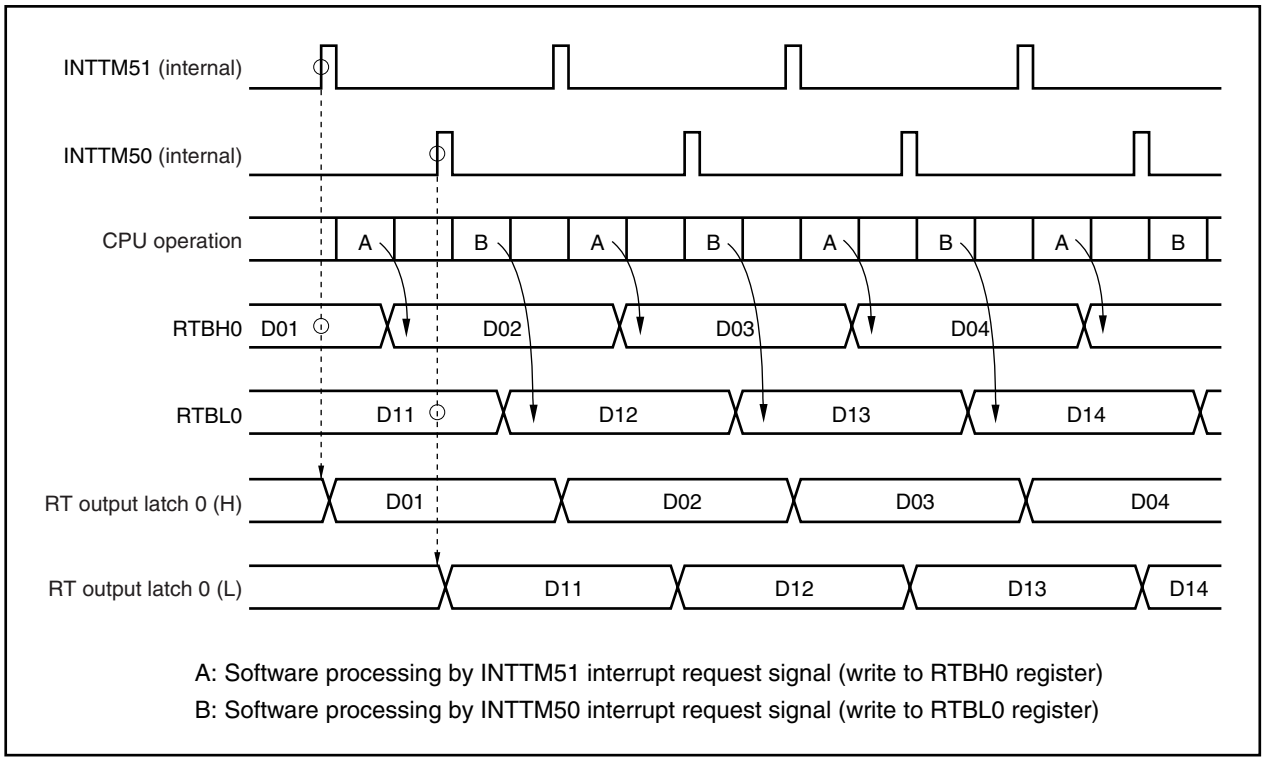
BYTE0	EXTR0	Operation Mode	RTBH0 (RTP04, RTP05)	RTBL0 (RTP00 to RTP03)
0	0	4 bits × 1 channel, 2 bits × 1 channel	INTTM51	INTTM50
	1		INTTM50	INTTM000
1	0	6 bits × 1 channel	INTTM50	
	1		INTTM000	

13.4 Operation

If the real-time output operation is enabled by setting the RTPC0.RTPOE0 bit to 1, the data of the RTBH0 and RTBL0 registers is transferred to the real-time output latch in synchronization with the generation of the selected transfer trigger (set by the RTPC0.EXTR0 and RTPC0.BYTE0 bits). Of the transferred data, only the data of the bits specified as real-time output enabled by the RTPM0 register is output from bits RTPOUT00 to RTPOUT05. The bits specified as real-time output disabled by the RTPM0 register output 0.

If the real-time output operation is disabled by clearing the RTPOE0 bit to 0, the RTPOUT00 to RTPOUT05 signals output 0 regardless of the setting of the RTPM0 register.

Figure 13-2. Example of Operation Timing of RTO0 (When EXTR0 and BYTE0 Bits = 00)



Remark For the operation during standby, refer to **CHAPTER 23 STANDBY FUNCTION**.

13.5 Usage

(1) Disable real-time output.
Clear the RTPC0.RTPOE0 bit to 0.

(2) Perform initialization as follows.
- Specify the real-time output port mode or port mode in 1-bit units.
  Set the RTPM0 register.
- Channel configuration: Select the trigger and valid edge.
  Set the RTPC0.EXTR0, RTPC0.BYTE0, and RTPC0.RTPEG0 bits.
- Set the initial values to the RTBH0 and RTBL0 registers[Note 1].

(3) Enable real-time output.
Set the RTPOE0 bit to 1.

(4) Set the next output value to the RTBH0 and RTBL0 registers by the time the selected transfer trigger is generated[Note 2].

(5) Set the next real-time output value to the RTBH0 and RTBL0 registers through interrupt servicing corresponding to the selected trigger.

Notes 1. If write to the RTBH0 and RTBL0 registers is performed when the RTPOE0 bit = 0, that value is transferred to real-time output latches 0H and 0L, respectively.

2. Even if write is performed to the RTBH0 and RTBL0 registers when the RTPOE0 bit = 1, data transfer to real-time output latches 0H and 0L is not performed.

Caution To reflect the real-time output signals (RTPOUT00 to RTPOUT05) to the pins, set the real-time output ports (RTP00 to RTP05) with the PMC5 and PFC5 registers.

13.6 Cautions

(1) Prevent the following conflicts by software.

- Conflict between real-time output disable/enable switching (RTPOE0 bit) and selected real-time output trigger
- Conflict between write to the RTBH0 and RTBL0 registers in the real-time output enabled status and the selected real-time output trigger.

(2) Before performing initialization, disable real-time output (RTPOE0 bit = 0).

(3) Once real-time output has been disabled (RTPOE0 bit = 0), be sure to initialize the RTBH0 and RTBL0 registers before enabling real-time output again (RTPOE0 bit = 0 → 1).

13.7 Security Function

A circuit that sets the pin outputs to high impedance as a security function for when malfunctions of a stepping motor controlled by RTO occur is provided on chip. It forcibly resets the pins allocated to RTP00 to RTP05 via external interrupt INTP0 pin edge detection, placing them in the high-impedance state.

The ports (P50 to P55 pins) placed in high impedance by INTP0[Note 1] pin are initialized[Note 2], so settings for these ports must be performed again.

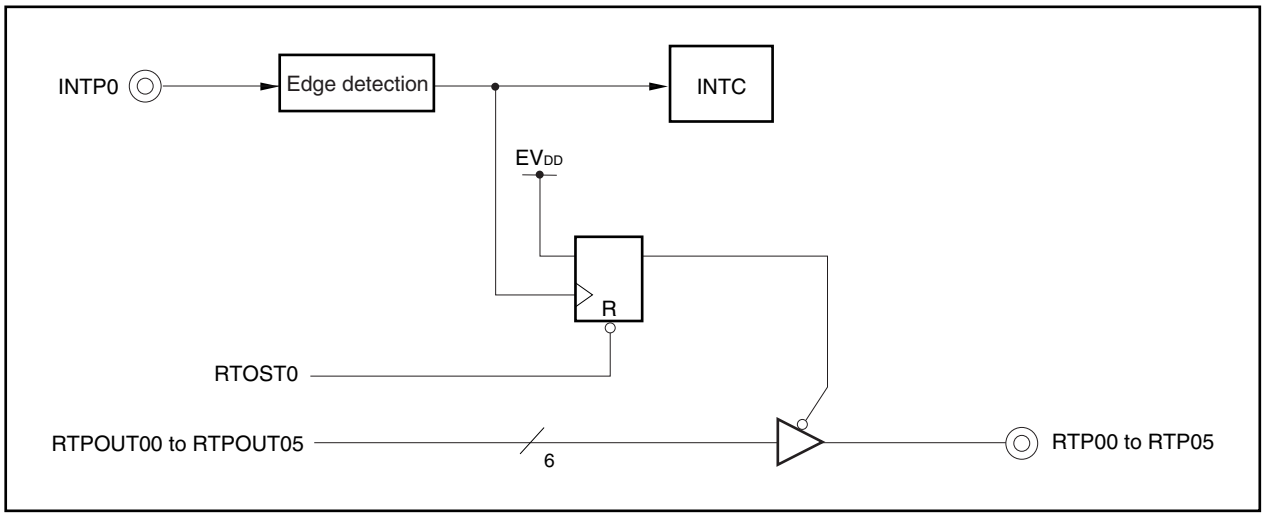
Notes 1. Regardless of the port settings, P50 to P55 pins are all placed in high impedance via the INTP0 pin.

2. The bits that are initialized are all the bits corresponding to P50 to P55 pins of the following registers.

- P5 register
- PM5 register
- PMC5 register
- PU5 register
- PFC5 register
- PF5 register

The block diagram of the security function is shown below.

Figure 13-3. Block Diagram of Security Function



This function is set with the PLLCTL.RTOST0 bit.

(1) PLL control register (PLLCTL)

The PLLCTL register is an 8-bit register that controls the RTO security function and PLL.

This register can be read or written in 8-bit or 1-bit units.

Reset sets PLLCTL to 01H.

After reset: 01H R/W Address: FFFFF806H

	7	6	5	4	3	<2>	<1>	<0>
PLLCTL	0	0	0	0	0	RTOST0	SELPLL Note	PLLON Note

RTOST0	Control of RTP00 to RTP05 security function
0	INTP0 pin is not used as trigger for security function
1	INTP0 pin is used as trigger for security function

Note For details on the SELPLL and PLLON bits, refer to **CHAPTER 6 CLOCK GENERATION FUNCTION**.

Cautions 1. Before outputting a value to the real-time output ports (RTP00 to RTP05), select the INTP0 pin interrupt edge detection and then set the RTOST0 bit.

2. To set again the ports (P50 to P55 pins) as real-time output ports after placing them in high impedance via the INTP0 pin, first cancel the security function.

[Procedure to set ports again]

<1> Cancel the security function and enable port setting by clearing the RTOST0 bit to 0.

<2> Set the RTOST0 bit to 1 (only if required)

<3> Set again as real-time output port.

3. Be sure to clear bits 4 to 7 to "0". Changing bit 3 does not affect the operation.

CHAPTER 14 A/D CONVERTER

14.1 Overview

The A/D converter converts analog input signals into digital values and has an 8-channel (ANI0 to ANI7) configuration.

The A/D converter has the following functions.

- ○ Operating voltage (AV_{REF0}): 2.7 to 5.5 V
- ○ Successive approximation method 10-bit A/D converter
- ○ Analog input pin: 8
- ○ Trigger mode:
  - Software trigger mode
  - Timer trigger mode (INTTM010)
  - External trigger mode (ADTRG pin)
- ○ Operation mode
  - Select mode
  - Scan mode
- ○ A/D conversion time:
  - Normal mode:
    14 to 100 μs @ 4.0 V ≤ AV_{REF0} ≤ 5.5 V
    17 to 100 μs @ 2.7 V ≤ AV_{REF0} < 4.0 V
  - High-speed mode:
    3 to 100 μs @ 4.5 V ≤ AV_{REF0} ≤ 5.5 V
    4.8 to 100 μs @ 4.0 V ≤ AV_{REF0} < 4.5 V
    6 to 100 μs @ 2.85 V ≤ AV_{REF0} < 4.0 V
    14 to 100 μs @ 2.7 V ≤ AV_{REF0} < 2.85 V
- ○ Power fail detection function

Caution When using the A/D converter, operate with AV_{REF0} at the same potential as V_{DD} and EV_{DD}.

14.2 Functions

(1) 10-bit resolution A/D conversion

1 analog input channel is selected from the ANI0 to ANI7 pins, and an A/D conversion operation with resolution of 10 bits is repeatedly executed. Every time A/D conversion is completed, an interrupt request signal (INTAD) is generated.

(2) Power fail detection function

This is a function to detect low voltage in a battery. The results of A/D conversion (the value in the ADCRH register) and the PFT register are compared, and INTAD signal is generated only when the comparison conditions match.

14.3 Configuration

The A/D converter includes the following hardware.

Figure 14-1. Block Diagram of A/D Converter

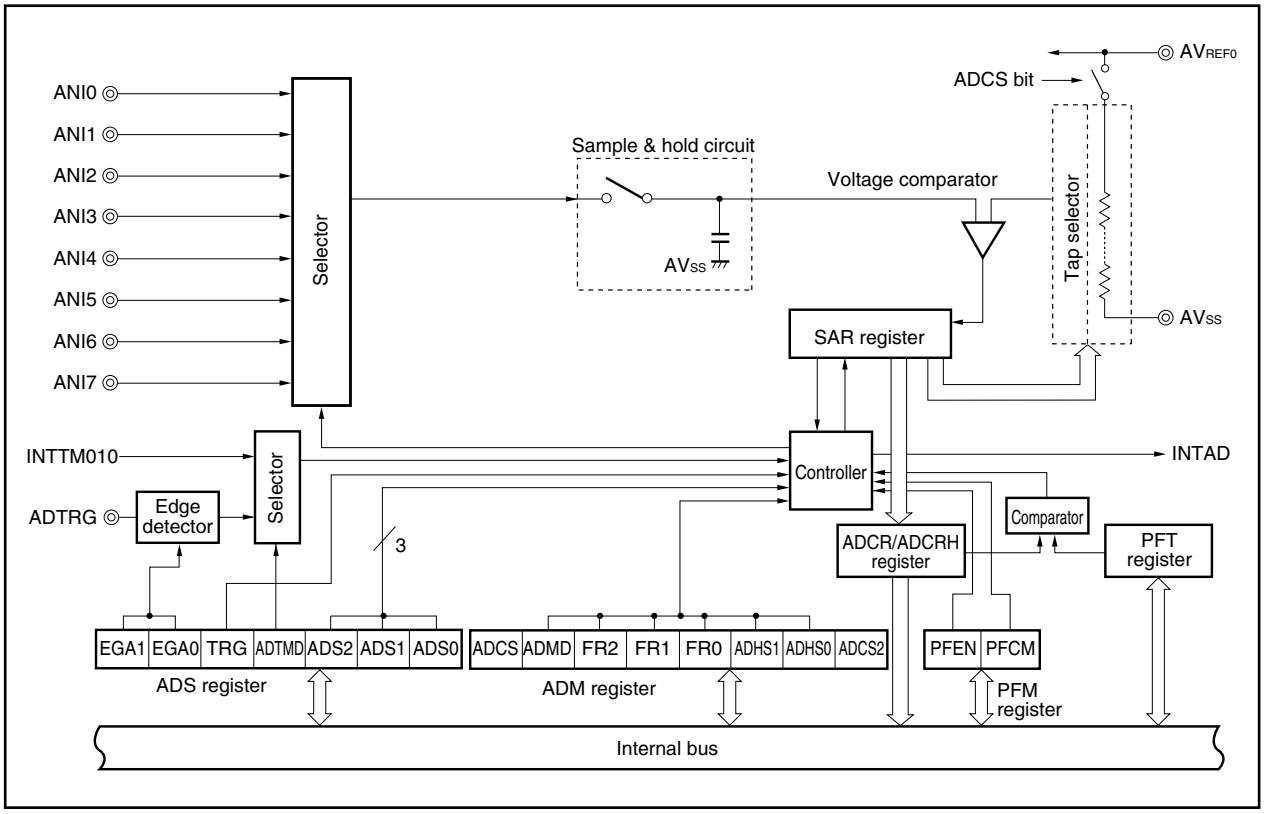


Table 14-1. Registers of A/D Converter Used by Software

Item	Configuration
Registers	A/D conversion result register (ADCR) A/D conversion result register H (ADCRH): Only higher 8 bits can be read Power fail comparison threshold register (PFT) A/D converter mode register (ADM) Analog input channel specification register (ADS) Power fail comparison mode register (PFM)

(1) ANI0 to ANI7 pins

These are analog input pins for the 8 channels of the A/D converter. They are used to input analog signals to be converted into digital signals. Pins other than those selected as analog input by the ADS register can be used as input ports.

(2) Sample & hold circuit

The sample & hold circuit samples the analog input signals selected by the input circuit and sends the sampled data to the voltage comparator. This circuit holds the sampled analog input voltage during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AV_{REF0} and AV_{SS} and generates a voltage for comparison with the analog input signal.

(4) Voltage comparator

The voltage comparator compares the value that is sampled and held with the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register compares the sampled analog voltage value with the voltage value from the series resistor string, and converts the comparison result starting from the most significant bit (MSB).

When the least significant bit (LSB) has been converted to a digital value (end of A/D conversion), the contents of the SAR register are transferred to the ADCR register.

The SAR register cannot be read or written directly.

(6) A/D conversion result register (ADCR), A/D conversion result register H (ADCRH)

Each time A/D conversion ends, the conversion results are loaded from the successive approximation register and the results of A/D conversion are held in the higher 10 bits of this register (the lower 6 bits are fixed to 0).

(7) Controller

The controller compares the A/D conversion results (the value of the ADCRH register) with the value of the PFT register when A/D conversion ends or the power fail detection function is used. It generates INTAD signal only when the comparison conditions match.

(8) AV_{REF0} pin

This is the analog power supply pin/reference voltage input pin of the A/D converter. Always use the same potential as the V_{DD} pin even when not using the A/D converter.

The signals input to the ANI0 to ANI7 pins are converted into digital signals based on the voltage applied across AV_{REF0} and AV_{SS}.

(9) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use the same potential as the V_{SS} pin even when not using the A/D converter.

(10) A/D converter mode register (ADM)

This register sets the conversion time of the analog input to be converted to a digital signal and the conversion operation start/stop.

(11) Analog input channel specification register (ADS)

This register specifies the input port for the analog voltage to be converted to a digital signal.

(12) Power fail comparison mode register (PFM)

This register sets the power fail detection mode.

(13) Power fail comparison threshold register (PFT)

This register sets the threshold to be compared with the ADCR register.

14.4 Registers

The A/D converter is controlled by the following registers.

- A/D converter mode register (ADM)
- Analog input channel specification register (ADS)
- Power fail comparison mode register (PFM)
- Power fail comparison threshold register (PFT)
- A/D conversion result register, A/D conversion result register H (ADCR, ADCRH)

(1) A/D converter mode register (ADM)

This register sets the conversion time of the analog input signal to be converted into a digital signal as well as conversion start and stop.

The ADM register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF200H

	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	ADMD	FR2 Note 1	FR1 Note 1	FR0 Note 1	ADHS1 Note 1	ADHS0 Note 1	ADCS2

ADCS	Control of A/D conversion operation
0	Conversion operation stopped
1	Conversion operation enabled

ADMD	Control of operation mode
0	Select mode
1	Scan mode

ADHS1	Selection of 5 V A/D conversion time mode ($AV_{REF0} \geq 4.5$ V)
0	Normal mode
1	High-speed mode (valid only when $AV_{REF0} \geq 4.5$ V)

ADHS0	Selection of 3 V A/D conversion time mode ($AV_{REF0} \geq 2.7$ or 2.85 V)
0	Normal mode
1	High-speed mode (valid only when $AV_{REF0} \geq 2.7$ or 2.85 V)

ADCS2	Control of reference voltage generator for boosting Note 2
0	Reference voltage generator operation stopped
1	Reference voltage generator operation enabled

Notes 1. For details of the FR2 to FR0 bits and the A/D conversion, refer to **Table 14-2 A/D Conversion Time**.

2. The operation of the reference voltage generator for boosting is controlled by the ADCS bit and it takes 1 μs (high-speed mode) or 14 μs (normal mode) after operation is started until it is stabilized. Therefore, the ADCS2 bit is set to 1 (A/D conversion is started) at least 1 μs (high-speed mode) or 14 μs (normal mode) after if the ADCS2 bit was set to 1 (reference voltage generator for boosting is on), the first conversion result is valid.

Cautions 1. Changing bits FR2 to FR0, ADHS1, and ADHS0 while the ADCS bit = 1 is prohibited (write access to the ADM register is enabled and rewriting of bits FR2 to FR0, ADHS1, and ADHS0 is prohibited).

2. Setting ADHS1 and ADHS0 bits to 11 is prohibited.

3. Do not access the ADM register when the main clock is stopped and the subclock is operating. For details, refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register.

Table 14-2. A/D Conversion Time

ADHS1	ADHS0	FR2	FR1	FR0		A/D Conversion Time (μs)				Conversion Time Mode
						20 MHz@ $AV_{REF0} \geq 4.5$ V	16 MHz@ $AV_{REF0} \geq 4.0$ V	8 MHz@ $AV_{REF0} \geq 2.85$ V	8 MHz@ $AV_{REF0} \geq 2.7$ V	
0	0	0	0	0	288/f_{XX}	14.4	18.0	36.0	36.0	Normal mode $AV_{REF0} \geq 2.7$ V
0	0	0	0	1	240/f_{XX}	Setting prohibited	15.0	30.0	30.0	
0	0	0	1	0	192/f_{XX}	Setting prohibited	Setting prohibited	24.0	24.0	
0	0	0	1	1	Setting prohibited					
0	0	1	0	0	144/f_{XX}	Setting prohibited	Setting prohibited	18.0	18.0	Normal mode $AV_{REF0} \geq 2.7$ V
0	0	1	0	1	120/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	0	1	1	0	96/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	0	1	1	1	Setting prohibited					
0	1	0	0	0	96/f_{XX}	4.8	6.0	12.0	Setting prohibited	High-speed mode $AV_{REF0} \geq 2.85$ V
0	1	0	0	1	72/f_{XX}	Setting prohibited	Setting prohibited	9.0	Setting prohibited	
0	1	0	1	0	48/f_{XX}	Setting prohibited	Setting prohibited	6.0	Setting prohibited	
0	1	0	1	1	24/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	1	1	0	0	224/f_{XX}	11.2	14.0	28.0	28.0	High-speed mode $AV_{REF0} \geq 2.7$ V
0	1	1	0	1	168/f_{XX}	Setting prohibited	10.5	21.0	21.0	
0	1	1	1	0	112/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
0	1	1	1	1	56/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
1	0	0	0	0	72/f_{XX}	3.6	Setting prohibited	Setting prohibited	Setting prohibited	High-speed mode $AV_{REF0} \geq 4.5$ V
1	0	0	0	1	54/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
1	0	0	1	0	36/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
1	0	0	1	1	18/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	
1	0	1	×	×	Setting prohibited					
1	1	×	×	×	Setting prohibited					

Remark f_{XX}: Main clock frequency

(a) Controlling reference voltage generator for boosting

When the ADCS2 bit = 0, power to the A/D converter drops. The converter requires a setup time of 1 μs (high-speed mode) or 14 μs (normal mode) or more after the ADCS2 bit has been set to 1.

Therefore, the result of A/D conversion becomes valid from the first result by setting the ADCS bit to 1 at least 1 μs (high-speed mode) or 14 μs (normal mode) after the ADCS2 bit has been set to 1.

Table 14-3. Setting of ADCS Bit and ADCS2 Bit

ADCS	ADCS2	A/D Conversion Operation
0	0	Stopped status (DC power consumption path does not exist)
0	1	Conversion standby mode (only the reference voltage generator for boosting consumes power)
1	0	Conversion mode (reference voltage generator stops operation[Note 1])
1	1	Conversion mode (reference voltage generator is operating[Note 2])

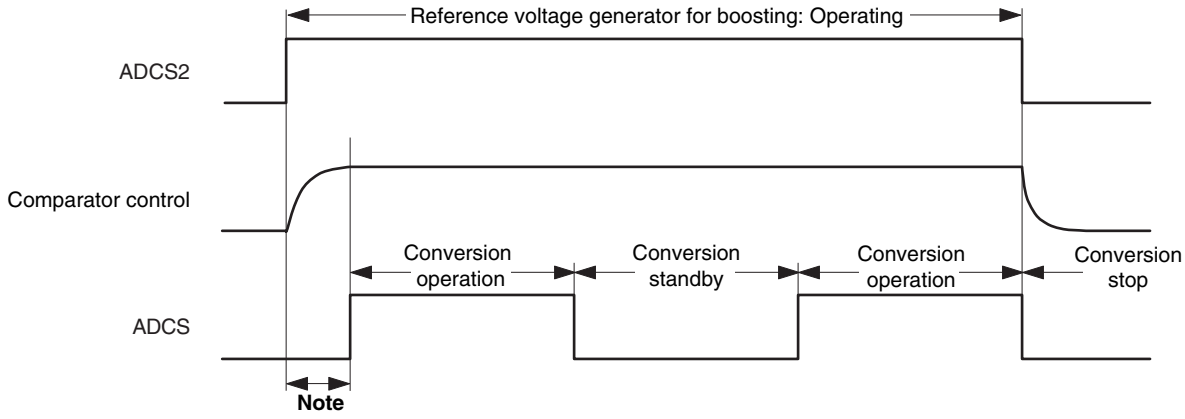
Notes 1. If the ADCS and ADCS2 bits are changed from 00B to 10B, the reference voltage generator for boosting automatically turns on. If the ADCS bit is cleared to 0 while the ADCS2 bit is 0, the voltage generator automatically turns off. In the software trigger mode (ADS.TRG bit = 0), use of the first A/D conversion result is prohibited.

In the hardware trigger mode (TRG bit = 1), use the A/D conversion result only if A/D conversion is started after the lapse of the oscillation stabilization time of the reference voltage generator for boosting.

2. If the ADCS and ADCS2 bits are changed from 00B to 11B, the reference voltage generator for boosting automatically turns on. If the ADCS bit is cleared to 0 while the ADCS2 bit is 1, the voltage generator stays on. In the software trigger mode (TRG bit = 0), use of the first A/D conversion result is prohibited.

In the hardware trigger mode (TRG bit = 1), use the A/D conversion result only if A/D conversion is started after the lapse of the oscillation stabilization time of the reference voltage generator for boosting.

Figure 14-2. Operation Sequence



Note 1 μs (high-speed mode) or 14 μs (normal mode) or more are required for the operation of the reference voltage generator for boosting between when the ADCS2 bit is set (1) and when the ADCS bit is set (1).

(2) Analog input channel specification register (ADS)

This register specifies the analog voltage input port for A/D conversion.

The ADS register can be read or written in 8-bit or 1-bit units.

Reset sets ADS to 00H.

After reset: 00H R/W Address: FFFFF201H

	7	6	5	4	3	2	1	0
ADS	EGA1 Note 1	EGA0 Note 1	TRG	ADTMD Note 2	0	ADS2	ADS1	ADS0

EGA1 Note 1	EGA0 Note 1	Specification of external trigger signal (ADTRG) edge
0	0	No edge detection
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

TRG	Trigger mode selection
0	Software trigger mode
1	Hardware trigger mode

ADTMD Note 2	Specification of hardware trigger mode
0	External trigger (ADTRG pin input)
1	Timer trigger (INTTM010 signal generated)

ADS2	ADS1	ADS0	Specification of analog input channel	
			Select mode	Scan mode
0	0	0	ANI0	ANI0
0	0	1	ANI1	ANI0, ANI1
0	1	0	ANI2	ANI0 to ANI2
0	1	1	ANI3	ANI0 to ANI3
1	0	0	ANI4	ANI0 to ANI4
1	0	1	ANI5	ANI0 to ANI5
1	1	0	ANI6	ANI0 to ANI6
1	1	1	ANI7	ANI0 to ANI7

Notes 1. The EGA1 and EGA0 bits are valid only when the hardware trigger mode (TRG bit = 1) and external trigger mode (ADTRG pin input: ADTMD bit = 1) are selected.

2. The ADTMD bit is valid only when the hardware trigger mode (TRG bit = 1) is selected.

Cautions 1. Do not access the ADS register when the main clock is stopped and the subclock is operating. For details, refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register.

2. Be sure to clear bit 3 to "0".

(3) A/D conversion result register, A/D conversion result register H (ADCR, ADCRH)

The ADCR and ADCRH registers store the A/D conversion results.

These registers are read-only in 16-bit or 8-bit units. However, specify the ADCR register for 16-bit access, and the ADCRH register for 8-bit access. In the ADCR register, the 10 bits of conversion results are read in the higher 10 bits and 0 is read in the lower 6 bits. In the ADCRH register, the higher 8 bits of the conversion results are read.

Reset makes these registers undefined.

After reset: Undefined R Address: FFFFF204H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCR	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	0	0	0	0	0

After reset: Undefined R Address: FFFFF205H

	7	6	5	4	3	2	1	0
ADCRH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

Caution Do not access the ADCR and ADCRH registers when the main clock is stopped and the subclock is operating. For details, refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register.

The following shows the relationship between the analog input voltage input to the analog input pins (ANI0 to ANI7) and A/D conversion results (ADCR register).

$$SAR = INT\left(\frac{V_{IN}}{AV_{REF0}} \times 1024 + 0.5\right)$$

$$ADCR^{Note} = SAR \times 64$$

Or,

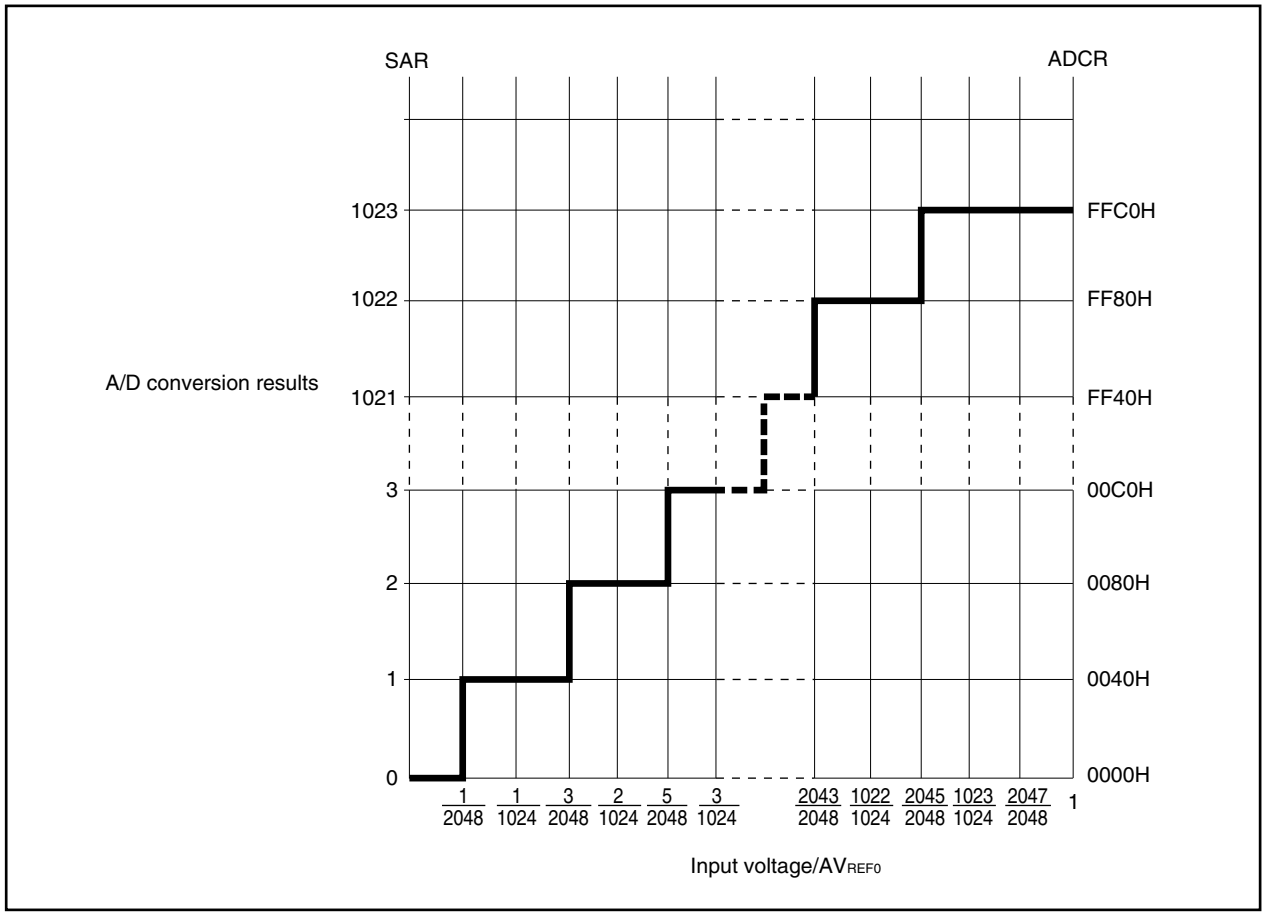
$$(SAR - 0.5) \times \frac{AV_{REF0}}{1024} \leq V_{IN} < (SAR + 0.5) \times \frac{AV_{REF0}}{1024}$$

INT ( ): Function that returns the integer part of the value in parentheses
V_{IN}: Analog input voltage
AV_{REF0}: Voltage of AV_{REF0} pin
ADCR: Value in the ADCR register

Note The lower 6 bits of the ADCR register are fixed to 0.

The following shows the relationship between the analog input voltage and A/D conversion results.

Figure 14-3. Relationship Between Analog Input Voltage and A/D Conversion Results



(4) Power fail comparison mode register (PFM)

This register sets the power fail detection mode.

The PFM register compares the value in the PFT register with the value of the ADCRH register.

The PFM register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF202H

	<7>	<6>	5	4	3	2	1	0
PFM	PFEN	PFCM	0	0	0	0	0	0

PFEN	Selection of power fail comparison enable/disable
0	Power fail comparison disabled
1	Power fail comparison enabled

PFCM	Selection of power fail comparison mode
0	Interrupt request signal (INTAD) generated when ADCR ≥ PFT
1	Interrupt request signal (INTAD) generated when ADCR < PFT

Caution Do not access the PFM register when the main clock is stopped and the subclock is operating. For details, refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register.

(5) Power fail comparison threshold register (PFT)

The PFT register sets the comparison value in the power fail detection mode.

The 8-bit data set in the PFT register is compared with the value of the ADCRH register.

The PFT register can be read or written in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF203H

	7	6	5	4	3	2	1	0
PFT								

Caution Do not access the PFT register when the main clock is stopped and the subclock is operating. For details, refer to 3.4.8 (1) (b) Access to special on-chip peripheral I/O register.

14.5 Operation

14.5.1 Basic operation

<1> Select the channel whose analog signal is to be converted into a digital signal using the ADS register.
Set the ADM.ADHS1 or ADM.ADHS0 bit.

<2> Set the ADM.ADCS2 bit to 1 and wait 1 μs (high-speed mode) or 14 μs (normal mode) or longer.

<3> Set the ADM.ADCS bit to 1 to start A/D conversion.
(Steps <4> to <10> are executed by hardware.)

<4> The sample & hold circuit samples the voltage input to the selected analog input channel.

<5> After sampling for a specific time, the sample & hold circuit enters the hold status and holds the input analog voltage until it has been converted into a digital signal.

<6> Set bit 9 of the successive approximation register (SAR) to 1. The tap selector sets the voltage tap of the series resistor string to (1/2) $\times$ AV_{REF0}.

<7> The voltage comparator compares the voltage difference between the voltage tap of the series resistor string and the analog input voltage. If the analog input voltage is greater than (1/2) $\times$ AV_{REF0}, the MSB of the SAR register remains set to 1. If the analog input voltage is less than (1/2) $\times$ AV_{REF0}, the MSB is cleared to 0.

<8> Next, bit 8 of the SAR register is automatically set to 1 and the next comparison starts. Depending on the previously determined value of bit 9, the voltage tap of the series resistor string is selected as follows.

- Bit 9 = 1: (3/4) $\times$ AV_{REF0}
- Bit 9 = 0: (1/4) $\times$ AV_{REF0}

The analog input voltage is compared with one of these voltage taps and bit 8 of the SAR register is manipulated as follows depending on the result of the comparison.

Analog input voltage $\geq$ voltage tap: Bit 8 = 1
Analog input voltage $\leq$ voltage tap: Bit 8 = 0

<9> The above steps are repeated until bit 0 of the SAR register has been manipulated.

<10> When comparison of all 10 bits of the SAR register has been completed, the valid digital value remains in the SAR register, and the value of the SAR register is transferred and latched to the ADCR register.
At the same time, an A/D conversion end interrupt request signal (INTAD) is generated.

<11> Repeat steps <4> to <10> until the ADCS bit is cleared to 0.
For another A/D conversion, start at <3>. However, when operating the A/D converter with the ADCS2 bit cleared to 0, start at <2>.

14.5.2 Trigger modes

The V850ES/KG2 has the following three trigger modes that set the A/D conversion start timing. These trigger modes are set by the ADS register.

- Software trigger mode
- External trigger mode (hardware trigger mode)
- Timer trigger mode (hardware trigger mode)

(1) Software trigger mode

This mode is used to start A/D conversion by setting the ADM.ADCS bit to 1 while the ADS.TRG bit is 0.

Conversion is repeatedly performed as long as the ADCS bit is not cleared to 0 after completion of A/D conversion.

If the ADM, ADS, PFM, or PFT register is written during conversion, A/D conversion is aborted and started again from the beginning.

(2) External trigger mode (hardware trigger mode)

This is the status in which the ADS.TRG bit is set to 1 and ADS.ADTMD bit is cleared to 0. This mode is used to start A/D conversion by detecting an external trigger (ADTRG) after the ADCS bit has been set to 1.

The A/D converter waits for the external trigger (ADTRG) after the ADCS bit is set to 1.

The valid edge of the signal input to the ADTRG pin is specified by using the ADS.EGA1 and ADS.EGA0 bits.

When the specified valid edge is detected, A/D conversion is started.

When A/D conversion is completed, the A/D converter waits for the external trigger (ADTRG) again.

If a valid edge is input to the ADTRG pin during A/D conversion, A/D conversion is aborted and started again from the beginning.

If the ADM, ADS, PFM, or PFT register is written during conversion, A/D conversion is aborted and the A/D converter waits for an external trigger (ADTRG).

(3) Timer trigger mode (hardware trigger mode)

This mode is used to start A/D conversion by detecting a timer trigger (INTTM010) after the ADCS bit has been set to 1 with the TGR bit = 1 and ADTMD bit = 1.

The A/D converter waits for the timer trigger (INTTM010) after the ADCS bit is set to 1.

When the INTTM010 signal is generated, A/D conversion is started.

When A/D conversion is completed, the A/D converter waits for the timer trigger (INTTM010) again.

If the INTTM010 signal is generated during A/D conversion, A/D conversion is aborted and started again from the beginning.

If the ADM, ADS, PFM, or PFT register is written during conversion, A/D conversion is aborted and the A/D converter waits for a timer trigger (INTTM010).

14.5.3 Operation modes

The following two operation modes are available. These operation modes are set by the ADM register.

- Select mode
- Scan mode

(1) Select mode

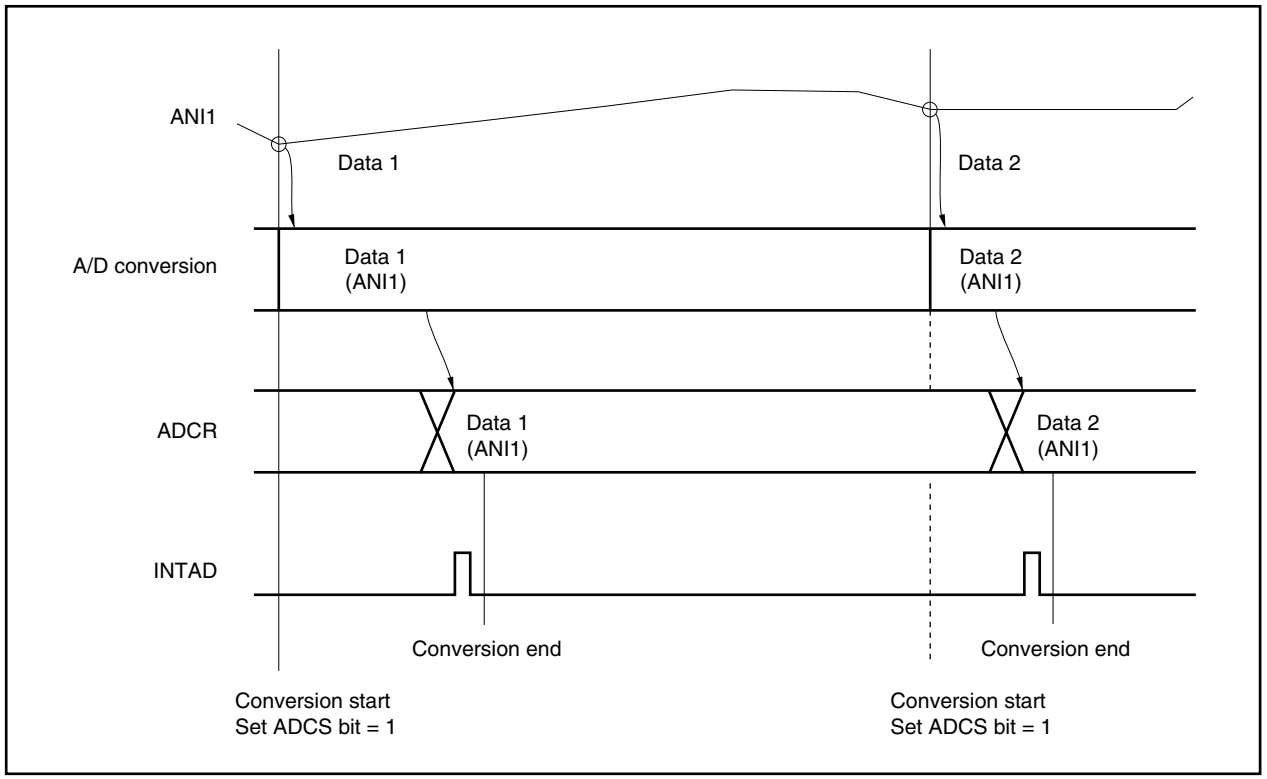
One input analog signal specified by the ADS register while the ADM.ADMD bit = 0 is converted. When conversion is complete, the result of conversion is stored in the ADCR register.

At the same time, the A/D conversion end interrupt request signal (INTAD) is generated. However, the INTAD signal may or may not be generated depending on setting of the PFM and PFT registers. For details, refer to **14.5.4 Power fail detection function**.

If anything is written to the ADM, ADS, PFM, and PFT registers during conversion, A/D conversion is aborted. In the software trigger mode, A/D conversion is started from the beginning again. In the hardware trigger mode, the A/D converter waits for a trigger.

If the trigger is detected during conversion in hardware trigger mode, A/D conversion is aborted and started again from the beginning.

Figure 14-4. Example of Select Mode Operation Timing (ADS.ADS2 to ADS.ADS0 Bits = 001B)



(2) Scan mode

In this mode, the analog signals specified by the ADS register and input from the ANI0 pin while the ADM.ADMD bit = 1 are sequentially selected and converted.

When conversion of one analog input signal is complete, the conversion result is stored in the ADCR register and, at the same time, the A/D conversion end interrupt request signal (INTAD) is generated.

The A/D conversion results of all the analog input signals are stored in the ADCR register. It is therefore recommended to save the contents of the ADCR register to RAM once A/D conversion of one analog input signal has been completed.

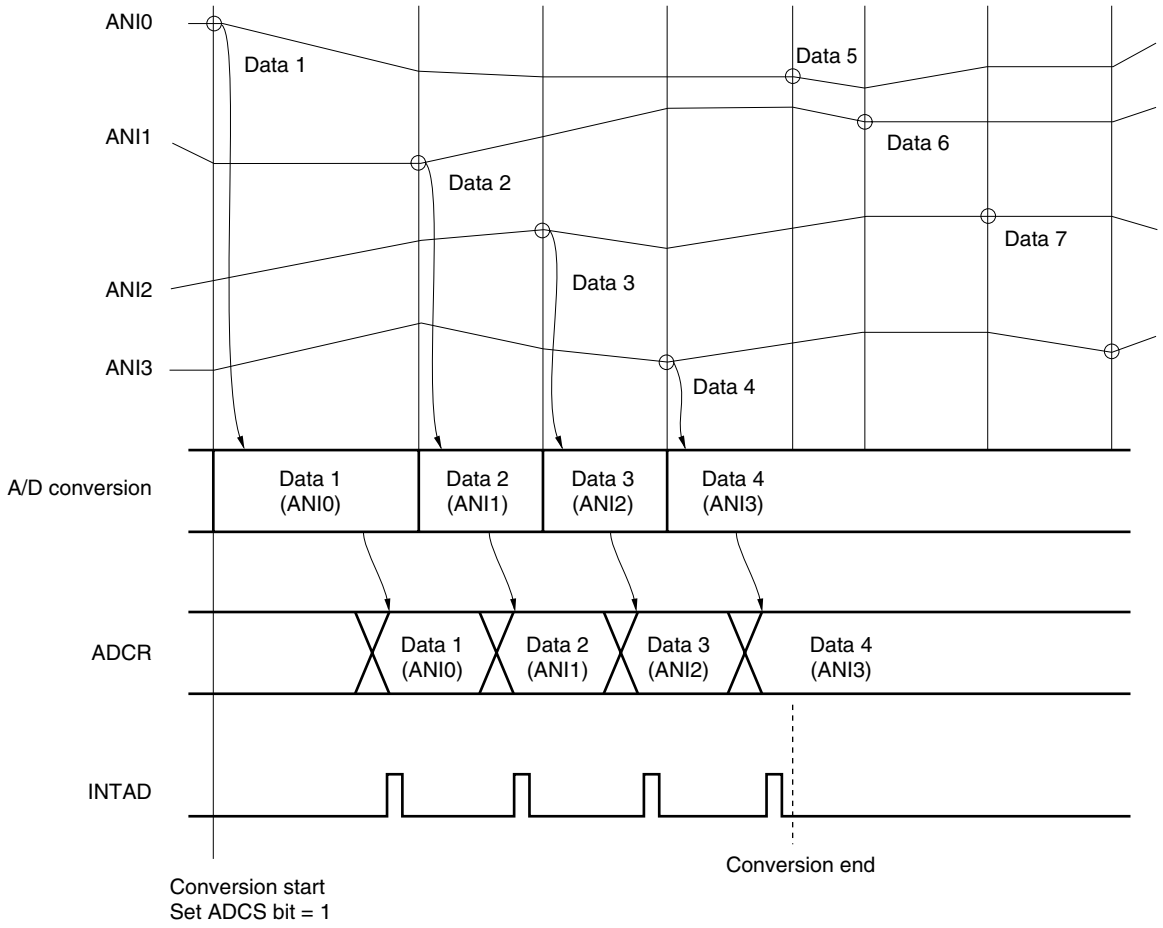
In the hardware trigger mode (ADS.TRG bit = 1), the A/D converter waits for a trigger after it has completed A/D conversion of the analog signals specified by the ADS register and input from the ANI0 pin.

If anything is written to the ADM, ADS, PFM, and PFT registers during conversion, A/D conversion is aborted. In the software trigger mode, A/D conversion is started from the beginning again. In the hardware trigger mode, the A/D converter waits for a trigger. Conversion starts again from the ANI0 pin.

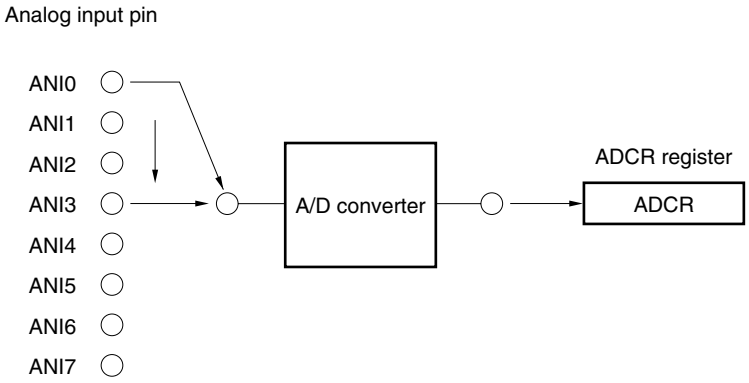
If the trigger is detected during conversion in hardware trigger mode, A/D conversion is aborted and started again from the beginning (ANI0 pin).

Figure 14-5. Example of Scan Mode Operation Timing (ADS.ADS2 to ADS.ADS0 Bits = 011B)

(a) Timing example



(b) Block diagram

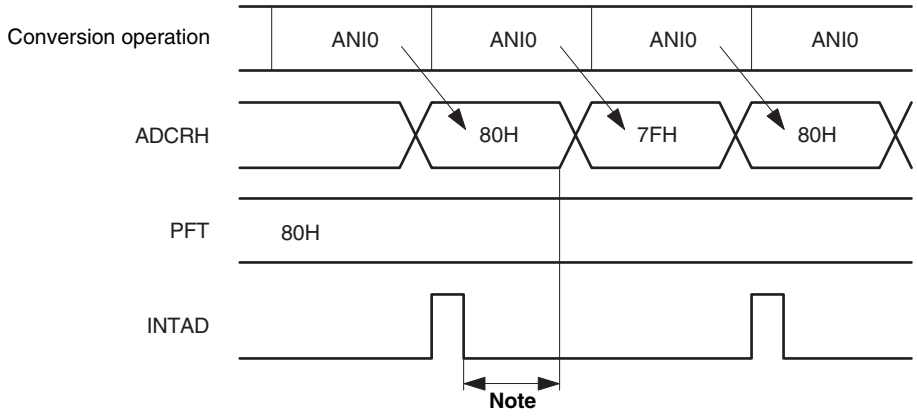


14.5.4 Power fail detection function

The conversion end interrupt request signal (INTAD) can be controlled as follows using the PFM and PFT registers.

- If the PFM.PFEN bit = 0, the INTAD signal is generated each time conversion ends.
- If the PFEN bit = 1 and the PFM.PFCM bit = 0, the conversion result (ADCRH register) and the value of the PFT register are compared when conversion ends, and the INTAD signal is generated only if ADCRH ≥ PFT.
- If the PFEN and PFCM bits = 1, the conversion result and the value of the PFT register are compared when conversion ends, and the INTAD signal is generated only if ADCRH < PFT.
- Because, when the PFEN bit = 1, the conversion result is overwritten after the INTAD signal has been generated, unless the conversion result is read by the time the next conversion ends, in some cases it may appear as if the actual operation differs from the operation described above (refer to **Figure 14-6**).

Figure 14-6. Power Fail Detection Function (PFCM Bit = 0)



Note If reading is not performed during this interval, the conversion result changes to the next conversion result.

14.5.5 Setting method

The following describes how to set registers.

(1) When using the A/D converter for A/D conversion

<1> Set (1) the ADM.ADCS2 bit.

<2> Select the channel and conversion time by setting the ADS.ADS2 to ADS.ADS0 bits and the ADM.ADHS1, ADM.ADHS0, and ADM.FR2 to ADM.FR0 bits.

<3> Set (1) the ADM.ADCS bit.

<4> Transfer the A/D conversion data to the ADCR register.

<5> An interrupt request signal (INTAD) is generated.

<Changing the channel>

<6> Change the channel by setting the ADS2 to ADS0 bits.

<7> Transfer the A/D conversion data to the ADCR register.

<8> The INTAD signal is generated.

<Ending A/D conversion>

<9> Clear (0) the ADCS bit.

<10> Clear (0) the ADCS2 bit.

Cautions 1. The time taken from <1> to <3> must be 1 μs (high-speed mode) or 14 μs (normal mode) or longer.

2. Steps <1> and <2> may be reversed.

3. Step <1> may be omitted. However, if omitted, do not use the first conversion result after <3>.

4. The time taken from <4> to <7> is different from the conversion time set by the ADHS1, ADHS0, and FR2 to FR0 bits.
The time taken for <6> and <7> is the conversion time set by the ADHS1, ADHS0, and FR2 to FR0 bits.

(2) When using the A/D converter for the power fail detection function

<1> Set (1) the PFM.PFEN bit.

<2> Set the power fail comparison conditions by using the PFM.PFCM bit.

<3> Set (1) the ADM.ADCS2 bit.

<4> Select the channel and conversion time by setting the ADS.ADS2 to ADS.ADS0 bits and the ADM.ADHS1, ADM.ADHS0, and ADM.FR2 to ADM.FR0 bits.

<5> Set the threshold value in the PFT register.

<6> Set (1) the ADM.ADCS bit.

<7> Transfer the A/D conversion data to the ADCR register.

<8> Compare the ADCRH register with the PFT register. An interrupt request signal (INTAD) is generated when the conditions match.

<Changing the channel>

<9> Change the channel by setting the ADS2 to ADS0 bits.

<10> Transfer the A/D conversion data to the ADCR register.

<11> The ADCRH register is compared with the PFT register. When the conditions match, an INTAD signal is generated.

<Ending A/D conversion>

<12> Clear (0) the ADCS bit.

<13> Clear (0) the ADCS2 bit.

Remark If the operation of the power fail detection function is enabled, all the A/D conversion results are compared, regardless of whether the select mode or scan mode is set.

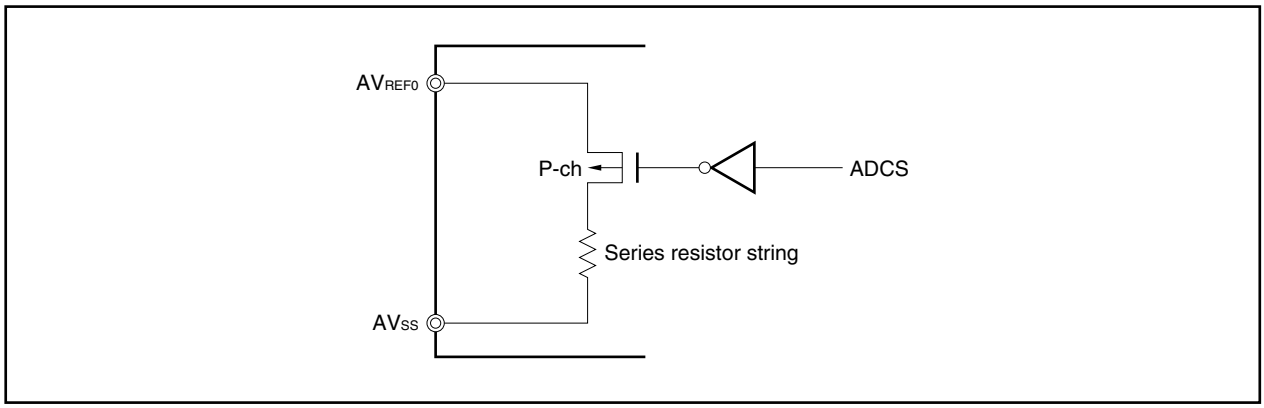
14.6 Cautions

(1) Power consumption in standby mode

The operation of the A/D converter stops in the standby mode. At this time, the power consumption can be reduced by stopping the conversion operation (the ADM.ADCS bit = 0).

Figure 14-7 shows an example of how to reduce the power consumption in the standby mode.

Figure 14-7. Example of How to Reduce Power Consumption in Standby Mode



(2) Input range of ANI0 to ANI7 pins

Use the A/D converter with the ANI0 to ANI7 pin input voltages within the specified range. If a voltage of AV_{REF0} or higher or AV_{SS} or lower (even if within the absolute maximum ratings) is input to these pins, the conversion value of the channel is undefined. Also, this may affect the conversion value of other channels.

(3) Conflicting operations

(a) Conflict between writing to the ADCR register and reading from ADCR register upon the end of conversion

Reading the ADCR register takes precedence. After the register has been read, a new conversion result is written to the ADCR register.

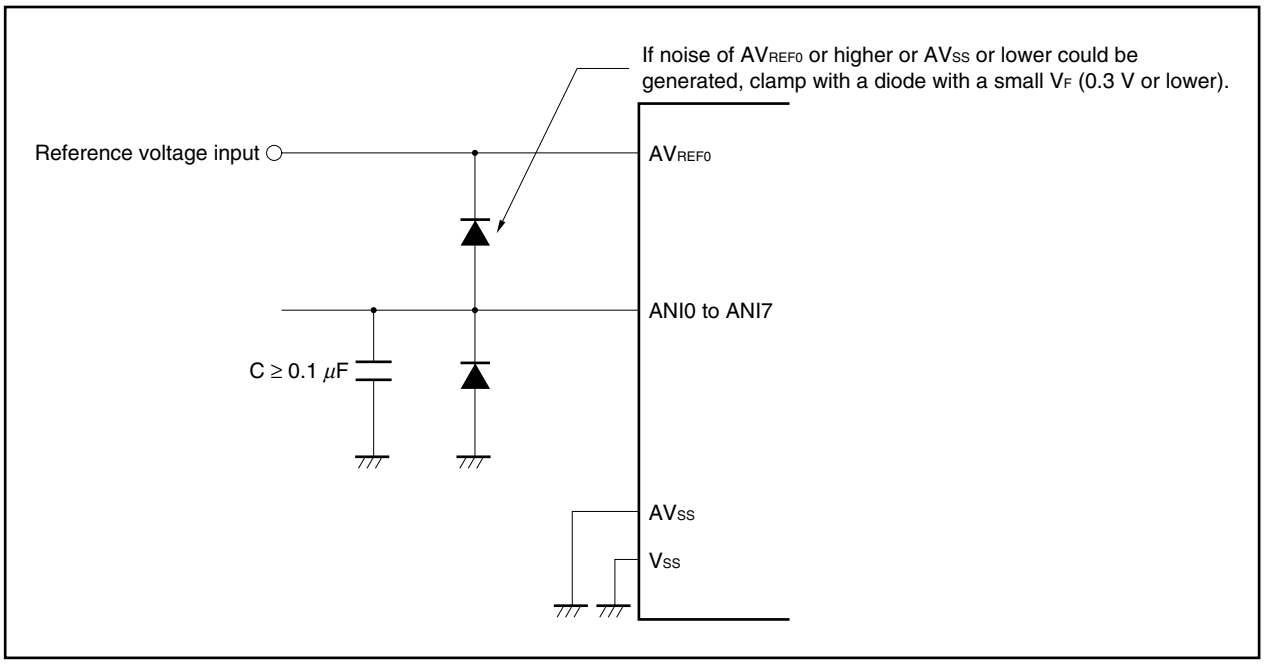
(b) Conflict between writing to the ADCR register and writing to the ADM register or writing to the ADS register upon the end of conversion

Writing to the ADM register or ADS register takes precedence. The ADCR register is not written, and neither is the conversion end interrupt request signal (INTAD) generated.

(4) Measures against noise

To keep a resolution of 10 bits, be aware of noise on the AV_{REF0} and ANI0 to ANI7 pins. The higher the output impedance of the analog input source, the greater the effect of noise. Therefore, it is recommended to connect external capacitors as shown in Figure 14-8 to reduce noise.

Figure 14-8. Handling of Analog Input Pins



(5) ANI0/P70 to ANI7/P77 pins

The analog input pins (ANI0 to ANI7) function alternately as input port pins (P70 to P77).

When performing A/D conversion by selecting any of the ANI0 to ANI7 pins, do not execute an input instruction to port 7 during conversion. This may decrease the conversion resolution.

If digital pulses are applied to the pin adjacent to the pin subject to A/D conversion, the value of the A/D conversion may differ from the expected value because of coupling noise. Therefore, do not apply pulses to the pin adjacent to the pin subject to A/D conversion.

(6) Input impedance of AV_{REF0} pin

A series resistor string of tens of kΩ is connected between the AV_{REF0} pin and AV_{SS} pin.

Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AV_{REF0} pin and AV_{SS} pin, resulting in a large reference voltage error.

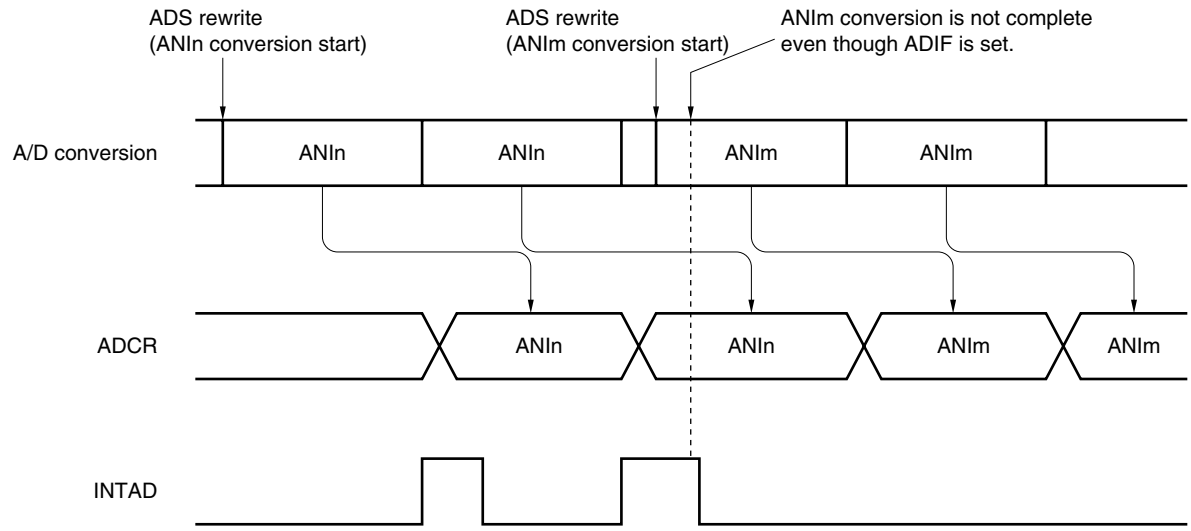
(7) Interrupt request flag (ADIC.ADIF bit)

Even when the ADS register is changed, the ADIF bit is not cleared (0).

Therefore, if the analog input pin is changed during A/D conversion, the ADIF bit may be set (1) because A/D conversion of the previous analog input pin ends immediately before the ADS register is rewritten. In a such case, note that if the ADIF bit is read immediately after the ADS register has been rewritten, the ADIF bit is set (1) even though A/D conversion of the analog input pin after the change has not been completed.

When stopping A/D conversion once and resuming it, clear the ADIF bit (0) before resuming A/D conversion.

Figure 14-9. A/D Conversion End Interrupt Request Occurrence Timing



Remark n = 0 to 7
m = 0 to 7

(8) Conversion results immediately after A/D conversion start

If the ADM.ADCS bit is set to 1 within 1 μs (high-speed mode) or 14 μs (normal mode) after the ADM.ADCS2 bit has been set to 1, or if the ADCS bit is set to 1 with the ADCS2 bit cleared to 0, the converted value immediately after the A/D conversion operation has started may not satisfy the rating. Take appropriate measures such as polling the A/D conversion end interrupt request signal (INTAD) and discarding the first conversion result.

(9) Reading A/D conversion result register (ADCR)

When the ADM or ADS register has been written, the contents of the ADCR register may become undefined. When the conversion operation is complete, read the conversion results before writing to the ADM or ADS register. A correct conversion result may not be able to be read at a timing other than the above.

Accessing the ADCR and ADCRH registers is prohibited when the CPU operates with the subclock and the main clock oscillation (fx) is stopped. For details, refer to **3.4.8 (1) (b) Access to special on-chip peripheral I/O register**.

(10) A/D converter sampling time and A/D conversion start delay time

The A/D converter sampling time differs depending on the set value of the ADM register. A delay time exists until actual sampling is started after A/D converter operation is enabled.

When using a set in which the A/D conversion time must be strictly observed, care is required for the contents shown in Figure 14-10 and Table 14-4.

Figure 14-10. Timing of A/D Converter Sampling and A/D Conversion Start Delay

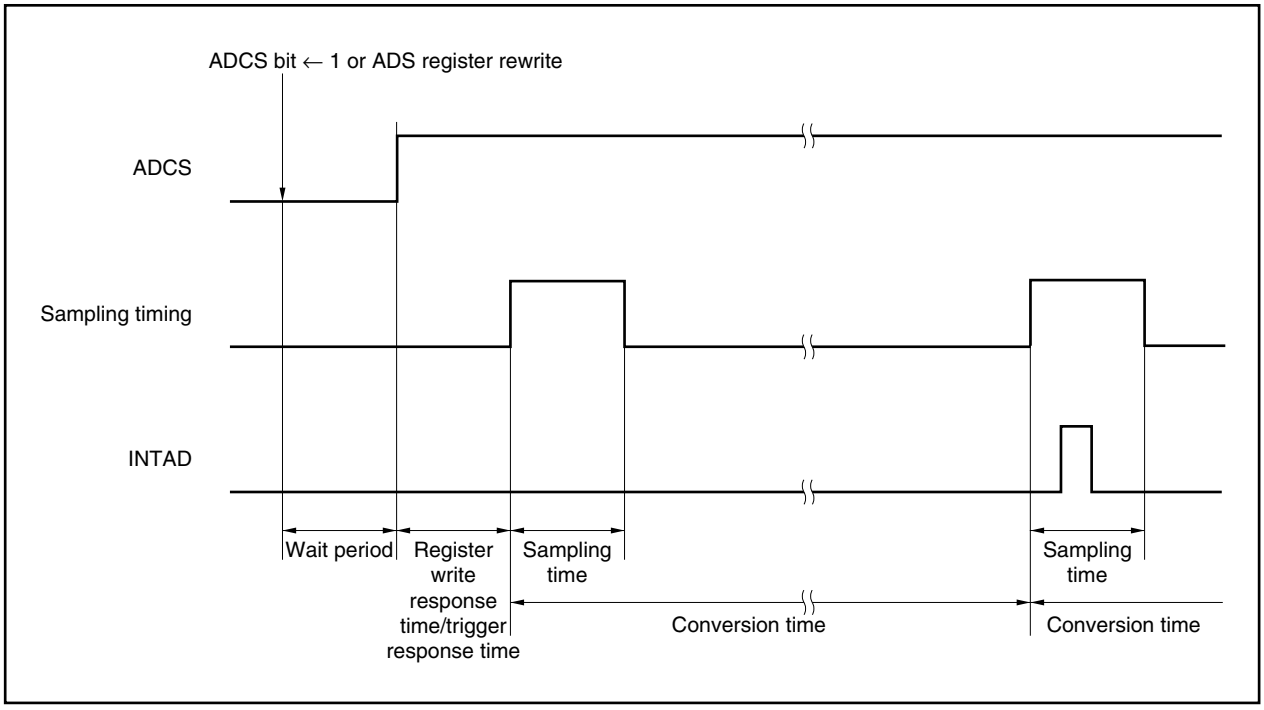


Table 14-4. A/D Converter Conversion Time

ADHS1	ADHS0	FR2	FR1	FR0	Conversion Time	Sampling Time	Register Write Response Time[Note]		Trigger Response Time[Note]	
							MIN.	MAX.	MIN.	MAX.
0	0	0	0	0	288/fxx	176/fxx	11/fxx	12/fxx	7/fxx	8/fxx
0	0	0	0	1	240/fxx	176/fxx	11/fxx	12/fxx	7/fxx	8/fxx
0	0	0	1	0	192/fxx	132/fxx	10/fxx	11/fxx	6/fxx	7/fxx
0	0	1	0	0	144/fxx	88/fxx	9/fxx	10/fxx	5/fxx	6/fxx
0	0	1	0	1	120/fxx	88/fxx	9/fxx	10/fxx	5/fxx	6/fxx
0	0	1	1	0	96/fxx	48/fxx	11/fxx	12/fxx	7/fxx	8/fxx
0	1	0	0	0	96/fxx	48/fxx	11/fxx	12/fxx	7/fxx	8/fxx
0	1	0	0	1	72/fxx	36/fxx	10/fxx	11/fxx	6/fxx	7/fxx
0	1	0	1	0	48/fxx	24/fxx	9/fxx	10/fxx	5/fxx	6/fxx
0	1	0	1	1	24/fxx	12/fxx	8/fxx	9/fxx	4/fxx	5/fxx
0	1	1	0	0	224/fxx	176/fxx	11/fxx	12/fxx	7/fxx	8/fxx
0	1	1	0	1	168/fxx	132/fxx	10/fxx	11/fxx	6/fxx	7/fxx
0	1	1	1	0	112/fxx	88/fxx	9/fxx	10/fxx	5/fxx	6/fxx
0	1	1	1	1	56/fxx	44/fxx	8/fxx	9/fxx	4/fxx	5/fxx
1	0	0	0	0	72/fxx	24/fxx	11/fxx	12/fxx	7/fxx	8/fxx
1	0	0	0	1	54/fxx	18/fxx	10/fxx	11/fxx	6/fxx	7/fxx
1	0	0	1	0	36/fxx	12/fxx	9/fxx	10/fxx	5/fxx	6/fxx
1	0	0	1	1	18/fxx	6/fxx	8/fxx	9/fxx	4/fxx	5/fxx
Other than above					Setting prohibited	–	–	–	–	–

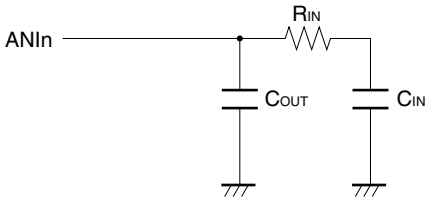
Note Each response time is the time after the wait period. For the wait function, refer to **3.4.8 (1) (b) Access to special on-chip peripheral I/O register**.

Remark fxx: Main clock frequency

(11) Internal equivalent circuit

The following shows the equivalent circuit of the analog input block.

Figure 14-11. Internal Equivalent Circuit of ANIn Pin



AV_{REF0}	R_{IN}	C_{OUT}	C_{IN}
4.5 V	3 kΩ	8 pF	15 pF
2.7 V	60 kΩ	8 pF	15 pF

Remarks 1. The above values are reference values.

2. n = 0 to 7

(12) Variation of A/D conversion results

The results of the A/D conversion may vary depending on the fluctuation of the supply voltage, or may be affected by noise. To reduce the variation, take counteractive measures with the program such as averaging the A/D conversion results.

(13) A/D conversion result hysteresis characteristics

The successive approximation type A/D converter holds the analog input voltage in the internal sample & hold capacitor and then performs A/D conversion. After the A/D conversion has finished, the analog input voltage remains in the internal sample & hold capacitor. As a result, the following phenomena may occur.

- When the same channel is used for A/D conversions, if the voltage is higher or lower than the previous A/D conversion, then hysteresis characteristics may appear where the conversion result is affected by the previous value. Thus, even if the conversion is performed at the same potential, the result may vary.
- When switching the analog input channel, hysteresis characteristics may appear where the conversion result is affected by the previous channel value. This is because one A/D converter is used for the A/D conversions. Thus, even if the conversion is performed at the same potential, the result may vary.

Therefore, to obtain more accurate conversion result, perform A/D conversion twice successively for the same channel, and discard the first conversion result.

14.7 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1 LSB (Least Significant Bit). The percentage of 1 LSB with respect to the full scale is expressed by %FSR (Full Scale Range). %FSR indicates the ratio of analog input voltage that can be converted as a percentage, and is always represented by the following formula regardless of the resolution.

1 %FSR = (Max. value of analog input voltage that can be converted − Min. value of analog input voltage that can be converted)/100
= (AV_{REF0} – 0)/100
= AV_{REF0}/100

1 LSB is as follows when the resolution is 10 bits.

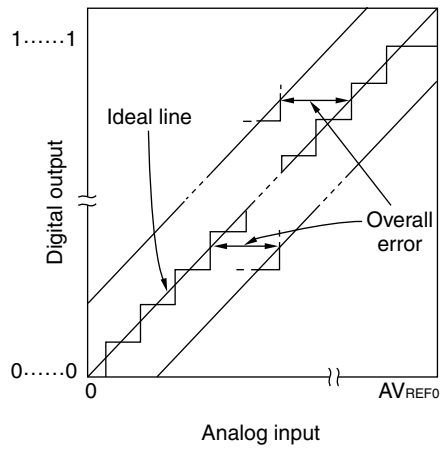
1 LSB = $1/2^{10}$ = 1/1024
= 0.098 %FSR

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, linearity error and errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

Figure 14-12. Overall Error

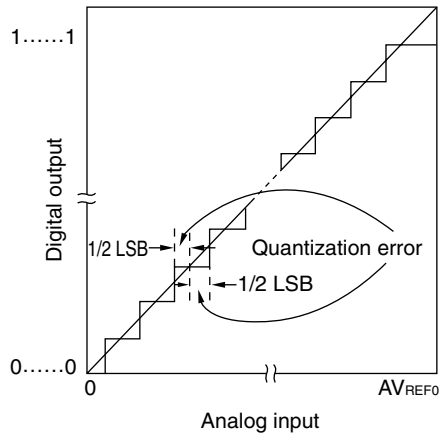


(3) Quantization error

When analog values are converted to digital values, a ±1/2 LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2 LSB is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

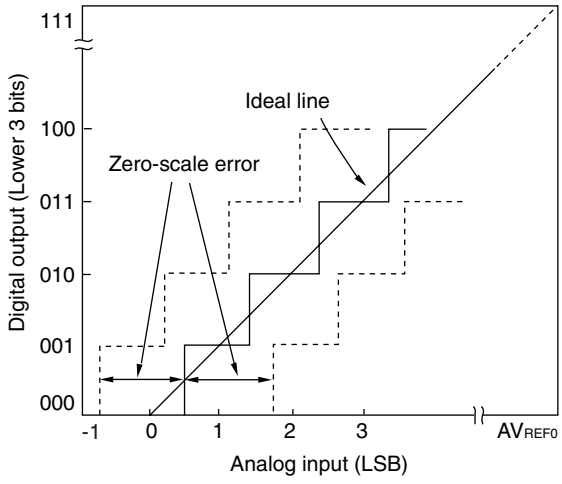
Figure 14-13. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2 LSB) when the digital output changes from 0……000 to 0……001.

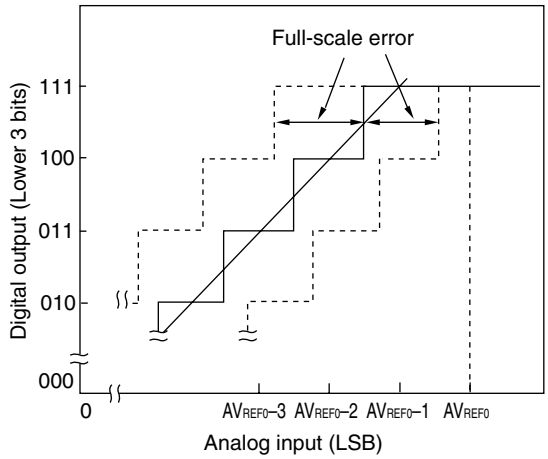
Figure 14-14. Zero-Scale Error



(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (full scale – 3/2 LSB) when the digital output changes from 1……110 to 1……111.

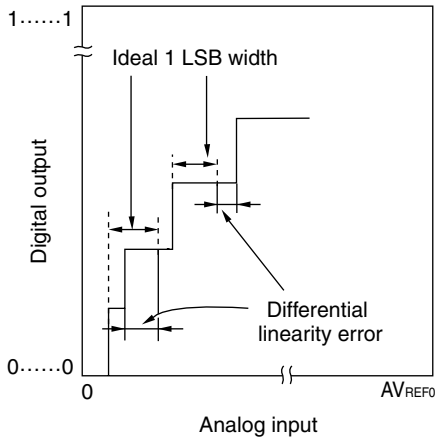
Figure 14-15. Full-Scale Error



(6) Differential linearity error

While the ideal width of code output is 1 LSB, this indicates the difference between the actual measurement value and the ideal value. This indicates the basic characteristics of the A/D conversion when the voltage applied to the analog input pins of the same channel is consistently increased bit by bit from AV_{SS} to AV_{REF0}. When the input voltage is increased or decreased, or when two or more channels are used, refer to **14.7 (2) Overall error**.

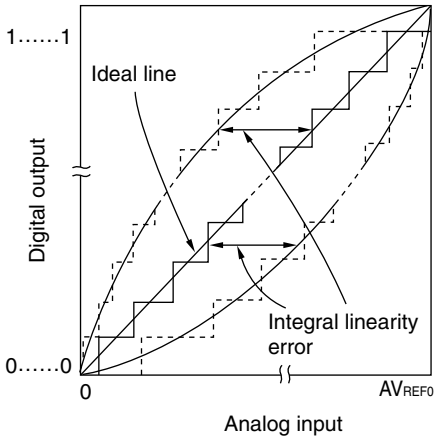
Figure 14-16. Differential Linearity Error



(7) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

Figure 14-17. Integral Linearity Error



(8) Conversion time

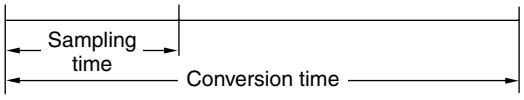
This expresses the time from when the analog input voltage was applied to the time when the digital output was obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.

Figure 14-18. Sampling Time



CHAPTER 15 D/A CONVERTER

15.1 Functions

In the V850ES/KG2, two channels of D/A converter (DAC0, DAC1) are provided.
The D/A converter has the following functions.

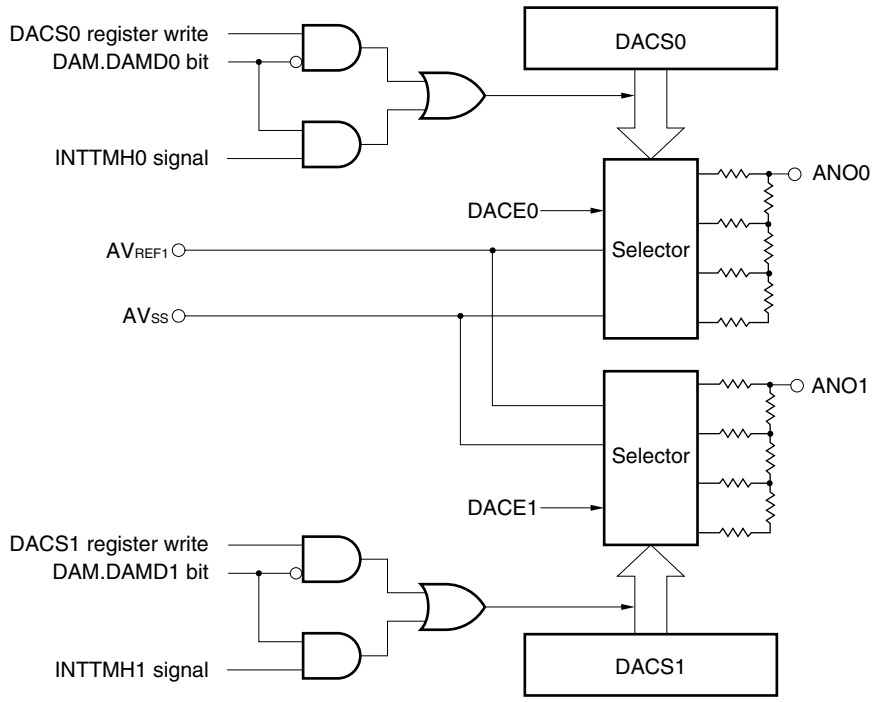
- 8-bit resolution × 2 channels
- R-2R ladder string method
- Conversion time: 20 μs (MAX.) (AV_{REF1} = 2.7 to 5.5 V)
- Analog output voltage: AV_{REF1} × m/256 (m = 0 to 255; value set to DACSn register)
- Operation modes: Normal mode, real-time output mode

Remark n = 0, 1

15.2 Configuration

The D/A converter configuration is shown below.

Figure 15-1. Block Diagram of D/A Converter



Caution DAC0 and DAC1 share the AV_{REF1} and AV_{SS} pins. The AV_{SS} pin is also shared by the A/D converter.

The D/A converter includes the following hardware.

Table 15-1. Configuration of D/A Converter

Item	Configuration
Control register	D/A converter mode register (DAM) D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

15.3 Registers

The registers that control the D/A converter are as follows.

- D/A converter mode register (DAM)
- D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

(1) D/A converter mode register (DAM)

This register controls the operation of the D/A converter.

The DAM register can be read or written in 8-bit or 1-bit units.

Reset sets DAM to 00H.

After reset: 00H R/W Address: FFFFF284H

	7	6	5	4	3	<2>	1	<0>
DAM	0	0	0	0	DAMD1	DACE1	DAMD0	DACE0

DAMDn	Selection of D/A converter operation mode (n = 0, 1)
0	Normal mode
1	Real-time output mode[Note]

DACEn	D/A converter operation enable/disable control (n = 0, 1)
0	Disable operation
1	Enable operation

Note The output trigger in the real-time output mode (DAMDn bit = 1) is as follows.

- When n = 0: INTTMH0 signal (Refer to **CHAPTER 10 8-BIT TIMER H**)
- When n = 1: INTTMH1 signal (Refer to **CHAPTER 10 8-BIT TIMER H**)

(2) D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

These registers set the analog voltage value output to the ANO0 and ANO1 pins.

These registers can be read or written in 8-bit units.

Reset sets DACS0 and DACS1 to 00H.

After reset: 00H R/W Address: DACS0 FFFFF280H, DACS1 FFFFF282H

	7	6	5	4	3	2	1	0
DACSn	DAn7	DAn6	DAn5	DAn4	DAn3	DAn2	DAn1	DAn0

(n = 0, 1)

Caution In the real-time output mode (DAM.DAMDn bit = 1), set the DACS0 and DACS1 registers before the INTTMH0 and INTTMH1 signals are generated. D/A conversion starts when the INTTMH0 and INTTMH1 signals are generated.

15.4 Operation

15.4.1 Operation in normal mode

D/A conversion is performed using a write operation to the DACSn register as the trigger.

The setting method is described below.

<1> Clear the DAM.DAMDn bit to 0 (normal mode).

<2> Set the analog voltage value to be output to the ANOn pin to the DACSn register.

Steps <1> and <2> above constitute the initial settings.

<3> Set the DAM.DACEn bit to 1 (D/A conversion enable).

D/A converted analog voltage value is output from the ANOn pin when this setting is performed.

<4> To change the analog voltage value, write to the DACSn register.

The analog voltage value immediately before set is held until the next write operation is performed.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. n = 0, 1

15.4.2 Operation in real-time output mode

D/A conversion is performed using the interrupt request signals (INTTMH0, INTTMH1) of 8-bit timers H0 and H1 as the trigger.

The setting method is described below.

<1> Set the DAM.DAMDn bit to 1 (real-time output mode).

<2> Set the analog voltage value to be output to the ANOn pin to the DACSn register.

<3> Set the DAM.DACEn bit to 1 (D/A conversion enable).

Steps <1> to <3> above constitute the initial settings.

<4> Operate 8-bit timers H0 and H1.

<5> D/A converted analog voltage value is output from the ANOn pin when the INTTMH0 and INTTMH1 signals are generated.

Set the next output analog voltage value to the DACSn register, before the next INTTMH0 and INTTMH1 signals are generated.

<6> After that, the value set in the DACSn register is output from the ANOn pin every time the INTTMH0 are INTTMH1 signals are generated.

Remarks 1. The output values of the ANO0 and ANO1 pins up to <5> above are undefined.

2. For the output values of the ANO0 and ANO1 pins in the IDLE, HALT, and STOP modes, refer to **CHAPTER 23 STANDBY FUNCTION**.

3. n = 0, 1

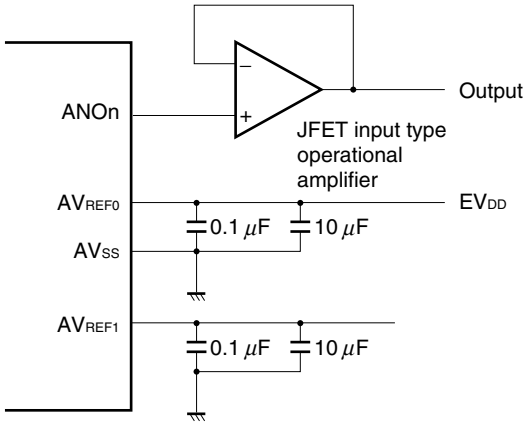
15.4.3 Cautions

Observe the following cautions when using the D/A converter.

- When using the D/A converter, set the port pins to the input mode (PM10, PM11 bits = 11)
- When using the D/A converter, reading of the port is prohibited.
- When using the D/A converter, use both P10 and P11 as D/A outputs.
  Using one of the port 1 for D/A output and the other as a port is prohibited.
- In the real-time output mode, do not change the set value of the DACSn register while the trigger signal is output.
- Make sure that $AV_{REF1} \leq V_{DD}$ and AV_{REF1} = 2.7 to 5.5 V. The operation is not guaranteed if ranges other than the above are used.
- Because the output impedance of the D/A converter is high, a current cannot be supplied from the ANOn pin. When connecting a resistor of 2 MΩ or lower, take appropriate measures such as inserting a JFET input type operational amplifier between the resistor and the ANOn pin.

Remark n = 0, 1

Figure 15-2. Example of External Pin Connection



Caution The figure shown here is only reference. Use it after fully evaluating.

16.3 Configuration

Table 16-1. Configuration of UARTn

Item	Configuration
Registers	Receive buffer register n (RXBn) Transmit buffer register n (TXBn) Receive shift register Transmit shift register Asynchronous serial interface mode register n (ASIMM) Asynchronous serial interface status register n (ASISn) Asynchronous serial interface transmit status register n (ASIFn)
Other	Reception control parity check Addition of transmission control parity

Remark n = 0 to 2

Figure 16-2 shows the configuration of UARTn.

(1) Asynchronous serial interface mode register n (ASIMn)

The ASIMn register is an 8-bit register for specifying the operation of UARTn.

(2) Asynchronous serial interface status register n (ASISn)

The ASISn register consists of a set of flags that indicate the error contents when a reception error occurs. The various reception error flags are set (1) when a reception error occurs and are cleared (0) when the ASISn register is read.

(3) Asynchronous serial interface transmit status register n (ASIFn)

The ASIFn register is an 8-bit register that indicates the status when a transmit operation is performed.

This register consists of a transmit buffer data flag, which indicates the hold status of the TXBn register data, and the transmit shift register data flag, which indicates whether transmission is in progress.

(4) Reception control parity check

The receive operation is controlled according to the contents set in the ASIMn register. A check for parity errors is also performed during a receive operation, and if an error is detected, a value corresponding to the error contents is set in the ASISn register.

(5) Receive shift register

This is a shift register that converts the serial data that was input to the RXDn pin to parallel data. One byte of data is received, and if a stop bit is detected, the receive data is transferred to the RXBn register.

This register cannot be directly manipulated.

(6) Receive buffer register n (RXBn)

The RXBn register is an 8-bit buffer register for holding receive data. When 7 characters are received, 0 is stored in the MSB.

During a reception enabled state, receive data is transferred from the receive shift register to the RXBn register, synchronized with the end of the shift-in processing of one frame.

Also, the reception completion interrupt request signal (INTSRn) is generated by the transfer of data to the RXBn register.

CHAPTER 16 ASYNCHRONOUS SERIAL INTERFACE (UART)

In the V850ES/KG2, three channels of asynchronous serial interface (UART) are provided.

16.1 Selecting UART2 or CSI00 Mode

UART2 and CSI00 of the V850ES/KG2 share pins, and therefore these interfaces cannot be used at the same time. Select UART2 or CSI00 in advance by using the PMC4 and PFC4 registers (refer to **4.3.4 Port 4**).

Caution UART2 or CSI00 transmission/reception operations are not guaranteed if the mode is changed during transmission or reception. Be sure to disable the operation of the unit that is not used.

Figure 16-1. Selecting Mode of UART2 or CSI00

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	0	0	PMC42	PMC41	PMC40

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	0	0	0	0	0	0	PFC41	PFC40

PFC4n	PMC4n	Operation mode
0	0	Port I/O mode
0	1	CSI00 mode
1	0	Port I/O mode
1	1	UART2 mode

Remark n = 0, 1

16.2 Features

- Maximum transfer speed: 312.5 kbps
- Full-duplex communications
  On-chip RXBn register
  On-chip TXBn register
- Two-pin configuration[Note]
  TXDn: Transmit data output pin
  RXDn: Receive data input pin
- Reception error detection functions
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 3 types
  - Reception error interrupt request signal (INTSREn): Interrupt is generated according to the logical OR of the three types of reception errors
  - Reception completion interrupt request signal (INTSRn): Interrupt is generated when receive data is transferred from the receive shift register to the RXBn register after serial transfer is completed during a reception enabled state
  - Transmission completion interrupt request signal (INTSTn): Interrupt is generated when the serial transmission of transmit data (8 or 7 bits) from the transmit shift register is completed
- Character length: 7 or 8 bits
- Parity functions: Odd, even, 0, or none
- Transmission stop bits: 1 or 2 bits
- On-chip dedicated baud rate generator

Note The ASCK0 pin (external clock input) is available only for UART0.

(7) Transmit shift register

This is a shift register that converts the parallel data that was transferred from the TXBn register to serial data. When one byte of data is transferred from the TXBn register, the shift register data is output from the TXDn pin.

The transmission completion interrupt request signal (INTSTn) is generated synchronized with the completion of transmission of one frame.

This register cannot be directly manipulated.

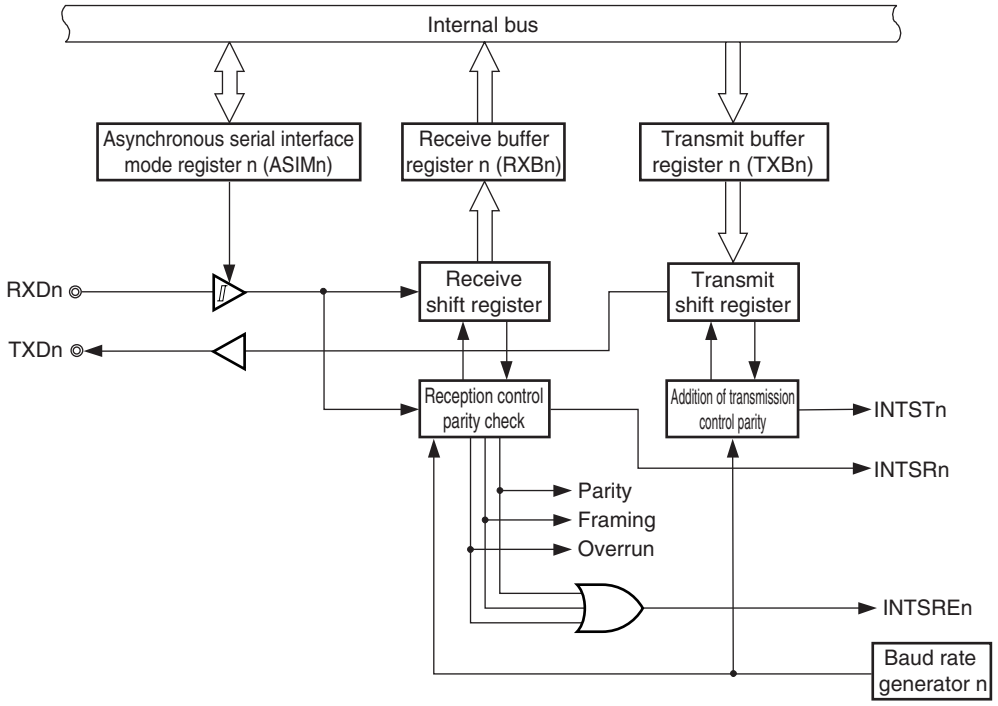
(8) Transmit buffer register n (TXBn)

The TXBn register is an 8-bit buffer for transmit data. A transmit operation is started by writing transmit data to the TXBn register.

(9) Addition of transmission control parity

A transmit operation is controlled by adding a start bit, parity bit, or stop bit to the data that is written to the TXBn register, according to the contents that were set in the ASIMn register.

Figure 16-2. Block Diagram of UARTn



Remark For the configuration of the baud rate generator, refer to **Figure 16-13**.

16.4 Registers

(1) Asynchronous serial interface mode register n (ASIMn)

The ASIMn register is an 8-bit register that controls the UARTn transfer operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 01H.

Cautions 1. When using UARTn, be sure to set the external pins related to UARTn functions to the control made before setting the CKSRn and BRGCn registers, and then set the UARTEn bit to 1. Then set the other bits.

2. Set the UARTEn and RXEn bits to 1 while a high level is input to the RXDn pin. If these bits are set to 1 while a low level is input to the RXDn pin, reception will be started.

(1/2)

After reset: 01H R/W Address: ASIM0 FFFFFA00H, ASIM1 FFFFFA10H, ASIM2 FFFFFA20H

	<7>	<6>	<5>	4	3	2	1	0
ASIMn	UARTEn	TXEn	RXEn	PSn1	PSn0	CLn	SLn	ISRMn

(n = 0 to 2)

UARTEn	Control of operating clock
0	Stop clock supply to UARTn.
1	Supply clock to UARTn.

- If the UARTEn bit is cleared to 0, UARTn is asynchronously reset[Note].
- If the UARTEn bit = 0, UARTn is reset. To operate UARTn, first set the UARTEn bit to 1.
- If the UARTEn bit is cleared from 1 to 0, all the registers of UARTn are initialized. To set the UARTEn bit to 1 again, be sure to re-set the registers of UARTn.

The output of the TXDn pin goes high when transmission is disabled, regardless of the setting of the UARTEn bit.

TXEn	Transmission enable/disable
0	Disable transmission
1	Enable transmission

- Set the TXEn bit to 1 after setting the UARTEn bit to 1 at startup. Clear the UARTEn bit to 0 after clearing the TXEn bit to 0 to stop.
- To initialize the transmission unit, clear (0) the TXEn bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the TXEn bit again. If the TXEn bit is not set again, initialization may not be successful. (For details about the base clock, refer to **16.7.1 (1) Base clock**.)

Note The ASISn, ASIFn, and RXBn registers are reset.

(2/2)

RXEn	Reception enable/disable
0	Disable reception[Note]
1	Enable reception

- Set the RXEn bit to 1 after setting the UARTEn bit to 1 at startup. Clear the UARTEn bit to 0 after clearing the RXEn bit to 0 to stop.
- To initialize the reception unit status, clear (0) the RXEn bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the RXEn bit again. If the RXEn bit is not set again, initialization may not be successful. (For details about the base clock, refer to **16.7.1 (1) Base clock**.)

PSn1	PSn0	Transmit operation	Receive operation
0	0	Don't output parity bit	Receive with no parity
0	1	Output 0 parity	Receive as 0 parity
1	0	Output odd parity	Judge as odd parity
1	1	Output even parity	Judge as even parity

- To overwrite the PSn1 and PSn0 bits, first clear (0) the TXEn and RXEn bits.
- If "0 parity" is selected for reception, no parity judgment is performed. Therefore, no error interrupt is generated because the ASISn.PEn bit is not set.

CLn	Specification of character length of 1 frame of transmit/receive data
0	7 bits
1	8 bits

- To overwrite the CLn bit, first clear (0) the TXEn and RXEn bits.

SLn	Specification of stop bit length of transmit data
0	1 bit
1	2 bits

- To overwrite the SLn bit, first clear (0) the TXEn bit.
- Since reception is always done with a stop bit length of 1, the SLn bit setting does not affect receive operations.

ISRMn	Enable/disable of generation of reception completion interrupt request signals when an error occurs
0	Generate a reception error interrupt request signal (INTSREn) as an interrupt when an error occurs. In this case, no reception completion interrupt request signal (INTSRn) is generated.
1	Generate a reception completion interrupt request signal (INTSRn) as an interrupt when an error occurs. In this case, no reception error interrupt request signal (INTSREn) is generated.

- To overwrite the ISRMn bit, first clear (0) the RXEn bit.

Note When reception is disabled, the receive shift register does not detect a start bit. No shift-in processing or transfer processing to the RXBn register is performed, and the contents of the RXBn register are retained.

When reception is enabled, the receive shift operation starts, synchronized with the detection of the start bit, and when the reception of one frame is completed, the contents of the receive shift register are transferred to the RXBn register. A reception completion interrupt request signal (INTSRn) is also generated in synchronization with the transfer to the RXBn register.

(2) Asynchronous serial interface status register n (ASISn)

The ASISn register, which consists of 3 error flag bits (PEn, FEn and OVEn), indicates the error status when UARTn reception is complete.

The ASISn register is cleared to 00H by a read operation. When a reception error occurs, the RXBn register should be read and the error flag should be cleared after the ASISn register is read.

This register is read-only in 8-bit units.

Reset sets this register to 00H.

Cautions 1. When the ASIMn.UARTEn bit or ASIMn.RXEn bit is cleared to 0, or when the ASISn register is read, the PEn, FEn, and OVEn bits are cleared (0).

2. Operation using a bit manipulation instruction is prohibited.

3. When the main clock is stopped and the CPU is operating on the subclock, do not access the ASISn register.
For details, refer to 3.4.8 (1) (b).

After reset: 00H R Address: ASIS0 FFFFFA03H, ASIS1 FFFFFA13H, ASIS2 FFFFFA23H

	7	6	5	4	3	2	1	0
ASISn	0	0	0	0	0	PEn	FEn	OVEn

(n = 0 to 2)

PEn	Status flag indicating a parity error
0	When the UARTEn or RXEn bit is cleared to 0, or after the ASISn register has been read
1	When reception was completed, the receive data parity did not match the parity bit
• The operation of the PEn bit differs according to the settings of the ASIMn.PSn1 and ASIMn.PSn0 bits.	

FEn	Status flag indicating framing error
0	When the UARTEn or RXEn bit is cleared to 0, or after the ASISn register has been read
1	When reception was completed, no stop bit was detected
• For receive data stop bits, only the first bit is checked regardless of the stop bit length.	

OVEn	Status flag indicating an overrun error
0	When the UARTEn or RXEn bit is cleared to 0, or after the ASISn register has been read.
1	UARTn completed the next receive operation before reading receive data of the RXBn register.
• When an overrun error occurs, the next receive data value is not written to the RXBn register and the data is discarded.	

(3) Asynchronous serial interface transmit status register n (ASIFn)

The ASIFn register, which consists of 2 status flag bits, indicates the status during transmission.

By writing the next data to the TXBn register after data is transferred from the TXBn register to the transmit shift register, transmit operations can be performed continuously without suspension even during an interrupt interval. When transmission is performed continuously, data should be written after referencing the TXBFn bit to prevent writing to the TXBn register by mistake.

This register is read-only in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R Address: ASIF0 FFFFFA05H, ASIF1 FFFFFA15H, ASIF2 FFFFFA25H

	7	6	5	4	3	2	<1>	<0>
ASIFn	0	0	0	0	0	0	TXBFn	TXSFn

(n = 0 to 2)

TXBFn	Transmission buffer data flag
0	Data to be transferred next to TXBn register does not exist (When the ASIMn.UARTEn or ASIMn.TXEn bit is cleared to 0, or when data has been transferred to the transmission shift register)
1	Data to be transferred next exists in TXBn register (Data exists in TXBn register when the TXBn register has been written to)
• When transmission is performed continuously, data should be written to the TXBn register after confirming that this flag is 0. If writing to TXBn register is performed when this flag is 1, transmit data cannot be guaranteed.	

TXSFn	Transmit shift register data flag (indicates the transmission status of UARTn)
0	Initial status or a waiting transmission (When the UARTEn or TXEn bit is cleared to 0, or when following transmission completion, the next data transfer from the TXBn register is not performed)
1	Transmission in progress (When data has been transferred from the TXBn register)
• When the transmission unit is initialized, initialization should be executed after confirming that this flag is 0 following the occurrence of a transmission completion interrupt request signal (INTSTn). If initialization is performed when this flag is 1, transmit data cannot be guaranteed.	

(4) Receive buffer register n (RXBn)

The RXBn register is an 8-bit buffer register for storing parallel data that had been converted by the receive shift register.

When reception is enabled (ASIMn.RXEn bit = 1), receive data is transferred from the receive shift register to the RXBn register, synchronized with the completion of the shift-in processing of one frame. Also, a reception completion interrupt request signal (INTSRn) is generated by the transfer to the RXBn register. For information about the timing for generating this interrupt request, refer to **16.6.4 Receive operation**.

If reception is disabled (ASIMn.RXEn bit = 0), the contents of the RXBn register are retained, and no processing is performed for transferring data to the RXBn register even when the shift-in processing of one frame is completed. Also, the INTSRn signal is not generated.

When 7 bits is specified for the data length, bits 6 to 0 of the RXBn register are transferred for the receive data and the MSB (bit 7) is always 0. However, if an overrun error (ASISn.OVEn bit = 1) occurs, the receive data at that time is not transferred to the RXBn register.

The RXBn register becomes FFH when a reset is input or ASIMn.UARTEn bit = 0.

This register is read-only in 8-bit units.

After reset: FFH R Address: RXB0 FFFFFA02H, RXB1 FFFFFA12H, RXB2 FFFFFA22H

	7	6	5	4	3	2	1	0
RXBn	RXBn7	RXBn6	RXBn5	RXBn4	RXBn3	RXBn2	RXBn1	RXBn0

(n = 0 to 2)

(5) Transmit buffer register n (TXBn)

The TXBn register is an 8-bit buffer register for setting transmit data.

When transmission is enabled (ASIMn.TXEn bit = 1), the transmit operation is started by writing data to TXBn register.

When transmission is disabled (TXEn bit = 0), even if data is written to TXBn register, the value is ignored.

The TXBn register data is transferred to the transmit shift register, and a transmission completion interrupt request signal (INTSTn) is generated, synchronized with the completion of the transmission of one frame from the transmit shift register. For information about the timing for generating this interrupt request, refer to **16.6.2 Transmit operation**.

When ASIFn.TXBFn bit = 1, writing must not be performed to TXBn register.

This register can be read or written in 8-bit units.

Reset sets this register to FFH.

After reset: FFH R/W Address: TXB0 FFFFFA04H, TXB1 FFFFFA14H, TXB2 FFFFFA24H

	7	6	5	4	3	2	1	0
TXBn	TXBn7	TXBn6	TXBn5	TXBn4	TXBn3	TXBn2	TXBn1	TXBn0

(n = 0 to 2)

16.5 Interrupt Requests

The following three types of interrupt request signals are generated from UARTn.

- Reception error interrupt request signal (INTSREn)
- Reception completion interrupt request signal (INTSRn)
- Transmission completion interrupt request signal (INTSTn)

The default priorities among these three types of interrupt request signals are, from high to low, reception error interrupt, reception completion interrupt, and transmission completion interrupt.

Table 16-2. Generated Interrupt Request Signals and Default Priorities

Interrupt Request Signal	Priority
Reception error interrupt request signal (INTSREn)	1
Reception completion interrupt request signal (INTSRn)	2
Transmission completion interrupt request signal (INTSTn)	3

(1) Reception error interrupt request signal (INTSREn)

When reception is enabled, the INTSREn signal is generated according to the logical OR of the three types of reception errors explained for the ASISn register. Whether the INTSREn signal or the INTSRn signal is generated when an error occurs can be specified according to the ASIMn.ISRMn bit.

When reception is disabled, the INTSREn signal is not generated.

(2) Reception completion interrupt request signal (INTSRn)

When reception is enabled, the INTSRn signal is generated when data is shifted in to the receive shift register and transferred to the RXBn register.

The INTSRn signal can be generated in place of the INTSREn signal according to the ASIMn.ISRMn bit even when a reception error has occurred.

When reception is disabled, the INTSRn signal is not generated.

(3) Transmission completion interrupt request signal (INTSTn)

The INTSTn signal is generated when one frame of transmit data containing 7-bit or 8-bit characters is shifted out from the transmit shift register.

16.6 Operation

16.6.1 Data format

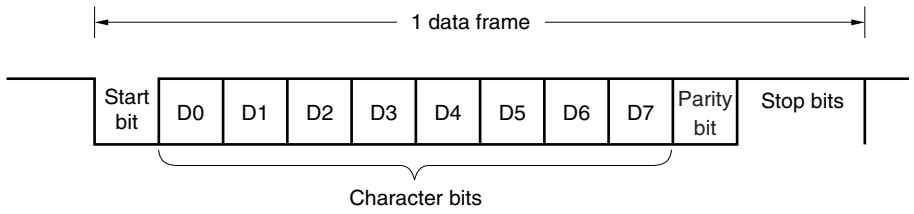
Full-duplex serial data transmission and reception can be performed.

The transmit/receive data format consists of one data frame containing a start bit, character bits, a parity bit, and stop bits as shown in Figure 16-3.

The character bit length within one data frame, the type of parity, and the stop bit length are specified according to the ASIMn register.

Also, data is transferred LSB first.

Figure 16-3. Format of UARTn Transmit/Receive Data



- Start bit ··· 1 bit
- Character bits ··· 7 bits or 8 bits
- Parity bit ··· Even parity, odd parity, 0 parity, or no parity
- Stop bits ··· 1 bit or 2 bits

16.6.2 Transmit operation

When the ASIMn.UARTEn bit is set to 1, a high level is output from the TXDn pin.

Then, when the ASIMn.TXEn bit is set to 1, transmission is enabled, and the transmit operation is started by writing transmit data to the TXBn register.

(1) Transmission enabled state

This state is set by the TXEn bit.

- TXEn bit = 1: Transmission enabled state
- TXEn bit = 0: Transmission disabled state

Since UARTn does not have a CTS (transmission enabled signal) input pin, a port should be used to confirm whether the destination is in a reception enabled state.

(2) Starting a transmit operation

In the transmission enabled state, a transmit operation is started by writing transmit data to the TXBn register. When a transmit operation is started, the data in the TXBn register is transferred to the transmit shift register. Then, the transmit shift register outputs data to the TXDn pin (the transmit data is transferred sequentially starting with the start bit). The start bit, parity bit, and stop bits are added automatically.

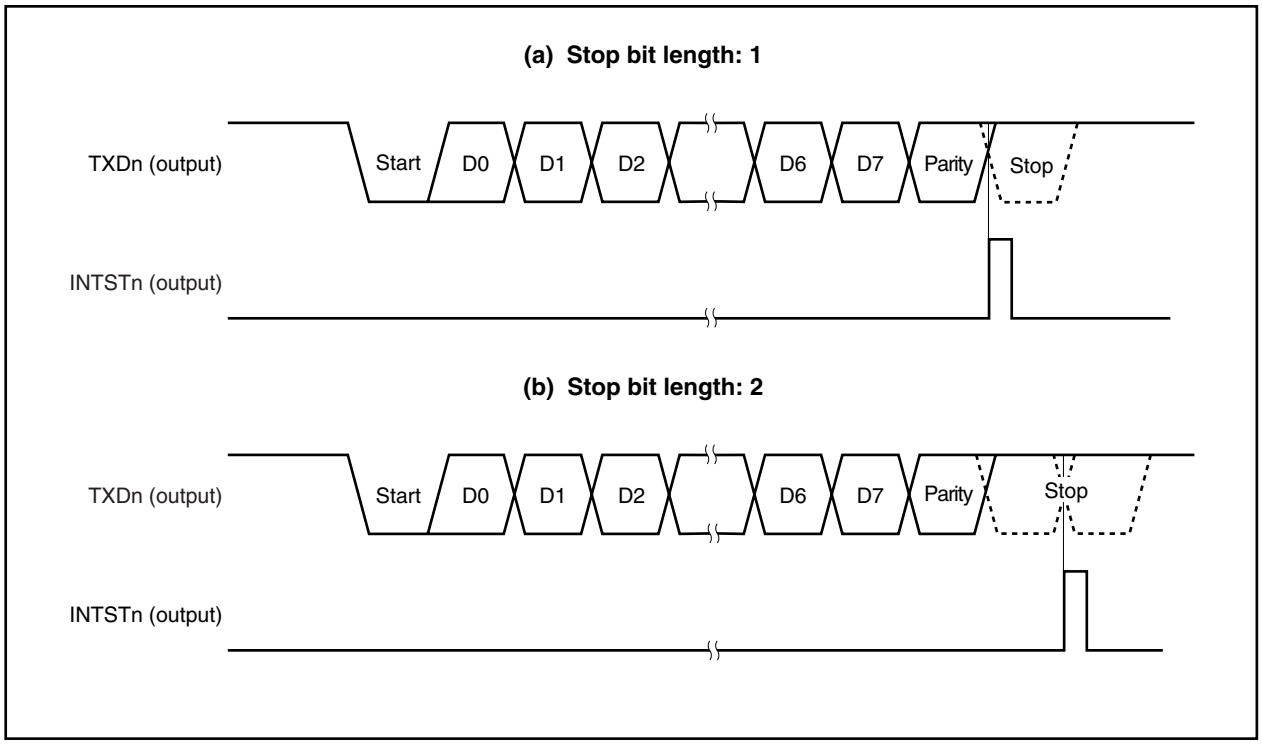
(3) Transmission interrupt

When the transmit shift register becomes empty, a transmission completion interrupt request signal (INTSTn) is generated. The timing for generating the INTSTn signal differs according to the specification of the stop bit length. The INTSTn signal is generated at the same time that the last stop bit is output.

If the data to be transmitted next has not been written to the TXBn register, the transmit operation is suspended.

Caution Normally, when the transmit shift register becomes empty, the INTSTn signal is generated. However, the INTSTn signal is not generated if the transmit shift register becomes empty due to reset.

Figure 16-4. UARTn Transmission Completion Interrupt Timing



16.6.3 Continuous transmission operation

UARTn can write the next transmit data to the TXBn register at the timing that the transmit shift register starts the shift operation. This enables an efficient transmission rate to be realized by continuously transmitting data even during the transmission completion interrupt service after the transmission of one data frame. In addition, reading the ASIFn.TXSFn bit after the occurrence of a transmission completion interrupt request signal (INTSTn) enables the TXBn register to be efficiently written twice (2 bytes) without waiting for the transmission of 1 data frame.

When continuous transmission is performed, data should be written after referencing the ASIFn register to confirm the transmission status and whether or not data can be written to the TXBn register.

Caution The values of the ASIF.TXBFn and ASIF.TXSFn bits change 10 → 11 → 01 in continuous transmission.
Therefore, do not confirm the status based on the combination of the TXBFn and TXSFn bits.
Read only the TXBFn bit during continuous transmission.

TXBFn	Whether or Not Writing to TXBn Register Is Enabled
0	Writing is enabled
1	Writing is not enabled

Caution When transmission is performed continuously, write the first transmit data (first byte) to the TXBn register and confirm that the TXBFn bit is 0, and then write the next transmit data (second byte) to TXBn register. If writing to the TXBn register is performed when the TXBFn bit is 1, transmit data cannot be guaranteed.

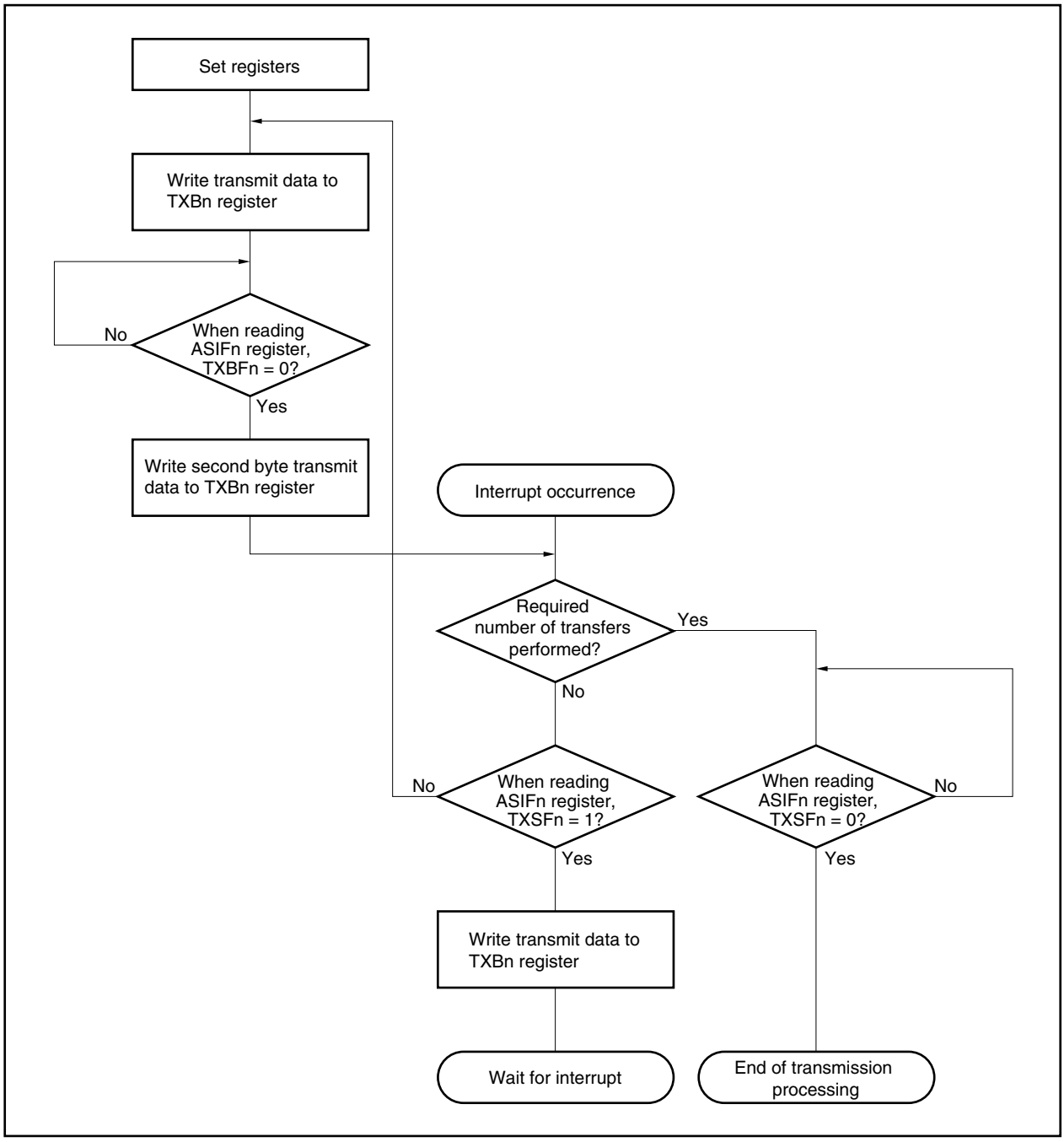
The communication status can be confirmed by referring to the TXSFn bit.

TXSFn	Transmission Status
0	Transmission is completed.
1	Under transmission.

Cautions 1. When initializing the transmission unit when continuous transmission is completed, confirm that the TXSFn bit is 0 after the occurrence of the transmission completion interrupt, and then execute initialization. If initialization is performed when the TXSFn bit is 1, transmit data cannot be guaranteed.

2. While transmission is being performed continuously, an overrun error may occur if the next transmission is completed before the INTSTn interrupt servicing following the transmission of 1 data frame is executed. An overrun error can be detected by embedding a program that can count the number of transmit data and referencing TXSFn bit.

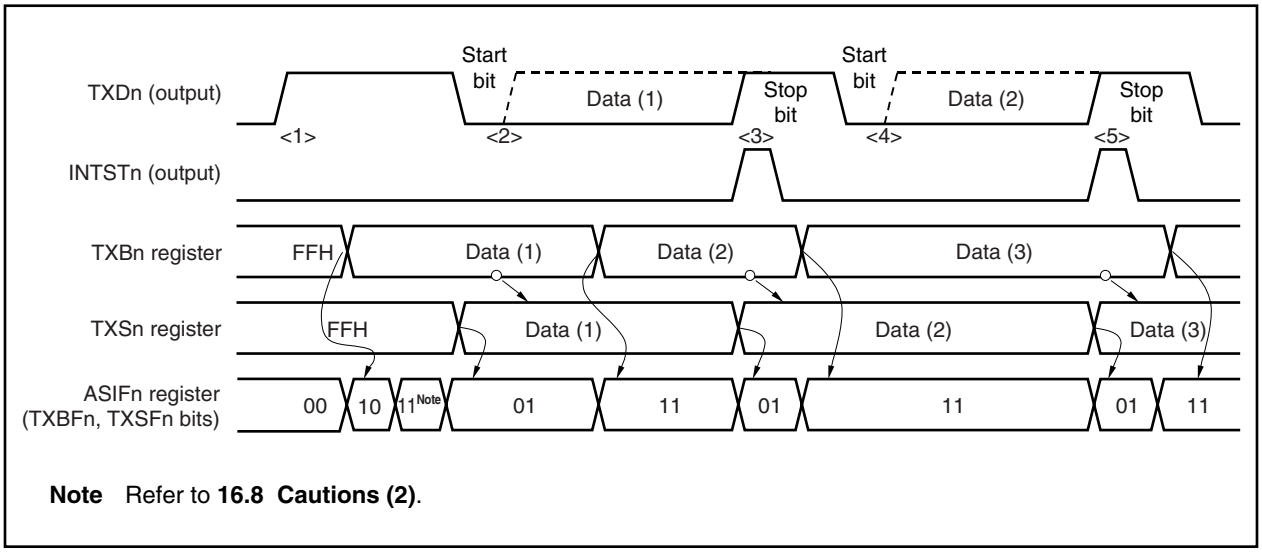
Figure 16-5. Continuous Transmission Processing Flow



(1) Starting procedure

The procedure to start continuous transmission is shown below.

Figure 16-6. Continuous Transmission Starting Procedure



Note Refer to **16.8 Cautions (2)**.

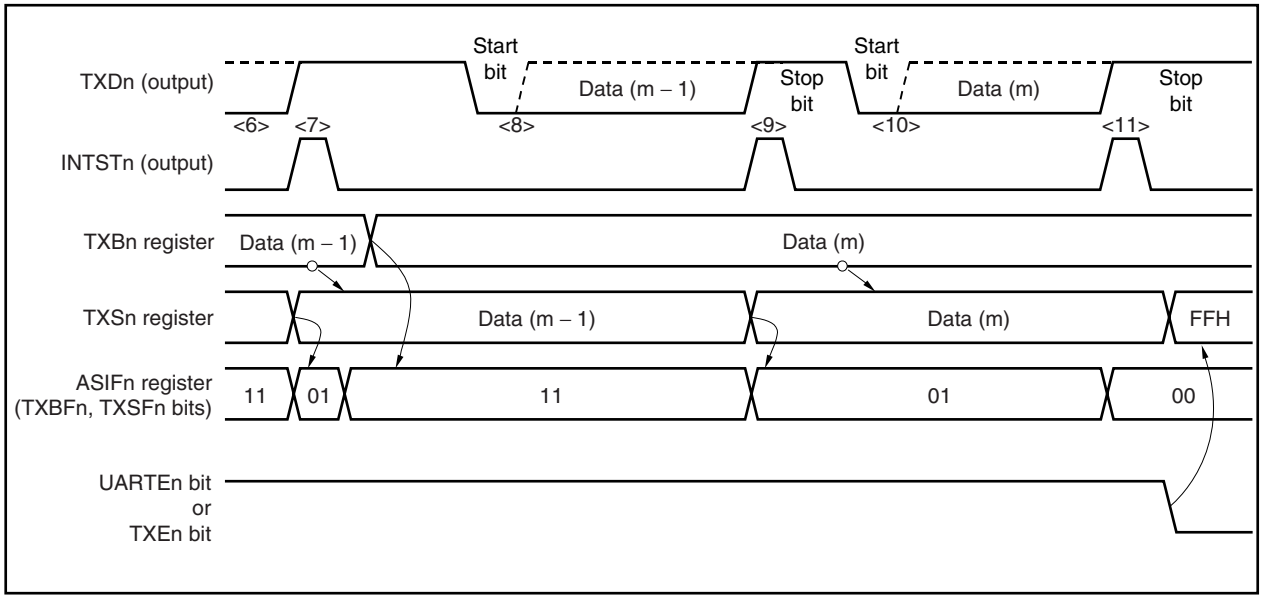
Transmission Starting Procedure	Internal Operation	ASIFn Register	
		TXBFn	TXSFn
• Set transmission mode	<1> Start transmission unit	0	0
• Write data (1) →		1	0
	<2> Generate start bit	1	1 Note
		0	1
	Start data (1) transmission →	0	1
• Read ASIFn register (confirm that TXBFn bit = 0) ←		0	1
• Write data (2) →		1	1
	<<Transmission in progress>>		
	<3> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXBFn bit = 0) ←		0	1
• Write data (3) →		1	1
	<4> Generate start bit		
	Start data (2) transmission		
	<<Transmission in progress>>		
	<5> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXBFn bit = 0) ←		0	1
• Write data (4) →		1	1

Note Refer to **16.8 Cautions (2)**.

(2) Ending procedure

The procedure for ending continuous transmission is shown below.

Figure 16-7. Continuous Transmission End Procedure



Transmission End Procedure	Internal Operation	ASIFn Register	
		TXBFn	TXSFn
	<6> Transmission of data (m – 2) is in progress	1	1
	<7> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXBFn bit = 0) ←		0	1
• Write data (m) →		1	1
	<8> Generate start bit Start data (m – 1) transmission <<Transmission in progress>>		
	<9> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXSFn bit = 1) ← There is no write data		0	1
	<10> Generate start bit Start data (m) transmission <<Transmission in progress>>		
	<11> Generate INTSTn interrupt →	0	0
• Read ASIFn register (confirm that TXSFn bit = 0) ←		0	0
• Clear (0) the UARTEn bit or TXEn bit	Initialize internal circuits		

16.6.4 Receive operation

The awaiting reception state is set by setting the ASIMn.UARTEn bit to 1 and then setting the ASIMn.RXEn bit to 1. To start the receive operation, start sampling at the falling edge when the falling of the RXDn pin is detected. If the RXDn pin is low level at a start bit sampling point, the start bit is recognized. When the receive operation begins, serial data is stored sequentially in the receive shift register according to the baud rate that was set. A reception completion interrupt request signal (INTSRn) is generated each time the reception of one frame of data is completed. Normally, the receive data is transferred from the RXBn register to memory by this interrupt servicing.

(1) Reception enabled state

The receive operation is set to the reception enabled state by setting the RXEn bit to 1.

- RXEn bit = 1: Reception enabled state
- RXEn bit = 0: Reception disabled state

In receive disabled state, the reception hardware stands by in the initial state. At this time, the contents of the RXBn register are retained, and no reception completion interrupt or reception error interrupt is generated.

(2) Starting a receive operation

A receive operation is started by the detection of a start bit.

The RXDn pin is sampled using the serial clock from baud rate generator n (BRGn).

(3) Reception completion interrupt

When the RXEn bit = 1 and the reception of one frame of data is completed (the stop bit is detected), the INTSRn signal is generated and the receive data within the receive shift register is transferred to the RXBn register at the same time.

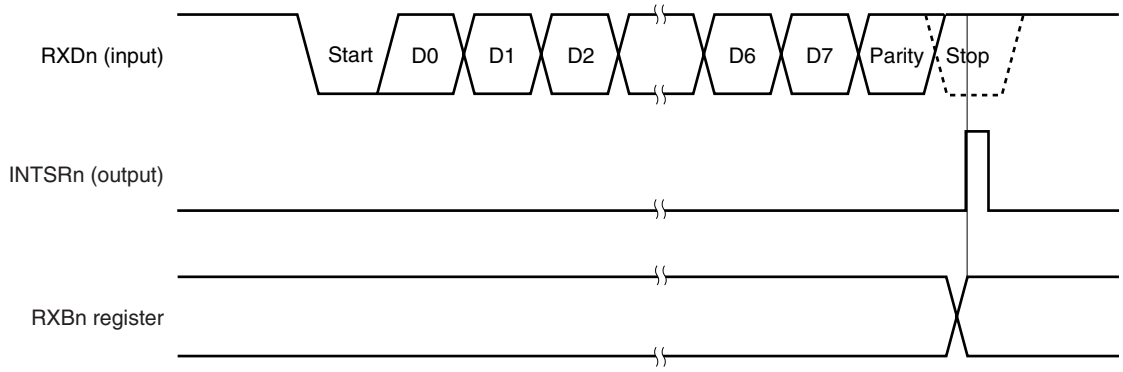
Also, if an overrun error (ASISn.OVEn bit = 1) occurs, the receive data at that time is not transferred to the RXBn register, and either the INTSRn signal or a reception error interrupt request signal (INTSREn) is generated according to the ASIMn.ISRMn bit setting.

Even if a parity error (ASISn.PEn bit = 1) or framing error (ASISn.FEn bit = 1) occurs during a reception operation, the receive operation continues until stop bit is received, and after reception is completed, either the INTSRn signal or the INTSREn signal is generated according to the ISRMn bit setting (the receive data within the receive shift register is transferred to the RXBn register).

If the RXEn bit is cleared (0) during a receive operation, the receive operation is immediately stopped. The contents of the RXBn register and the ASISn register at this time do not change, and the INTSRn signal or the INTSREn signal is not generated.

The INTSRn signal or the INTSREn signal is not generated when the RXEn bit = 0 (reception is disabled).

Figure 16-8. UARTn Reception Completion Interrupt Timing



Cautions 1. Be sure to read the RXBn register even when a reception error occurs. If the RXBn register is not read, an overrun error will occur at the next data reception and the reception error status will continue infinitely.

2. Reception is always performed assuming a stop bit length of 1.
A second stop bit is ignored.

16.6.5 Reception error

The three types of errors that can occur during a receive operation are a parity error, framing error, and overrun error. As a result of data reception, the various flags of the ASISn register are set (1), and a reception error interrupt request signal (INTSREn) or a reception completion interrupt request signal (INTSRn) is generated at the same time. The ASIMn.ISRMn bit specifies whether the INTSREn signal or the INTSRn signal is generated.

The type of error that occurred during reception can be detected by reading the contents of the ASISn register during the INTSREn or INTSRn interrupt servicing.

The contents of the ASISn register are cleared (0) by reading the ASISn register.

Table 16-3. Reception Error Causes

Error Flag	Reception Error	Cause
PEn	Parity error	The parity specification during transmission did not match the parity of the reception data
FEn	Framing error	No stop bit was detected
OVEn	Overrun error	The reception of the next data was completed before data was read from the RXBn register

(1) Separation of reception error interrupt request signal

A reception error interrupt request signal can be separated from the INTSRn signal and generated as the INTSREn signal by clearing the ISRMn bit to 0.

Figure 16-9. When Reception Error Interrupt Request Signal Is Separated from INTSRn Signal (ISRMn Bit = 0)

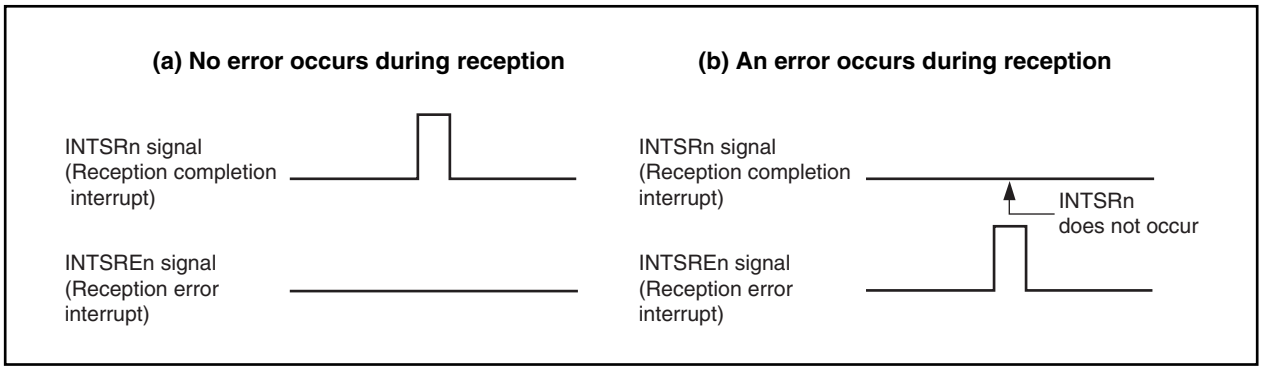
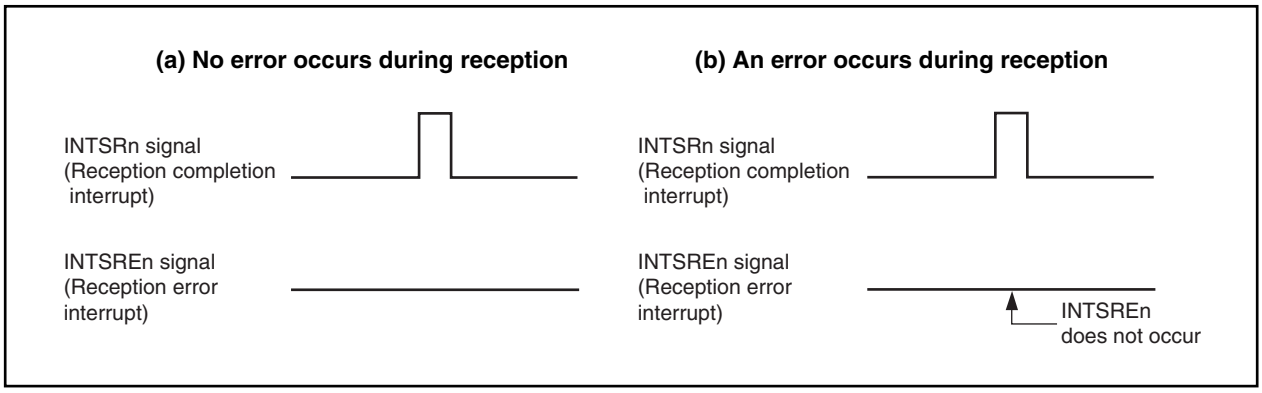


Figure 16-10. When Reception Error Interrupt Request Signal Is Included in INTSRn Signal (ISRMn Bit = 1)



16.6.6 Parity types and corresponding operation

A parity bit is used to detect a bit error in communication data. Normally, the same type of parity bit is used on the transmission and reception sides.

(1) Even parity

(i) During transmission

The parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is even. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 1
- If the number of bits with the value “1” within the transmit data is even: 0

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is odd.

(2) Odd parity

(i) During transmission

In contrast to even parity, the parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is odd. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 0
- If the number of bits with the value “1” within the transmit data is even: 1

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is even.

(3) 0 parity

During transmission the parity bit is set to “0” regardless of the transmit data.

During reception, no parity bit check is performed. Therefore, no parity error is generated regardless of whether the parity bit is “0” or “1”.

(4) No parity

No parity bit is added to the transmit data.

During reception, the receive operation is performed as if there were no parity bit. Since there is no parity bit, no parity error is generated.

16.6.7 Receive data noise filter

The RXDn signal is sampled at the rising edge of the prescaler output base clock (f_{UCLK}). If the same sampling value is obtained twice, the match detector output changes, and this output is sampled as input data. Therefore, data not exceeding one clock width is judged to be noise and is not delivered to the internal circuit (refer to **Figure 16-12**). Refer to **16.7.1 (1) Base clock** regarding the base clock.

Also, since the circuit is configured as shown in Figure 16-11, internal processing during a receive operation is delayed by up to 2 clocks according to the external signal status.

Figure 16-11. Noise Filter Circuit

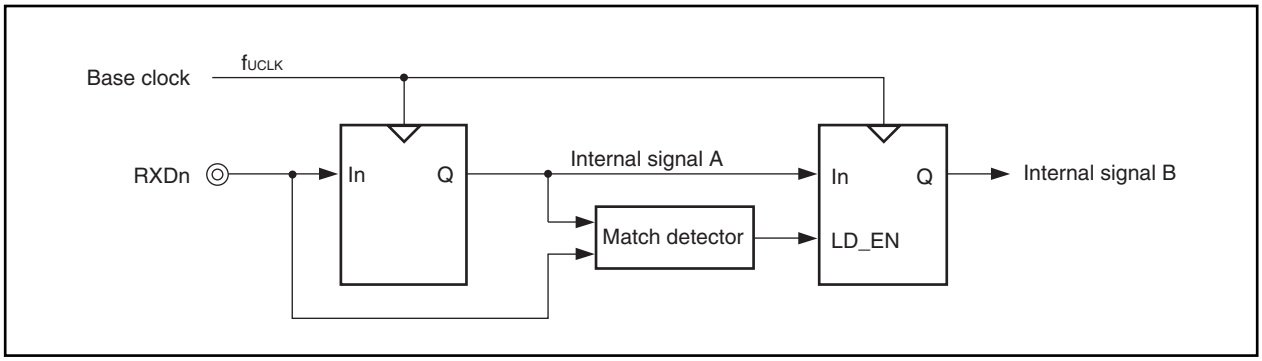
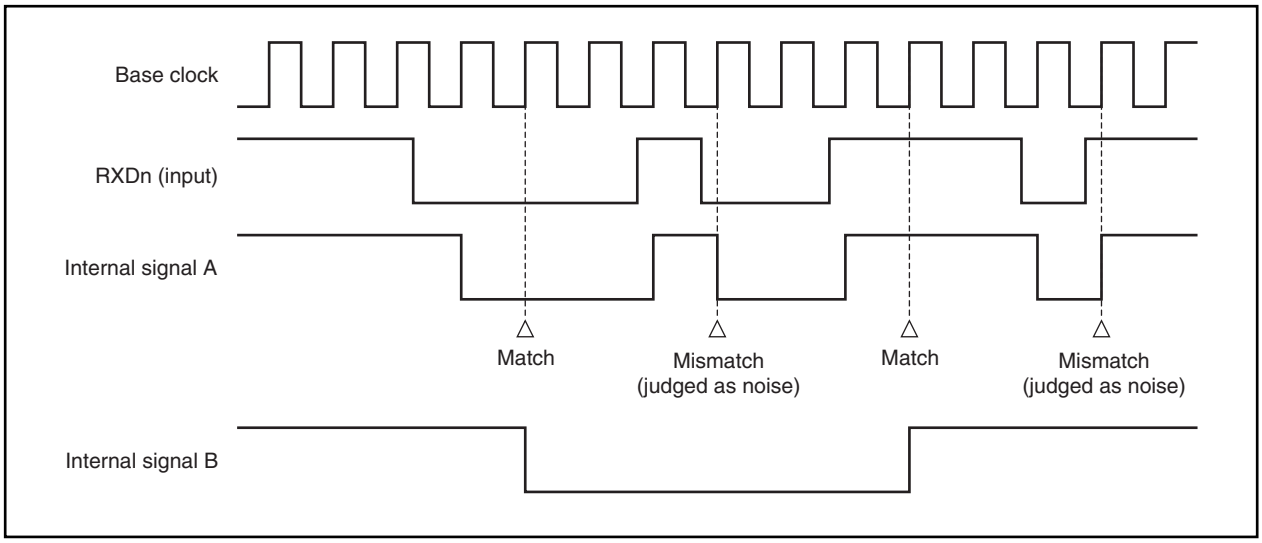


Figure 16-12. Timing of RXDn Signal Judged as Noise



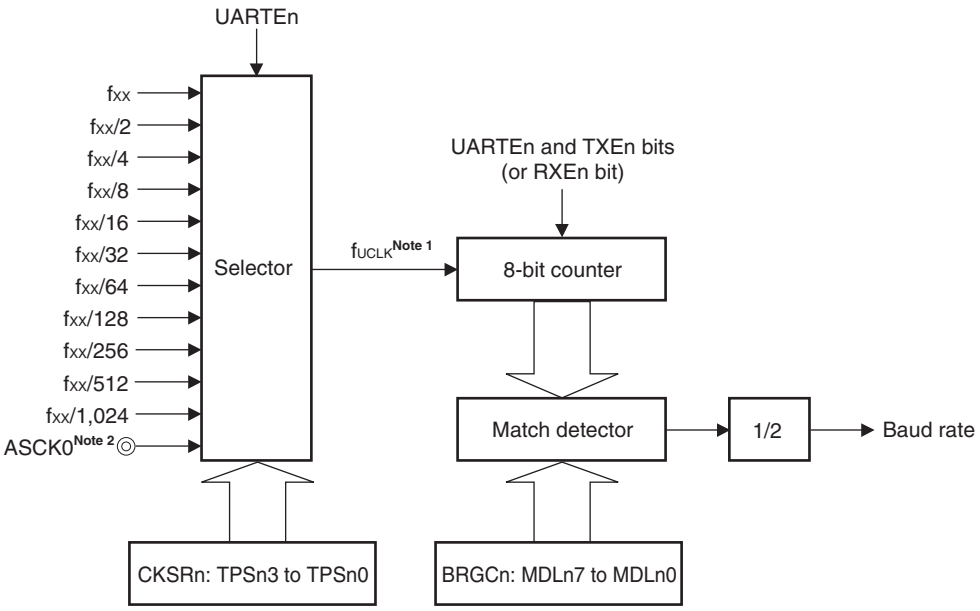
16.7 Dedicated Baud Rate Generator n (BRGn)

A dedicated baud rate generator, which consists of a source clock selector and an 8-bit programmable counter, generates serial clocks during transmission/reception by UARTn. The dedicated baud rate generator output can be selected as the serial clock for each channel.

Separate 8-bit counters exist for transmission and for reception.

16.7.1 Baud rate generator n (BRGn) configuration

Figure 16-13. Configuration of Baud Rate Generator n (BRGn)



Notes 1. Set f_{UCLK} so as to satisfy the following conditions.

- V_{DD} = REGC = 4.5 to 5.5 V: $f_{UCLK} \leq 12$ MHz
- V_{DD} = 4.0 to 5.5 V, REGC = 10 μF: $f_{UCLK} \leq 6$ MHz
- V_{DD} = REGC = 2.7 to 4.5 V: $f_{UCLK} \leq 6$ MHz

2. ASCK0 pin input can be used only by UART0.

Remark f_{XX}: Main clock frequency
f_{UCLK}: Base clock

(1) Base clock

When the ASIMn.UARTEn bit = 1, the clock selected according to the CKSRn.TPSn3 to CKSRn.TPSn0 bits is supplied to the transmission/reception unit. This clock is called the base clock (f_{UCLK}). When the UARTEn bit = 0, f_{UCLK} is fixed to low level.

16.7.2 Serial clock generation

A serial clock can be generated according to the settings of the CKSRn and BRGCn registers.

The base clock to the 8-bit counter is selected by the CKSRn.TPSn3 to CKSRn.TPSn0 bits.

The 8-bit counter divisor value can be set by the BRGCn.MDLn7 to BRGCn.MDLn0 bits.

(1) Clock select register n (CKSRn)

The CKSRn register is an 8-bit register for selecting the basic block using the TPSn3 to TPSn0 bits. The clock selected by the TPSn3 to TPSn0 bits becomes the base clock (f_{UCLK}) of the transmission/reception module.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

Caution Clear the ASIMn.UARTEn bit to 0 before rewriting the TPSn3 to TPSn0 bits.

After reset: 00H R/W Address: CKSR0 FFFFFA06H, CKSR1 FFFFFA16H, CKSR2 FFFFFA26H

	7	6	5	4	3	2	1	0
CKSRn	0	0	0	0	TPSn3	TPSn2	TPSn1	TPSn0

(n = 0 to 2)

TPSn3	TPSn2	TPSn1	TPSn0	Base clock (f_{UCLK})[Note 1]
0	0	0	0	f_{XX}
0	0	0	1	$f_{XX}/2$
0	0	1	0	$f_{XX}/4$
0	0	1	1	$f_{XX}/8$
0	1	0	0	$f_{XX}/16$
0	1	0	1	$f_{XX}/32$
0	1	1	0	$f_{XX}/64$
0	1	1	1	$f_{XX}/128$
1	0	0	0	$f_{XX}/256$
1	0	0	1	$f_{XX}/512$
1	0	1	0	$f_{XX}/1,024$
1	0	1	1	External clock[Note 2] (ASCK0 pin)
Other than above				Setting prohibited

Notes 1. Set f_{UCLK} so as to satisfy the following conditions.

- REGC = V_{DD} = 4.5 to 5.5 V: $f_{UCLK} \leq$ 12 MHz
- REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: $f_{UCLK} \leq$ 6 MHz
- REGC = V_{DD} = 2.7 to 4.5 V: $f_{UCLK} \leq$ 6 MHz

2. ASCK0 pin input clock can be used only by UART0.
Setting of UART1 and UART2 is prohibited.

Remark f_{XX}: Main clock frequency

(2) Baud rate generator control register n (BRGCn)

The BRGCn register is an 8-bit register that controls the baud rate (serial transfer speed) of UARTn.

This register can be read or written in 8-bit units.

Reset sets this register to FFH.

Caution If the MDLn7 to MDLn0 bits are to be overwritten, the ASIMn.TXEn and ASIMn.RXEn bits should be cleared to 0 first.

After reset: FFH R/W Address: BRGC0 FFFFFA07H, BRGC1 FFFFFA17H, BRGC2 FFFFFA27H

	7	6	5	4	3	2	1	0
BRGCn	MDLn7	MDLn6	MDLn5	MDLn4	MDLn3	MDLn2	MDLn1	MDLn0

(n = 0 to 2)

MDLn7	MDLn6	MDLn5	MDLn4	MDLn3	MDLn2	MDLn1	MDLn0	Set value (k)	Serial clock
0	0	0	0	0	×	×	×	–	Setting prohibited
0	0	0	0	1	0	0	0	8	f_{UCLK}/8
0	0	0	0	1	0	0	1	9	f_{UCLK}/9
0	0	0	0	1	0	1	0	10	f_{UCLK}/10
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	0	250	f_{UCLK}/250
1	1	1	1	1	0	1	1	251	f_{UCLK}/251
1	1	1	1	1	1	0	0	252	f_{UCLK}/252
1	1	1	1	1	1	0	1	253	f_{UCLK}/253
1	1	1	1	1	1	1	0	254	f_{UCLK}/254
1	1	1	1	1	1	1	1	255	f_{UCLK}/255

Remarks 1. f_{UCLK}: Frequency [Hz] of base clock selected by CKSR0.TPSn3 to CKSR0.TPSn0 bits

2. k: Value set by MDLn7 to MDLn0 bits (k = 8, 9, 10, ..., 255)

3. The baud rate is the output clock for the 8-bit counter divided by 2.

4. ×: don't care

(3) Baud rate

The baud rate is the value obtained by the following formula.

$$\text{Baud rate [bps]} = \frac{f_{UCLK}}{2 \times k}$$

f_{UCLK} = Frequency [Hz] of base clock selected by CKSRn.TPSn3 to CKSRn.TPSn0 bits.
k = Value set by BRGCn.MDLn7 to BRGCn.MDLn0 bits (k = 8, 9, 10, ..., 255)

(4) Baud rate error

The baud rate error is obtained by the following formula.

$$\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Target baud rate (normal baud rate)}} - 1 \right) \times 100 \text{ [\%]}$$

Cautions 1. Make sure that the baud rate error during transmission does not exceed the allowable error of the reception destination.

2. Make sure that the baud rate error during reception is within the allowable baud rate range during reception, which is described in 16.7.4 Allowable baud rate range during reception.

Example: Base clock frequency = 10 MHz = 10,000,000 Hz
Setting of BRGCn.MDLn7 to BRGCn.MDLn0 bits = 00100001B (k = 33)
Target baud rate = 153,600 bps

Baud rate = 10,000,000/(2 × 33)
= 151,515 [bps]

Error = (151,515/153,600 − 1) × 100
= −1.357 [%]

16.7.3 Baud rate setting example

Table 16-4. Baud Rate Generator Setting Data

Baud Rate (bps)	f_{XX} = 20 MHz			f_{XX} = 16 MHz			f_{XX} = 10 MHz		
	f_{UCLK}	k	ERR	f_{UCLK}	k	ERR	f_{UCLK}	k	ERR
300	f_{XX}/512	41H (65)	0.16	f_{XX}/1024	1AH (26)	0.16	f_{XX}/256	41H (65)	0.16
600	f_{XX}/256	41H (65)	0.16	f_{XX}/1024	0DH (13)	0.16	f_{XX}/128	41H (65)	0.16
1200	f_{XX}/128	41H (65)	0.16	f_{XX}/512	0DH (13)	0.16	f_{XX}/64	41H (65)	0.16
2400	f_{XX}/64	41H (65)	0.16	f_{XX}/256	0DH (13)	0.16	f_{XX}/32	41H (65)	0.16
4800	f_{XX}/32	41H (65)	0.16	f_{XX}/128	0DH (13)	0.16	f_{XX}/16	41H (65)	0.16
9600	f_{XX}/16	41H (65)	0.16	f_{XX}/64	0DH (13)	0.16	f_{XX}/8	41H (65)	0.16
10400	f_{XX}/64	0FH (15)	0.16	f_{XX}/64	0CH (12)	0.16	f_{XX}/32	0FH (15)	0.16
19200	f_{XX}/8	41H (65)	0.16	f_{XX}/32	0DH (13)	0.16	f_{XX}/4	41H (65)	0.16
24000	f_{XX}/32	0DH (13)	0.16	f_{XX}/2	A7H (167)	–0.20	f_{XX}/16	0DH (13)	0.16
31250	f_{XX}/32	0AH (10)	0.00	f_{XX}/32	08H (8)	0.00	f_{XX}/16	0AH (10)	0
33600	f_{XX}/2	95H (149)	–0.13	f_{XX}/2	77H (119)	0.04	f_{XX}	95H (149)	–0.13
38400	f_{XX}/4	41H (65)	0.16	f_{XX}/16	0DH (13)	0.16	f_{XX}/2	41H (65)	0.16
48000	f_{XX}/16	0DH (13)	0.16	f_{XX}/2	53H (83)	0.40	f_{XX}/8	0DH (13)	0.16
56000	f_{XX}/2	59H (89)	0.32	f_{XX}/2	47H (71)	0.60	f_{XX}	59H (89)	0.32
62500	f_{XX}/16	0AH (10)	0.00	f_{XX}/16	08H (8)	0.00	f_{XX}/8	0AH (10)	0.00
76800	f_{XX}/2	41H (65)	0.16	f_{XX}/8	0DH (13)	0.16	f_{XX}	41H (65)	0.16
115200	f_{XX}/2	2BH (43)	0.94	f_{XX}/2	23H (35)	–0.79	f_{XX}	2BH (43)	0.94
153600	f_{XX}/2	21H (33)	–1.36	f_{XX}/4	0DH (13)	0.16	f_{XX}	21H (33)	–1.36
312500	f_{XX}/4	08H (8)	0	f_{XX}/2	0DH (13)	–1.54	f_{XX}/2	08H (8)	0.00

Caution The allowable frequency of the base clock (f_{UCLK}) is as follows.

- **REGC = V_{DD} = 4.5 to 5.5 V: $f_{UCLK} \leq$ 12 MHz**
- **REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: $f_{UCLK} \leq$ 6 MHz**
- **REGC = V_{DD} = 2.7 to 4.5 V: $f_{UCLK} \leq$ 6 MHz**

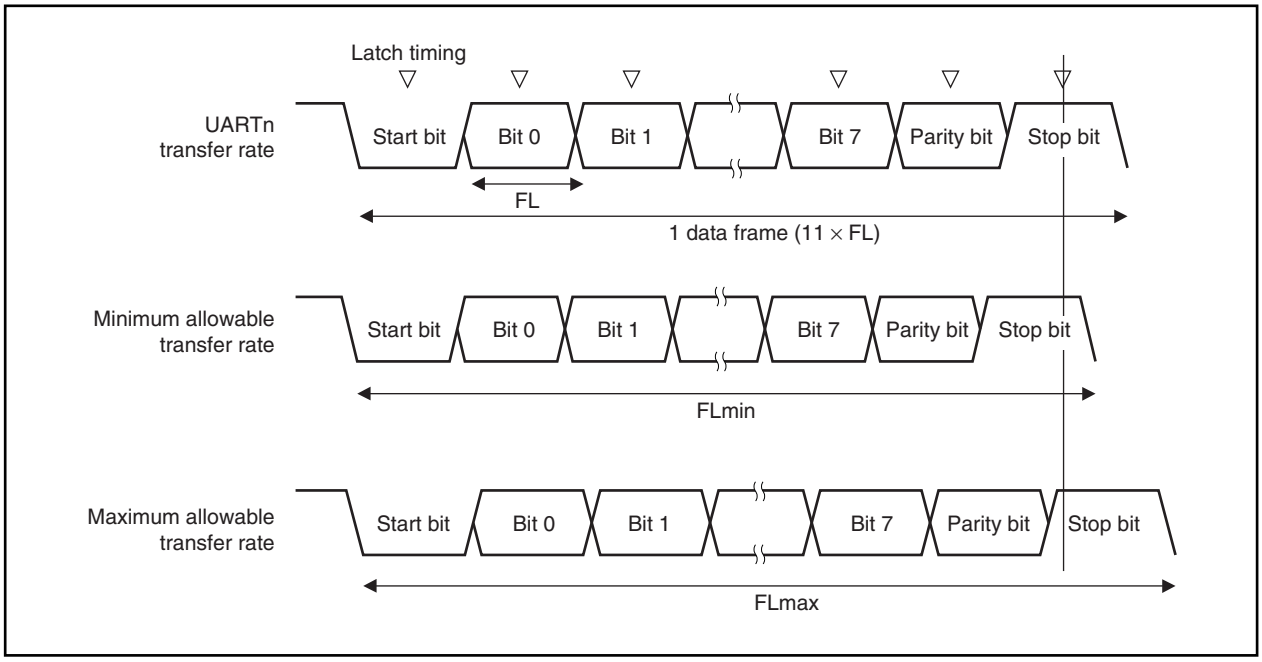
Remark f_{XX}: Main clock frequency
f_{UCLK}: Base clock frequency
k: Set values of BRGCn.MDLn7 to BRGCn.MDLn0 bits
ERR: Baud rate error [%]
n = 0 to 2

16.7.4 Allowable baud rate range during reception

The degree to which a discrepancy from the transmission destination's baud rate is allowed during reception is shown below.

Caution The equations described below should be used to set the baud rate error during reception so that it always is within the allowable error range.

Figure 16-14. Allowable Baud Rate Range During Reception



As shown in Figure 16-14, after the start bit is detected, the receive data latch timing is determined according to the counter that was set by the BRGCn register. If all data up to the final data (stop bit) is in time for this latch timing, the data can be received normally.
If this is applied to 11-bit reception, the following is theoretically true.

$$FL = (Brate)^{-1}$$

Brate: UARTn baud rate
k: BRGCn register set value
FL: 1-bit data length

When the latch timing margin is 2 base clocks, the minimum allowable transfer rate (FLmin) is as follows.

$$FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$$

Therefore, the transfer destination's maximum receivable baud rate (BRmax) is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} \text{ Brate}$$

Similarly, the maximum allowable transfer rate (FLmax) can be obtained as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k + 2}{2 \times k} \times FL = \frac{21k - 2}{2 \times k} FL$$

$$FLmax = \frac{21k - 2}{20k} FL \times 11$$

Therefore, the transfer destination's minimum receivable baud rate (BRmin) is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 2} \text{ Brate}$$

The allowable baud rate error of UARTn and the transfer destination can be obtained as follows from the expressions described above for computing the minimum and maximum baud rate values.

Table 16-5. Maximum and Minimum Allowable Baud Rate Error

Division Ratio (k)	Maximum Allowable Baud Rate Error	Minimum Allowable Baud Rate Error
8	+3.53%	–3.61%
20	+4.26%	–4.31%
50	+4.56%	–4.58%
100	+4.66%	–4.67%
255	+4.72%	–4.73%

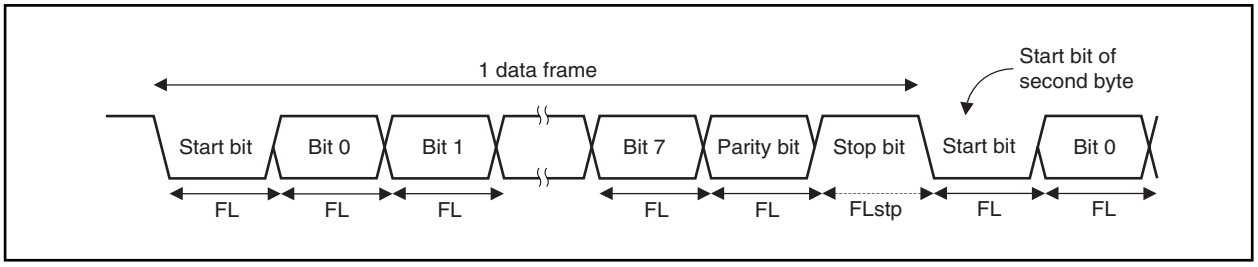
Remarks 1. The reception precision depends on the number of bits in one frame, the base clock frequency, and the division ratio (k). The higher the base clock frequency and the larger the division ratio (k), the higher the precision.

2. k: BRGCn register set value

16.7.5 Transfer rate during continuous transmission

During continuous transmission, the transfer rate from a stop bit to the next start bit is extended two clocks of the base clock longer than normal. However, on the reception side, the transfer result is not affected since the timing is initialized by the detection of the start bit.

Figure 16-15. Transfer Rate During Continuous Transmission



Representing the 1-bit data length by FL, the stop bit length by FLstp, and the base clock frequency by f_{UCLK} yields the following equation.

$$FLstp = FL + 2/f_{UCLK}$$

Therefore, the transfer rate during continuous transmission is as follows (when the stop bit length = 1).

$$\text{Transfer rate} = 11 \times FL + (2/f_{UCLK})$$

16.8 Cautions

Cautions to be observed when using UARTn are shown below.

(1) When the supply of clocks to UARTn is stopped (for example, in IDLE or STOP mode), operation stops with each register retaining the value it had immediately before the supply of clocks was stopped. The TXDn pin output also holds and outputs the value it had immediately before the supply of clocks was stopped. However, operation is not guaranteed after the supply of clocks is restarted. Therefore, after the supply of clocks is restarted, the circuits should be initialized by clearing the ASIMn.UARTEn, ASIMn.RXEn, and ASIMn.TXEn bits to 000.

(2) UARTn has a 2-stage buffer configuration consisting of the TXBn register and the transmission shift register, and has status flags (ASIFn.TXBFn and ASIFn.TXSFn bits) that indicate the status of each buffer. If the TXBFn and TXSFn bits are read in continuous transmission, the value changes 10 → 11 → 01. For the timing to write the next data to the TXBn register, read only the TXBFn bit during continuous transmission.

CHAPTER 17 CLOCKED SERIAL INTERFACE 0 (CSI0)

In the V850ES/KG2, two channels of clocked serial interface 0 (CSI0) are provided.

17.1 Features

- Maximum transfer speed: 5 Mbps
- Master mode/slave mode selectable
- Transmission data length: 8 bits or 16 bits can be set
- MSB/LSB-first selectable for transfer data
- Eight clock signals can be selected (7 master clocks and 1 slave clock)
- 3-wire type SO0n: Serial transmit data output
  SI0n: Serial receive data input
  $\overline{\text{SCK0n}}$: Serial clock I/O
- Interrupt sources: 1 type
  - Transmission/reception completion interrupt request signal (INTCSI0n)
- Transmission/reception mode or reception-only mode selectable
- Two transmission buffer registers (SOTBFn/SOTBFLn, SOTBn/SOTBLn) and two reception buffer registers (SIRBn/SIRBLn, SIRBEn/SIRBELn) are provided on chip
- Single transfer mode/continuous transfer mode selectable

Remark n = 0, 1

17.2 Configuration

CSI0n is controlled via the CSIM0n register.

(1) Clocked serial interface mode register 0n (CSIM0n)

The CSIM0n register is an 8-bit register that specifies the operation of CSI0n.

(2) Clocked serial interface clock selection register n (CSICn)

The CSICn register is an 8-bit register that controls the CSI0n serial transfer operation.

(3) Serial I/O shift register 0n (SIO0n)

The SIO0n register is a 16-bit shift register that converts parallel data into serial data.
The SIO0n register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by accessing the buffer register.

(4) Serial I/O shift register 0nL (SIO0nL)

The SIO0nL register is an 8-bit shift register that converts parallel data into serial data.
The SIO0nL register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by access of the buffer register .

(5) Clocked serial interface receive buffer register n (SIRBn)

The SIRBn register is a 16-bit buffer register that stores receive data.

(6) Clocked serial interface receive buffer register nL (SIRBnL)

The SIRBnL register is an 8-bit buffer register that stores receive data.

(7) Clocked serial interface read-only receive buffer register n (SIRBEn)

The SIRBEn register is a 16-bit buffer register that stores receive data.
The SIRBEn register is the same as the SIRBn register. It is used to read the contents of the SIRBn register.

(8) Clocked serial interface read-only receive buffer register nL (SIRBEnL)

The SIRBEnL register is an 8-bit buffer register that stores receive data.
The SIRBEnL register is the same as the SIRBnL register. It is used to read the contents of the SIRBnL register.

(9) Clocked serial interface transmit buffer register n (SOTBn)

The SOTBn register is a 16-bit buffer register that stores transmit data.

(10) Clocked serial interface transmit buffer register nL (SOTBLnL)

The SOTBnL register is an 8-bit buffer register that stores transmit data.

(11) Clocked serial interface initial transmit buffer register n (SOTBFn)

The SOTBFn register is a 16-bit buffer register that stores the initial transmit data in the continuous transfer mode.

(12) Clocked serial interface initial transmit buffer register nL (SOTBFnL)

The SOTBFnL register is an 8-bit buffer register that stores initial transmit data in the continuous transfer mode.

(13) Selector

The selector selects the serial clock to be used.

(14) Serial clock controller

Controls the serial clock supply to the shift register. Also controls the clock output to the $\overline{\text{SCK0n}}$ pin when the internal clock is used.

(15) Serial clock counter

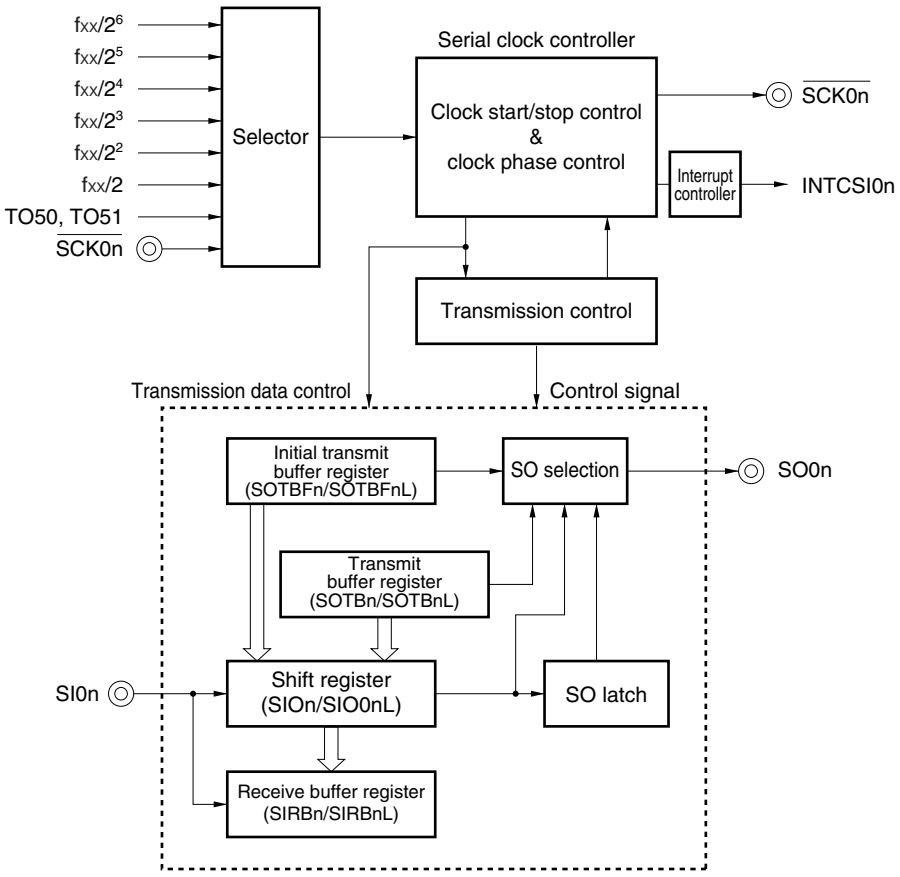
Counts the serial clock output or input during transmission/reception, and checks whether 8-bit or 16-bit data transmission/reception has been performed.

(16) Interrupt controller

Controls the interrupt request timing.

Remark n = 0, 1

Figure 17-1. Block Diagram of Clocked Serial Interface



Remarks 1. n = 0, 1

2. fxx: Main clock

17.3 Registers

(1) Clocked serial interface mode register 0n (CSIM0n)

The CSIM0n register controls the CSI0n operation.

This register can be read or written in 8-bit or 1-bit units (however, CSOTn bit is read-only).

Reset sets CSIM0n to 00H.

Caution Overwriting the CSIM0n.TRMDn, CSIM0n.CCLn, CSIM0n.DIRn, CSIM0n.CSITn, and CSIM0n.AUTOn bits can be done only when the CSOTn bit = 0. If these bits are overwritten at any other time, the operation cannot be guaranteed.

After reset: 00H R/W Address: CSIM00 FFFFFD00H, CSIM01 FFFFFD10H

	<7>	<6>	5	<4>	3	2	1	<0>
CSIM0n	CSI0En	TRMDn	CCLn	DIRn	CSITn	AUTOn	0	CSOTn

(n = 0, 1)

CSI0En	CSI0n operation enable/disable
0	Disable CSI0n operation.
1	Enable CSI0n operation.
The internal CSI0n circuit can be reset[Note] asynchronously by clearing the CSI0En bit to 0. For the $\overline{\text{SCK0n}}$ and SO0n pin output status when the CSI0En bit = 0, refer to **17.5 Output Pins**.	

TRMDn	Specification of transmission/reception mode
0	Receive-only mode
1	Transmission/reception mode
When the TRMDn bit = 0, reception is performed and the SO0n pin outputs a low level. Data reception is started by reading the SIRBn register. When the TRMDn bit = 1, transmission/reception is started by writing data to the SOTBn register.	

CCLn	Specification of data length
0	8 bits
1	16 bits

DIRn	Specification of transfer direction mode (MSB/LSB)
0	First bit of transfer data is MSB
1	First bit of transfer data is LSB

CSITn	Control of delay of interrupt request signal
0	No delay
1	Delay mode (interrupt request signal is delayed 1/2 cycle compared to the serial clock)
The delay mode (CSITn bit = 1) is valid only in the master mode (CSICn.CKS0n2 to CSICn.CSK0n0 bits are not 111B). In the slave mode (CKS0n2 to CKS0n0 bits are 111B), do not set the delay mode.	

AUTOn	Specification of single transfer mode or continuous transfer mode
0	Single transfer mode
1	Continuous mode

CSOTn	Communication status flag
0	Communication stopped
1	Communication in progress
The CSOTn bit is cleared (0) by writing 0 to the CSI0En bit.	

Note The CSOTn bit and the SIRBn, SIRBnL, SIRBE, SIRBEnL, SIOn, and SIOnL registers are reset.

(2) Clocked serial interface clock selection register n (CSICn)

The CSICn register is an 8-bit register that controls the CSI0n transfer operation.

This register can be read or written in 8-bit or 1-bit units.

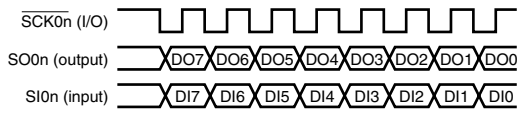
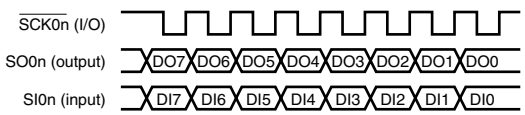
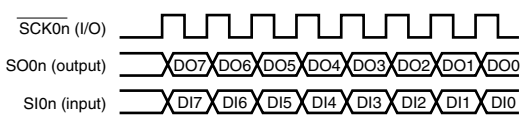
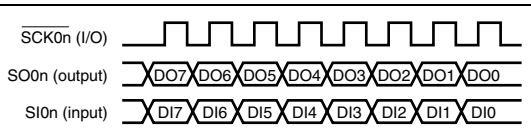
Reset sets CSICn to 00H.

Caution The CSICn register can be overwritten only when the CSIM0n.CSI0En bit = 0.

After reset: 00H R/W Address: CSIC0 FFFFFD01H, CSIC1 FFFFFD11H

	7	6	5	4	3	2	1	0
CSICn	0	0	0	CKPn	DAPn	CKS0n2	CKS0n1	CKS0n0

(n = 0, 1)

CKPn	DAPn	Specification of timing of transmitting/receiving data to/from $\overline{SCK0n}$
0	0	(Type 1) 
0	1	(Type 2) 
1	0	(Type 3) 
1	1	(Type 4) 

CKS0n2	CKS0n1	CKS0n0	Serial clock[Note]	Mode
0	0	0	$f_{XX}/2$	Master mode
0	0	1	$f_{XX}/2^2$	Master mode
0	1	0	$f_{XX}/2^3$	Master mode
0	1	1	$f_{XX}/2^4$	Master mode
1	0	0	$f_{XX}/2^5$	Master mode
1	0	1	$f_{XX}/2^6$	Master mode
1	1	0	Clock generated by TO5n	Master mode
1	1	1	External clock ($\overline{SCK0n}$ pin)	Slave mode

Note Set the serial clock so as to satisfy the following conditions.

- REGC = V_{DD} = 4.0 to 5.5 V: Serial clock ≤ 5 MHz
- REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: Serial clock ≤ 2.5 MHz
- REGC = V_{DD} = 2.7 to 4.0 V: Serial clock ≤ 2.5 MHz

Remark f_{XX}: Main clock frequency

(3) Clocked serial interface receive buffer registers n, nL (SIRBn, SIRBnL)

The SIRBn register is a 16-bit buffer register that stores receive data.

When the receive-only mode is set (CSIM0n.TRMDn bit = 0), the reception operation is started by reading data from the SIRBn register.

This register is read-only in 16-bit units. When the lower 8 bits are used as the SIRBnL register, this register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIM0n.CSI0En bit.

Cautions 1. Read the SIRBn register only when a 16-bit data length has been set (CSIM0n.CCLn bit = 1).

Read the SIRBnL register only when an 8-bit data length has been set (CCLn bit = 0).

2. When the single transfer mode has been set (CSIM0n.AUTOn bit = 0), perform a read operation only in the idle state (CSIM0n.CSOTn bit = 0). If the SIRBn or SIRBnL register is read during data transfer, the data cannot be guaranteed.

(a) SIRBn register

After reset: 0000H R Address: SIRB0 FFFFFD02H, SIRB1 FFFFFD12H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn	SIRBn
(n = 0, 1)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(b) SIRBnL register

After reset: 00H R Address: SIRB0L FFFFFD02H, SIRB1L FFFFFD12H

	7	6	5	4	3	2	1	0
SIRBnL	SIRBn7	SIRBn6	SIRBn5	SIRBn4	SIRBn3	SIRBn2	SIRBn1	SIRBn0
(n = 0, 1)								

(4) Clocked serial interface read-only receive buffer registers n, nL (SIRBEn, SIRBEnL)

The SIRBEn register is a 16-bit buffer register that stores receive data.

The SIRBEn register is the same as the SIRBn register. Even if the SIRBEn register is read, the next operation will not start. The SIRBEn register is used to read the contents of the SIRBn register when the serial reception is not continued.

This register is read-only in 16-bit units. However, when the lower 8 bits are used as the SIRBEnL register, the register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIM0n.CSI0En bit.

Cautions 1. The receive operation is not started even if data is read from the SIRBEn and SIRBEnL registers.

2. The SIRBEn register can be read only if a 16-bit data length has been set (CSIM0n.CCLn bit = 1).

The SIRBEnL register can be read only if an 8-bit data length has been set (CCLn bit = 0).

(a) SIRBEn register

After reset: 0000H R Address: SIRBE0 FFFFFD06H, SIRBE1 FFFFFD16H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn	SIRBEn
(n = 0, 1)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(B) SIRBEnL register

After reset: 00H R Address: SIRBE0L FFFFFD06H, SIRBE1L FFFFFD16H

	7	6	5	4	3	2	1	0
SIRBEnL	SIRBEn7	SIRBEn6	SIRBEn5	SIRBEn4	SIRBEn3	SIRBEn2	SIRBEn1	SIRBEn0
(n = 0, 1)								

(5) Clocked serial interface transmit buffer registers n, nL (SOTBn, SOTBnL)

The SOTBn register is a 16-bit buffer register that stores transmit data.

When the transmission/reception mode is set (CSIM0n.TRMDn bit = 1), the transmission operation is started by writing data to the SOTBn register.

This register can be read or written in 16-bit units. However, when the lower 8 bits are used as the SOTBnL register, the register is read-only in 8-bit units.

After reset, this register is initialized.

Cautions 1. Access the SOTBn register only when a 16-bit data length has been set (CSIM0n.CCLn bit = 1).

Access the SOTBnL register only when an 8-bit data length has been set (CCLn bit = 0).

2. When the single transfer mode is set (CSIM0n.AUTOn bit = 0), perform access only in the idle state (CSIM0n.CSOTn bit = 0). If the SOTBn and SOTBnL registers are accessed during data transfer, the data cannot be guaranteed.

(a) SOTBn register

After reset: 0000H R/W Address: SOTB0 FFFFFD04H, SOTB1 FFFFFD14H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn	SOTBn
(n = 0, 1)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(b) SOTBnL register

After reset: 00H R/W Address: SOTB0L FFFFFD04H, SOTB1L FFFFFD14H

	7	6	5	4	3	2	1	0
SOTBnL	SOTBn7	SOTBn6	SOTBn5	SOTBn4	SOTBn3	SOTBn2	SOTBn1	SOTBn0
(n = 0, 1)								

(6) Clocked serial interface initial transmit buffer registers n, nL (SOTBFn, SOTBFnL)

The SOTBFn register is a 16-bit buffer register that stores initial transmission data in the continuous transfer mode.

The transmission operation is not started even if data is written to the SOTBFn register.

This register can be read or written in 16-bit units. However, when the lower 8 bits are used as the SOTBFnL register, the register can be read or written in 8-bit units.

After reset, this register is initialized.

Caution Access the SOTBFn register and SOTBFnL register only when a 16-bit data length has been set (CSIM0n.CCLn bit = 1), and only when an 8-bit data length has been set (CCLn bit = 0), respectively, and only in the idle state (CSIM0n.CSOTn bit = 0). If the SOTBFn and SOTBFnL registers are accessed during data transfer, the data cannot be guaranteed.

(a) SOTBFn register

After reset: 0000H R/W Address: SOTBF0 FFFFFD08H, SOTBF1 FFFFFD18H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOTBFn (n = 0, 1)	SOTBFn 15	SOTBFn 14	SOTBFn 13	SOTBFn 12	SOTBFn 11	SOTBFn 10	SOTBFn 9	SOTBFn 8	SOTBFn 7	SOTBFn 6	SOTBFn 5	SOTBFn 4	SOTBFn 3	SOTBFn 2	SOTBFn 1	SOTBFn 0

(b) SOTBFnL register

After reset: 00H R/W Address: SOTBF0L FFFFFD08H, SOTBF1L FFFFFD18H

	7	6	5	4	3	2	1	0
SOTBFnL (n = 0, 1)	SOTBFn7	SOTBFn6	SOTBFn5	SOTBFn4	SOTBFn3	SOTBFn2	SOTBFn1	SOTBFn0

(7) Serial I/O shift registers n, nL (SIO0n, SIO0nL)

The SIO0n register is a 16-bit shift register that converts parallel data into serial data.

The transfer operation is not started even if the SIO0n register is read.

This register is read-only in 16-bit units. However, when the lower 8 bits are used as the SIO0nL register, the register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSIM0n.CSI0En bit.

Caution Read the SIO0n register and SIO0nL register only when a 16-bit data length has been set (CSIM0n.CCLn bit = 1), and only when an 8-bit data length has been set (CCLn bit = 0), respectively, and only in the idle state (CSIM0n.CSOTn bit = 0). If the SIO0n and SIO0nL registers are read during data transfer, the data cannot be guaranteed.

(a) SIO0n register

After reset: 0000H R Address: SIO00 FFFFFD0AH, SIO01 FFFFFD1AH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIO0n	SIOn15	SIOn14	SIOn13	SIOn12	SIOn11	SIOn10	SIOn9	SIOn8	SIOn7	SIOn6	SIOn5	SIOn4	SIOn3	SIOn2	SIOn1	SIOn0

(n = 0, 1)

(b) SIO0nL register

After reset: 00H R Address: SIO00L FFFFFD0AH, SIO01L FFFFFD1AH

	7	6	5	4	3	2	1	0
SIO0nL	SIOn7	SIOn6	SIOn5	SIOn4	SIOn3	SIOn2	SIOn1	SIOn0

(n = 0, 1)

Table 17-1. Use of Each Buffer Register

Register Name	R/W		Single Transfer		Continuous Transfer[Note 1]	
			Transmission/Reception Mode	Receive-Only Mode	Transmission/Reception Mode	Receive-Only Mode
SIRBn (SIRBnL)	Read	Function	Storing received data[Note 2]	• Reading starts reception • Storing received data	Storing up to the (N – 1)th received data (other than the last)[Note 2]	• Reading starts reception • Storing up to the (N – 2)th data (other than the last two)
		Use method	When transmission and reception are complete, read the received data from this register.	• First, read dummy data and start transfer. • To perform reception of the next data after reception is complete, read the received data from this register.	When reception is complete, read the received data from this register. Repeat this operation until the (N – 1)th data has been received.	When reception is complete, read the received data from this register. Repeat this operation until the (N – 2)th data has been received. (Supplement) Do not read the (N – 1)th data from this register. If read, a reception operation starts and continuous transfer cannot be completed.
SIRBEn (SIRBEnL)	Read	Function	–	Storing the data received last[Note 2]	–	Storing the (N – 1)th received data[Note 2]
		Use method	Not used.	If reception of the next data will not be performed after reception is complete, read the received data from this register.	Not used	Read the (N – 1)th received data from this register when the (N – 1)th or Nth (last) data has been received.
SIO0n (SIO0nL)	Read	Function	–	–	Storing the Nth (last) received data[Note 2]	Storing the Nth (last) received data[Note 2]
		Use method	Not used.	Not used	When the Nth (last) transmission/reception is complete, read the Nth (last) data.	When the Nth (last) data has been received, read the Nth (last) data.
SOTBn (SOTBnL)	Write	Function	• Starting transmission/reception when written • Storing the data to be transmitted	–	• Starting transmission/reception when written • Storing the data to be transmitted second and subsequently	–
		Use method	• When transmission/reception is complete, write the data to be transmitted next.	Not used	When transmission/reception is complete, write the data to be transmitted next to this register to start the next transmission/reception.	Not used
SOTBFn (SOTBFnL)	Write	Function	–	–	Storing the data to be transmitted first[Note 2]	–
		Use method	Not used	Not used	Before starting transmission/reception (writing to SOTBn), write the data to be transmitted first.	Not used

Notes 1. It is assumed that the number of data to be transmitted is N.

2. Neither reading nor writing will start communication.

Remark In the 16-bit mode, the registers not enclosed in parentheses are used; in the 8-bit mode, the registers in parentheses are used.

17.4 Operation

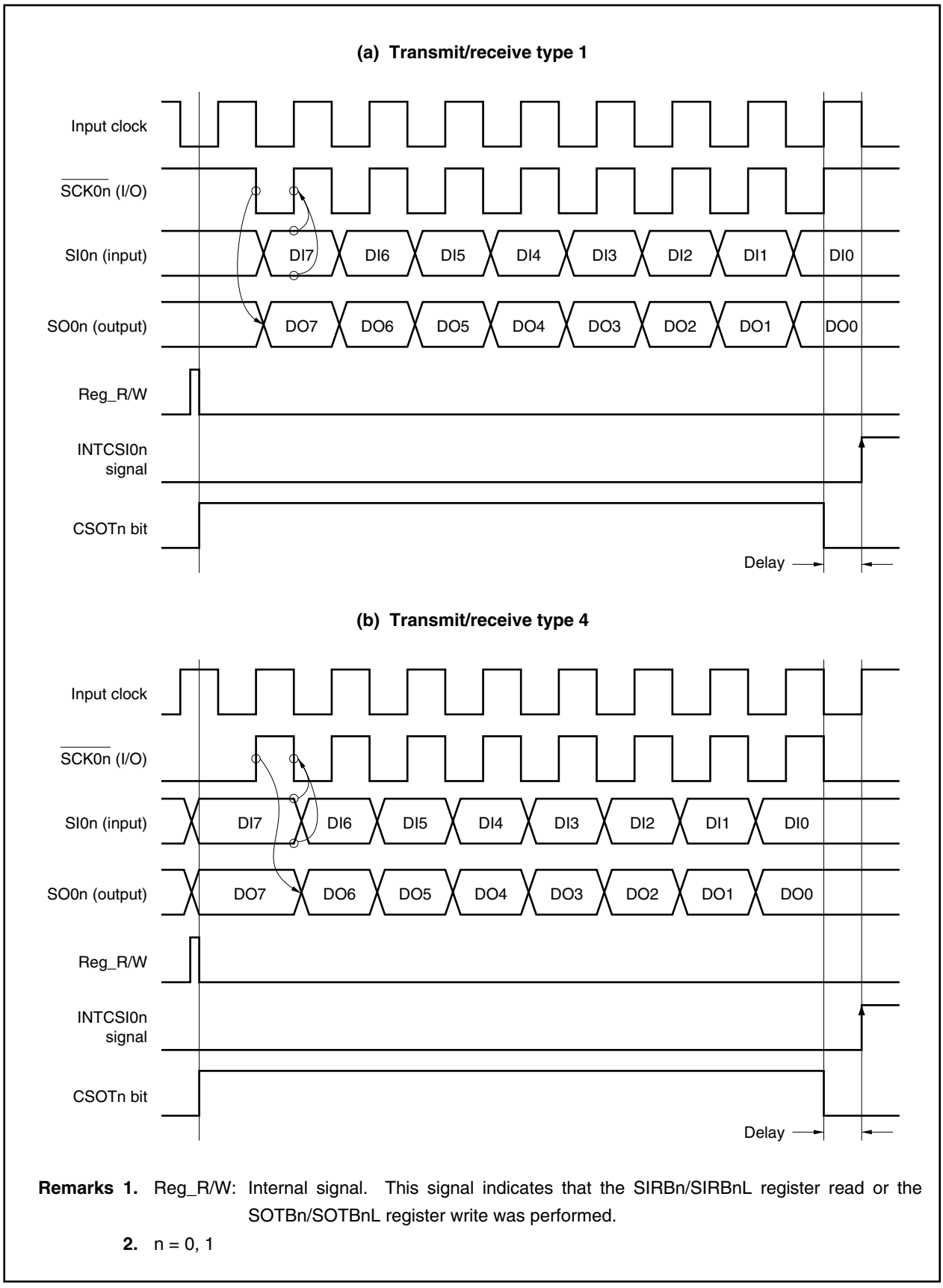
17.4.1 Transmission/reception completion interrupt request signal (INTCSI0n)

The INTCSI0n signal is set (1) upon completion of data transmission/reception.

Writing to the CSIM0n register clears (0) the INTCSI0n signal.

Caution The delay mode (CSIM0n.CSITn bit = 1) is valid only in the master mode (CSICn.CKS0n2 to CSICn.CKS0n0 bits are not 111B). The delay mode cannot be set when the slave mode is set (CKS0n2 to CKS0n0 bits = 111B).

Figure 17-2. Timing Chart of INTCSI0n Signal Output in Delay Mode



Remarks 1. Reg_R/W: Internal signal. This signal indicates that the SIRBn/SIRBnL register read or the SOTBn/SOTBnL register write was performed.

2. n = 0, 1

17.4.2 Single transfer mode

(1) Usage

In the receive-only mode (CSIM0n.TRMDn bit = 0), communication is started by reading the SIRBn/SIRBnL register.

In the transmission/reception mode (TRMDn bit = 1), communication is started by writing to the SOTBn/SOTBnL register.

In the slave mode, the operation must be enabled beforehand (CSIM0n.CSI0En bit = 1).

When communication is started, the value of the CSIM0n.CSOTn bit becomes 1 (transmission execution status).

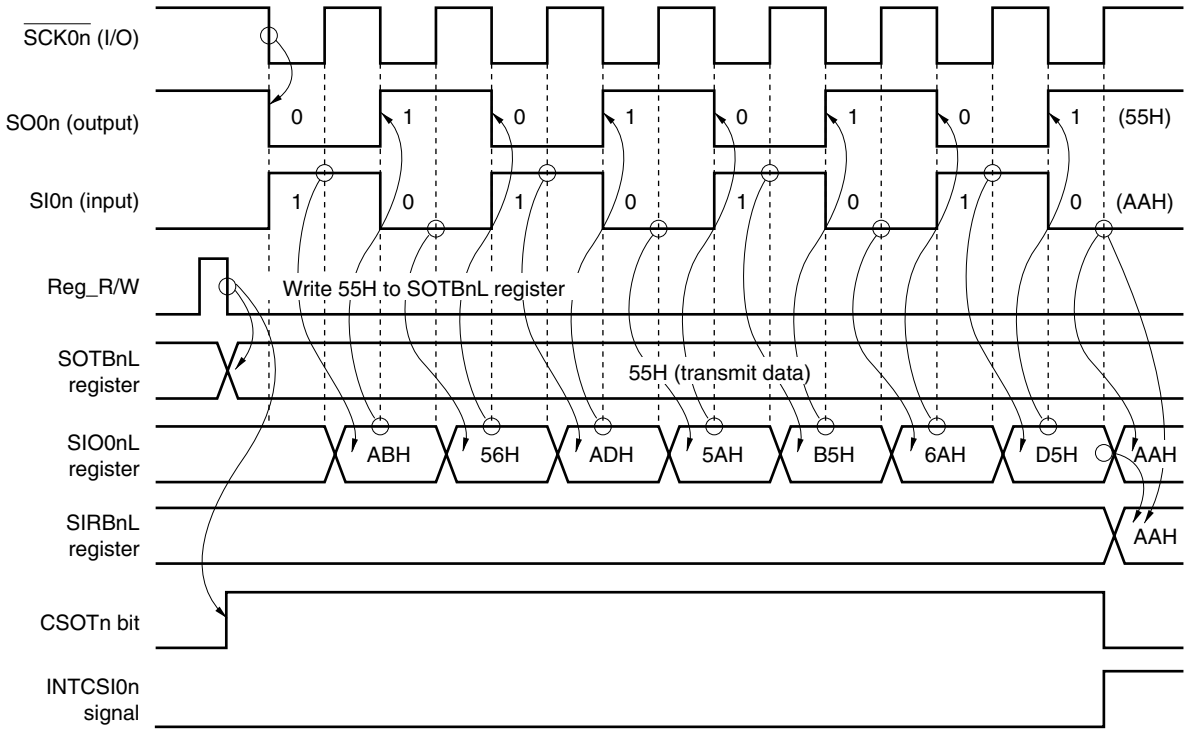
Upon communication completion, the transmission/reception completion interrupt request signal (INTCSI0n) is generated, and the CSOTn bit is cleared (0). The next data communication request is then waited for.

Caution When the CSOTn bit = 1, do not manipulate the CSI0n register.

Remark n = 0, 1

Figure 17-3. Timing Chart in Single Transfer Mode (1/2)

(a) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, when AAH is received and 55H is transmitted, transmit/receive type 1



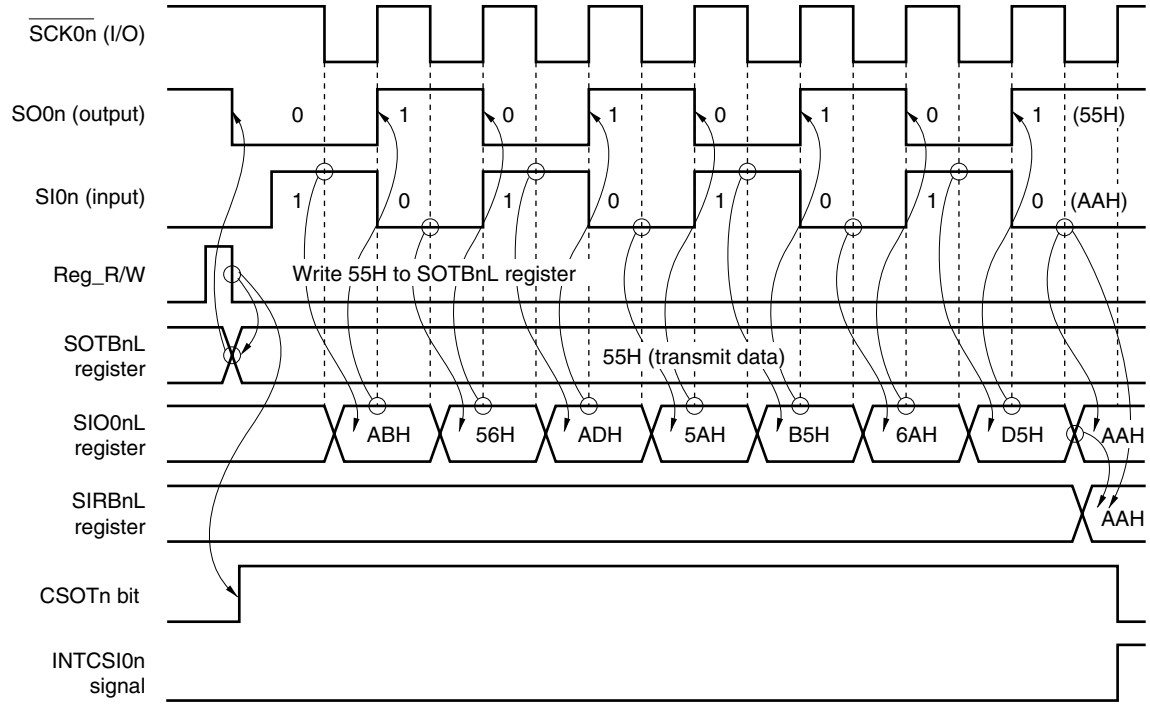
Remarks 1. Reg_R/W: Internal signal. This signal indicates that the SIRBn/SIRBnL register read or the SOTBn/SOTBnL register write was performed.

2. For the transmit/receive types, refer to **17.3 (2) Clocked serial interface clock selection register n (CSICn)**.

3. n = 0, 1

Figure 17-3. Timing Chart in Single Transfer Mode (2/2)

(b) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, when AAH is received and 55H is transmitted, transmit/receive type 2



Remarks 1. Reg_R/W: Internal signal. This signal indicates that the SIRBn/SIRBnL register read or the SOTBn/SOTBnL register write was performed.

2. For the transmit/receive types, refer to **17.3 (2) Clocked serial interface clock selection register n (CSICn)**.

3. n = 0, 1

17.4.3 Continuous transfer mode

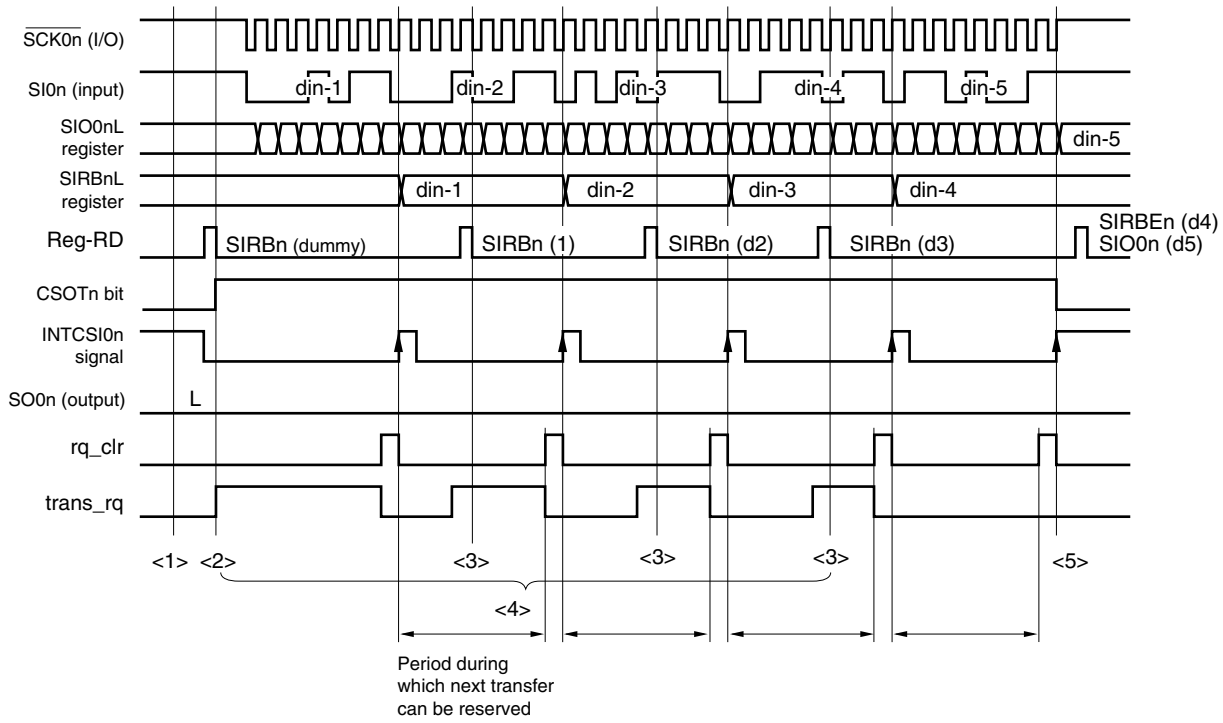
(1) Usage (receive-only: 8-bit data length)

<1> Set the continuous transfer mode (CSIM0n.AUTOn bit = 1) and the receive-only mode (CSIM0n.TRMDn bit = 0).
<2> Read the SIRBnL register (start transfer with dummy read).
<3> When the transmission/reception completion interrupt request signal (INTCSI0n) has been generated, read the SIRBnL register[Note] (reserve next transfer).
<4> Repeat step <3> (N – 2) times. (N: Number of transfer data)
Ignore the interrupt triggered by reception of the (N – 1)th data (at this time, the SIRBEnL register can be read).
<5> Following generation of the last INTCSI0n signal, read the SIRBEnL register and the SIO0nL register[Note].

Note When transferring N number of data, receive data is loaded by reading the SIRBnL register from the first data to the (N – 2)th data. The (N – 1)th data is loaded by reading the SIRBEnL register, and the Nth (last) data is loaded by reading the SIO0nL register (refer to **Table 17-1 Use of Each Buffer Register**).

Figure 17-4. Continuous Transfer (Receive-Only) Timing Chart

- Transmit/receive type 1, 8-bit data length



Remarks 1. Reg_RD: Internal signal. This signal indicates that the SIRBnL register has been read.
rq_clr: Internal signal. Transfer request clear signal.
trans_rq: Internal signal. Transfer request signal.

2. n = 0, 1

In the case of the continuous transfer mode, two transfer requests are set at the start of the first transfer. Following the INTCSI0n signal, transfer is continued if the SIRBnL register can be read within the next transfer reservation period. If the SIRBnL register cannot be read, transfer ends and the SIRBnL register does not receive the new value of the SIO0nL register.

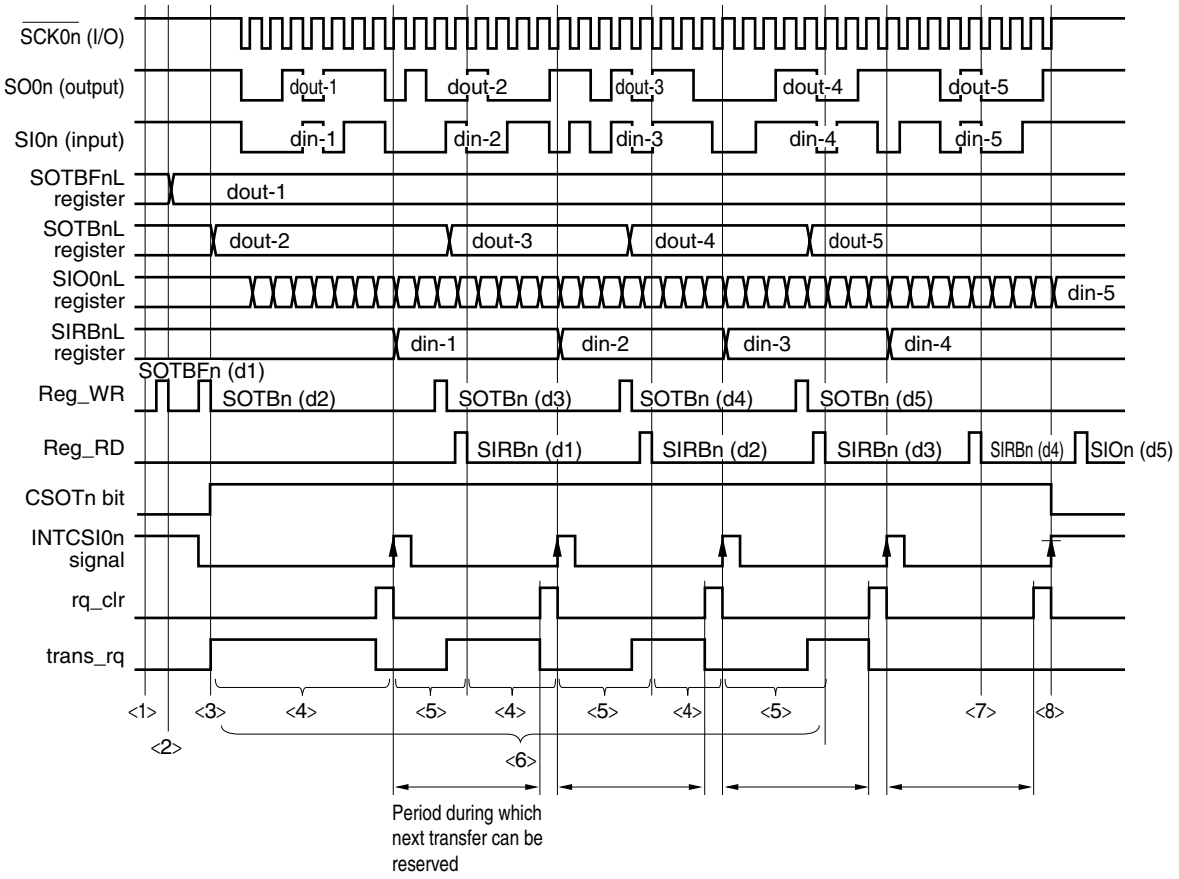
The last data can be obtained by reading the SIO0nL register following completion of the transfer.

(2) Usage (transmission/reception: 8-bit data length)

<1> Set the continuous transfer mode (CSIM0n.AUTOn bit = 1) and the transmission/reception mode (CSIM0n.TRMDn bit = 1).
<2> Write the first data to the SOTBFnL register.
<3> Write the 2nd data to the SOTBnL register (start transfer).
<4> When the transmission/reception completion interrupt request signal (INTCSI0n) has been generated, write the next data to the SOTBnL register (reserve next transfer). Read the SIRBnL register to load the receive data.
<5> Repeat step <4> as long as data to be sent remains.
<6> When the INTCSI0n signal is generated, read the SIRBnL register to load the (N − 1)th receive data (N: Number of transfer data).
<7> Following the last INTCSI0n signal, read the SIO0nL register to load the Nth (last) receive data.

Figure 17-5. Continuous Transfer (Transmission/Reception) Timing Chart

- Transmit/receive type 1, 8-bit data length



Remarks 1. Reg_WR: Internal signal. This signal indicates that the SOTBnL register has been written.
Reg_RD: Internal signal. This signal indicates that the SIRBnL register has been read.
rq_clr: Internal signal. Transfer request clear signal.
trans_rq: Internal signal. Transfer request signal.

2. n = 0, 1

In the case of the continuous transfer mode, two transfer requests are set at the start of the first transfer. Following the INTCSI0n signal, transfer is continued if the SOTBnL register can be written within the next transfer reservation period. If the SOTBnL register cannot be written, transfer ends and the SIRBnL register does not receive the new value of the SIO0nL register.

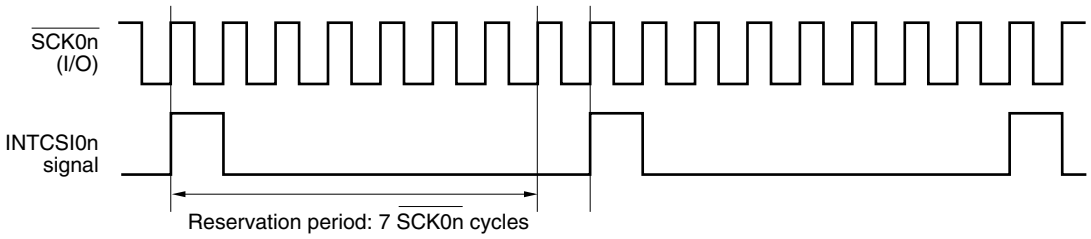
The last receive data can be obtained by reading the SIO0nL register following completion of the transfer.

(3) Next transfer reservation period

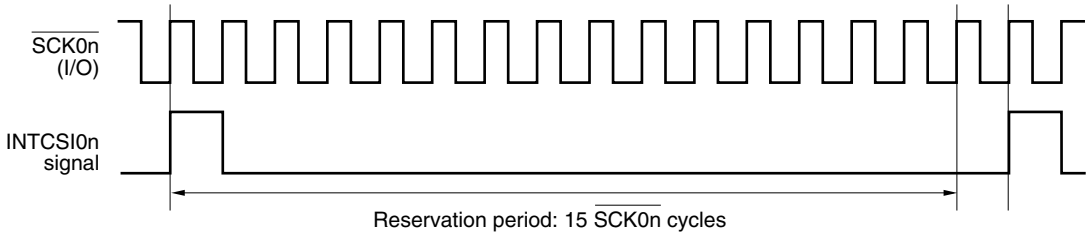
In the continuous transfer mode, the next transfer must be prepared with the period shown in Figure 17-6.

Figure 17-6. Timing Chart of Next Transfer Reservation Period (1/2)

(a) When data length: 8 bits, transmit/receive type 1



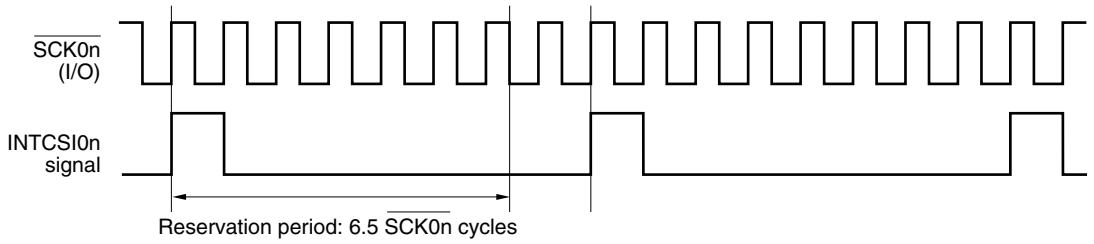
(b) When data length: 16 bits, transmit/receive type 1



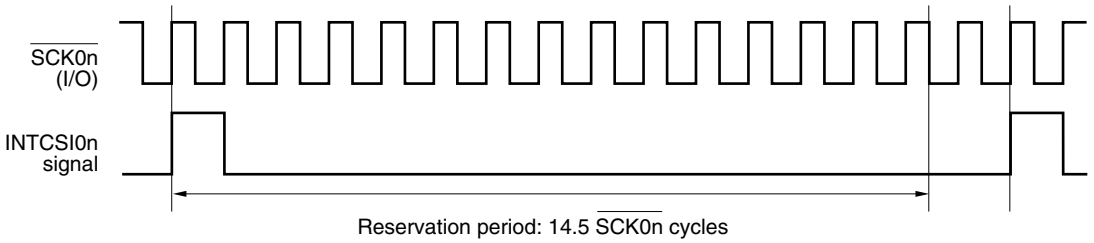
Remark n = 0, 1

Figure 17-6. Timing Chart of Next Transfer Reservation Period (2/2)

(c) When data length: 8 bits, transmit/receive type 2



(d) When data length: 16 bits, transmit/receive type 2



Remark n = 0, 1

(4) Cautions

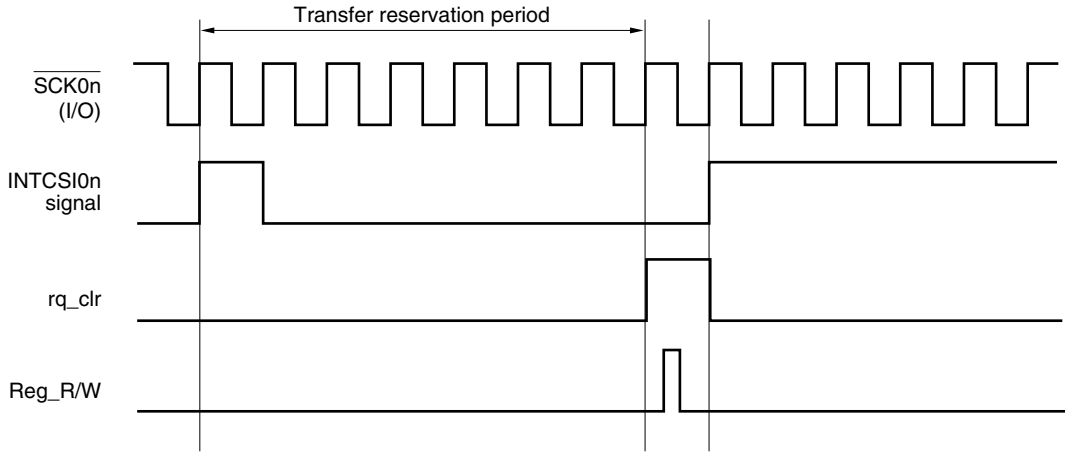
To continue continuous transfers, it is necessary to either read the SIRBn register or write to the SOTBn register during the transfer reservation period.

If access is performed to the SIRBn register or the SOTBn register when the transfer reservation period is over, the following occurs.

(i) In case of conflict between transfer request clear and register access

Since transfer request clear has higher priority, the next transfer request is ignored. Therefore, transfer is interrupted, and normal data transfer cannot be performed.

Figure 17-7. Transfer Request Clear and Register Access Conflict



Remarks 1. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that the SIRBn/SIRBnL register read or the SOTBn/SOTBnL register write was performed.

2. n = 0, 1

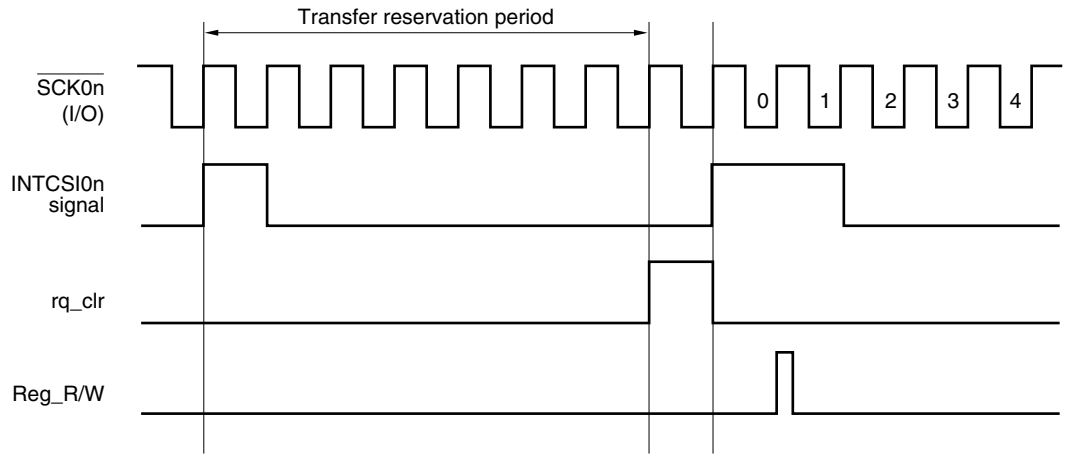
(ii) In case of conflict between transmission/reception completion interrupt request signal (INTCSI0n) generation and register access

Since continuous transfer has stopped once, executed as a new continuous transfer.

In the slave mode, a bit phase error transfer error results (refer to **Figure 17-8**).

In the transmission/reception mode, the value of the SOTBFn register is retransmitted, and illegal data is sent.

Figure 17-8. Interrupt Request and Register Access Conflict



Remarks 1. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that the SIRBn/SIRBnL register read or the SOTBn/SOTBnL register write was performed.

2. n = 0, 1

17.5 Output Pins

The following describes the output pins. For the setting of each pin, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

(1) $\overline{\text{SCK0n}}$ pin

When the CSI0n operation is disabled (CSIM0n.CSI0En bit = 0), the $\overline{\text{SCK0n}}$ pin output status is as follows.

Table 17-2. $\overline{\text{SCK0n}}$ Pin Output Status

CKPn	CKS0n2	CKS0n1	CKS0n0	$\overline{\text{SCK0n}}$ Pin Output
0	Don't care	Don't care	Don't care	Fixed to high level
1	1	1	1	High impedance
	Other than above			Fixed to low level

Remark n = 0, 1

(2) SO0n pin

When the CSI0n operation is disabled (CSI0En bit = 0), the SO0n pin output status is as follows.

Table 17-3. SO0n Pin Output Status

TRMDn	DAPn	AUTOn	CCLn	DIRn	SO0n Pin Output
0	Don't care	Don't care	Don't care	Don't care	Fixed to low level
1	0	Don't care	Don't care	Don't care	SO latch value (low level)
	1	0	0	0	SOTBn7 bit value
				1	SOTBn0 bit value
			1	0	SOTBn15 bit value
				1	SOTBn0 bit value
		1	0	0	SOTBFn7 bit value
				1	SOTBFn0 bit value
			1	0	SOTBFn15 bit value
				1	SOTBFn0 bit value

Remark n = 0, 1

CHAPTER 18 CLOCKED SERIAL INTERFACE A (CSIA) WITH AUTOMATIC TRANSMIT/RECEIVE FUNCTION

In the V850ES/KG2, two channels of clocked serial interface A (CSIA) with automatic transmit/receive function are provided.

18.1 Functions

CSIAn has the following two modes.

- 3-wire serial I/O mode
- 3-wire serial I/O mode with automatic transmit/receive function

(1) 3-wire serial I/O mode

This mode is used to transfer 8-bit data using three lines: a serial clock pin ($\overline{\text{SCKAn}}$) and two serial data pins (SIAn and SOAn).

In addition, whether 8-bit data is transferred MSB or LSB first can be specified, so this interface can be connected to any device.

(2) 3-wire serial I/O mode with automatic transmit/receive function

This mode is used to transfer 8-bit data using three lines: a serial clock pin ($\overline{\text{SCKAn}}$) and two serial data pins (SIAn and SOAn).

In addition, whether 8-bit data is transferred MSB or LSB first can be specified, so this interface can be connected to any device.

Data can be transferred to/from a display driver etc. without using software since a 32-byte buffer RAM is incorporated for automatic transfer.

- Maximum transfer speed: 2 Mbps (in master mode)
- Master mode/slave mode selectable
- Transfer data length: 8 bits
- MSB/LSB-first selectable for transfer data
- Automatic transmit/receive function:
  Number of transfer bytes can be specified between 1 and 32
  Transfer interval can be specified (0 to 63 clocks)
  Single transfer/repeat transfer selectable
- On-chip dedicated baud rate generator (6/8/16/32 divisions)
- 3-wire SOAn: Serial data output
  SIAn: Serial data input
  $\overline{\text{SCKAn}}$: Serial clock I/O
- Transmission/reception completion interrupt request signal: INTCSIAn
- Internal 32-byte buffer RAM (used in 3-wire serial I/O mode with automatic transmit/receive function)

Remark n = 0, 1

18.2 Configuration

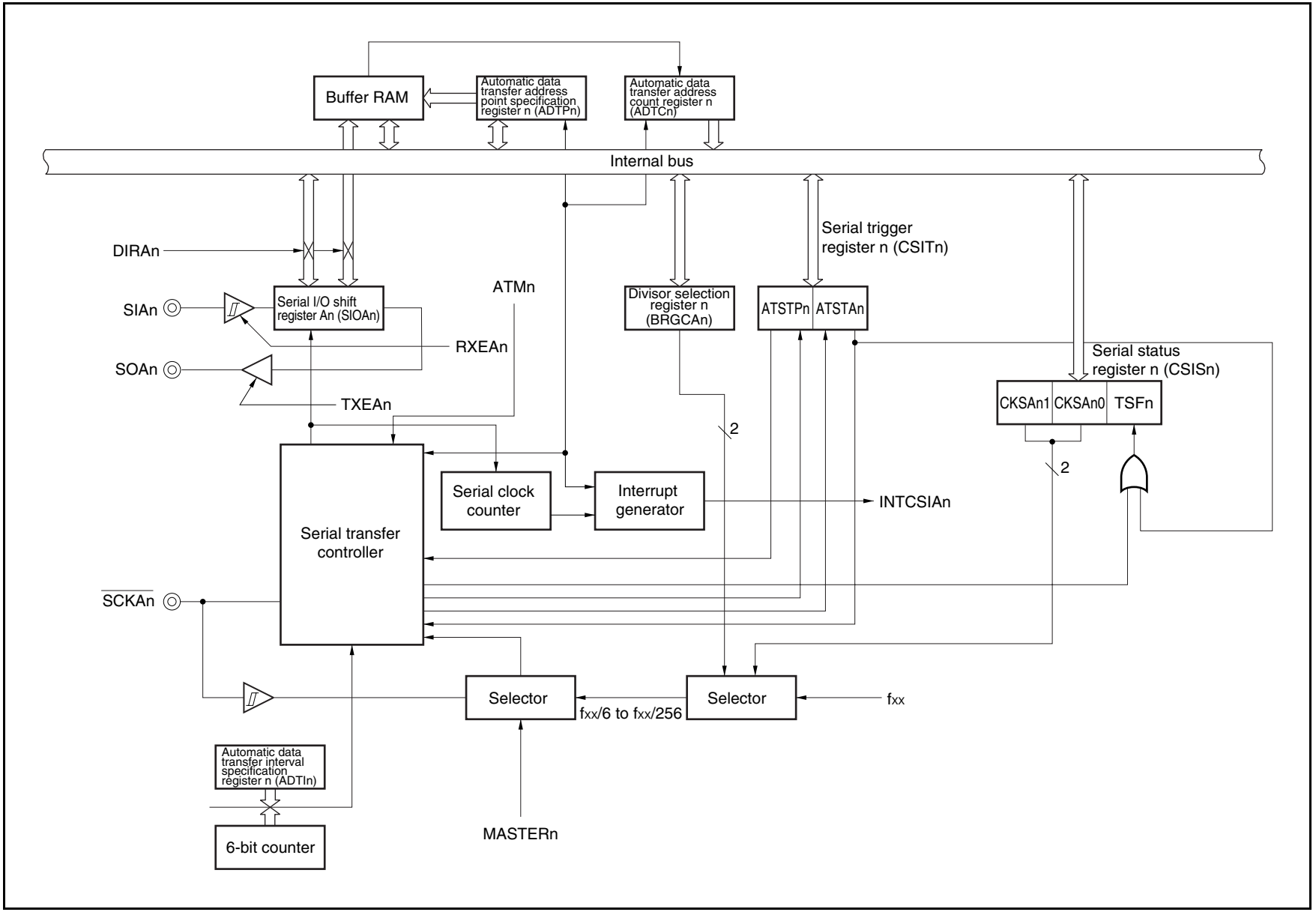
CSIAn includes the following hardware.

Table 18-1. Configuration of CSIAn

Item	Configuration
Register	Serial I/O shift register An (SIOAn) Automatic data transfer address count register n (ADTCn) CSIAn buffer RAM (CSIAnBm, CSIAnBmL, CSIAnBmH) (m = 0 to F)
Control registers	Serial operation mode specification register n (CSIMAn) Serial status register n (CSISn) Serial trigger register n (CSITn) Divisor selection register n (BRGCAn) Automatic data transfer address point specification register n (ADTPn) Automatic data transfer interval specification register n (ADTIn)

Remark For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

Figure 18-1. Block Diagram of CSIAn



(2) Serial status register n (CSISn)

This is an 8-bit register used to select the serial clock and to indicate the transfer status of CSIAn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H. However, rewriting the CSISn register is prohibited when the TSFn bit is 1.

After reset: 00H R/W Address: CSIS0 FFFFFD41H, CSIS1 FFFFD51H

CSISn (n = 0, 1)

7	6	5	4	3	2	1	0
CKSAn1	CKSAn0	0	0	0	0	0	TSFn

CKSAn1	CKSAn0	Serial clock (f_{SCKA}) selection[Note]			
			20 MHz	16 MHz	10 MHz
0	0	fxx	Setting prohibited	Setting prohibited	100 ns
0	1	fxx/2	100 ns	125 ns	200 ns
1	0	fxx/4	200 ns	250 ns	400 ns
1	1	fxx/8	400 ns	500 ns	800 ns
Rewriting CSISn is prohibited when the CSIMAn.CSIAEn bit is 1.					

TSFn	Transfer status
0	CSIAEn bit = 0 At reset input At completion of specified transfer When transfer has been suspended by setting the CSITn.ATSTPn bit to 1
1	From transfer start to completion of specified transfer

Note Set f_{SCKA} so as to satisfy the following conditions.

- REGC = V_{DD} = 4.0 to 5.5 V: $f_{SCKA} \leq$ 12 MHz
- REGC = 10 μF, V_{DD} = 4.0 to 5.5 V: $f_{SCKA} \leq$ 6 MHz
- REGC = V_{DD} = 2.7 to 4.0 V: $f_{SCKA} \leq$ 6 MHz

Cautions 1. The TSFn bit is read-only.

2. When the TSFn bit = 1, rewriting the CSIMAn, CSISn, BRGCAn, ADTPn, ADTIn, and SIOAn registers is prohibited. However, the transfer buffer RAM can be rewritten.

3. Be sure to clear bits 1 to 5 to "0".

(1) Serial I/O shift register An (SIOAn)

This is an 8-bit register used to store transmit/receive data in 1-byte transfer mode (CSIMAn.ATEn bit = 0). Writing transmit data to the SIOAn register starts the transfer. In addition, after a transfer completion interrupt request signal (INTCSIAn) is generated (CSISn.TSFn bit = 0), data can be received by reading data from the SIOAn register.

This register can be read or written in 8-bit units. However, writing to the SIOAn register is prohibited when the CSISn.TSFn bit = 1.

Reset sets this register to 00H.

Cautions 1. A transfer operation is started by writing to SIOAn register. Consequently, when transmission is disabled (CSIMAn.TXEAn bit = 0), write dummy data to the SIOAn register to start the transfer operation, and then perform a receive operation.

2. Do not write data to the SIOAn register while the automatic transmit/receive function is operating.

After reset: 00H R/W Address: SIOA0 FFFFFD46H, SIOA1 FFFFFD56H

	7	6	5	4	3	2	1	0
SIOAn	SIOAn7	SIOAn6	SIOAn5	SIOAn4	SIOAn3	SIOAn2	SIOAn1	SIOAn0

(n = 0, 1)

(2) Automatic data transfer address count register n (ADTCn)

This is a register used to indicate buffer RAM addresses during automatic transfer. When automatic transfer is stopped, the data position when transfer stopped can be ascertained by reading ADTCn register value.

This register is read-only in 8-bit units. However, reading from the ADTCn register is prohibited when the CSISn.TSFn bit = 1.

Reset sets this register to 00H.

After reset: 00H R Address: ADTC0 FFFFFD47H, ADTC1 FFFFD57H

	7	6	5	4	3	2	1	0
ADTCn	ADTCn7	ADTCn6	ADTCn5	ADTCn4	ADTCn3	ADTCn2	ADTCn1	ADTCn0

(n = 0, 1)

18.3 Registers

Serial interface CSIAn is controlled by the following six registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Serial trigger register n (CSITn)
- Divisor selection register n (BRGCAn)
- Automatic data transfer address point specification register n (ADTPn)
- Automatic data transfer interval specification register n (ADTIn)

(1) Serial operation mode specification register n (CSIMAn)

This is an 8-bit register used to control the serial transfer operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: CSIMA0 FFFFFD40H, CSIMA1 FFFFD50H

	<7>	6	5	4	<3>	<2>	<1>	0
CSIMAn	CSIAEn	ATEn	ATMn	MASTERn	TXEAn	RXEAn	DIRAn	0

(n = 0, 1)

CSIAEn	CSIAn operation enable/disable control
0	Disable CSIAn operation (SOAn: Low level, $\overline{\text{SCKAn}}$: High level)
1	Enable CSIAn operation

- When the CSIAEn bit is cleared to 0, the CSIAn unit is reset[Note] asynchronously.
- When the CSIAEn bit = 0, the CSIAn unit is reset, so to operate CSIAn, first set the CSIAEn bit to 1.
- If the CSIAEn bit is cleared from 1 to 0, all the registers in the CSIAn unit are initialized. Before the CSIAEn bit is set to 1 again, first re-set the registers of the CSIAn unit.
- If the CSIAEn bit is cleared from 1 to 0, the buffer RAM value is not held. Also, when the CSIAEn bit = 0, the buffer RAM cannot be accessed.

ATEn	Automatic transfer operation enable/disable control
0	1-byte transfer mode
1	Automatic transfer mode

ATMn	Specification of automatic transfer mode
0	Single transfer mode (stops at address specified with ADTPn register)
1	Repeat transfer mode (Following transfer completion, the ADTCn register is cleared to 00H and transmission starts again.)

MASTERn	Specification of CSIAn master/slave mode
0	Slave mode (synchronized with $\overline{\text{SCKAn}}$ input clock)
1	Master mode (synchronized with internal clock)

TXEAn	Transmission enable/disable control
0	Disable transmission (SOAn: Low level)
1	Enable transmission

RXEAn	Reception enable/disable control
0	Disable reception
1	Enable reception

DIRAn	Specification of transfer data direction
0	MSB first
1	LSB first

Note The ADTCn, CSITn, and SIOAn registers and the CSIS.TSFn bit are reset.

(3) Serial trigger register n (CSITn)

The CSITn register between the buffer RAM and shift register is an 8-bit register used to control execution/stop of automatic data transfer.

This register can be read or written in 8-bit or 1-bit units. However, manipulate only when the CSIMAn.ATEn bit is 1 (manipulation prohibited when ATEn bit = 0).

Reset sets this register to 00H.

After reset: 00H R/W Address: CSIT0 FFFFFD42H, CSIT1 FFFFD52H

	7	6	5	4	3	2	<1>	<0>
CSITn	0	0	0	0	0	0	ATSTPn	ATSTAn

(n = 0, 1)

ATSTPn	Automatic data transfer suspension
0	–
1	Stop automatic data transfer

Even when the ATSTPn bit is set to 1, transfer does not stop until 1 byte has been transferred.
1 is held until immediately before the transmission/reception completion interrupt request signal (INTCSIAn) is generated, and ATSTPn is automatically cleared to 0 after that.
After automatic transfer has been suspended, the data address at the point of suspension is stored in the ADTCn register.
A function to resume automatic data transfer is not provided, so if transfer has been interrupted by setting the ATSTPn bit to 1, set each register again, and set the ATSTAn bit to 1 to start automatic data transfer.

ATSTAn	Automatic data transfer start
0	–
1	Start automatic data transfer

Even when the ATSTAn bit is set to 1, automatic data transfer does not start until 1 byte has been transferred.
1 is held until immediately before the INTCSIAn signal is generated, and ATSTAn is automatically cleared to 0 after that.

(4) Divisor selection register n (BRGCAn)

This is an 8-bit register used to control the serial transfer speed (divisor of CSIA clock).

This register can be read or written in 8-bit units. However, when the CSISn.TSFn bit is 1, rewriting the BRGCAn register is prohibited.

Reset sets this register to 03H.

After reset: 03H R/W Address: BRGCA0 FFFFFD43H, BRGCA1 FFFFD53H

BRGCAn (n = 0, 1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	BRGCn1	BRGCn0

BRGCn1	BRGCn0	Selection of CSIAn serial clock (f_{SCKA} division ratio)
0	0	6 (f_{SCKA}/6)
0	1	8 (f_{SCKA}/8)
1	0	16 (f_{SCKA}/16)
1	1	32 (f_{SCKA}/32)

(5) Automatic data transfer address point specification register n (ADTPn)

This is an 8-bit register used to specify the buffer RAM address that ends transfer during automatic data transfer (CSIMAn.ATEn bit = 1).

This register can be read or written in 8-bit units. However, when the CSISn.TSFn bit is 1, rewriting the ADTPn register is prohibited.

Reset sets this register to 00H.

In the V850ES/KG2, 00H to 1FH can be specified because 32 bytes of buffer RAM are incorporated.

Example When the ADTP0 register is set to 07H
8 bytes of FFFFFE00H to FFFFFE07H are transferred.

In repeat transfer mode (CSIMAn.ATMn bit = 1), transfer is performed repeatedly up to the address value specified by ADTPn.

Example When the ADTP0 register is set to 07H (repeat transfer mode)
Transfer is repeated as FFFFFE00H to FFFFFE07H, … .

After reset: 00H R/W Address: ADTP0 FFFFFD44H, ADTP1 FFFFD54H

ADTPn (n = 0, 1)

7	6	5	4	3	2	1	0
0	0	0	ADTPn4	ADTPn3	ADTPn2	ADTPn1	ADTPn0

Caution Be sure to clear bits 5 to 7 to "0".

The relationship between buffer RAM address values and the ADTPn register setting values is shown below.

Table 18-2. Relationship Between Buffer RAM Address Values and ADTP0 Register Setting Values

Buffer RAM Address Value	ADTP0 Register Setting Value	Buffer RAM Address Value	ADTP0 Register Setting Value
FFFFFE00H	00H	FFFFFE10H	10H
FFFFFE01H	01H	FFFFFE11H	11H
FFFFFE02H	02H	FFFFFE12H	12H
FFFFFE03H	03H	FFFFFE13H	13H
FFFFFE04H	04H	FFFFFE14H	14H
FFFFFE05H	05H	FFFFFE15H	15H
FFFFFE06H	06H	FFFFFE16H	16H
FFFFFE07H	07H	FFFFFE17H	17H
FFFFFE08H	08H	FFFFFE18H	18H
FFFFFE09H	09H	FFFFFE19H	19H
FFFFFE0AH	0AH	FFFFFE1AH	1AH
FFFFFE0BH	0BH	FFFFFE1BH	1BH
FFFFFE0CH	0CH	FFFFFE1CH	1CH
FFFFFE0DH	0DH	FFFFFE1DH	1DH
FFFFFE0EH	0EH	FFFFFE1EH	1EH
FFFFFE0FH	0FH	FFFFFE1FH	1FH

Table 18-3. Relationship Between Buffer RAM Address Values and ADTP1 Register Setting Values

Buffer RAM Address Value	ADTP1 Register Setting Value	Buffer RAM Address Value	ADTP1 Register Setting Value
FFFFFE20H	00H	FFFFFE30H	10H
FFFFFE21H	01H	FFFFFE31H	11H
FFFFFE22H	02H	FFFFFE32H	12H
FFFFFE23H	03H	FFFFFE33H	13H
FFFFFE24H	04H	FFFFFE34H	14H
FFFFFE25H	05H	FFFFFE35H	15H
FFFFFE26H	06H	FFFFFE36H	16H
FFFFFE27H	07H	FFFFFE37H	17H
FFFFFE28H	08H	FFFFFE38H	18H
FFFFFE29H	09H	FFFFFE39H	19H
FFFFFE2AH	0AH	FFFFFE3AH	1AH
FFFFFE2BH	0BH	FFFFFE3BH	1BH
FFFFFE2CH	0CH	FFFFFE3CH	1CH
FFFFFE2DH	0DH	FFFFFE3DH	1DH
FFFFFE2EH	0EH	FFFFFE3EH	1EH
FFFFFE2FH	0FH	FFFFFE3FH	1FH

(6) Automatic data transfer interval specification register n (ADTIn)

This is an 8-bit register used to specify the interval period between 1-byte transfers during automatic data transfer (CSIMAn.ATEn bit = 1).

Set this register when in master mode (CSIMAn.MASTERn bit = 1) (setting is unnecessary in slave mode). Setting in 1-byte transfer mode (ATEn bit = 0) is also valid. When the interval time specified by the ADTIn register after the end of 1-byte transfer has elapsed, a transmission/reception completion interrupt request signal (INTCSIAn) is output. The number of clocks for the interval can be set to between 0 and 63 clocks.

This register can be read or written in 8-bit units. However, when the CSISn.TSFn bit is 1, rewriting the ADTIn register is prohibited.

Reset sets this register to 00H.

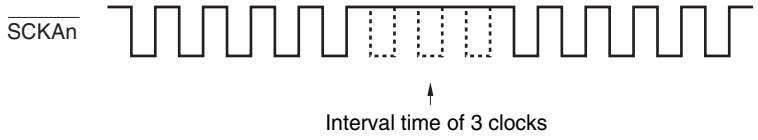
After reset: 00H R/W Address: ADTI0 FFFFFD45H, ADTI1 FFFFD55H

	7	6	5	4	3	2	1	0
ADTIn	0	0	ADTIn5	ADTIn4	ADTIn3	ADTIn2	ADTIn1	ADTIn0

(n = 0, 1)

The specified interval time is the transfer clock (specified by the BRGCAn register) multiplied by an integer value.

Example When ADTIn register = 03H



(7) CSIAn buffer RAM (CSIAnBm)

This area holds transmit/receive data (up to 32 bytes) in automatic transfer mode in 1-byte units.

This register can be read or written in 16-bit units. However, when the higher 8 bits and the lower 8 bits of the CSIAnBm register are used as the CSIAnBmH register and CSIAnBmL register, respectively, these registers can be read or written in 8-bit units.

After automatic transfer is started, only data equal to one byte more than the number of bytes stored in the ADTPn register is transmitted/received in sequence from the CSIAmB0L register.

Cautions 1. To read the value of the CSIAnBm register after data is written to the register, wait for the duration of more than six clocks of f_{SCKA} (serial clock set by the CSISn.CKSAn1 and CSISn.CKSAn0 bits) or until data is written to the buffer RAM at another address.

2. When the main clock stops and the CPU operates on the subclock, do not access the CSIAnBm register.

For details, refer to 3.4.8 (1) (b).

Remark n = 0, 1

m = 0 to F

Table 18-4. CSIA0 Buffer RAM

Address	Symbol	R/W	Manipulatable Bits		After Reset
			8	16	
FFFFFE00H	CSIA0B0	R/W		√	Undefined
FFFFFE00H	CSIA0B0L	R/W	√		Undefined
FFFFFE01H	CSIA0B0H	R/W	√		Undefined
FFFFFE02H	CSIA0B1	R/W		√	Undefined
FFFFFE02H	CSIA0B1L	R/W	√		Undefined
FFFFFE03H	CSIA0B1H	R/W	√		Undefined
FFFFFE04H	CSIA0B2	R/W		√	Undefined
FFFFFE04H	CSIA0B2L	R/W	√		Undefined
FFFFFE05H	CSIA0B2H	R/W	√		Undefined
FFFFFE06H	CSIA0B3	R/W		√	Undefined
FFFFFE06H	CSIA0B3L	R/W	√		Undefined
FFFFFE07H	CSIA0B3H	R/W	√		Undefined
FFFFFE08H	CSIA0B4	R/W		√	Undefined
FFFFFE08H	CSIA0B4L	R/W	√		Undefined
FFFFFE09H	CSIA0B4H	R/W	√		Undefined
FFFFFE0AH	CSIA0B5	R/W		√	Undefined
FFFFFE0AH	CSIA0B5L	R/W	√		Undefined
FFFFFE0BH	CSIA0B5H	R/W	√		Undefined
FFFFFE0CH	CSIA0B6	R/W		√	Undefined
FFFFFE0CH	CSIA0B6L	R/W	√		Undefined
FFFFFE0DH	CSIA0B6H	R/W	√		Undefined
FFFFFE0EH	CSIA0B7	R/W		√	Undefined
FFFFFE0EH	CSIA0B7L	R/W	√		Undefined
FFFFFE0FH	CSIA0B7H	R/W	√		Undefined
FFFFFE10H	CSIA0B8	R/W		√	Undefined
FFFFFE10H	CSIA0B8L	R/W	√		Undefined
FFFFFE11H	CSIA0B8H	R/W	√		Undefined
FFFFFE12H	CSIA0B9	R/W		√	Undefined
FFFFFE12H	CSIA0B9L	R/W	√		Undefined
FFFFFE13H	CSIA0B9H	R/W	√		Undefined
FFFFFE14H	CSIA0BA	R/W		√	Undefined
FFFFFE14H	CSIA0BAL	R/W	√		Undefined
FFFFFE15H	CSIA0BAH	R/W	√		Undefined
FFFFFE16H	CSIA0BB	R/W		√	Undefined
FFFFFE16H	CSIA0BBL	R/W	√		Undefined
FFFFFE17H	CSIA0BBH	R/W	√		Undefined
FFFFFE18H	CSIA0BC	R/W		√	Undefined
FFFFFE18H	CSIA0BCL	R/W	√		Undefined
FFFFFE19H	CSIA0BCH	R/W	√		Undefined
FFFFFE1AH	CSIA0BD	R/W		√	Undefined
FFFFFE1AH	CSIA0BDL	R/W	√		Undefined
FFFFFE1BH	CSIA0BDH	R/W	√		Undefined
FFFFFE1CH	CSIA0BE	R/W		√	Undefined
FFFFFE1CH	CSIA0BEL	R/W	√		Undefined
FFFFFE1DH	CSIA0BEH	R/W	√		Undefined
FFFFFE1EH	CSIA0BF	R/W		√	Undefined
FFFFFE1EH	CSIA0BFL	R/W	√		Undefined
FFFFFE1FH	CSIA0BFH	R/W	√		Undefined

Table 18-5. CSIA1 Buffer RAM

Address	Symbol	R/W	Manipulatable Bits		After Reset
			8	16	
FFFFFE20H	CSIA1B0	R/W		√	Undefined
FFFFFE20H	CSIA1B0L	R/W	√		Undefined
FFFFFE21H	CSIA1B0H	R/W	√		Undefined
FFFFFE22H	CSIA1B1	R/W		√	Undefined
FFFFFE22H	CSIA1B1L	R/W	√		Undefined
FFFFFE23H	CSIA1B1H	R/W	√		Undefined
FFFFFE24H	CSIA1B2	R/W		√	Undefined
FFFFFE24H	CSIA1B2L	R/W	√		Undefined
FFFFFE25H	CSIA1B2H	R/W	√		Undefined
FFFFFE26H	CSIA1B3	R/W		√	Undefined
FFFFFE26H	CSIA1B3L	R/W	√		Undefined
FFFFFE27H	CSIA1B3H	R/W	√		Undefined
FFFFFE28H	CSIA1B4	R/W		√	Undefined
FFFFFE28H	CSIA1B4L	R/W	√		Undefined
FFFFFE29H	CSIA1B4H	R/W	√		Undefined
FFFFFE2AH	CSIA1B5	R/W		√	Undefined
FFFFFE2AH	CSIA1B5L	R/W	√		Undefined
FFFFFE2BH	CSIA1B5H	R/W	√		Undefined
FFFFFE2CH	CSIA1B6	R/W		√	Undefined
FFFFFE2CH	CSIA1B6L	R/W	√		Undefined
FFFFFE2DH	CSIA1B6H	R/W	√		Undefined
FFFFFE2EH	CSIA1B7	R/W		√	Undefined
FFFFFE2EH	CSIA1B7L	R/W	√		Undefined
FFFFFE2FH	CSIA1B7H	R/W	√		Undefined
FFFFFE30H	CSIA1B8	R/W		√	Undefined
FFFFFE30H	CSIA1B8L	R/W	√		Undefined
FFFFFE31H	CSIA1B8H	R/W	√		Undefined
FFFFFE32H	CSIA1B9	R/W		√	Undefined
FFFFFE32H	CSIA1B9L	R/W	√		Undefined
FFFFFE33H	CSIA1B9H	R/W	√		Undefined
FFFFFE34H	CSIA1BA	R/W		√	Undefined
FFFFFE34H	CSIA1BAL	R/W	√		Undefined
FFFFFE35H	CSIA1BAH	R/W	√		Undefined
FFFFFE36H	CSIA1BB	R/W		√	Undefined
FFFFFE36H	CSIA1BBL	R/W	√		Undefined
FFFFFE37H	CSIA1BBH	R/W	√		Undefined
FFFFFE38H	CSIA1BC	R/W		√	Undefined
FFFFFE38H	CSIA1BCL	R/W	√		Undefined
FFFFFE39H	CSIA1BCH	R/W	√		Undefined
FFFFFE3AH	CSIA1BD	R/W		√	Undefined
FFFFFE3AH	CSIA1BDL	R/W	√		Undefined
FFFFFE3BH	CSIA1BDH	R/W	√		Undefined
FFFFFE3CH	CSIA1BE	R/W		√	Undefined
FFFFFE3CH	CSIA1BEL	R/W	√		Undefined
FFFFFE3DH	CSIA1BEH	R/W	√		Undefined
FFFFFE3EH	CSIA1BF	R/W		√	Undefined
FFFFFE3EH	CSIA1BFL	R/W	√		Undefined
FFFFFE3FH	CSIA1BFH	R/W	√		Undefined

18.4 Operation

CSIAn can be used in the following two modes.

- 3-wire serial I/O mode
- 3-wire serial I/O mode with automatic transmit/receive function

18.4.1 3-wire serial I/O mode

The one-byte data transmission/reception is executed in the mode in which the CSIMAn.ATEn bit is cleared to 0.

In this mode, communication is executed by using three lines: serial clock ($\overline{\text{SCKAn}}$), serial data output (SOAn), and serial data input (SIAn) pins.

The 3-wire serial I/O mode is controlled by the following three registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Divisor selection register n (BRGCAn)

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. n = 0, 1

(1) 1-byte transmission/reception communication operation

(a) 1-byte transmission/reception

When the CSIMAn.CSIAEn bit and the CSIMAn.ATEn bit = 1, 0, respectively, if transfer data is written to the SIOAn register, the data is output via the SOA0 pin in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge, and then input via the SIAn pin in synchronization with the falling edge of the $\overline{\text{SCKAn}}$ pin, and stored in the SIOAn register in synchronization with the rising edge 1 clock later.

Data transmission and data reception can be performed simultaneously.

If only reception is to be performed, transfer can only be started by writing a dummy value to the SIOAn register.

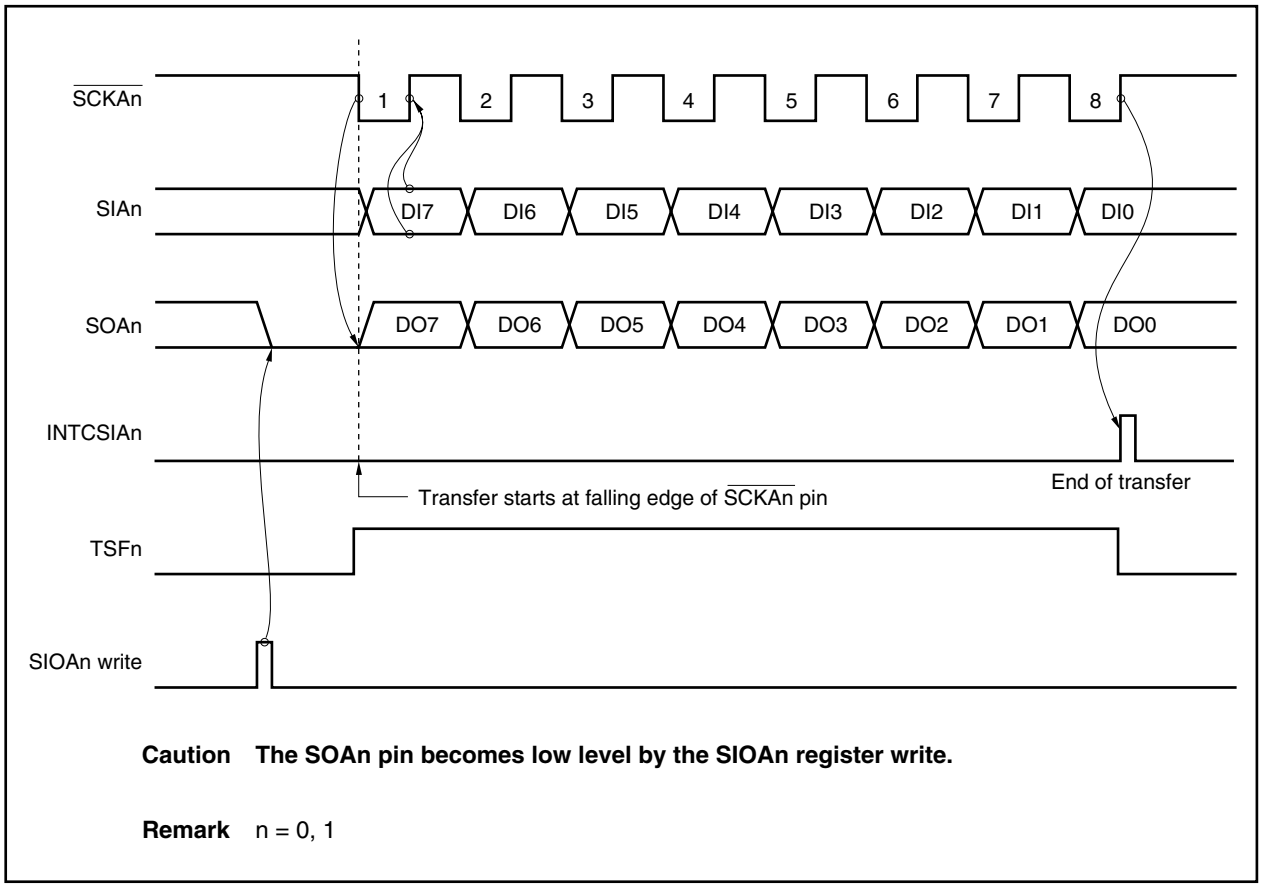
When transfer of 1 byte is complete, a transmission/reception completion interrupt request signal (INTCSIAn) is generated.

In 1-byte transmission/reception, the setting of the CSIMAn.ATMn bit is invalid.

Be sure to read data after confirming that the CSISn.TSFn bit = 0.

Caution Determine the setting procedure of alternate-function pins considering the relationship with the communication partner.

Figure 18-2. 3-Wire Serial I/O Mode Timing



Caution The SOAn pin becomes low level by the SIOAn register write.

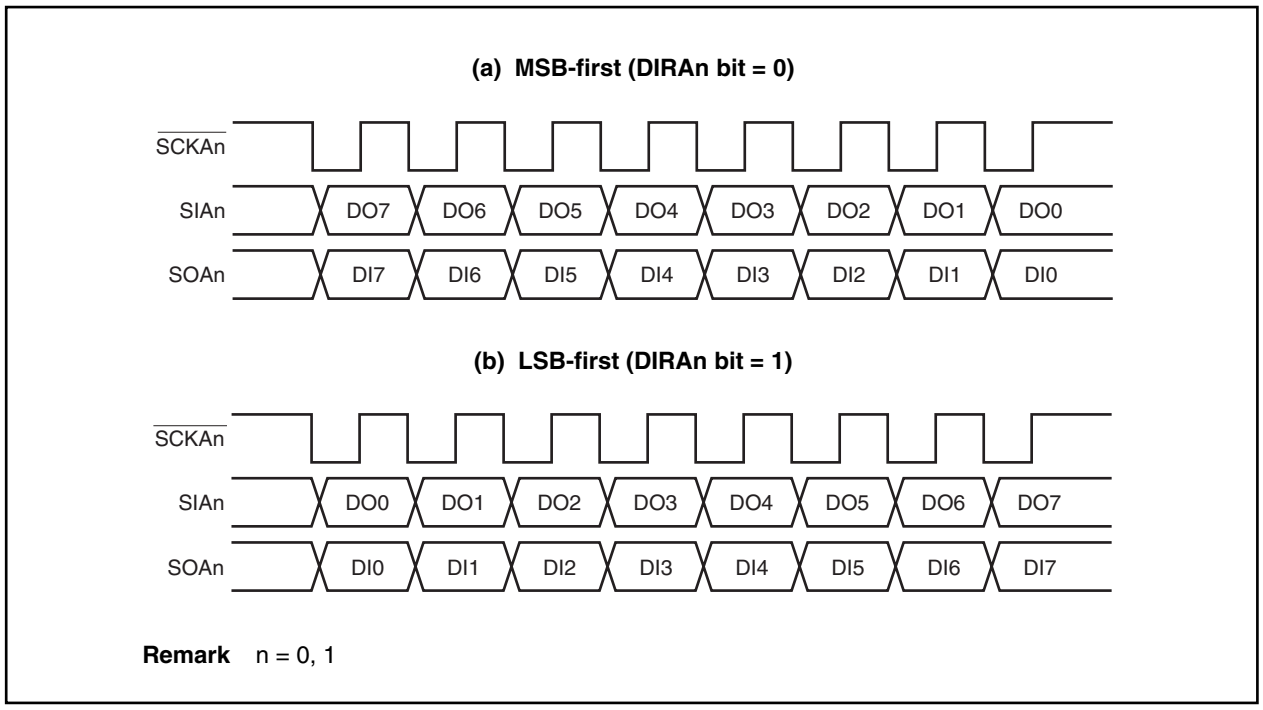
Remark n = 0, 1

(b) Data format

In the data format, data is changed in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge as shown in Figure 18-3.

The data length is fixed to 8 bits and the data transfer direction can be switched by the specification of the CSIMAn.DIRAn bit.

Figure 18-3. Format of Transmit/Receive Data



Remark n = 0, 1

(c) Switching MSB/LSB as start bit

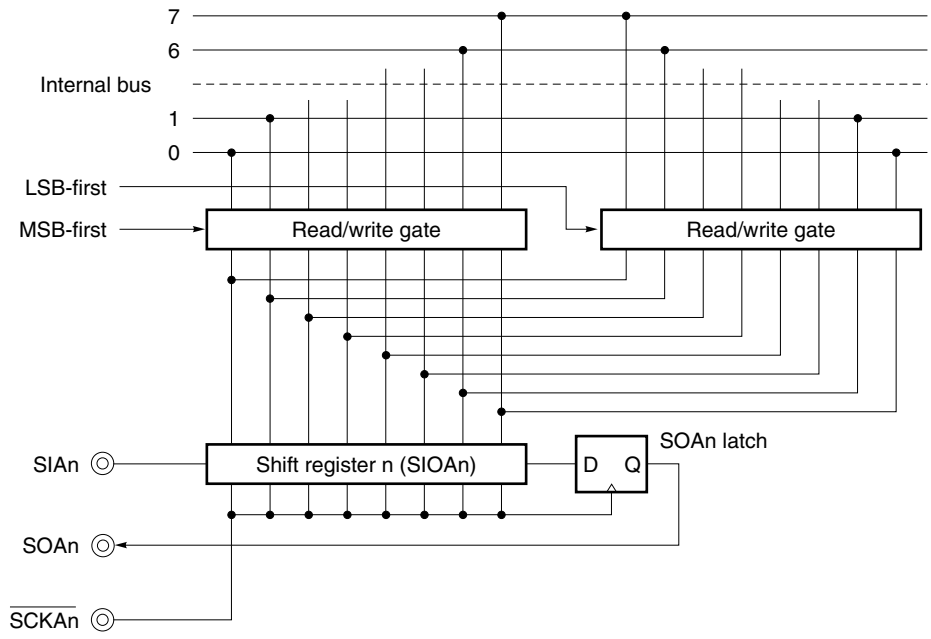
Figure 18-4 shows the configuration of the SIOAn register and the internal bus. As shown in the figure, MSB/LSB can be read or written in reverse form.

Switching MSB/LSB as the start bit can be specified using the CSIMAn.DIRAn bit.

Start bit switching is realized by switching the bit order for data written to the SIOAn register. The SIOAn register shift order remains unchanged.

Thus, switching between MSB-first and LSB-first must be performed before writing data to the SIOAn register.

Figure 18-4. Transfer Bit Order Switching Circuit



Remark n = 0, 1

(d) Transfer start

Serial transfer is started by setting transfer data to the SIOAn register when the following two conditions are satisfied.

- CSIAn operation control bit (CSIMAn.CSIAEn) = 1
- Other than during serial communication

Caution If the CSIAEn bit is set to 1 after data is written to the SIOAn register, communication does not start.

Upon termination of 8-bit communication, serial communication automatically stops and the transmission/reception completion interrupt request signal (INTCSIAn) is generated.

Remark n = 0, 1

18.4.2 3-wire serial I/O mode with automatic transmit/receive function

Up to 32 bytes of data can be transmitted/received without using software in the mode in which the CSIMAn.ATEn bit is set to 1. After communication is started, only data of the set number of bytes stored in RAM in advance can be transmitted, and only data of the set number of bytes can be received and stored in RAM.

The 3-wire serial I/O mode with automatic transmit/receive function is controlled by the following registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Serial trigger register n (CSITn)
- Divisor selection register n (BRGCAn)
- Automatic data transfer address point specification register n (ADTPn)
- Automatic data transfer interval specification register n (ADTIn)

Remarks 1. For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

2. n = 0, 1

(1) Automatic transmit/receive data setting

(a) Transmit data setting

<1> Write transmit data from the least significant address FFFFFE00H/FFFFFE20H of buffer RAM (up to FFFFFE1FH/FFFFFE3FH at maximum). The transmit data should be in the order from lower address to higher address.

<2> Set the ADTPn register to the value obtained by subtracting 1 from the number of transmit data bytes.

(b) Automatic transmission/reception mode setting

<1> Set the CSIMAn.CSIAEn bit and the CSIMAn.ATEn bit to 11.

<2> Set the CSIMAn.RXEAn bit and the CSIMAn.TXEAn bit to 11.

<3> Set a data transfer interval in the ADTIn register.

<4> Set the CSITn.ATSTAn bit to 1.

The following operations are automatically carried out when (a) and (b) are carried out.

- After the buffer RAM data indicated by the ADTCn register is transferred to the SIOAn register, transmission is carried out (start of automatic transmission/reception).
- The received data is written to the buffer RAM address indicated by the ADTCn register.
- ADTCn register is incremented and the next data transmission/reception is carried out. Data transmission/reception continues until the ADTCn register incremental output matches the set value of the ADTPn register (end of automatic transmission/reception). However, if the CSIMAn.ATMn bit is set to 1 (continuous transfer mode), the ADTCn register is cleared after a match between the ADTPn and ADTCn registers, and then repeated transmission/reception is started.
- When automatic transmission/reception is terminated, the CSISn.TSFn bit is cleared to 0.

Caution Determine the setting procedure of alternate-function pins considering the relationship with the communication partner.

Remark n = 0, 1

(2) Automatic transmission/reception communication operation

(a) Automatic transmission/reception mode

Automatic transmission/reception can be performed using buffer RAM.

The data stored in the buffer RAM is output from the SOAn pin via the SIOAn register in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge by performing (a) and (b) in **(1) Automatic transmit/receive data setting**.

The data is then input from the SIAn pin via the SIOAn register in synchronization with the serial clock falling edge of the $\overline{\text{SCKAn}}$ pin and the receive data is stored in the buffer RAM in synchronization with the rising edge 1 clock later.

Data transfer ends if the CSISn.TSFn bit is cleared to 0 when any of the following conditions is met.

- Reset by clearing the CSIMAn.CSIAEn bit to 0
- Transfer of 1 byte is complete by setting the CSITn.ATSTPn bit to 1
- Transfer of the range specified by the ADTPn register is complete

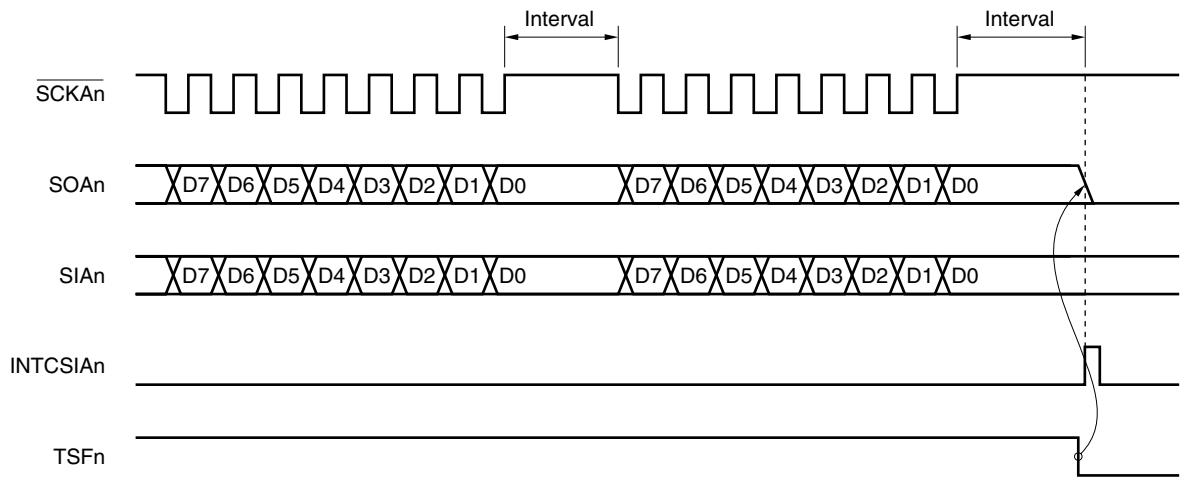
At this time, a transmission/reception completion interrupt request signal (INTCSIAn) is generated except when the CSIAEn bit = 0.

If a transfer is terminated in the middle, transfer starting from the remaining data is not possible. Read the ADTCn register to confirm how much of the data has already been transferred, set the transfer data again, and perform (a) and (b) in **(1) Automatic transmit/receive data setting**.

Figure 18-5 shows the operation timing in automatic transmission/reception mode and Figure 18-6 shows the operation flowchart. Figure 18-7 shows the operation of the buffer RAM when 6 bytes of data are transmitted/received.

Remark n = 0, 1

Figure 18-5. Automatic Transmission/Reception Mode Operation Timings



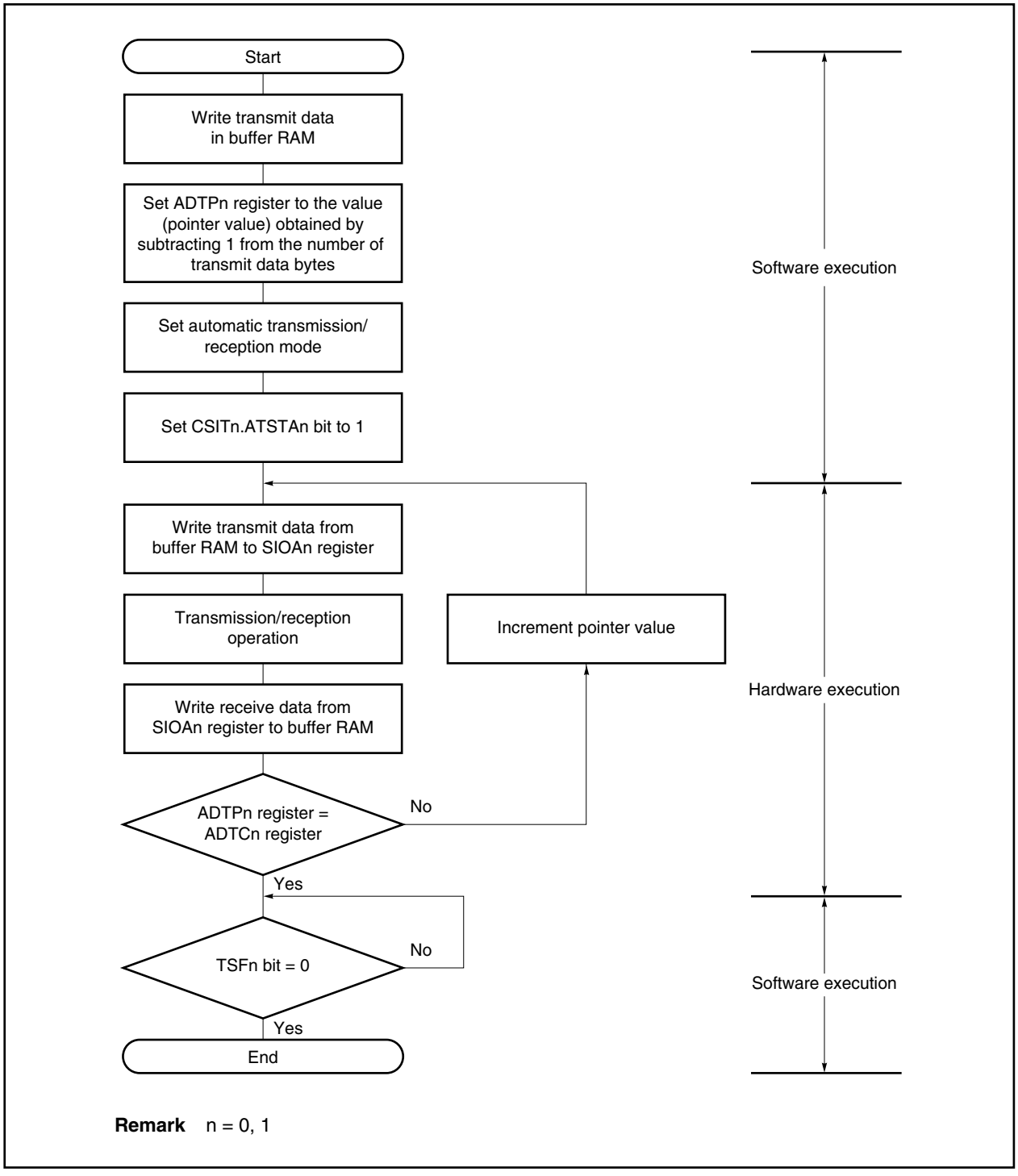
Cautions 1. Because, in the automatic transmission/reception mode, the automatic transmit/receive function reads/writes data from/to the buffer RAM after 1-byte transmission/reception, an interval is inserted until the next transmission/reception. As the buffer RAM read/write is performed at the same time as CPU processing, the interval is dependent upon the value of the ADTIn register.

2. When the TSFn bit is cleared, the SOAn pin becomes low level.

3. If CPU access to the buffer RAM conflicts with CSIAn read/write during the interval time, the interval time becomes longer.

Remark n = 0, 1

Figure 18-6. Automatic Transmission/Reception Mode Flowchart



Remark n = 0, 1

In 6-byte transmission/reception (CSIMAn.ATMn bit = 0, CSIMAn.RXEAn bit = 1, CSIMAn.TXEAn bit = 1) in automatic transmission/reception mode, buffer RAM operates as follows.

(i) When transmission/reception operation is started (refer to Figure 18-7 (a).)

When the CSITn.ATSTAn bit is set to 1, transmit data 1 (T1) is transferred from the buffer RAM to the SIOAn register. When transmission of the first byte is completed, receive data 1 (R1) is transferred from the SIOAn register to the buffer RAM, and the ADTCn register is incremented. Then transmit data 2 (T2) is transferred from the buffer RAM to the SIOAn register.

(ii) 4th byte transmission/reception point (refer to Figure 18-7 (b).)

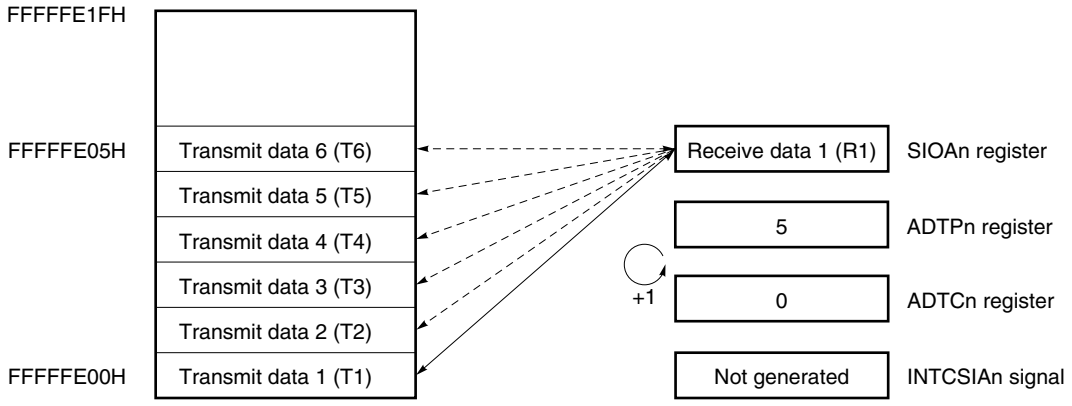
Transmission/reception of the third byte is completed, and transmit data 4 (T4) is transferred from the buffer RAM to the SIOAn register. When transmission of the fourth byte is completed, the receive data 4 (R4) is transferred from the SIOAn register to the buffer RAM, and the ADTCn register is incremented.

(iii) Completion of transmission/reception (refer to Figure 18-7 (c).)

When transmission of the sixth byte is completed, receive data 6 (R6) is transferred from SIOAn register to the buffer RAM, and the transmission/reception completion interrupt request signal (INTCSIAn) is generated.

Figure 18-7. Buffer RAM Operation in 6-Byte Transmission/Reception (in Automatic Transmission/Reception Mode) (1/2)

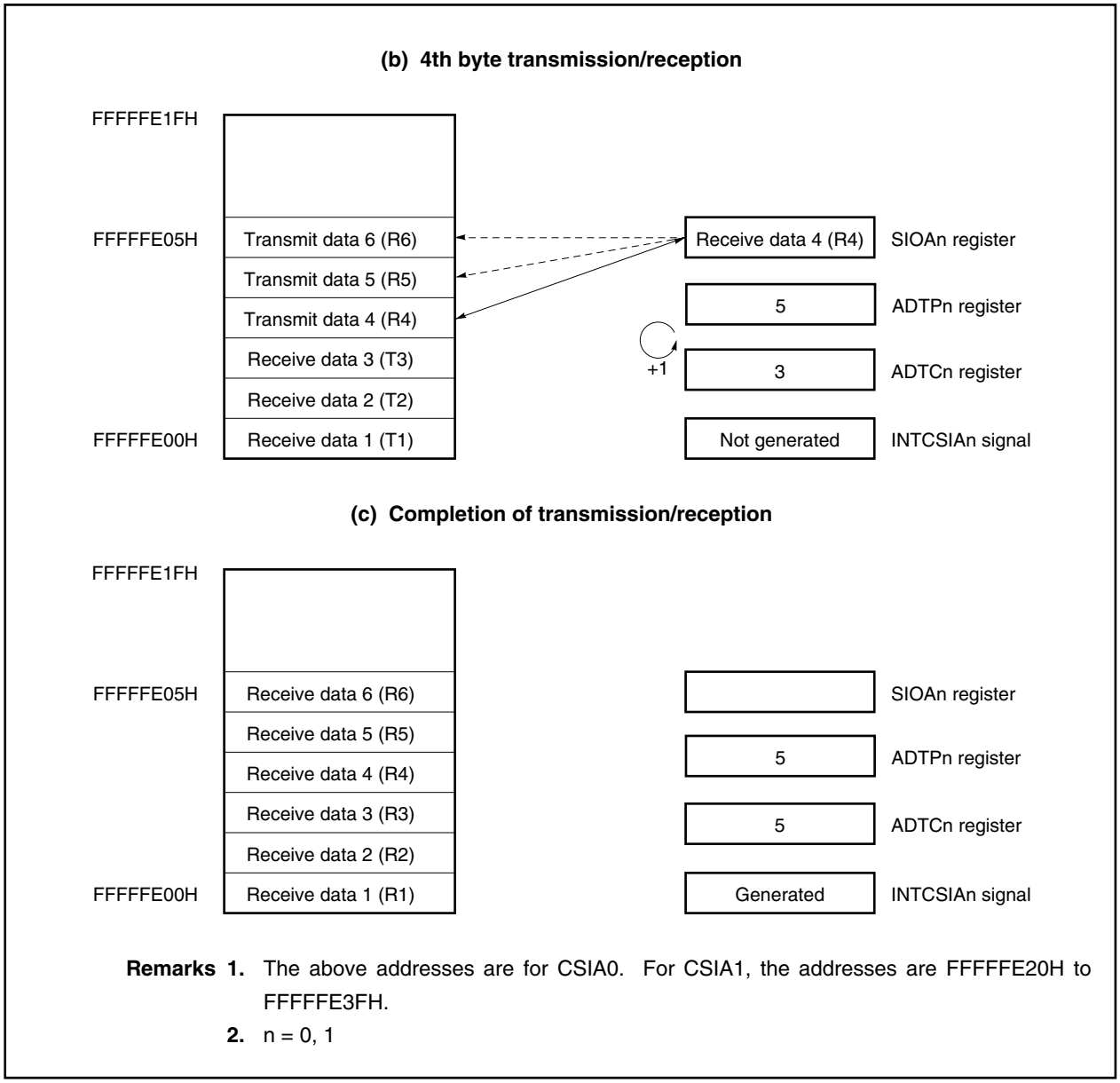
(a) When transmission/reception operation is started



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

2. n = 0, 1

Figure 18-7. Buffer RAM Operation in 6-Byte Transmission/Reception (in Automatic Transmission/Reception Mode) (2/2)



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

2. n = 0, 1

(b) Automatic transmission mode

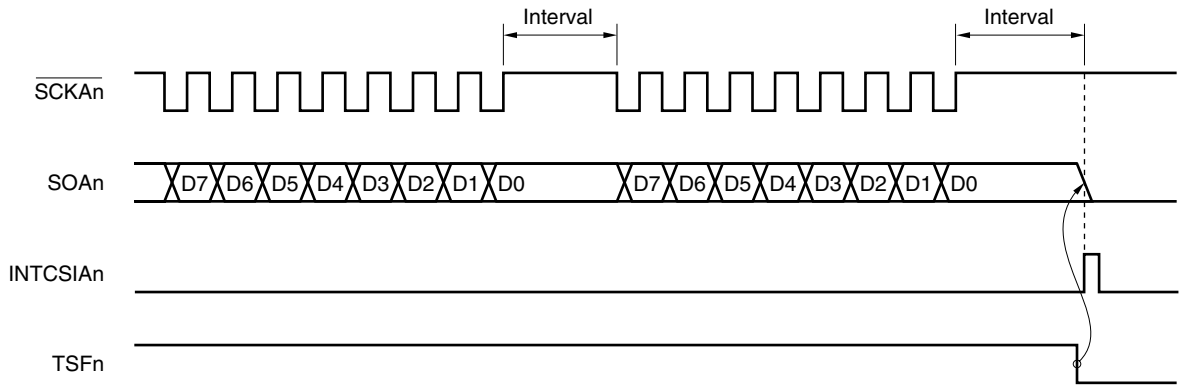
In this mode, the specified number of 8-bit unit data are transmitted.

Serial transfer is started when the CSITn.ATSTAn bit is set to 1 while the CSIMAn.CSIAEn, CSIMAn.ATEn, and CSIMAn.TXEAn bits are set to 1.

When the final byte has been transmitted, an interrupt request signal (INTCSIAn) is generated.

Figure 18-8 shows the automatic transmission mode operation timing, and Figure 18-9 shows the operation flowchart. Figure 18-10 shows the operation of the buffer RAM when 6 bytes of data are transmitted.

Figure 18-8. Automatic Transmission Mode Operation Timing



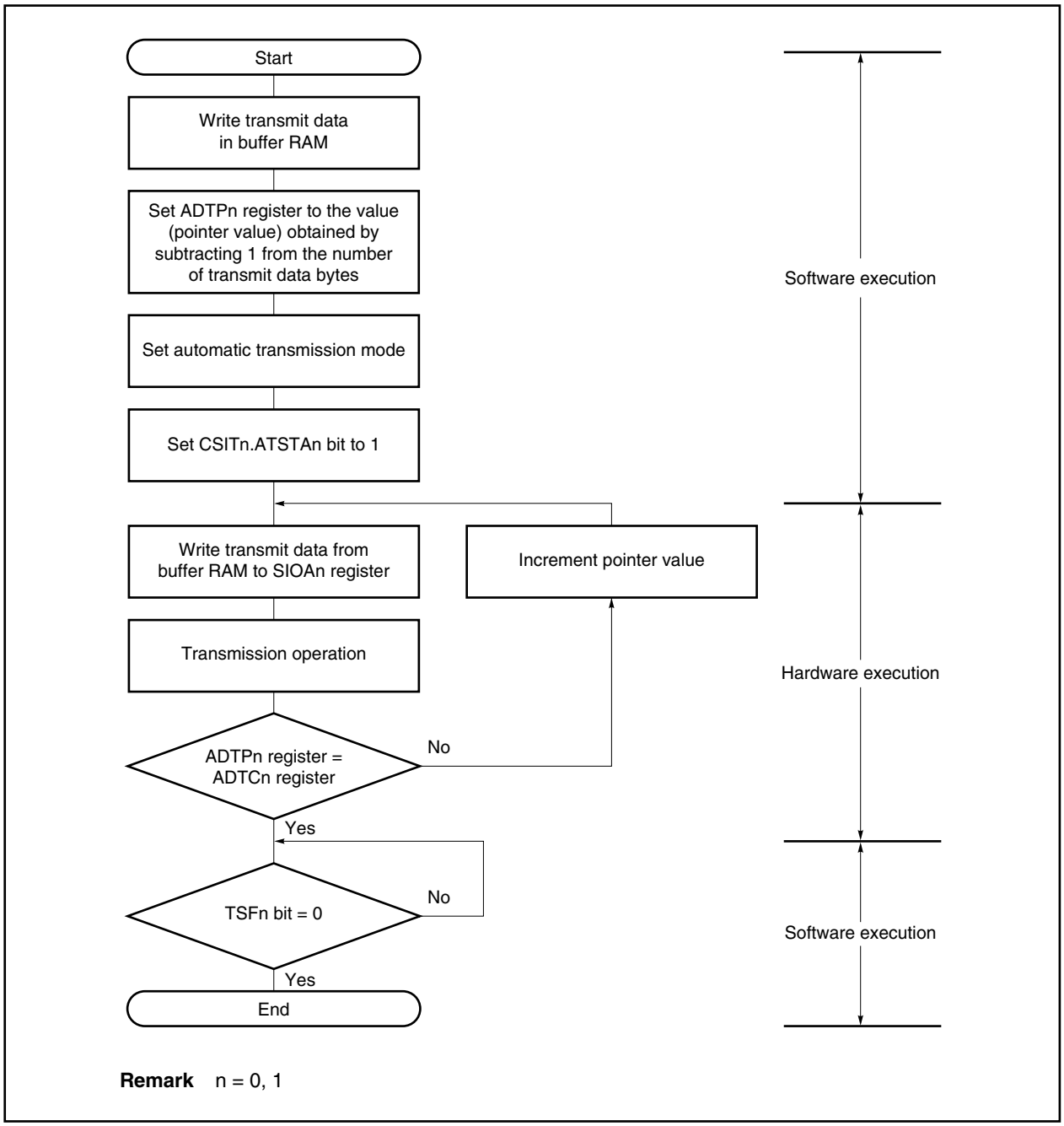
Cautions 1. Because, in the automatic transmission mode, the automatic transmit/receive function reads data from the buffer RAM after 1-byte transmission, an interval is inserted until the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon the value of the ADTIn register.

2. When the TSFn bit is cleared, the SOAn pin becomes low level.

3. If CPU access to the buffer RAM conflicts with CSIAn read/write during the interval time, the interval time becomes longer.

Remark n = 0, 1

Figure 18-9. Automatic Transmission Mode Flowchart



Remark n = 0, 1

In 6-byte transmission (CSIMAn.ATMn bit = 0, CSIMAn.RXEAn bit = 0, CSIMAn.TXEAn bit = 1, CSIMAn.ATEn bit = 1) in automatic transmission mode, buffer RAM operates as follows.

(i) When transmission is started (refer to Figure 18-10 (a).)

When the CSITn.ATSTAn bit is set to 1, transmit data 1 (T1) is transferred from the buffer RAM to the SIOAn register. When transmission of the first byte is completed, the ADTCn register is incremented. Then transmit data 2 (T2) is transferred from the buffer RAM to the SIOAn register.

(ii) 4th byte transmission point (refer to Figure 18-10 (b).)

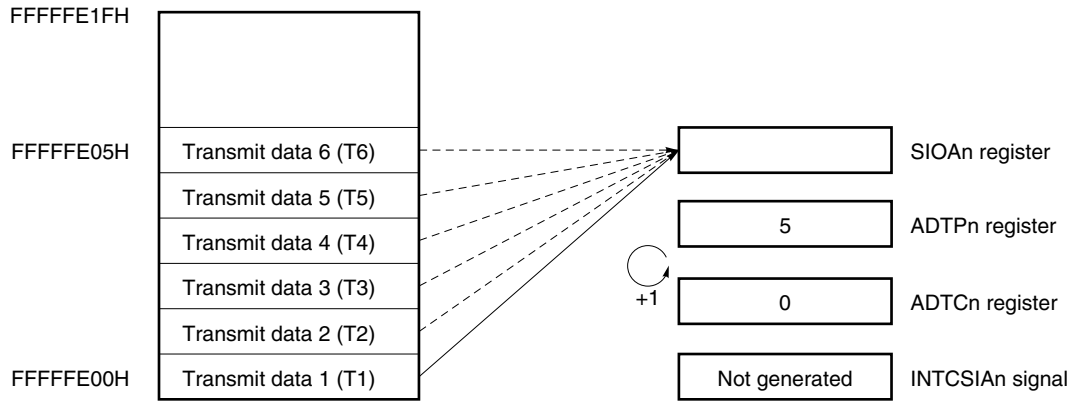
Transmission of the third byte is completed, and transmit data 4 (T4) is transferred from the buffer RAM to the SIOAn register. When transmission of the fourth byte is completed, the ADTCn register is incremented.

(iii) Completion of transmission (refer to Figure 18-10 (c).)

When transmission of the sixth byte is completed, the interrupt request signal (INTCSIAn) is generated, and the TFSn flag is cleared to 0.

Figure 18-10. Buffer RAM Operation in 6-Byte Transmission (in Automatic Transmission Mode) (1/2)

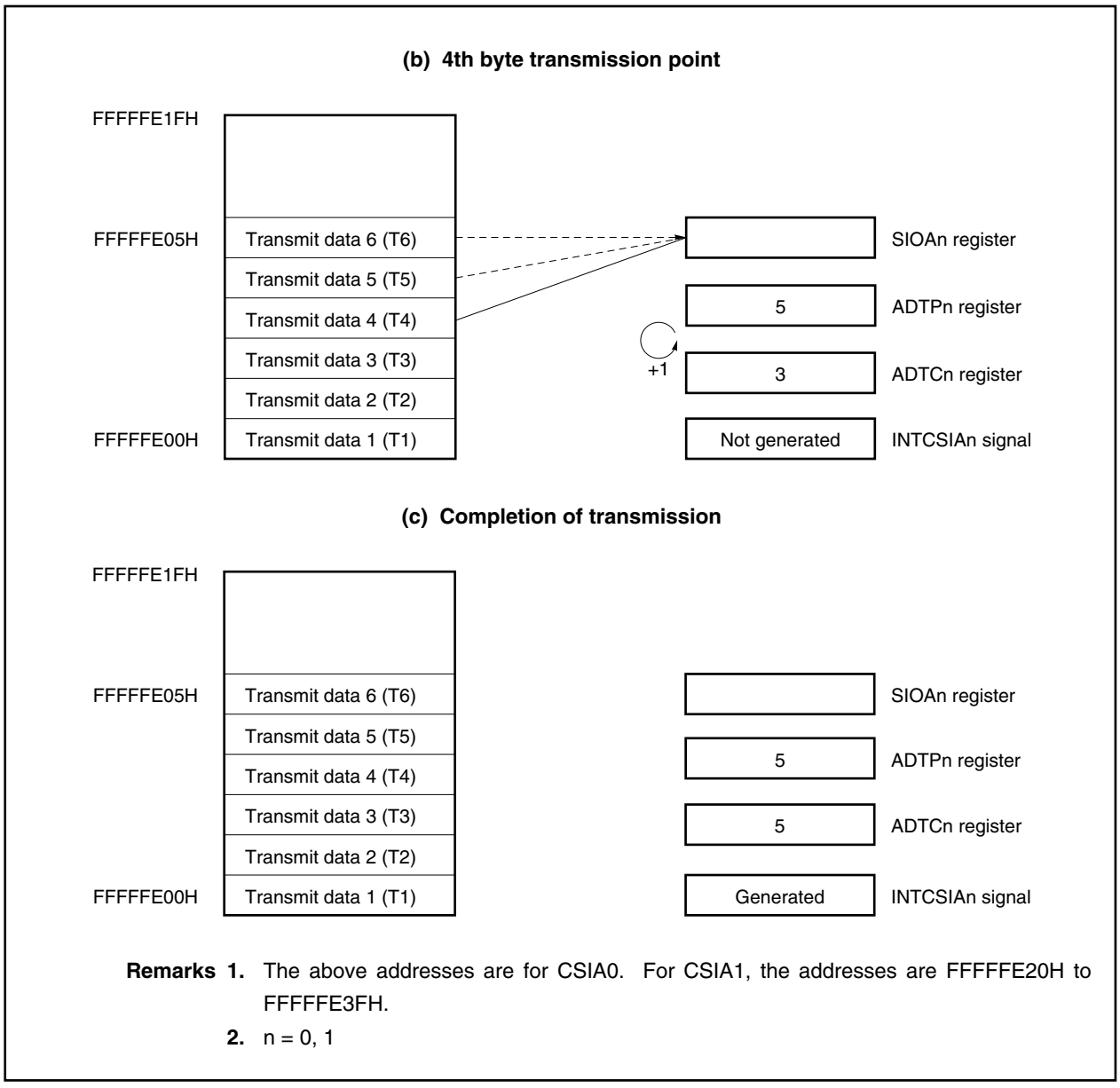
(a) When transmission is started



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

2. n = 0, 1

Figure 18-10. Buffer RAM Operation in 6-Byte Transmission (in Automatic Transmission Mode) (2/2)



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

2. n = 0, 1

(c) Repeat transmission mode

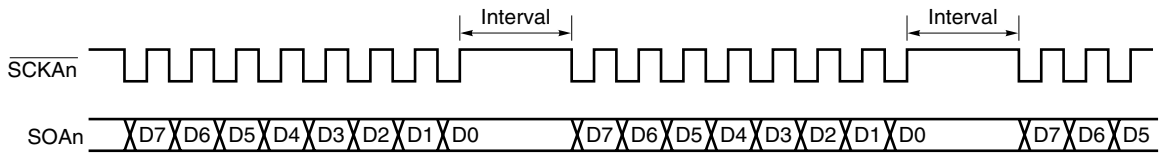
In this mode, data stored in the buffer RAM is transmitted repeatedly.

Serial transfer is started when the CSITn.ATSTAn bit is set to 1 while the CSIMAn.CSIAEn, CSIMAn.ATEn, CSIMAn.ATMn, and CSIMAn.TXEAn bits are set to 1.

Unlike the basic transmission mode, after the specified number of bytes has been transmitted, the transmission/reception completion interrupt request signal (INTCSIAn) is not generated, the ADTCn register is reset to 0, and the buffer RAM contents are transmitted again.

The repeat transmission mode operation timing is shown in Figure 18-11, and the operation flowchart in Figure 18-12. Figure 18-13 shows the operation of the buffer RAM when 6 bytes of data are transmitted in the repeat transmission mode.

Figure 18-11. Repeat Transmission Mode Operation Timing

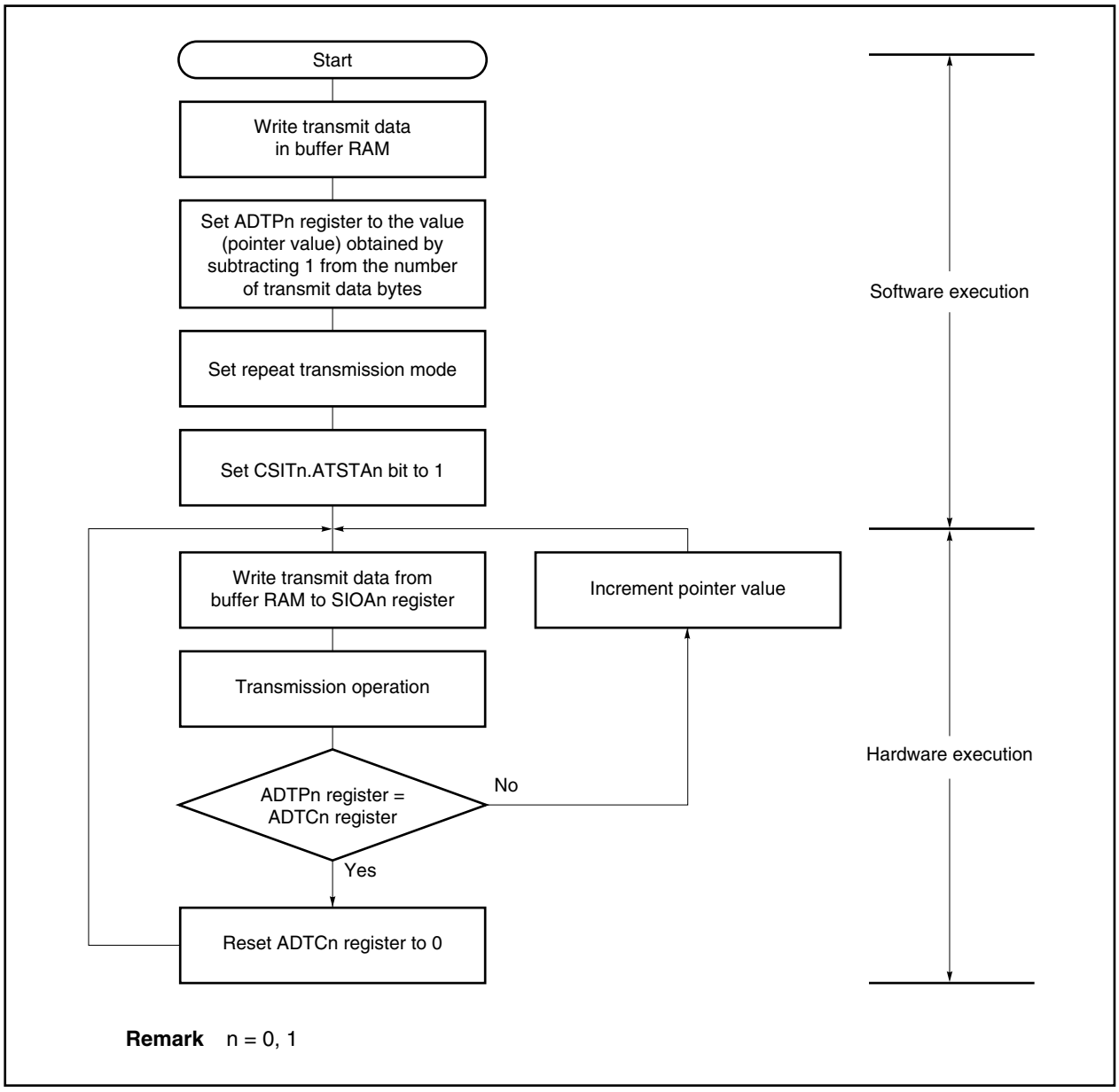


Cautions 1. Because, in the repeat transmission mode, a read is performed on the buffer RAM after the transmission of one byte, the interval is included in the period up to the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon the ADTIn register.

2. If CPU access to the buffer RAM conflicts with CSIA read/write during the interval time, the interval time becomes longer.

Remark n = 0, 1

Figure 18-12. Repeat Transmission Mode Flowchart



Remark n = 0, 1

In 6-byte transmission (CSIMAn.ATMn bit = 1, CSIMAn.RXEAn bit = 0, CSIMAn.TXEAn bit = 1, CSIMAn.ATEn bit = 1) in repeat transmission mode, buffer RAM operates as follows.

(i) When transmission is started (refer to Figure 18-13 (a).)

When the CSITn.ATSTAn bit is set to 1, transmit data 1 (T1) is transferred from the buffer RAM to the SIOAn register. When transmission of the first byte is completed, the ADTCn register is incremented. Then transmit data 2 (T2) is transferred from the buffer RAM to the SIOAn register.

(ii) Upon completion of transmission of 6 bytes (refer to Figure 18-13 (b).)

When transmission of the sixth byte is completed, the interrupt request signal (INTCSIAn) is not generated.

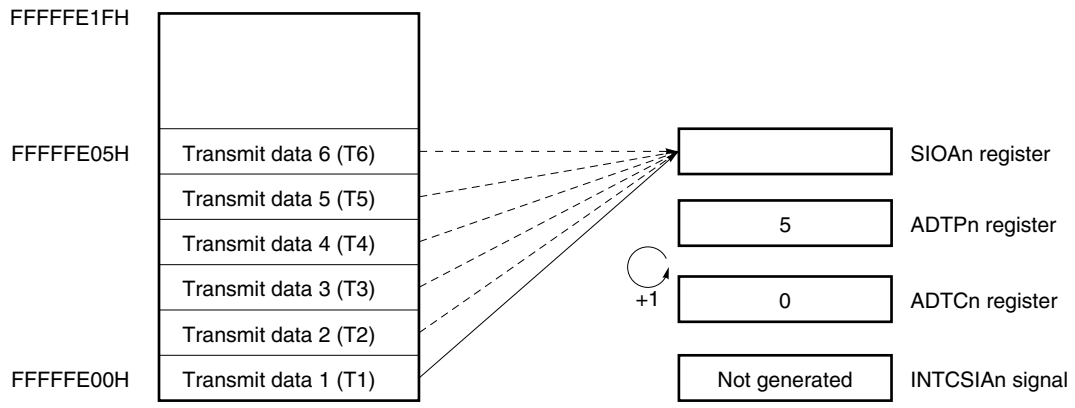
The ADTCn register is reset to 0.

(iii) 7th byte transmission point (refer to Figure 18-13 (c).)

Transmit data 1 (T1) is transferred from the buffer RAM to SIOAn register again. When transmission of the first byte is completed, the ADTCn register is incremented. Then transmit data 2 (T2) is transferred from the buffer RAM to the SIOAn register.

Figure 18-13. Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmission Mode) (1/2)

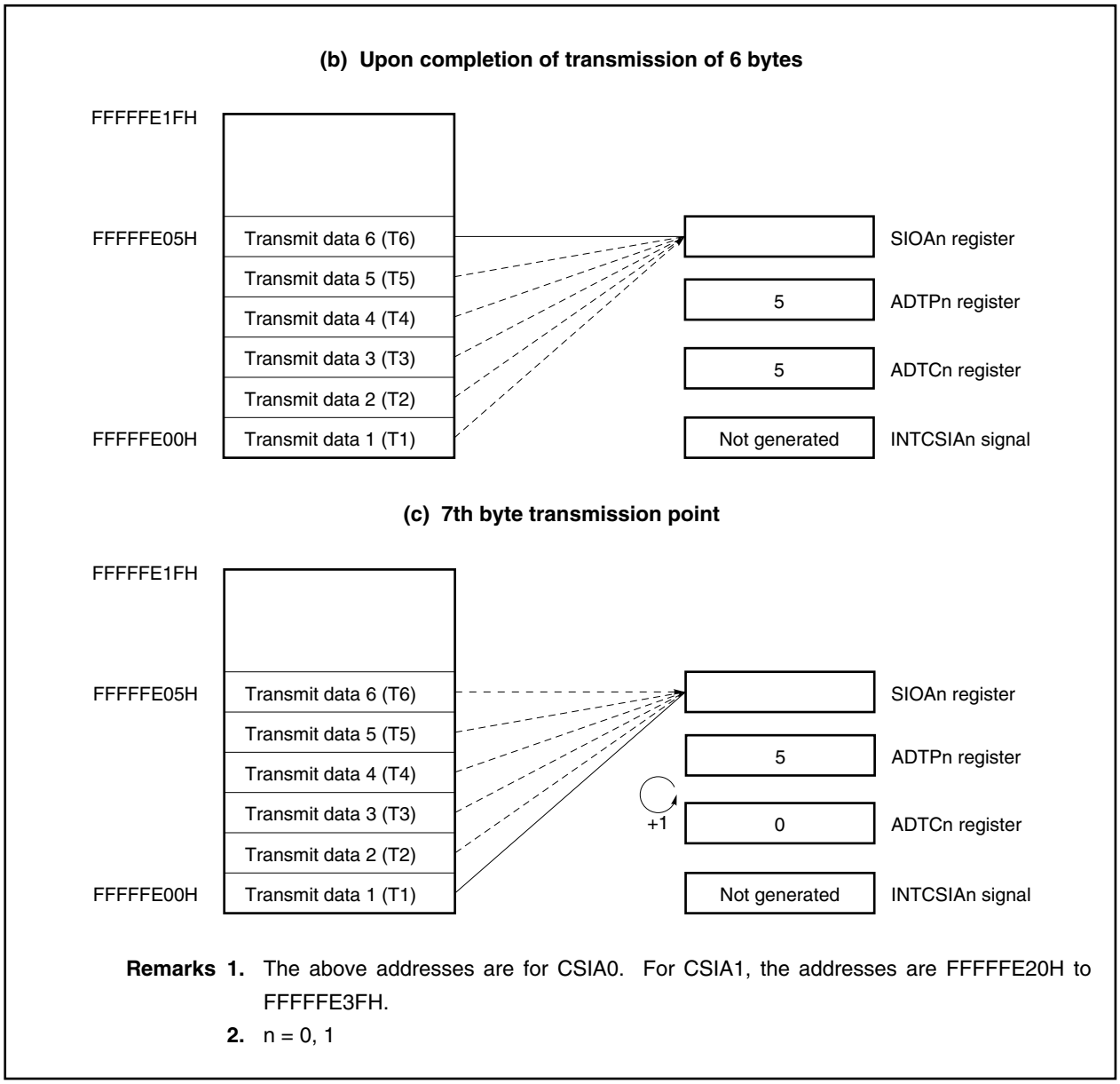
(a) When transmission is started



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

2. n = 0, 1

Figure 18-13. Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmission Mode) (2/2)



Remarks 1. The above addresses are for CSIA0. For CSIA1, the addresses are FFFFFE20H to FFFFFE3FH.

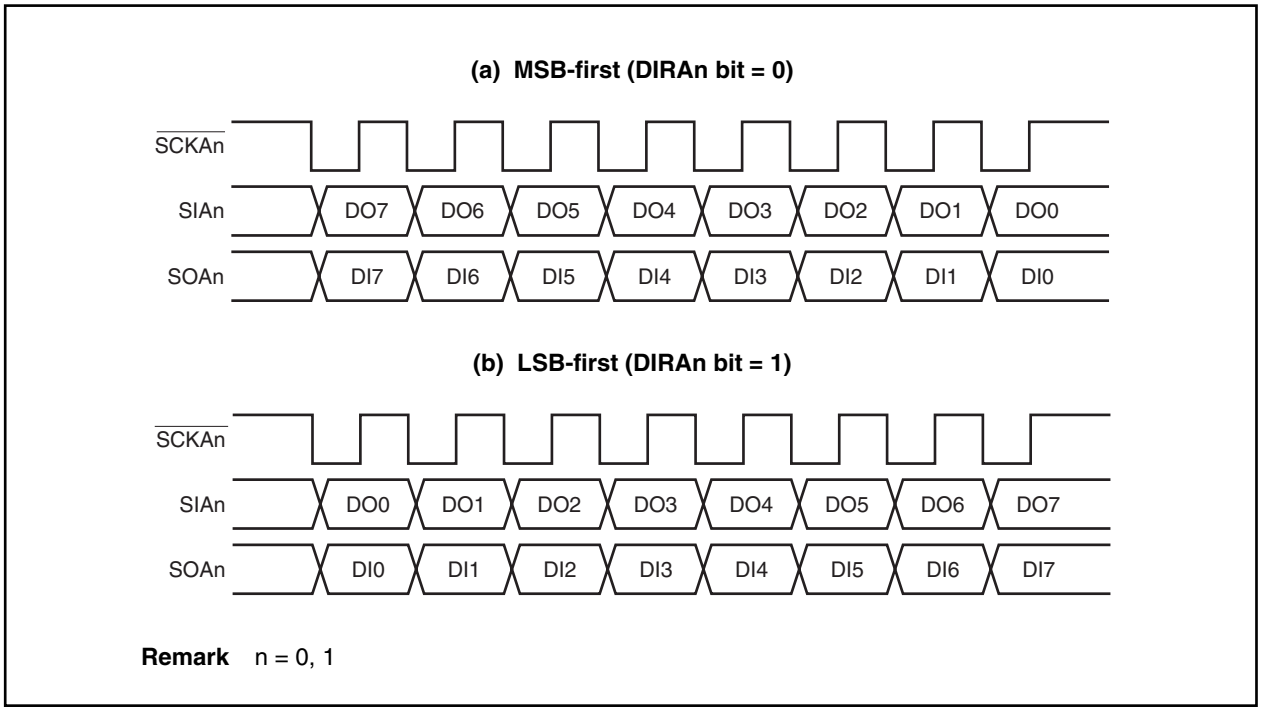
2. n = 0, 1

(d) Data format

In the data format, data is changed in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge as shown in Figure 18-14.

The data length is fixed to 8 bits and the data transfer direction can be switched by the specification of the CSIMAn.DIRAn bit.

Figure 18-14. Format of CSIAn Transmit/Receive Data



Remark n = 0, 1

(e) Automatic transmission/reception suspension and restart

Automatic transmission/reception can be temporarily suspended by setting the CSITn.ATSTPn bit to 1. During 8-bit data transfer, the transmission/reception is not suspended. It is suspended upon completion of 8-bit data transfer.

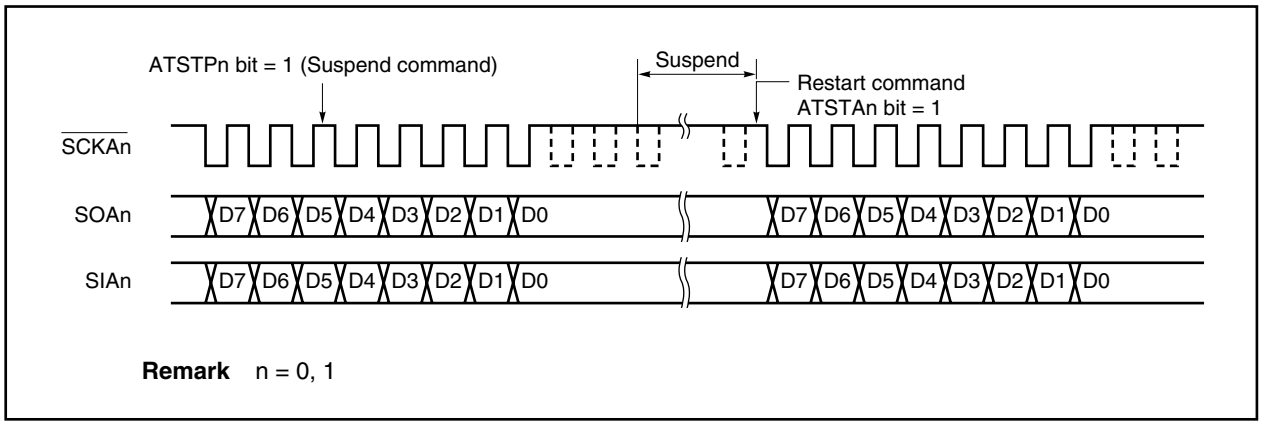
When suspended, the CSISn.TSFn bit is cleared to 0 after transfer of the 8th bit.

To restart automatic transmission/reception, set the CSITn.ATSTAn bit to 1. The remaining data can be transmitted in this way.

Cautions 1. If the IDLE instruction is executed during automatic transmission/reception, transfer is suspended and the IDLE mode is set if during 8-bit data transfer. When the IDLE mode is cleared, automatic transmission/reception is restarted from the suspended point.

2. When suspending automatic transmission/reception, do not change the operating mode to 3-wire serial I/O mode while the TSFn bit = 1.

Figure 18-15. Automatic Transmission/Reception Suspension and Restart



Remark n = 0, 1

CHAPTER 19 I²C BUS

To use the I²C bus function, use the P38/SDA0 and P39/SCL0 pins as the serial transmit/receive data I/O pin (SDA0) and serial clock I/O pin (SCL0), respectively, and set them to N-ch open-drain output.

In the V850ES/KG2, one channel of I²C bus is provided.

19.1 Features

The I²C0 has the following two modes.

- Operation stop mode
- I²C (Inter IC) bus mode (multimaster supported)

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

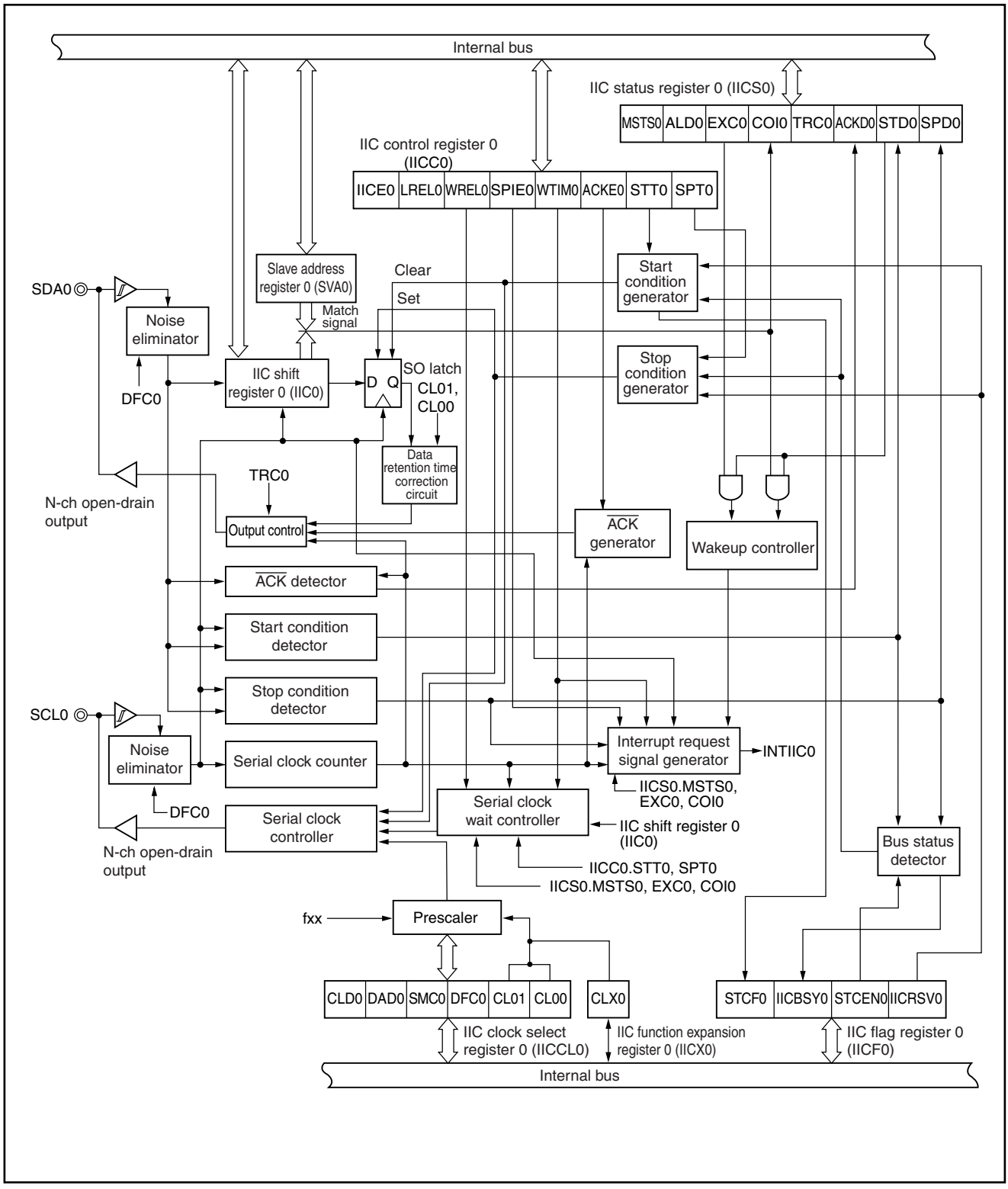
(2) I²C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCL0) line and a serial data bus (SDA0) line.

This mode complies with the I²C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received state and data by hardware. This function can simplify the part of application program that controls the I²C bus.

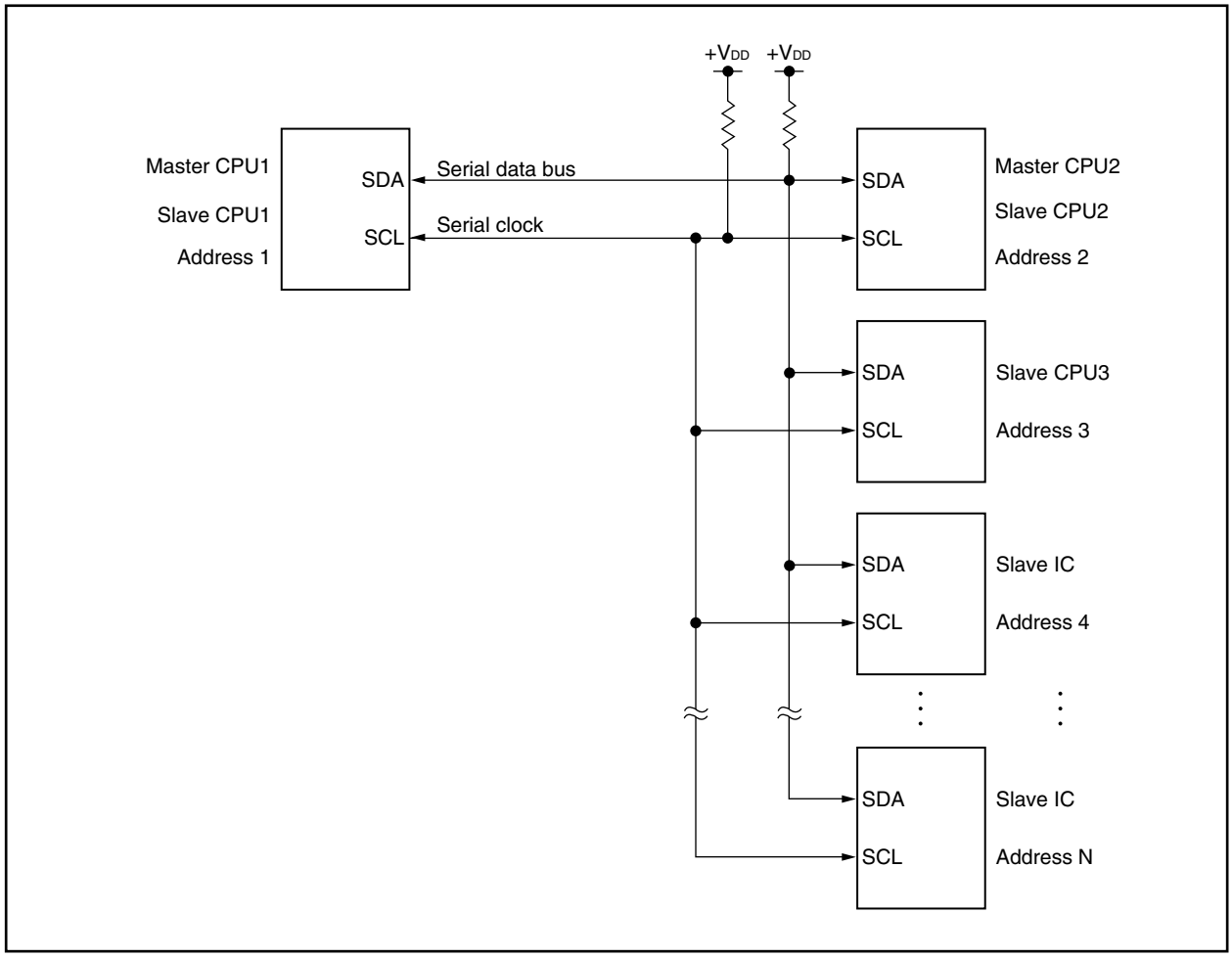
Since the SCL0 and SDA0 pins are used for N-ch open drain outputs, I²C0 requires pull-up resistors for the serial clock line and the serial data bus line.

Figure 19-1. Block Diagram of I²C0



A serial bus configuration example is shown below.

Figure 19-2. Serial Bus Configuration Example Using I²C Bus



19.2 Configuration

I²C0 includes the following hardware.

Table 19-1. Configuration of I²C0

Item	Configuration
Registers	IIC shift register 0 (IIC0) Slave address register 0 (SVA0)
Control registers	IIC control register 0 (IICC0) IIC status register 0 (IICS0) IIC flag register 0 (IICCF0) IIC clock selection register 0 (IICCL0) IIC function expansion register 0 (IICX0)

(1) IIC shift register 0 (IIC0)

The IIC0 register is used to convert 8-bit serial data to 8-bit parallel data and to convert 8-bit parallel data to 8-bit serial data. The IIC0 register can be used for both transmission and reception.

Write and read operations to the IIC0 register are used to control the actual transmit and receive operations.

The IIC0 register can be read or written in 8-bit units.

Reset sets IIC0 to 00H.

(2) Slave address register 0 (SVA0)

The SVA0 register sets local addresses when in slave mode.

The SVA0 register can be read or written in 8-bit units.

Reset sets SVA0 to 00H.

(3) SO latch

The SO latch is used to retain the SDA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request signal (INTIIC0) when the address received by this register matches the address value set to the SVA0 register or when an extension code is received.

(5) Prescaler

This selects the sampling clock to be used.

(6) Serial clock counter

This counter counts the serial clocks that are output and the serial clocks that are input during transmit/receive operations and is used to verify that 8-bit data was sent or received.

(7) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIIC0).

An I²C interrupt is generated following either of two triggers.

- Falling of the eighth or ninth clock of the serial clock (set by IICC0.WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by IICC0.SPIE0 bit)

(8) Serial clock controller

In master mode, this circuit generates the clock output via the SCL0 pin from a sampling clock.

(9) Serial clock wait controller

This circuit controls the wait timing.

(10) $\overline{\text{ACK}}$ generator, stop condition detector, start condition detector, and $\overline{\text{ACK}}$ detector

These circuits are used to generate and detect various statuses.

(11) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(12) Start condition generator

This circuit generates a start condition when the IICC0.STT0 bit is set.

However, in the communication reservation disabled status (IICF0.IICRSV0 bit = 1), when the bus is not released (IICF0.IICBSY0 bit = 1), start condition requests are ignored and the IICF0.STCF0 bit is set to 1.

(13) Stop condition generator

A stop condition is generated when the IIC0.SPT0 bit is set (1).

(14) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the IICF0.STCEN0 bit.

19.3 Registers

I²C0 is controlled by the following registers.

- IIC control register 0 (IICC0)
- IIC status register 0 (IICS0)
- IIC flag register 0 (IICF0)
- IIC clock selection register 0 (IICCL0)
- IIC function expansion register 0 (IICX0)

The following registers are also used.

- IIC shift register 0 (IIC0)
- Slave address register 0 (SVA0)

Remark For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

(1) IIC control register 0 (IICC0)

The IICC0 register is used to enable/stop I²C0 operations, set wait timing, and set other I²C operations.

The IICC0 register can be read or written in 8-bit or 1-bit units. However, set the SPIE0, WTIM0, and ACKE0 bits when the IICE0 bit is 0 or during the wait period. When setting the IICE0 bit from “0” to “1”, these bits can also be set at the same time.

Reset sets this register to 00H.

(1/4)

After reset: 00H R/W Address: IICC0 FFFFFD82H

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I²C0 operation enable/disable specification
0	Stop operation. Reset the IICS0 register[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit to 1 when the SCL0 and SDA0 lines are high level.	
Condition for clearing (IICE0 bit = 0)	Condition for setting (IICE0 bit = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Note 2]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines are set to high impedance. The STT0, SPT0, IICS0.MSTS0, IICS0.EXC0, IICS0.COI0, IICS0.TRC0, IICS0.ACKD0, and IICS0.STD0 bits are cleared to 0.
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 bit = 0)	Condition for setting (LREL0 bit = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0[Note 2]	Wait cancellation control
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared to 0 after wait is canceled.
Condition for clearing (WREL0 bit = 0)	Condition for setting (WREL0 bit = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICS0 register, and the IICF0.STCF0, IICF0.IICBSY0, IICCL0.CLD0, and IICCL0.DAD0 bits are reset.

2. This flag's signal is invalid when the IICE0 bit = 0.

Caution If the I²C0 operation is enabled (IICE0 bit = 1) when the SCL0 line is high level and the SDA0 line is low level, the start condition is detected immediately. To avoid this, after enabling the I²C0 operation, immediately set the LREL0 bit to 1 with a bit manipulation instruction.

(2/4)

SPIE0[Note]	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Condition for clearing (SPIE0 bit = 0)	Condition for setting (SPIE0 bit = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIM0[Note]	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.

An interrupt is generated at the falling of the 9th clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after $\overline{ACK}$ is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.

Condition for clearing (WTIM0 bit = 0)	Condition for setting (WTIM0 bit = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKE0[Note]	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDA0 line is set to low level.

The ACKE0 bit setting is invalid for address reception. In this case, $\overline{ACK}$ is generated when the addresses match. However, the ACKE0 bit setting is valid for address reception of the extension code.

Condition for clearing (ACKE0 bit = 0)	Condition for setting (ACKE0 bit = 1)
• Cleared by instruction • Reset	• Set by instruction

Note This flag's signal is invalid when the IICE0 bit = 0.

(3/4)

STT0	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in STOP mode): Generate a start condition (for starting as master). The SDA0 line is changed from high level to low level while the SCL0 line is high level and then the start condition is generated. Next, after the rated amount of time has elapsed, the SCL0 line is changed to low level (wait status). When a third party is communicating • When communication reservation function is enabled (IICF0.IICRSV0 bit = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSV0 bit = 1) The IICF0.STCF0 bit is set to 1 and the information set (1) to the STT0 bit is cleared. No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.

Cautions concerning set timing

For master reception: Cannot be set to 1 during transfer. Can be set to 1 only when the ACKE0 bit has been cleared to 0 and slave has been notified of final reception.

For master transmission: A start condition may not be generated normally during the $\overline{\text{ACK}}$ period. Set to 1 during the wait period that follows output of the ninth clock.

- Cannot be set to 1 at the same time as the SPT0 bit.
- When the STT0 bit is set to 1, setting the STT0 bit to 1 again is disabled until the setting is cleared to 0.

Condition for clearing (STT0 bit = 0)	Condition for setting (STT0 bit = 1)
• When the STT0 bit is set to 1 in the communication reservation disabled status • Cleared when start condition is generated by master device • When the LREL0 bit = 1 (exit from communications) • When the IICE0 bit = 0 (operation stop) • Reset	• Set by instruction

Remark The STT0 bit is 0 if it is read after data setting.

(4/4)

SPT0	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer). After the SDA0 line goes to low level, either set the SCL0 line to high level or wait until the SCL0 pin goes to high level. Next, after the rated amount of time has elapsed, the SDA0 line is changed from low level to high level and a stop condition is generated.

Cautions concerning setting timing

For master reception: Cannot be set to 1 during transfer. Can be set to 1 only when the ACKE0 bit has been cleared to 0 and during the wait period after slave has been notified of final reception.

For master transmission: A stop condition may not be generated normally during the $\overline{\text{ACK}}$ period. Set to 1 during the wait period that follows output of the ninth clock.

- Cannot be set to 1 at the same time as the STT0 bit.
- The SPT0 bit can be set to 1 only when in master mode[Note].
- When the WTIM0 bit has been cleared to 0, if the SPT0 bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock.
  The WTIM0 bit should be changed from 0 to 1 during the wait period following output of eight clocks, and the SPT0 bit should be set to 1 during the wait period that follows output of the ninth clock.
- When the SPT0 bit is set to 1, setting the SPT0 bit to 1 again is disabled until the setting is cleared to 0.

Condition for clearing (SPT0 bit = 0)	Condition for setting (SPT0 bit = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • When the LREL0 bit = 1 (exit from communications) • When the IICE0 bit = 0 (operation stop) • Reset	• Set by instruction

Note Set the SPT0 bit to 1 only in master mode. However, the SPT0 bit must be set to 1 and a stop condition generated before the first stop condition is detected following the switch to operation enable status. For details, refer to **19.14 Cautions**.

Caution When the IICS0.TRC0 bit is set to 1, the WREL0 bit is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared to 0 and the SDA0 line is set to high impedance.

Remark The SPT0 bit is 0 if it is read after data setting.

(2) IIC status register 0 (IICS0)

The IICS0 register indicates the status of the I²C0 bus.

The IICS0 register is read-only, in 8-bit or 1-bit units.

However, the IICS0 register can only be read when the IICC0.STT0 bit is 1 or during the wait period.

Reset sets this register to 00H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the IICS0 register.
For details, refer to 3.4.8 (1) (b).

(1/3)

After reset: 00H R Address: IICS0 FFFFFD86H

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

MSTS0	Master device status
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTS0 bit = 0)	Condition for setting (MSTS0 bit = 1)
• When a stop condition is detected • When the ALD0 bit = 1 (arbitration loss) • Cleared by the IICC0.LREL0 bit = 1 (exit from communications) • When the IICC0.IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALD0	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. The MSTS0 bit is cleared to 0.

Condition for clearing (ALD0 bit = 0)	Condition for setting (ALD0 bit = 1)
• Automatically cleared after the IICS0 register is read[Note] • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

Note This bit is also cleared when a bit manipulation instruction is executed for another bit in the IICS0 register.

(2/3)

EXC0	Detection of extension code reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXC0 bit = 0)	Condition for setting (EXC0 bit = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When the higher four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock).

COI0	Detection of matching addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COI0 bit = 0)	Condition for setting (COI0 bit = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 • Reset	• When the received address matches the local address (SVA0 register) (set at the rising edge of the eighth clock).

TRC0	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDA0 line is set for high impedance.
1	Transmit status. The value in the SO latch is enabled for output to the SDA0 line (valid starting at the rising edge of the first byte’s ninth clock).

Condition for clearing (TRC0 bit = 0)	Condition for setting (TRC0 bit = 1)
• When a stop condition is detected • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Cleared by the IICC0.WREL0 bit = 1[Note] (wait release) • When the ALD0 bit changes from 0 to 1 (arbitration loss) • Reset Master • When “1” is output to the first byte’s LSB (transfer direction specification bit) Slave • When a start condition is detected When not used for communication	Master • When a start condition is generated • When “0” is output to the first byte’s LSB (transfer direction specification bit) Slave • When “1” is input in the first byte’s LSB (transfer direction specification bit)

Note The IICS0.TRC0 bit is cleared to 0 and the SDA0 line become high impedance when the IICC0.WREL0 bit is set to 1 and wait state is released at the ninth clock with the TRC0 bit = 1.

(3/3)

ACKD0	Detection of $\overline{ACK}$
0	$\overline{ACK}$ was not detected.
1	$\overline{ACK}$ was detected.

Condition for clearing (ACKD0 bit = 0)	Condition for setting (ACKD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• After the SDA0 pin is set to low level at the rising edge of the SCL0 pin's ninth clock

STD0	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect

Condition for clearing (STD0 bit = 0)	Condition for setting (STD0 bit = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by the LREL0 bit = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD0 bit = 0)	Condition for setting (SPD0 bit = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

(3) IIC flag register 0 (IICF0)

IICF0 is a register that set the operation mode of I²C0 and indicate the status of the I²C bus.

These registers can be read or written in 8-bit or 1-bit units. However, the STCF0 and IICBSY0 bits are read-only.

The IICRSV0 bit can be used to enable/disable the communication reservation function (refer to **19.13 Communication Reservation**).

The STCEN0 bit can be used to set the initial value of the IICBSY0 bit (refer to **19.14 Cautions**).

The IICRSV0 and STCEN0 bits can be written only when the operation of I²C0 is disabled (IICC0.IICE0 bit = 0).

When operation is enabled, the IICF0 register can be read.

Reset sets this register to 00H.

After reset: 00H R/W[Note] Address: IICF0 FFFFFD8AH

	<7>	<6>	5	4	3	2	<1>	<0>
IICF0	STCF0	IICBSY0	0	0	0	0	STCEN0	IICRSV0

STCF0	IICC0.STT0 clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear STT0 flag

Condition for clearing (STCF0 bit = 0)	Condition for setting (STCF0 bit = 1)
• Clearing by setting the STT0 bit = 1 • When the IICE0 bit = 0 • Reset	• Generating start condition unsuccessful and the STT0 bit cleared to 0 when communication reservation is disabled (IICRSV0 bit = 1).

IICBSY0	I²C0 bus status flag
0	Bus release status (initial communication status when STCEN0 bit = 1)
1	Bus communication status (initial communication status when STCEN0 bit = 0)

Condition for clearing (IICBSY0 bit = 0)	Condition for setting (IICBSY0 bit = 1)
• Detection of stop condition • When the IICE0 bit = 0 • Reset	• Detection of start condition • Setting of the IICE0 bit when the STCEN0 bit = 0

STCEN0	Initial start enable trigger
1	After operation is enabled (IICE0 bit = 1), enable generation of a start condition upon detection of a stop condition.
	After operation is enabled (IICE0 bit = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEN0 bit = 0)	Condition for setting (STCEN0 bit = 1)
• Detection of start condition • Reset	• Setting by instruction

IICRSV0	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSV0 bit = 0)	Condition for setting (IICRSV0 bit = 1)
• Clearing by instruction • Reset	• Setting by instruction

Note Bits 6 and 7 are read-only bits.

Cautions 1. Write to the STCEN0 bit only when the operation is stopped (IICE0 bit = 0).

2. As the bus release status (IICBSY0 bit = 0) is recognized regardless of the actual bus status when the STCEN0 bit = 1, when generating the first start condition (STT0 bit = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

3. Write to the IICRSV0 bit only when the operation is stopped (IICE0 bit = 0).

(4) IIC clock selection register 0 (IICCL0)

The IICCL0 register is used to set the transfer clock for the I²C0 bus.

The IICCL0 register can be read or written in 8-bit or 1-bit units. However, the CLD0 and DAD0 bits are read-only. The SMC0, CL01 and CL00 bits are set in combination with the IICX0.CLX0 bit (refer to **19.3 (6) I²C0 transfer clock setting method**).

Set the IICCL0 register when the IICC0.IICE0 bit = 0.

Reset sets this register to 00H.

After reset: 00H R/W[Note] Address: IICCL0 FFFFFD84H

	7	6	<5>	<4>	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

CLD0	Detection of SCL0 pin level (valid only when IICC0.IICE0 bit = 1)
0	The SCL0 pin was detected at low level.
1	The SCL0 pin was detected at high level.

Condition for clearing (CLD0 bit = 0)	Condition for setting (CLD0 bit = 1)
• When the SCL0 pin is at low level • When the IICE0 bit = 0 (operation stop) • Reset	• When the SCL0 pin is at high level

DAD0	Detection of SDA0 pin level (valid only when IICE0 bit = 1)
0	The SDA0 pin was detected at low level.
1	The SDA0 pin was detected at high level.

Condition for clearing (DAD0 bit = 0)	Condition for setting (DAD0 bit = 1)
• When the SDA0 pin is at low level • When IICE0 bit = 0 (operation stop) • Reset	• When the SDA0 pin is at high level

SMC0	Operation mode switching
0	Operates in standard mode.
1	Operates in high-speed mode.

DFC0	Digital filter operation control
0	Digital filter off.
1	Digital filter on.
Digital filter can be used only in high-speed mode. In high-speed mode, the transfer clock does not vary regardless of DFC0 bit set/clear. The digital filter is used for noise elimination in high-speed mode.	

Note Bits 4 and 5 are read-only bits.

(5) IIC function expansion register 0 (IICX0)

These registers set the function expansion of I²C0 (valid only in high-speed mode).

These registers can be read or written in 8-bit or 1-bit units. The CLX0 bit is set in combination with the IICCL0.SMC0, IICCL0.CL01, and IICCL0.CL00 bits (refer to **19.3 (6) I²C0 transfer clock setting method**).

Set the IICX0 register when the IICC0.IICE0 bit = 0.

Reset sets this register to 00H.

After reset: 00H R/W Address: IICX0 FFFFFD85H

	7	6	5	4	3	2	1	<0>
IICX0	0	0	0	0	0	0	0	CLX0

(6) I²C0 transfer clock setting method

The I²C0 transfer clock frequency (f_{SCL}) is calculated using the following expression.

$$f_{SCL} = 1/(m \times T + t_R + t_F)$$

m = 12, 24, 48, 54, 86, 88, 172, 198 (refer to **Table 19-2 Selection Clock Setting**.)

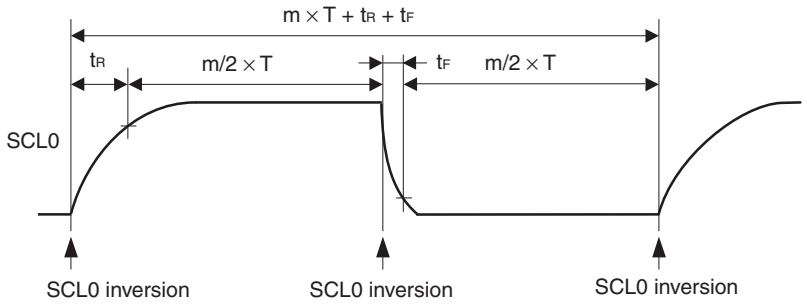
T: $1/f_{XX}$

t_R: SCL0 rise time

t_F: SCL0 fall time

For example, the I²C0 transfer clock frequency (f_{SCL}) when f_{XX} = 20 MHz, m = 54, t_R = 200 ns, and t_F = 50 ns is calculated using following expression.

$$f_{SCL} = 1/(54 \times 50 \text{ ns} + 200 \text{ ns} + 50 \text{ ns}) \cong 339 \text{ kHz}$$



The selection clock is set using a combination of the IICCL0.SMC0, IICCL0.CL01, and IICCL0.CL00 bits and the IICX0.CLX0 bit.

Table 19-2. Selection Clock Setting

IICX0	IICCL0			Selection Clock	Transfer Clock (fxx/m)	Settable Internal System Clock Frequency (fxx) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	fxx/2	fxx/88	4.0 MHz to 8.38 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	fxx/2	fxx/172	8.38 MHz to 16.76 MHz	
0	0	1	0	fxx	fxx/86	4.19 MHz to 8.38 MHz	
0	0	1	1	fxx/3	fxx/198	16.0 MHz to 19.8 MHz	
0	1	0	x	fxx/2	fxx/48	8 MHz to 16.76 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	fxx	fxx/24	4 MHz to 8.38 MHz	
0	1	1	1	fxx/3	fxx/54	16 MHz to 20 MHz	
1	0	x	x	Setting prohibited			
1	1	0	x	fxx/2	fxx/24	8.00 MHz to 8.38 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	fxx	fxx/12	4.00 MHz to 4.19 MHz	
1	1	1	1	Setting prohibited			

Remark x: don't care

(7) IIC shift register 0 (IIC0)

The IIC0 shift register is used for serial transmission/reception (shift operations) that is synchronized with the serial clock.

The IIC0 shift register can be read or written in 8-bit units, but data should not be written to the IIC0 shift register during a data transfer.

Access (read/write) the IIC0 shift register only during the wait period. Accessing this register in communication states other than the wait period is prohibited. However, for the master device, the IIC0 shift register can be written once only after the transmission trigger bit (IICC0.STT0 bit) has been set to 1.

When the IIC0 shift register is written during wait, the wait is cancelled and data transfer is started.

Reset sets this register to 00H.

After reset: 00H R/W Address: IIC0 FFFFFD80H

	7	6	5	4	3	2	1	0
IIC0								

(8) Slave address register 0 (SVA0)

The SVA0 register holds the I²C bus's slave addresses.

However, rewriting this register is prohibited when the IICS0.STD0 bit = 1 (start condition detection).

The SVA0 register can be read or written in 8-bit units, but bit 0 is fixed to 0.

Reset sets this register to 00H.

After reset: 00H R/W Address: SVA0 FFFFFD83H

	7	6	5	4	3	2	1	0
SVA0								0

19.4 Functions

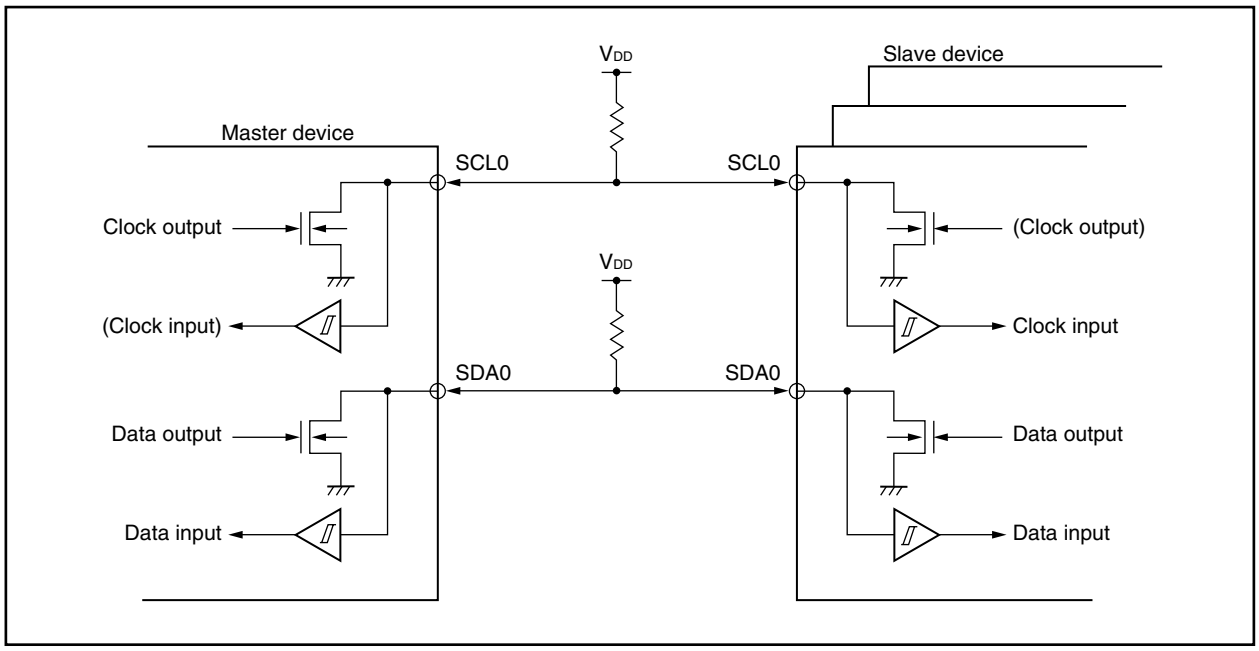
19.4.1 Pin configuration

The serial clock pin (SCL0) and serial data bus pin (SDA0) are configured as follows.

SCL0 ..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.
SDA0 ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

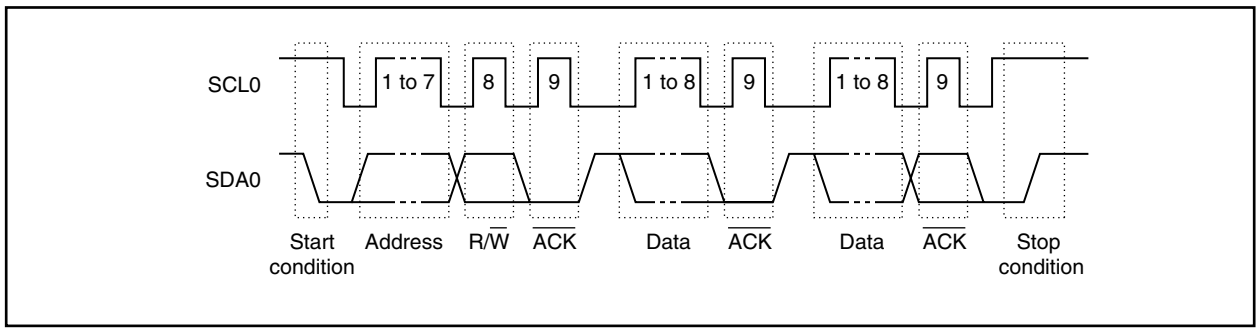
Figure 19-3. Pin Configuration Diagram



19.5 I²C Bus Definitions and Control Methods

The following section describes the I²C bus's serial data communication format and the status generated by the I²C bus. The transfer timing for the "start condition", "address", "transfer direction specification", "data", and "stop condition" generated via the I²C bus's serial data bus is shown below.

Figure 19-4. I²C Bus's Serial Data Transfer Timing



The master device generates the start condition, slave address, and stop condition.

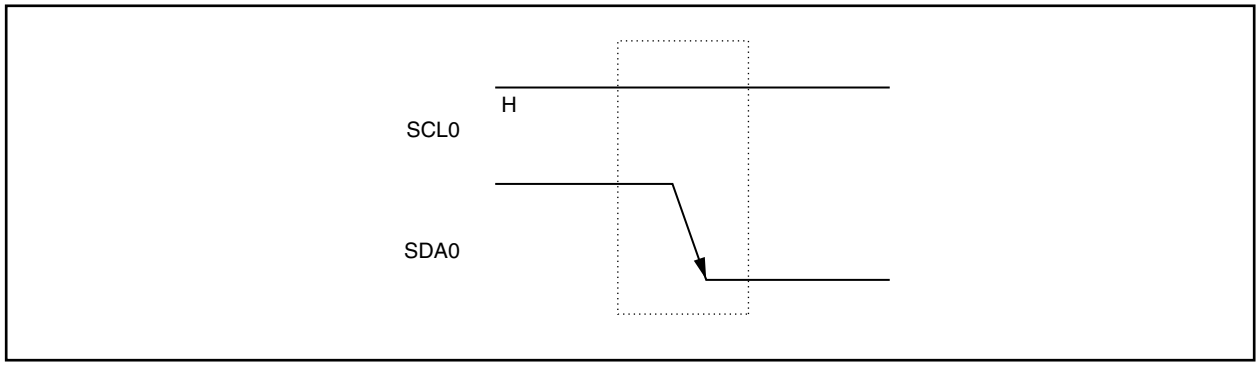
ACK can be generated by either the master or slave device (normally, it is generated by the device that receives 8-bit data).

The serial clock (SCL0) is continuously output by the master device. However, in the slave device, the SCL0's low-level period can be extended and a wait can be inserted.

19.5.1 Start condition

A start condition is met when the SCL0 pin is at high level and the SDA0 pin changes from high level to low level. The start conditions for the SCL0 pin and SDA0 pin are generated when the master device starts a serial transfer to the slave device. Start conditions can be detected when the device is used as a slave.

Figure 19-5. Start Conditions



A start condition is generated when the IICC0.STT0 bit is set to 1 after a stop condition has been detected (IICS0.SPD0 bit = 1). When a start condition is detected, IICS0.STD0 bit is set to 1.

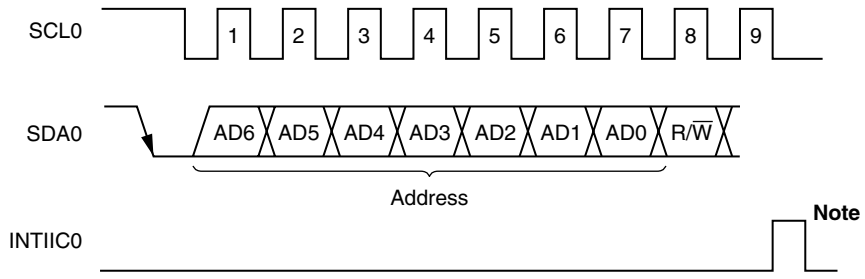
19.5.2 Addresses

The 7 bits of data that follow the start condition are defined as an address.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the SVA0 register. If the address data matches the SVA0 values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 19-6. Address



Note The interrupt request signal (INTIIC0) is generated if a local address or extension code is received during slave device operation.

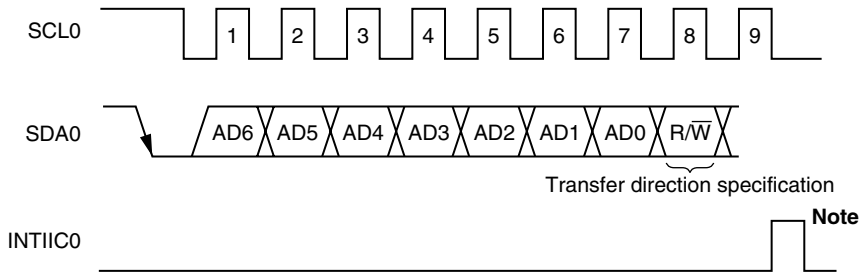
The slave address and the eighth bit, which specifies the transfer direction as described in **19.5.3 Transfer direction specification** below, are together written to the IIC0 register and are then output. Received addresses are written to the IIC0 register.

The slave address is assigned to the higher 7 bits of the IIC0 register.

19.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction. When this transfer direction specification bit has a value of 0, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of 1, it indicates that the master device is receiving data from a slave device.

Figure 19-7. Transfer Direction Specification



Note The interrupt request signal (INTIIC0) is generated if a local address or extension code is received during slave device operation.

19.5.4 $\overline{\text{ACK}}$

$\overline{\text{ACK}}$ is used to confirm the serial data status of the transmitting and receiving devices.

The receiving device returns $\overline{\text{ACK}}$ for every 8 bits of data it receives.

The transmitting device normally receives $\overline{\text{ACK}}$ after transmitting 8 bits of data. When $\overline{\text{ACK}}$ is returned from the receiving device, the reception is judged as normal and processing continues. The detection of $\overline{\text{ACK}}$ is confirmed with the IICS0.ACKD0 bit.

When the master device is the receiving device, after receiving the final data, it does not return $\overline{\text{ACK}}$ and generates the stop condition. When the slave device is the receiving device and does not return $\overline{\text{ACK}}$, the master device generates either a stop condition or a restart condition, and then stops the current transmission. Failure to return $\overline{\text{ACK}}$ may be caused by the following factors.

(a) Reception was not performed normally.
(b) The final data was received.
(c) The receiving device (slave) does not exist for the specified address.

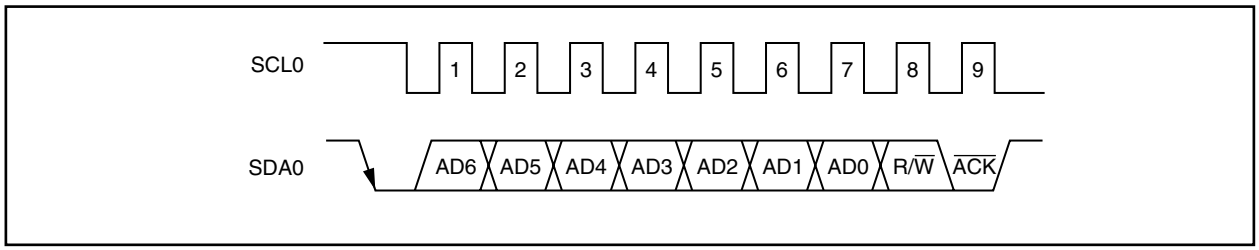
When the receiving device sets the SDA0 line to low level during the ninth clock, $\overline{\text{ACK}}$ is generated (normal reception).

When the IICC0.ACKE0 bit is set to 1, automatic $\overline{\text{ACK}}$ generation is enabled. Transmission of the eighth bit following the 7 address data bits causes the IICS0.TRC0 bit to be set. Normally, set the ACKE0 bit to 1 for reception (TRC0 bit = 0).

When the slave device is receiving (when TRC0 bit = 0), if the slave device cannot receive data or does not need to receive any more data, clear the ACKE0 bit to 0 to indicate to the master that no more data can be received.

Similarly, when the master device is receiving (when TRC0 bit = 0) and the subsequent data is not needed, clear the ACKE0 bit to 0 to prevent $\overline{\text{ACK}}$ from being generated. This notifies the slave device (transmitting device) of the end of the data transmission (transmission stopped).

Figure 19-8. $\overline{\text{ACK}}$



When the local address is received, $\overline{\text{ACK}}$ is automatically generated regardless of the value of the ACKE0 bit. No $\overline{\text{ACK}}$ is generated if the received address is not a local address (NACK).

When receiving the extension code, set the ACKE0 bit to 1 in advance to generate $\overline{\text{ACK}}$.

The $\overline{\text{ACK}}$ generation method during data reception is based on the wait timing setting, as described by the following.

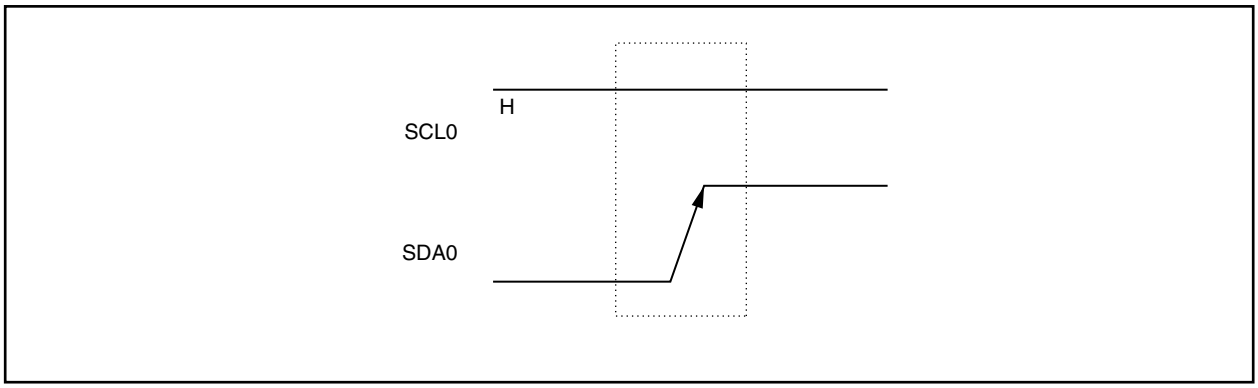
- When 8-clock wait is selected (IICC0.WTIM0 bit = 0):
  $\overline{\text{ACK}}$ is generated at the falling edge of the SCL0n pin's eighth clock if the ACKE0 bit is set to 1 before the wait state cancellation.
- When 9-clock wait is selected (IICC0.WTIM0 bit = 1):
  $\overline{\text{ACK}}$ is generated if the ACKE0 bit is set to 1 in advance.

19.5.5 Stop condition

When the SCL0 pin is at high level, changing the SDA0 pin from low level to high level generates a stop condition.

A stop condition is generated when serial transfer from the master device to the slave device has been completed. Stop conditions can be detected when the device is used as a slave.

Figure 19-9. Stop Condition



A stop condition is generated when the IICC0.SPT0 bit is set to 1. When the stop condition is detected, the IICS0.SPD0 bit is set to 1 and the interrupt request signal (INTIIC0) is generated when the IICC0.SPIE0 bit is set to 1.

19.5.6 Wait state

The wait state is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCL0 pin to low level notifies the communication partner of the wait status. When wait status has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 19-10. Wait State (1/2)

(a) When master device has a nine-clock wait and slave device has an eight-clock wait (master: transmission, slave: reception, and IICC0.ACKE0 bit = 1)

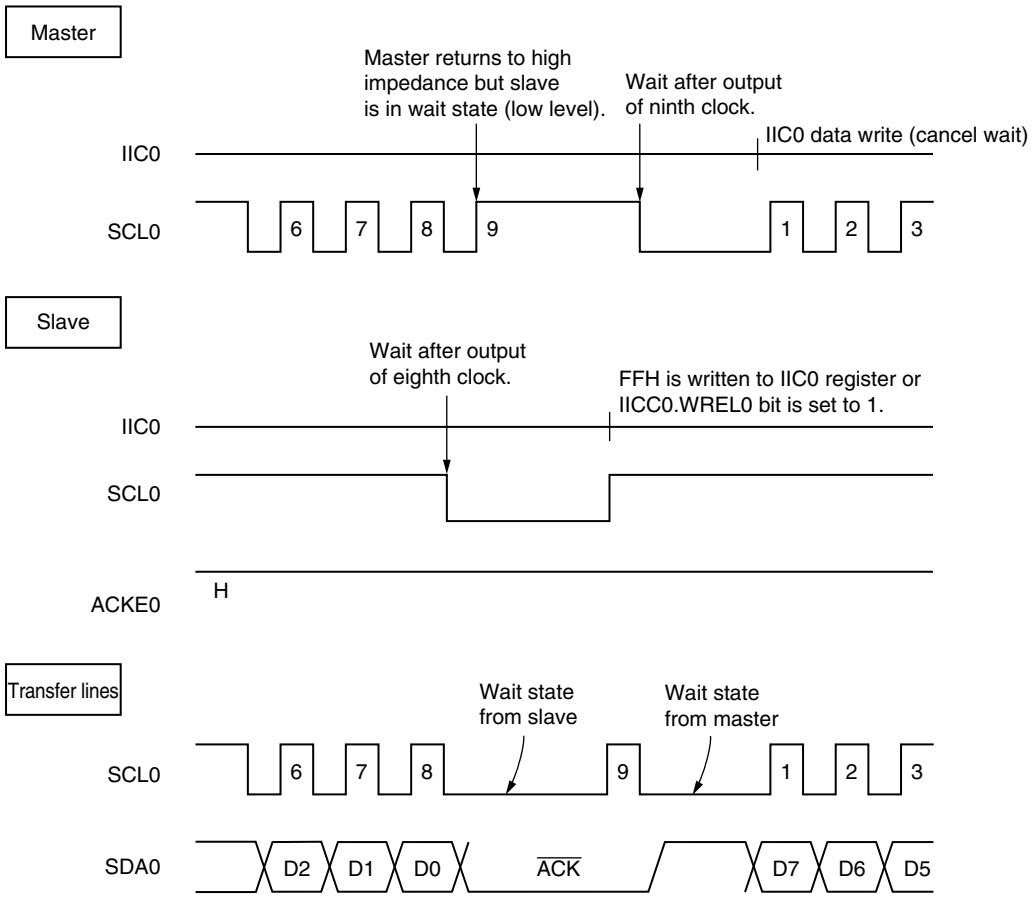
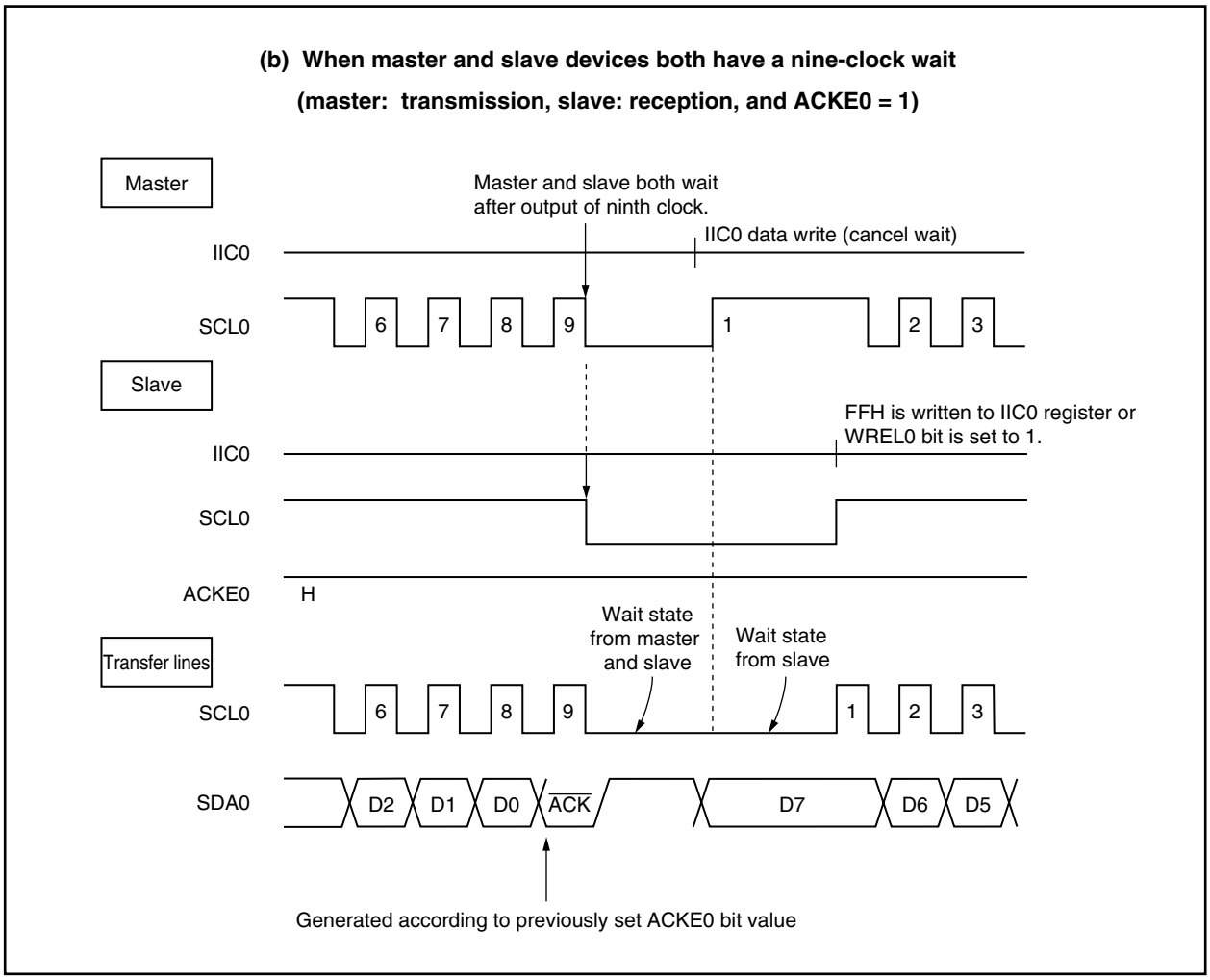


Figure 19-10. Wait State (2/2)



A wait state is automatically generated after a start condition is generated. Moreover, a wait state is automatically generated depending on the setting of the IICC0.WTIM0 bit.

Normally, when the IICC0.WREL0 bit is set to 1 or when FFH is written to the IIC0 register, the wait status is canceled and the transmitting side writes data to the IIC0 register to cancel the wait status.

The master device can also cancel the wait status via either of the following methods.

- By setting the IICC0.STT0 bit to 1
- By setting the IICC0.SPT0 bit to 1

19.5.7 Wait state cancellation method

In the case of I²C0, wait state can be canceled normally in the following ways.

- By writing data to the IIC0 register
- By setting the IICC0.WREL0 bit to 1 (wait state cancellation)
- By setting the IICC0.STT0 bit to 1 (start condition generation)[Note]
- By setting the IICC0.SPT0 bit to 1 (stop condition generation)[Note]

Note Master only

If any of these wait state cancellation actions is performed, I²C0 will cancel wait state and restart communication.

When canceling wait state and sending data (including address), write data to the IIC0 register.

To receive data after canceling wait state, or to complete data transmission, set the WREL0 bit to 1.

To generate a restart condition after canceling wait state, set the STT0 bit to 1.

To generate a stop condition after canceling wait state, set the SPT0 bit to 1.

Execute cancellation only once for each wait state.

For example, if data is written to the IIC0 register following wait state cancellation by setting the WREL0 bit to 1, conflict between the SDA0 line change timing and IIC0 register write timing may result in the data output to the SDA0 line may be incorrect.

Even in other operations, if communication is stopped halfway, clearing the IICC0.IICE0 bit to 0 will stop communication, enabling wait state to be cancelled.

If the I²C bus dead-locks due to noise, etc., setting the IICC0.LREL0 bit to 1 causes the communication operation to be exited, enabling wait state to be cancelled.

19.6 I²C Interrupt Request Signals (INTIIC0)

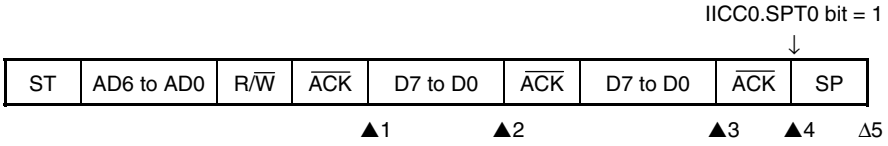
The following shows the value of the IICS0 register at the INTIIC0 interrupt request signal generation timing and at the INTIIC0 signal timing.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

19.6.1 Master device operation

(1) Start ~ Address ~ Data ~ Data ~ Stop (normal transmission/reception)

<1> When IICC0.WTIM0 bit = 0



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X000B

▲3: IICS0 register = 1000X000B (WTIM0 bit = 1[Note])

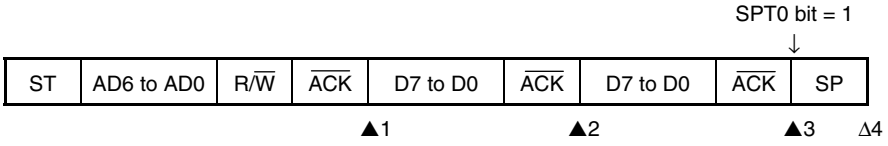
▲4: IICS0 register = 1000XX00B

Δ 5: IICS0 register = 00000001B

Note To generate a stop condition, set the WTIM0 bit to 1 and change the timing of the generation of the interrupt request signal (INTIIC0).

Remark ▲: Always generated
Δ: Generated only when IICC0.SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X100B

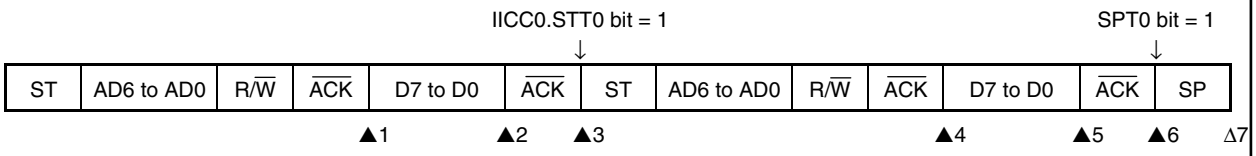
▲3: IICS0 register = 1000XX00B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(2) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

<1> When WTIM0 bit = 0



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X000B (WTIM0 bit = 1[Note 1])

▲3: IICS0 register = 1000XX00B (WTIM0 bit = 0[Note 2])

▲4: IICS0 register = 1000X110B

▲5: IICS0 register = 1000X000B (WTIM0 bit = 1[Note 3])

▲6: IICS0 register = 1000XX00B

Δ 7: IICS0 register = 00000001B

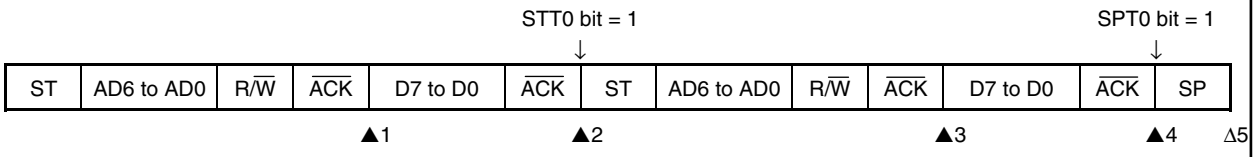
Notes 1. To generate a start condition, set the WTIM0 bit to 1 and change the timing of the generation of the interrupt request signal (INTIIC0).

2. Clear the WTIM0 bit to 0 to make the settings original.

3. To generate a stop condition, set the WTIM0 bit to 1 and change the timing of the generation of the interrupt request signal (INTIIC0).

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000XX00B

▲3: IICS0 register = 1000X110B

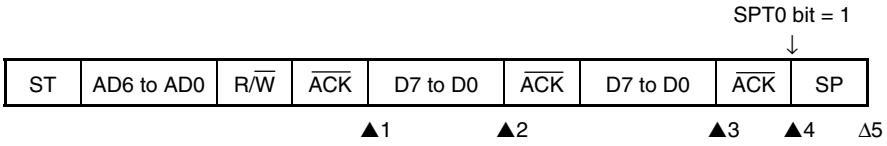
▲4: IICS0 register = 1000XX00B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(3) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

<1> When WTIM0 bit = 0



▲1: IICS0 register = 1010X110B

▲2: IICS0 register = 1010X000B

▲3: IICS0 register = 1010X000B (WTIM0 bit = 1[Note])

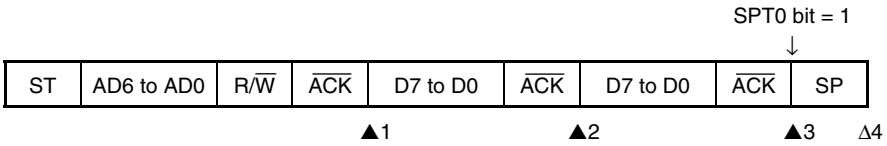
▲4: IICS0 register = 1010XX00B

Δ 5: IICS0 register = 00000001B

Note To generate a stop condition, set the WTIM0 bit to 1 and change the timing of the generation of the interrupt request signal (INTIIC0).

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1010X110B

▲2: IICS0 register = 1010X100B

▲3: IICS0 register = 1010XX00B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

19.6.2 Slave device operation (when receiving slave address data (address match))

(1) Start ~ Address ~ Data ~ Data ~ Stop

<1> When IICC0.WTIM0 bit = 0

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001X000B

▲3: IICS0 register = 0001X000B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when IICC0.SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001X100B

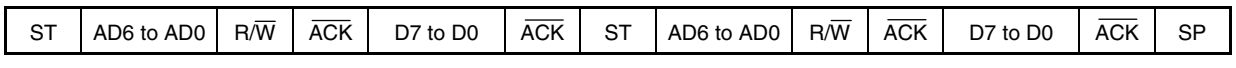
▲3: IICS0 register = 0001XX00B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(2) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, address match)



▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001X000B

▲3: IICS0 register = 0001X110B

▲4: IICS0 register = 0001X000B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1 (after restart, address match)

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001XX00B

▲3: IICS0 register = 0001X110B

▲4: IICS0 register = 0001XX00B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

(3) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2				▲3		▲4	Δ5

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001X000B

▲3: IICS0 register = 0010X010B

▲4: IICS0 register = 0010X000B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2				▲3	▲4		▲5 Δ6

▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001XX00B

▲3: IICS0 register = 0010X010B

▲4: IICS0 register = 0010X110B

▲5: IICS0 register = 0010XX00B

Δ 6: IICS0 register = 00000001B

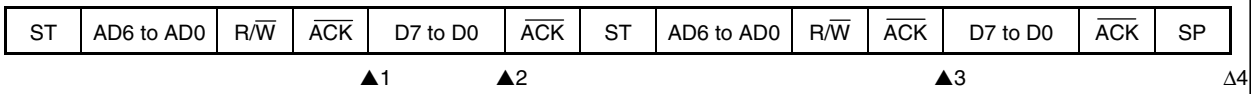
Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

(4) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, address mismatch (= not extension code))



▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001X000B

▲3: IICS0 register = 00000110B

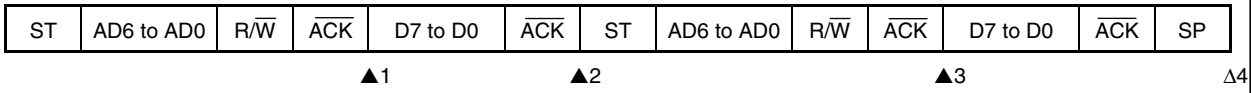
Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1 (after restart, address mismatch (= not extension code))



▲1: IICS0 register = 0001X110B

▲2: IICS0 register = 0001XX00B

▲3: IICS0 register = 00000110B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

19.6.3 Slave device operation (when receiving extension code)

Always under communication when receiving the extension code.

(1) Start ~ Code ~ Data ~ Data ~ Stop

<1> When IICC0.WTIM0 bit = 0

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0010X000B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when IICC0.SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010X100B

▲4: IICS0 register = 0010XX00B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(2) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, address match)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0001X110B

▲4: IICS0 register = 0001X000B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1 (after restart, address match)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 ▲5 Δ6

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010XX00B

▲4: IICS0 register = 0001X110B

▲5: IICS0 register = 0001XX00B

Δ 6: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

(3) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2				▲3		▲4	Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0010X010B

▲4: IICS0 register = 0010X000B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1 (after restart, extension code reception)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3			▲4	▲5		▲6 Δ7

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010XX00B

▲4: IICS0 register = 0010X010B

▲5: IICS0 register = 0010X110B

▲6: IICS0 register = 0010XX00B

Δ 7: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM0 bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 00000110B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0010X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010XX00B

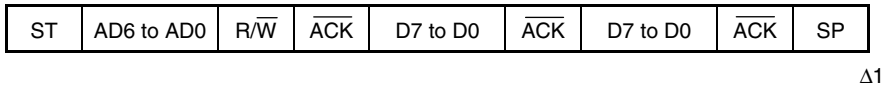
▲4: IICS0 register = 00000110B

Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

19.6.4 Operation without communication

(1) Start ~ Code ~ Data ~ Data ~ Stop



Δ 1: IICS0 register = 00000001B

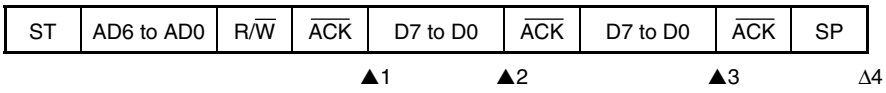
Remark Δ: Generated only when IICC0.SPIE0 bit = 1

19.6.5 Arbitration loss operation (operation as slave after arbitration loss)

When used as master in the multi-master system, check the arbitration result by reading the IICS0.MSTS0 bit for checking arbitration result by each INTIIC0 interrupt occurrence.

(1) When arbitration loss occurs during transmission of slave address data

<1> When IICC0.WTIM0 bit = 0



▲1: IICS0 register = 0101X110B

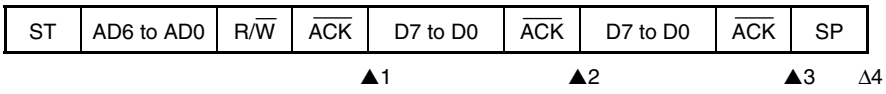
▲2: IICS0 register = 0001X000B

▲3: IICS0 register = 0001X000B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when IICC0.SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 0101X110B

▲2: IICS0 register = 0001X100B

▲3: IICS0 register = 0001XX00B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(2) When arbitration loss occurs during transmission of extension code

<1> When WTIM0 bit = 0

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICS0 register = 0110X010B

▲2: IICS0 register = 0010X000B

▲3: IICS0 register = 0010X000B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICS0 register = 0110X010B

▲2: IICS0 register = 0010X110B

▲3: IICS0 register = 0010X100B

▲4: IICS0 register = 0010XX00B

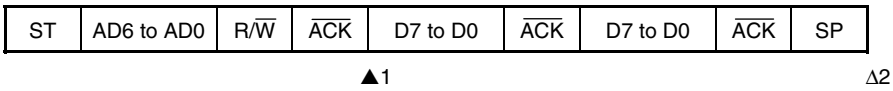
Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

19.6.6 Operation when arbitration loss occurs (no communication after arbitration loss)

When used as master in the multi-master system, check the arbitration result by reading the IICS0.MSTS0 bit for checking arbitration result by each INTIIC0 interrupt occurrence.

(1) When arbitration loss occurs during transmission of slave address data



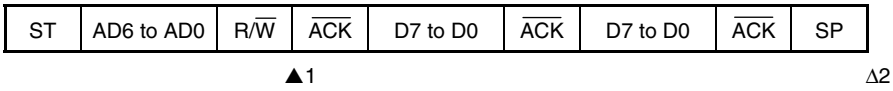
▲1 Δ2

▲1: IICS0 register = 01000110B

Δ 2: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when IICC0.SPIE0 bit = 1

(2) When arbitration loss occurs during transmission of extension code



▲1 Δ2

▲1: IICS0 register = 0110X010B

IICC0.LREL0 bit is set to 1 by software

Δ 2: IICS0 register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(3) When arbitration loss occurs during data transfer

<1> When IICC0.WTIM0 bit = 0

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 Δ3

▲1: IICS0 register = 10001110B

▲2: IICS0 register = 01000000B

Δ 3: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

<2> When WTIM0 bit = 1

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 Δ3

▲1: IICS0 register = 10001110B

▲2: IICS0 register = 01000100B

Δ 3: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

(4) When arbitration loss occurs due to restart condition during data transfer

<1> Not extension code (Example: Address mismatch)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to Dn	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1					▲2			Δ3

▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 01000110B

Δ 3: IICS0 register = 00000001B

Remarks 1. ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

2. Dn = D6 to D0

<2> Extension code

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to Dn	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1					▲2			Δ3

▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 0110X010B

IICC0.LREL0 bit is set to 1 by software

Δ 3: IICS0 register = 00000001B

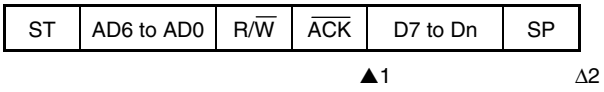
Remarks 1. ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

2. Dn = D6 to D0

(5) When arbitration loss occurs due to stop condition during data transfer



▲1 Δ2

▲1: IICS0 register = 1000X110B

Δ 2: IICS0 register = 01000001B

Remarks 1. ▲: Always generated

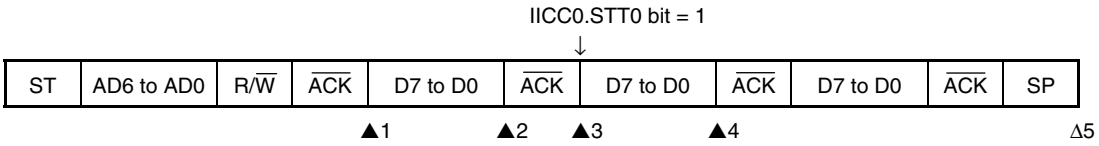
Δ: Generated only when SPIE0 bit = 1

X: don't care

2. Dn = D6 to D0

(6) When arbitration loss occurs due to low level of SDA0n pin when attempting to generate a restart condition

<1> When WTIM0 bit = 0



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X000B (WTIM0 bit = 1)

▲3: IICS0 register = 1000X100B (WTIM0 bit = 0)

▲4: IICS0 register = 01000000B

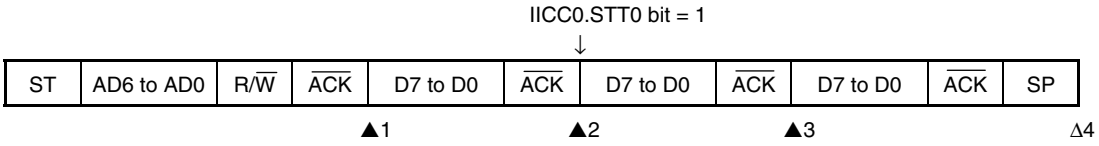
Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X100B

▲3: IICS0 register = 01000100B

Δ 4: IICS0 register = 00000001B

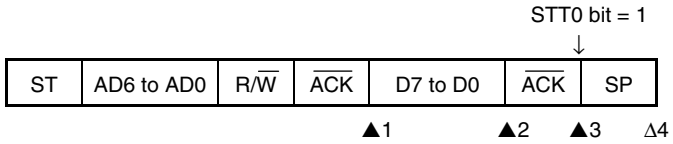
Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

(7) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

<1> When WTIM0 bit = 0



▲1: IICS0 register = 1000X110B

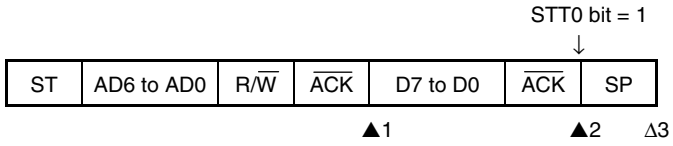
▲2: IICS0 register = 1000X000B (WTIM0 bit = 1)

▲3: IICS0 register = 1000XX00B

Δ 4: IICS0 register = 01000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1000X110B

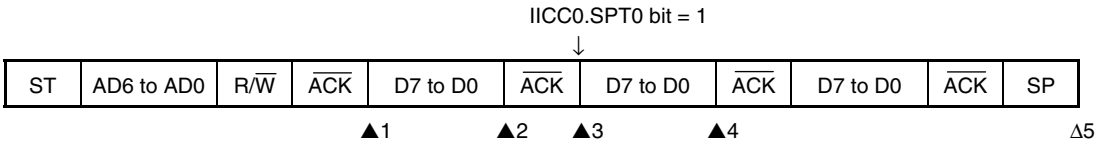
▲2: IICS0 register = 1000XX00B

Δ 3: IICS0 register = 01000001B

Remark ▲: Always generated
Δ: Generated only when SPIE0 bit = 1
X: don't care

(8) When arbitration loss occurs due to low level of SDA0n pin when attempting to generate a stop condition

<1> When WTIM0 bit = 0



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X000B (WTIM0 bit = 1)

▲3: IICS0 register = 1000X100B (WTIM0 bit = 0)

▲4: IICS0 register = 01000100B

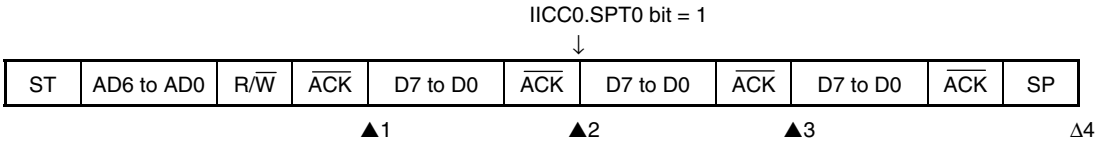
Δ 5: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

<2> When WTIM0 bit = 1



▲1: IICS0 register = 1000X110B

▲2: IICS0 register = 1000X100B

▲3: IICS0 register = 01000100B

Δ 4: IICS0 register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIE0 bit = 1

X: don't care

19.7 Interrupt Request Signal (INTIIC0) Generation Timing and Wait Control

The setting of the IICC0.WTIM0 bit determines the timing by which the INTIIC0 signal is generated and the corresponding wait control, as shown below.

Table 19-3. INTIIC0 Signal Generation Timing and Wait Control

WTIM0 Bit	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIIC0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the SVA0 register.
At this point, $\overline{ACK}$ is generated regardless of the value set to the IICC0.ACKE0 bit. For a slave device that has received an extension code, the INTIIC0 signal occurs at the falling edge of the eighth clock.
When the address does not match after restart, the INTIIC0 signal is generated at the falling edge of the ninth clock, but no wait occurs.

2. If the received address does not match the contents of the SVA0 register and extension codes have not been received, neither the INTIIC0 signal nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions in Notes 1 and 2 above regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- By writing data to the IIC0 register
- By setting the IICC0.WREL0 bit (canceling wait state)
- By setting the IICC0.STT0 bit (generating start condition)[Note]
- By setting the IICC0.SPT0 bit (generating stop condition)[Note]

Note Master only

When an 8-clock wait has been selected (WTIM0 bit = 0), whether or not $\overline{ACK}$ has been generated must be determined prior to wait cancellation.

(5) Stop condition detection

The INTIIC0 signal is generated when a stop condition is detected.

19.8 Address Match Detection Method

When in I²C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match detection is performed automatically by hardware. An INTIIC0 interrupt request signal occurs when a local address has been set to the SVA0 register and when the address set to the SVA0 register matches the slave address sent by the master device, or when an extension code has been received.

19.9 Error Detection

In I²C bus mode, the status of the serial data bus (SDA0) during data transmission is captured by the IIC0 register of the transmitting device, so the IIC0 register data prior to transmission can be compared with the transmitted IIC0 register data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

19.10 Extension Code

(1) When the higher 4 bits of the receive address are either 0000 or 1111, the extension code flag (EXC0) is set for extension code reception and an interrupt request signal (INTIIC0) is issued at the falling edge of the eighth clock. The local address stored in the SVA0 register is not affected.

(2) If 11110xx0 is set to the SVA0 register by a 10-bit address transfer and 11110xx0 is transferred from the master device, the results are as follows. Note that the INTIIC0 signal occurs at the falling edge of the eighth clock.

- Higher 4 bits of data match: IICS0.EXC0 bit = 1
- 7 bits of data match: IICS0.COI0 bit = 1

(3) Since the processing after the INTIIC0 signal occurs differs according to the data that follows the extension code, such processing is performed by software. The slave that has received an extension code is always under communication, even if the addresses mismatch.
For example, when operation as a slave is not desired after the extension code is received, set the IICC0.LREL0 bit to 1 and the CPU will enter the next communication wait state.

Table 19-4. Extension Code Bit Definitions

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General call address
0000 000	1	Start byte
0000 001	X	CBUS address
0000 010	X	Address that is reserved for different bus format
1111 0xx	X	10-bit slave address specification

19.11 Arbitration

When several master devices simultaneously generate a start condition (when the IICC0.STT0 bit is set to 1 before the IICS0.STD0 bit is set to 1), communication among the master devices is performed as the number of clocks is adjusted until the data differs. This kind of operation is called arbitration.

When one of the master devices loses in arbitration, an arbitration loss flag (IICS0.ALD0 bit) is set (1) via the timing by which the arbitration loss occurred, and the SCL0 and SDA0 lines are both set for high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request signal (INTIIC0) (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD0 bit = 1 setting that has been made by software.

For details of interrupt request timing, refer to **19.6 I²C Interrupt Request Signals (INTIIC0)**.

Figure 19-11. Arbitration Timing Example

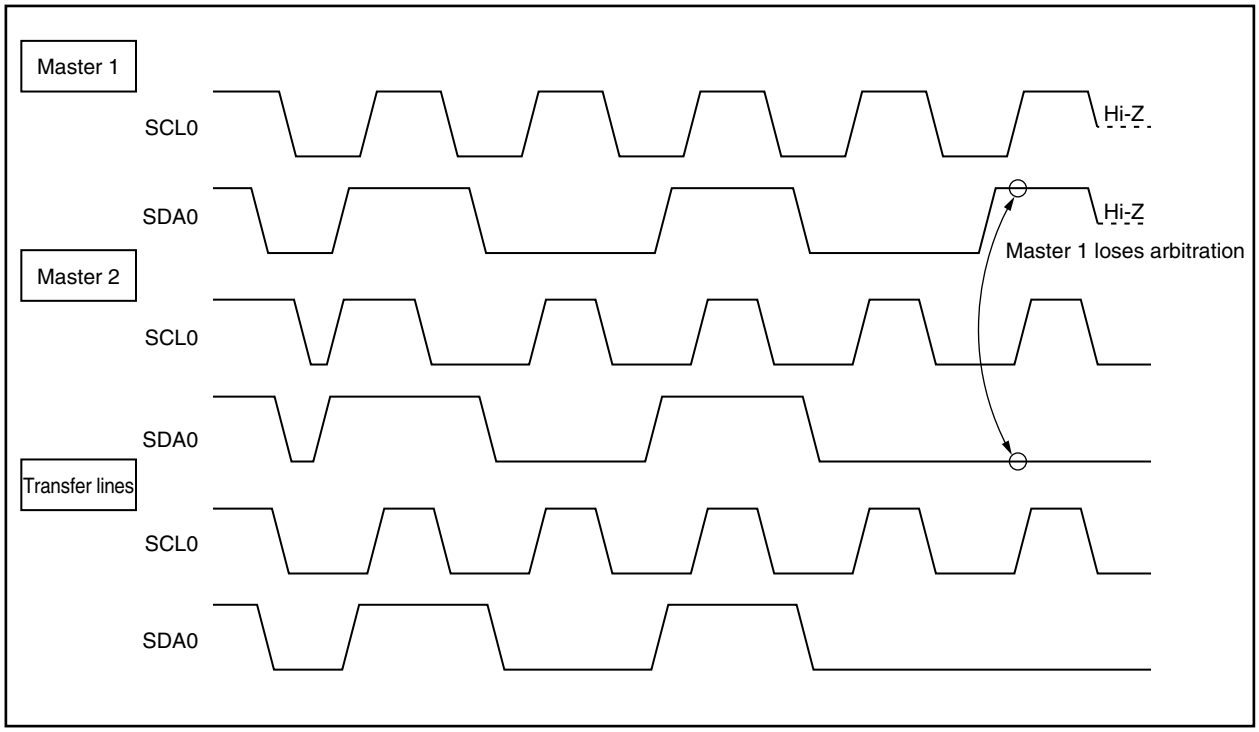


Table 19-5. Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer[Note 1]
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During $\overline{ACK}$ transfer period after data reception	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is generated (when IICC0.SPIE0 bit = 1)[Note 2]
When the SDA0 pin is at low level while attempting to generate a restart condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When stop condition is detected while attempting to generate a restart condition	When stop condition is generated (when SPIE0 bit = 1)[Note 2]
When the SDA0 pin is at low level while attempting to generate a stop condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When the SCL0 pin is at low level while attempting to generate a restart condition	

Notes 1. When the IICC0.WTIM0 bit = 1, an interrupt request occurs at the falling edge of the ninth clock. When the WTIM0 bit = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.

2. When there is a possibility that arbitration will occur, set the SPIE0 bit = 1 for master device operation.

19.12 Wakeup Function

The I²C bus slave function is a function that generates an interrupt request signal (INTIIC0) when a local address or extension code has been received.

This function makes processing more efficient by preventing unnecessary interrupt requests from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

However, when a stop condition is detected, the IICC0.SPIE0 bit is set regardless of the wake up function, and this determines whether interrupt requests are enabled or disabled.

19.13 Communication Reservation

19.13.1 When communication reservation function is enabled (IICF0.IICRSV0 bit = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released when the IICC0.LREL0 bit was set to “1”).

If the IICC0.STT0 bit is set (1) while the bus is not used, a start condition is automatically generated and wait status is set after the bus is released (after a stop condition is detected).

A communication is automatically started as the master by setting the IICC0.SPIE0 bit to 1, detecting the bus release due to an interrupt request (INTIIC0) occurrence (detecting a stop condition), and then writing the address to the IIC0 register. Before detecting a stop condition, data written to the IIC0 register is set to invalid.

When the STT0 bit has been set (1), the operation mode (as start condition or as communication reservation) is determined according to the bus status.

If the bus has been released.....a start condition is generated
If the bus has not been released (standby mode).....communication reservation

To detect which operation mode has been determined for the STT0 bit, set the STT0 bit (1), wait for the wait period, then check the IICS0.MSTS0 bit.

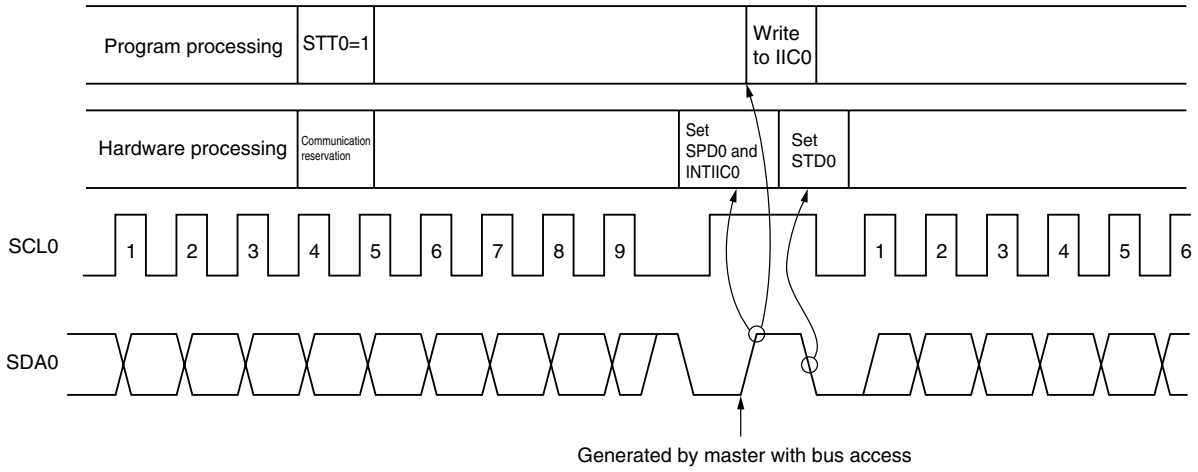
Wait periods, which should be set via software, are listed in Table 19-6. These wait periods can be set via the settings for the IICX0.CLX0, IICCL0.SMC0, IICCL0.CL01, and IICCL0.CL00 bits.

Table 19-6. Wait Periods

CLX0	SMC0	CL01	CL00	Selected Clock	Wait Period
0	0	0	0	$f_{XX}/2$	46 clocks
0	0	0	1	$f_{XX}/2$	86 clocks
0	0	1	0	f_{XX}	43 clocks
0	0	1	1	$f_{XX}/3$	102 clocks
0	1	0	1/0	$f_{XX}/2$	30 clocks
0	1	1	0	f_{XX}	15 clocks
0	1	1	1	$f_{XX}/3$	36 clocks
1	1	0	1/0	$f_{XX}/2$	18 clocks
1	1	1	0	f_{XX}	9 clocks

The communication reservation timing is shown below.

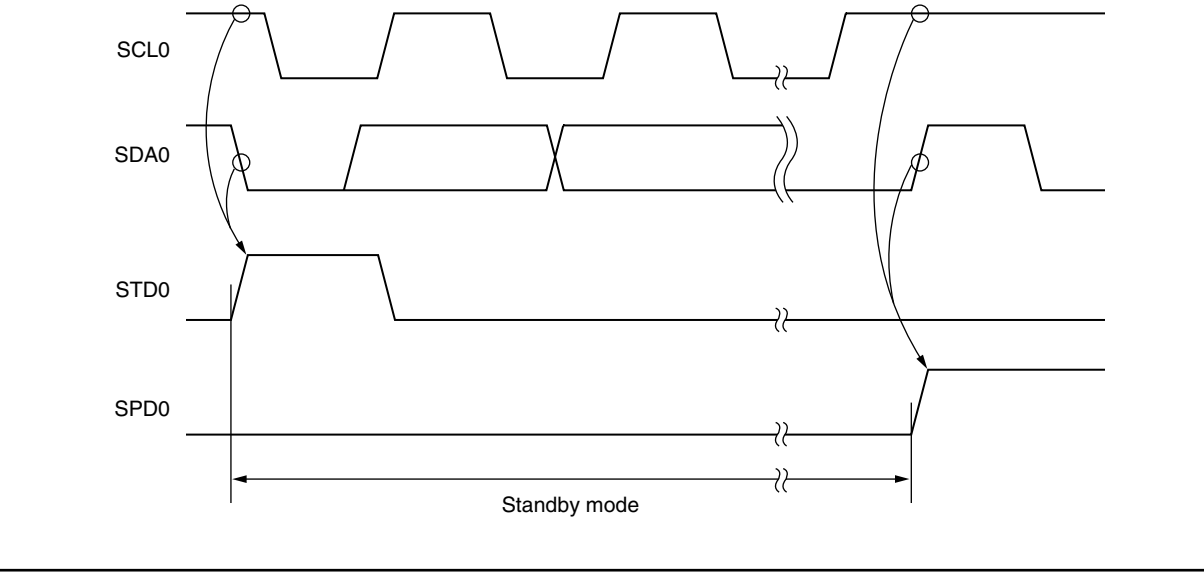
Figure 19-12. Communication Reservation Timing



IIC0: IIC shift register 0
STT0: Bit 1 of IIC control register 0 (IICC0)
STD0: Bit 1 of IIC status register 0 (IICS0)
SPD0: Bit 0 of IIC status register 0 (IICS0)

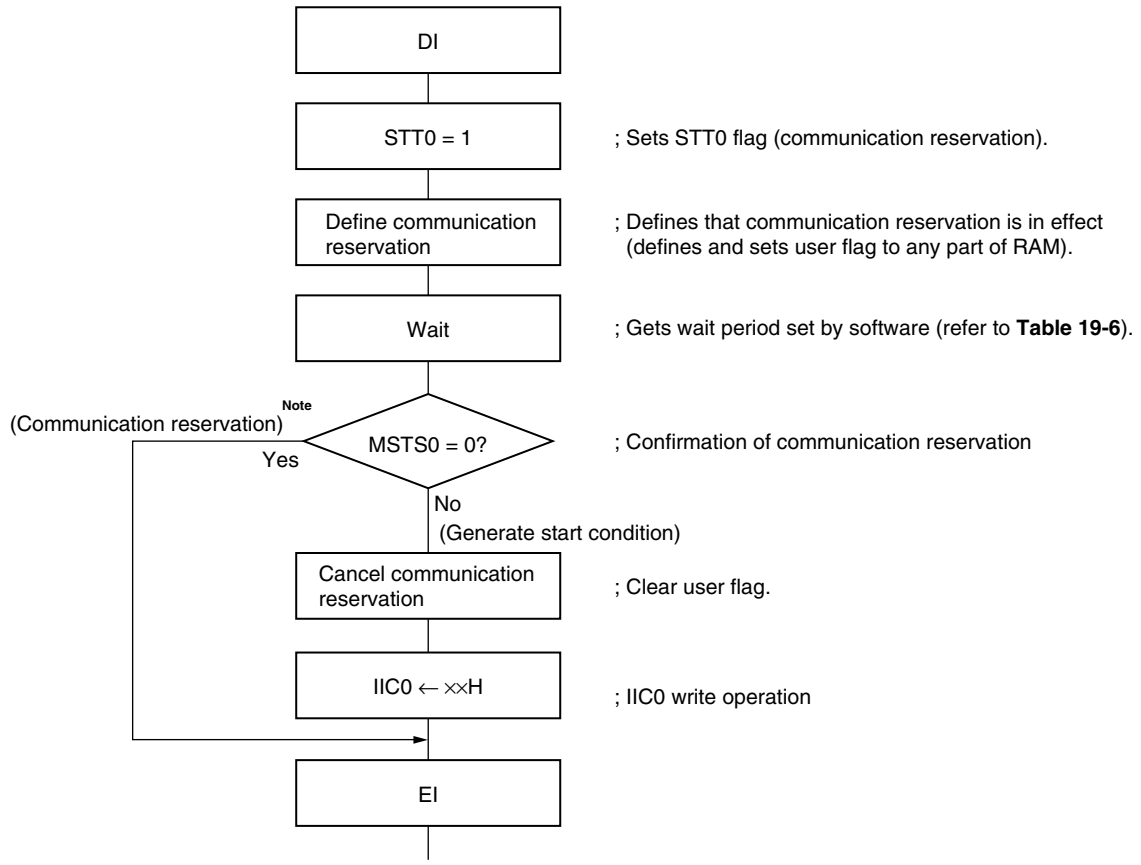
Communication reservations are accepted via the following timing. After the IICS0.STD0 bit is set to 1, a communication reservation can be made by setting the IICC0.STT0 bit to 1 before a stop condition is detected.

Figure 19-13. Timing for Accepting Communication Reservations



The communication reservation flowchart is illustrated below.

Figure 19-14. Communication Reservation Flowchart



Note The communication reservation operation executes a write to the IIC0 register when a stop condition interrupt request occurs.

19.13.2 When communication reservation function is disabled (IICF0.IICRSV0 bit = 1)

When the IICC0.STT0 bit is set when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released when the IICC0.LREL0 bit was set to 1)

To confirm whether the start condition was generated or request was rejected, check the IICF0.STCF0 flag. The time shown in Table 19-7 is required until the STCF0 flag is set after setting the STT0 bit = 1. Therefore, secure the time by software.

Table 19-7. Wait Periods

CL01	CL00	Selected Clock	Wait Period
0	0	$f_{XX}/2$	6 clocks
0	1	$f_{XX}/2$	6 clocks
1	0	f_{XX}	3 clocks
1	1	$f_{XX}/3$	9 clocks

19.14 Cautions

(1) When IICF0.STCEN0 bit = 0

Immediately after I²C0 operation is enabled, the bus communication status (IICF0.IICBSY0 bit = 1) is recognized regardless of the actual bus status. To execute master communication in the status where a stop condition has not been detected, generate a stop condition and then release the bus before starting the master communication.

Use the following sequence for generating a stop condition.

<1> Set the IICCL0 register.
<2> Set the IICC0.IICE0 bit.
<3> Set the IICC0.SPT0 bit.

(2) When IICF0.STCEN0 bit = 1

Immediately after I²C0 operation is enabled, the bus released status (IICBSY0 bit = 0) is recognized regardless of the actual bus status. To generate the first start condition (IICC0.STT0 bit = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) When the IICC0.IICE0 bit of the V850ES/KG2 is set to 1 while communications with other devices are in progress, the start condition may be detected depending on the status of the communication line. Be sure to set the IICC0.IICE0 bit to 1 when the SCL0 and SDA0 lines are high level.

(4) Determine the operation clock frequency by the IICCL0 and IICX0 registers before enabling the operation (IICC0.IICE0 bit = 1). To change the operation clock frequency, clear the IICC0.IICE0 bit to 0 once.

(5) After the IICC0.STT0 and IICC0.SPT0 bits have been set to 1, they must not be re-set without being cleared to 0 first.

(6) If transmission has been reserved, set the IICC0.SPIE0 bit to 1 so that an interrupt request is generated by the detection of a stop condition. After an interrupt request has been generated, the wait state will be released by writing communication data to I²C0, then transferring will begin. If an interrupt is not generated by the detection of a stop condition, transmission will halt in the wait state because an interrupt request was not generated. However, it is not necessary to set the SPIE0 bit to 1 for the software to detect the IICS0.MSTS0 bit.

19.15 Communication Operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the V850ES/KG2 as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I²C0 bus multimaster system, whether the bus is released or used cannot be judged by the I²C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the V850ES/KG2 takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the V850ES/KG2 looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

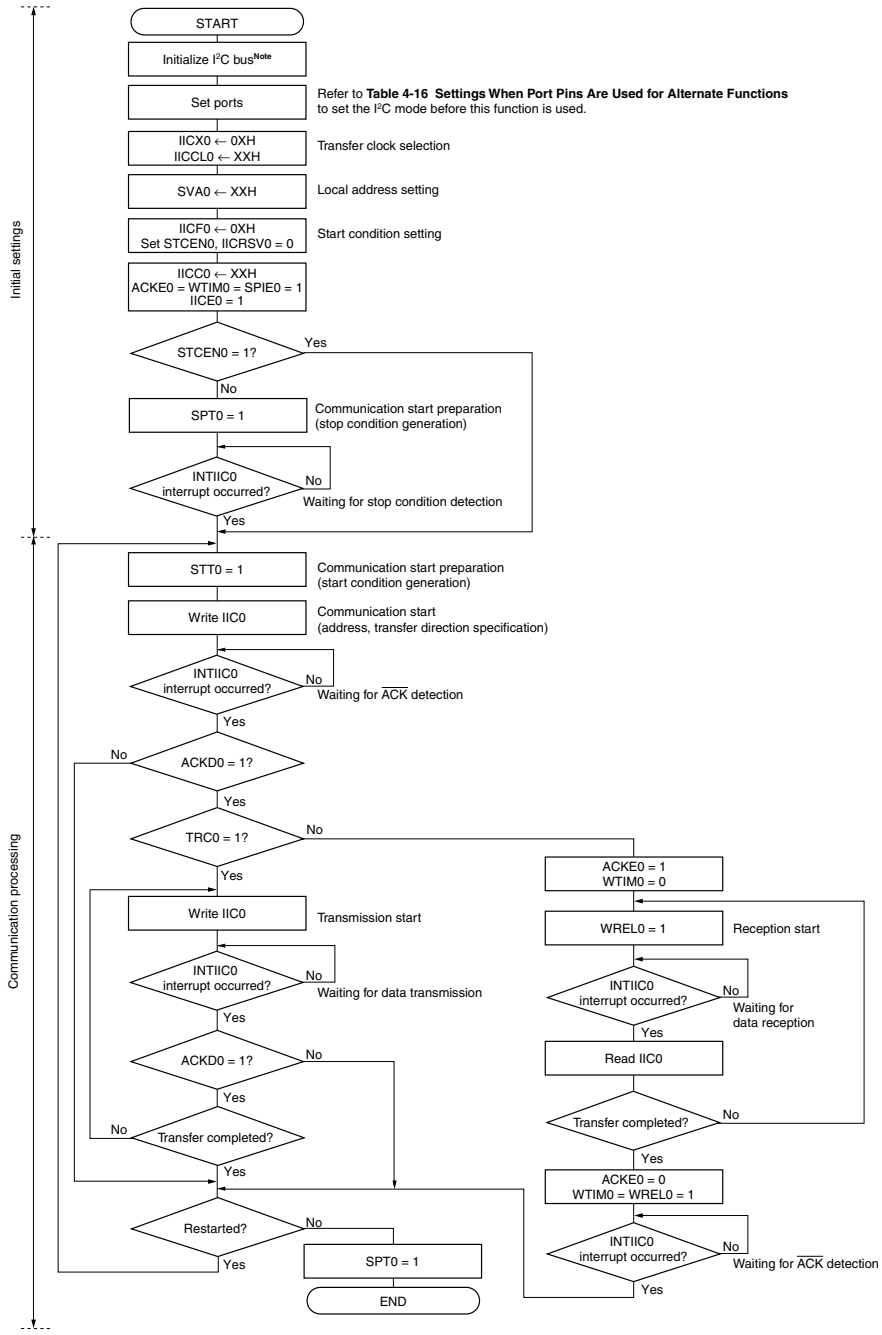
An example of when the V850ES/KG2 is used as the slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIIC0 interrupt occurrence (communication waiting). When the INTIIC0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

19.15.1 Master operation in single master system

Figure 19-15. Master Operation in Single Master System



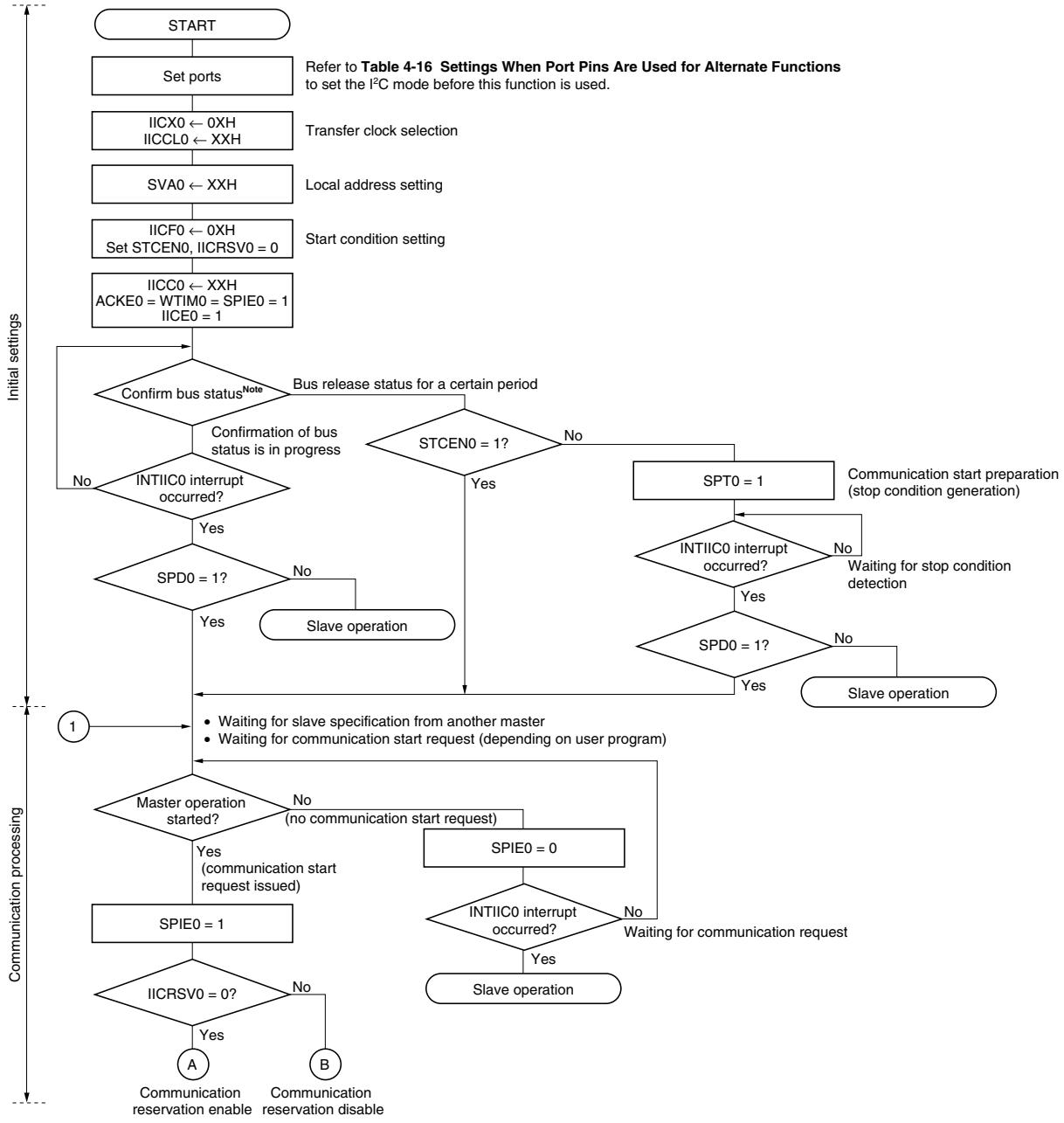
Note Release the I²C0 bus (SCL0, SDA0 pins = high level) in conformity with the specifications of the product in communication.

For example, when the EEPROM™ outputs a low level to the SDA0 pin, set the SCL0 pin to the output port and output clock pulses from that output port until when the SDA0 pin is constantly high level.

Remark For the transmission and reception formats, conform to the specifications of the product in communication.

19.15.2 Master operation in multimaster system

Figure 19-16. Master Operation in Multimaster System (1/3)



Note Confirm that the bus release status (IICCL0.CLD0 bit = 1, IICCL0.DAD0 bit = 1) has been maintained for a certain period (1 frame, for example). When the SDA0 pin is constantly low level, determine whether to release the I²C0 bus (SCL0, SDA0 pins = high level) by referring to the specifications of the product in communication.

Figure 19-16. Master Operation in Multimaster System (2/3)

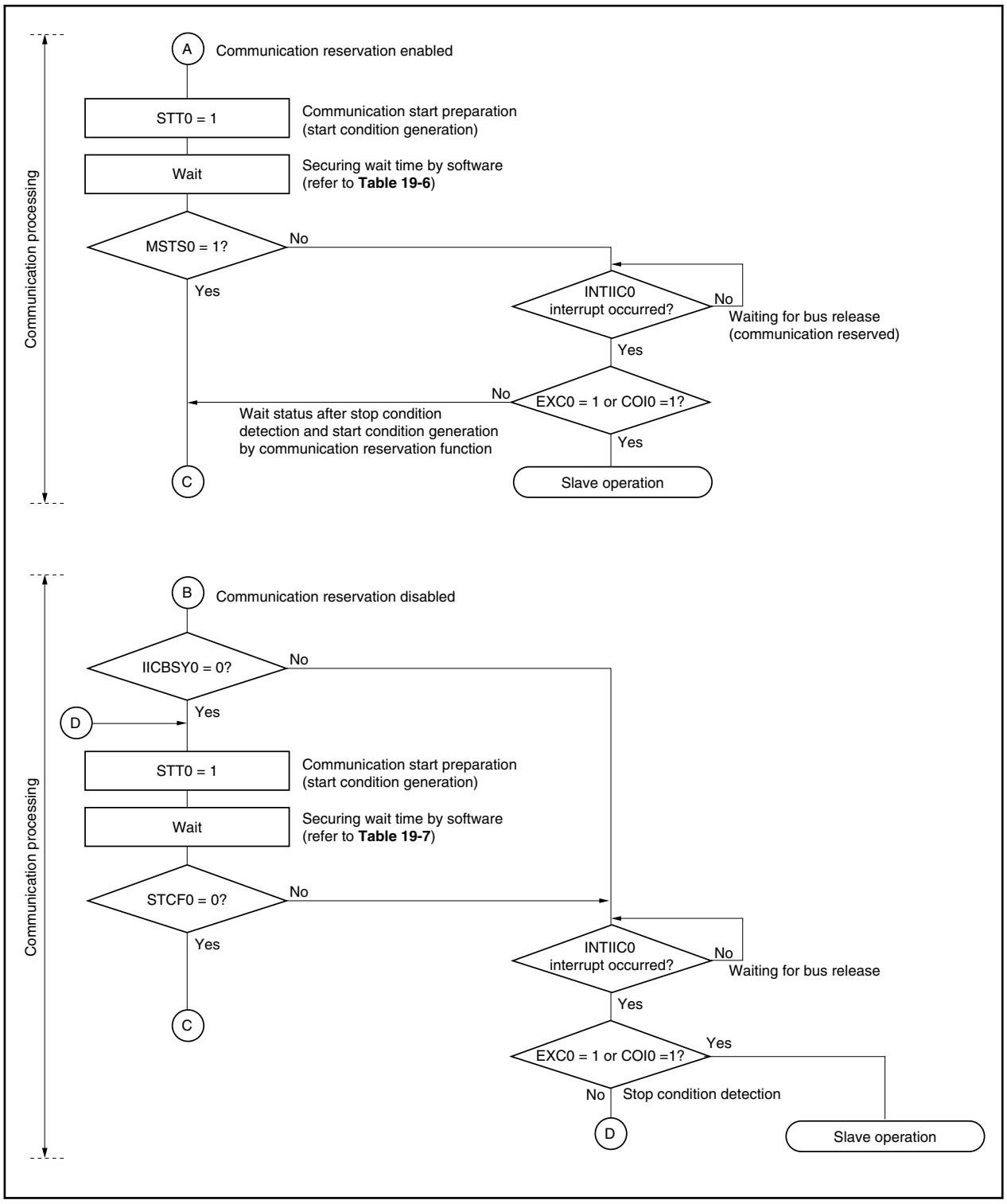
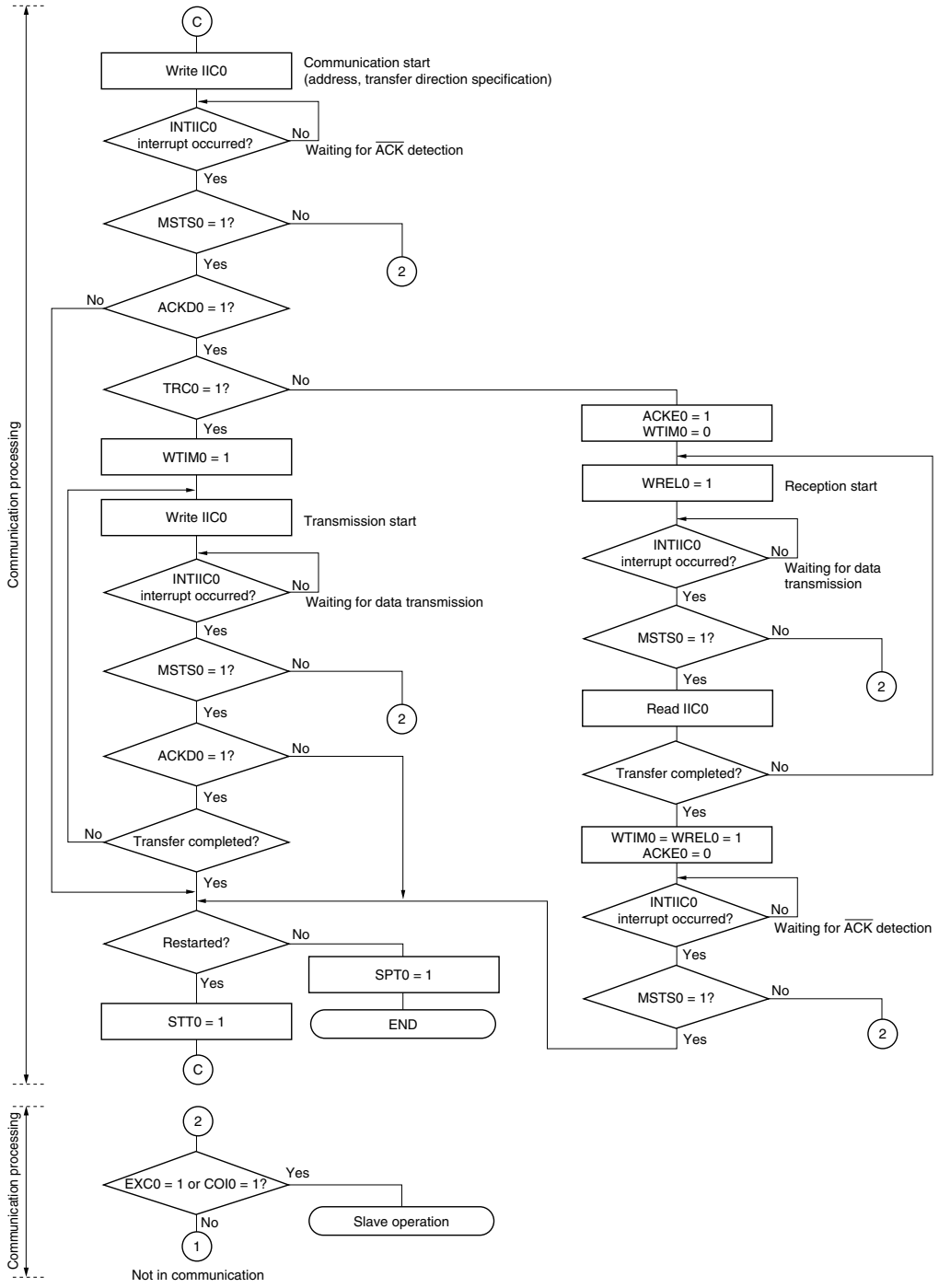


Figure 19-16. Master Operation in Multimaster System (3/3)



Remarks 1. Conform the transmission and reception formats to the specifications of the product in communication.

2. When using the V850ES/KG2 as the master in the multimaster system, read the IICS0.MSTS0 bit for each INTIIC0 interrupt occurrence to confirm the arbitration result.

3. When using the V850ES/KG2 as the slave in the multimaster system, confirm the status using the IICS0 and IICF0 registers for each INTIIC0 interrupt occurrence to determine the next processing.

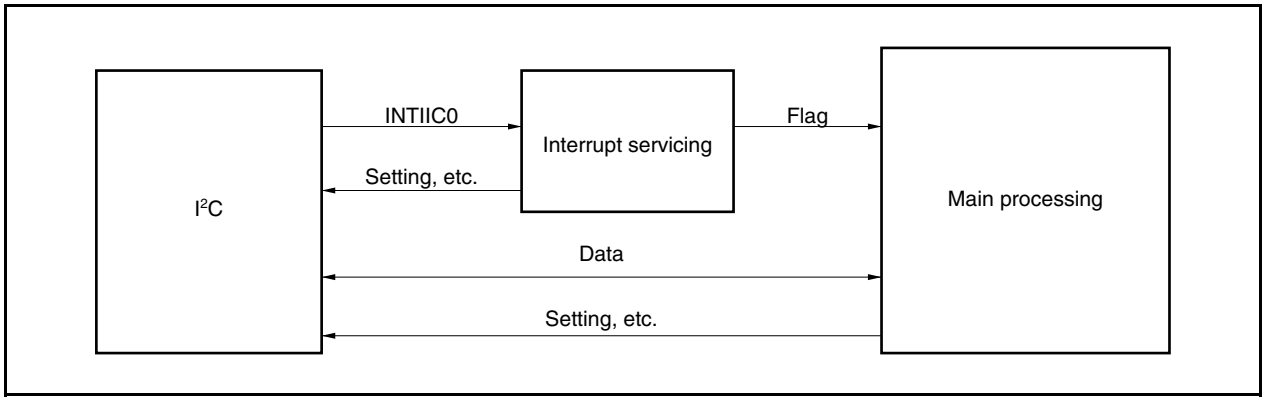
19.15.3 Slave operation

The following shows the processing procedure of the slave operation.

Basically, the operation of the slave device is event-driven. Therefore, processing by an INTIIC0 interrupt (processing requiring a significant change of the operation status, such as stop condition detection during communication) is necessary.

The following description assumes that data communication does not support extension codes. Also, it is assumed that the INTIIC0 interrupt servicing performs only status change processing and that the actual data communication is performed during the main processing.

Figure 19-17. Software Outline During Slave Operation



Therefore, the following three flags are prepared so that the data transfer processing can be performed by transmitting these flags to the main processing instead of the INTIIC0 signal.

(1) Communication mode flag

This flag indicates the following communication statuses.

Clear mode: Data communication not in progress

Communication mode: Data communication in progress (valid address detection stop condition detection, $\overline{\text{ACK}}$ from master not detected, address mismatch)

(2) Ready flag

This flag indicates that data communication is enabled. This is the same status as an INTIIC0 interrupt during normal data transfer. This flag is set in the interrupt processing block and cleared in the main processing block. The ready flag for the first data for transmission is not set in the interrupt processing block, so the first data is transmitted without clearance processing (the address match is regarded as a request for the next data).

(3) Communication direction flag

This flag indicates the direction of communication and is the same as the value of the IICS0.TRC0 bit.

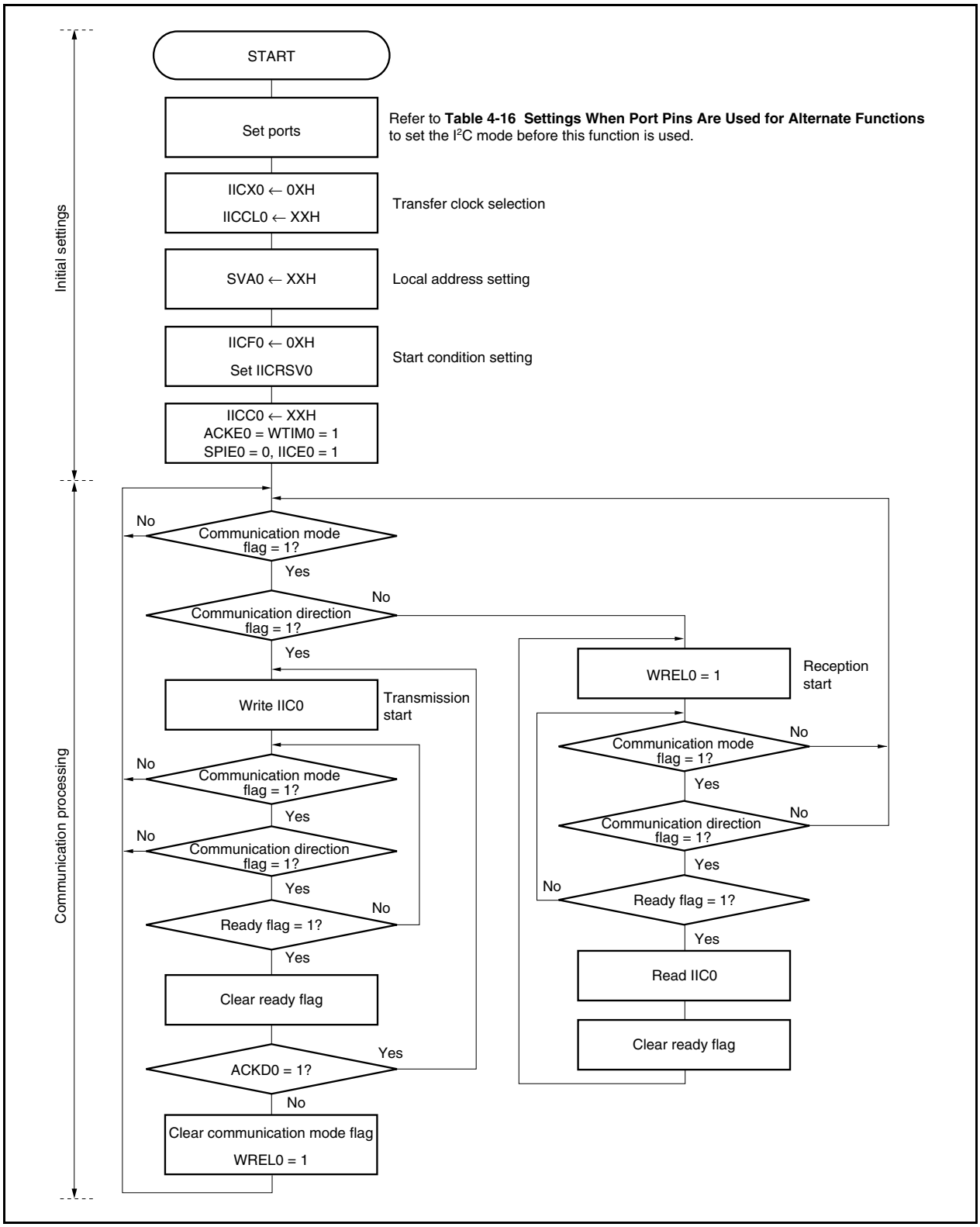
The following shows the operation of the main processing block during slave operation.

Start I²C0 and wait for the communication enabled status. When communication is enabled, perform transfer using the communication mode flag and ready flag (the processing of the stop condition and start condition is performed by interrupts, conditions are confirmed by flags).

For transmission, repeat the transmission operation until the master device stops returning $\overline{\text{ACK}}$. When the master device stops returning $\overline{\text{ACK}}$, transfer is complete.

For reception, receive the required number of data and do not return $\overline{ACK}$ for the next data immediately after transfer is complete. After that, the master device generates the stop condition or restart condition. This causes exit from communications.

Figure 19-18. Slave Operation Flowchart (1)



The following shows an example of the processing of the slave device by an INTIIC0 interrupt (it is assumed that no extension codes are used here). During an INTIIC0 interrupt, the status is confirmed and the following steps are executed.

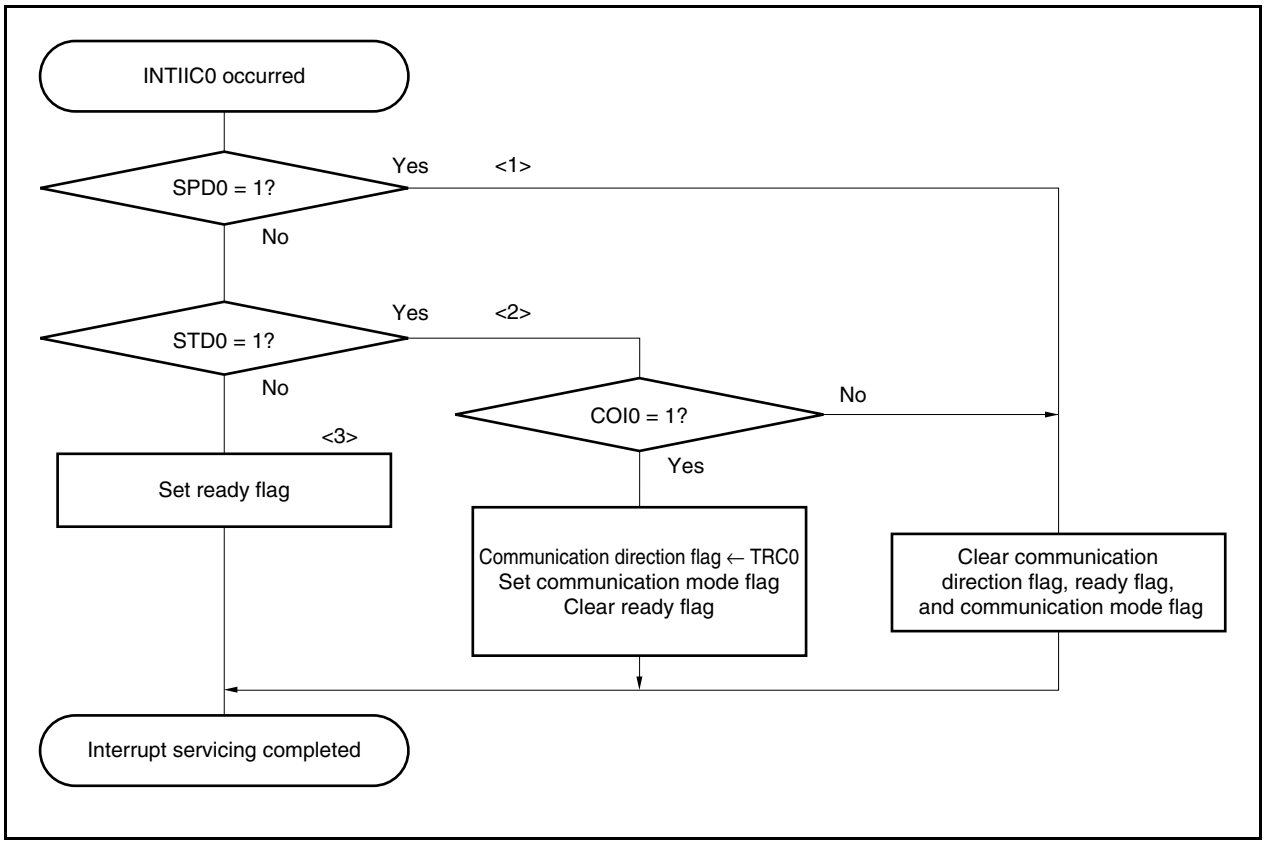
<1> When a stop condition is detected, communication is terminated.

<2> When a start condition is detected, the address is confirmed. If the address does not match, communication is terminated. If the address matches, the communication mode is set and wait is released, and operation returns from the interrupt (the ready flag is cleared).

<3> For data transmission/reception, when the ready flag is set, operation returns from the interrupt while the I²C0 bus remains in the wait status.

Remark <1> to <3> in the above correspond to <1> to <3> in **Figure 19-19 Slave Operation Flowchart (2)**.

Figure 19-19. Slave Operation Flowchart (2)



19.16 Timing of Data Communication

When using I²C bus mode, the master device generates an address via the serial bus to select one of several slave devices as its communication partner.

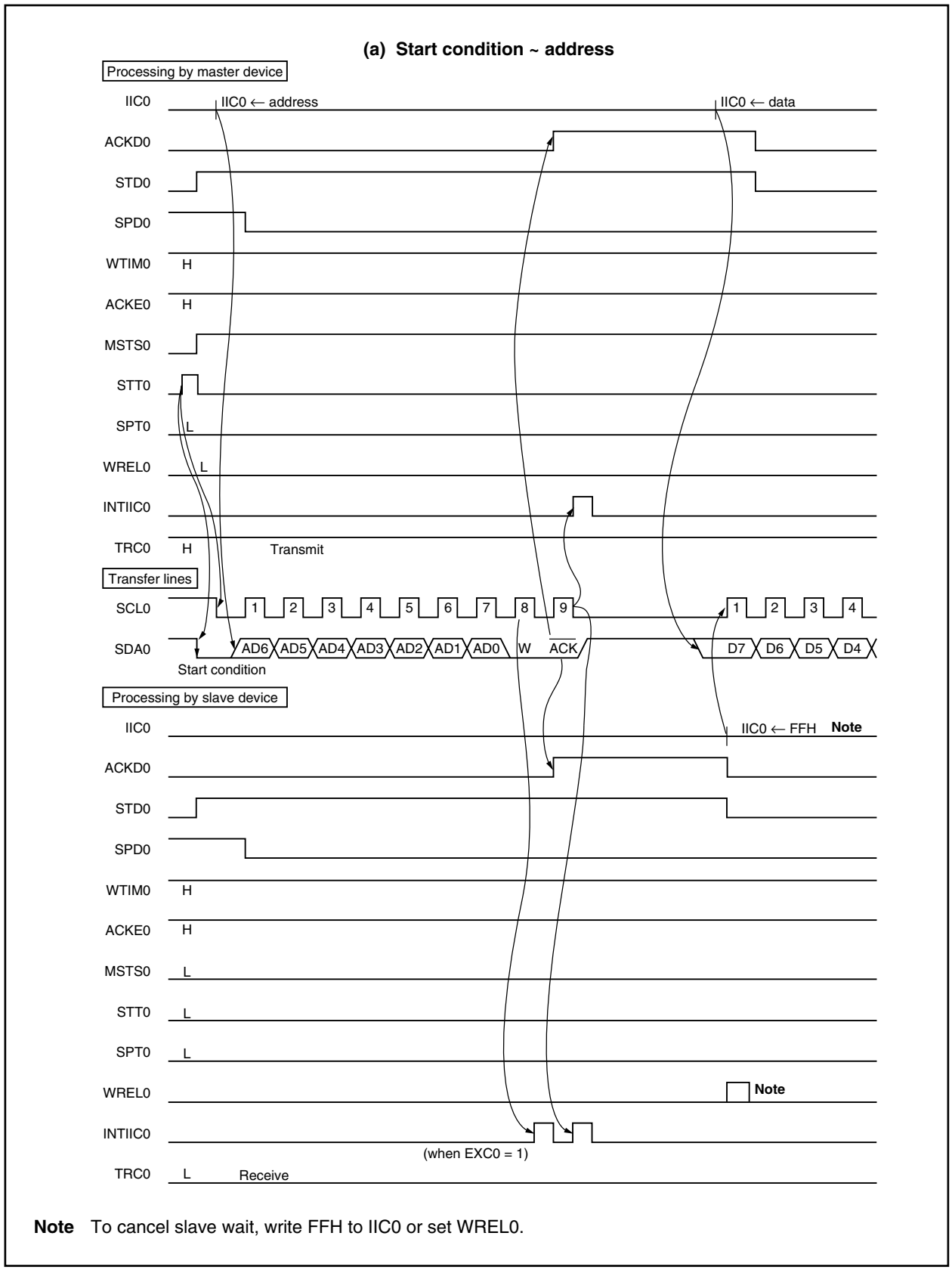
After outputting the slave address, the master device transmits the IICS0.TRC0 bit that specifies the data transfer direction and then starts serial communication with the slave device.

The IIC0 register's shift operation is synchronized with the falling edge of the serial clock (SCL0 pin). The transmit data is transferred to the SO latch and is output (MSB first) via the SDA0 pin.

Data input via the SDA0 pin is captured by the IIC0 register at the rising edge of the SCL0 pin.

The data communication timing is shown below.

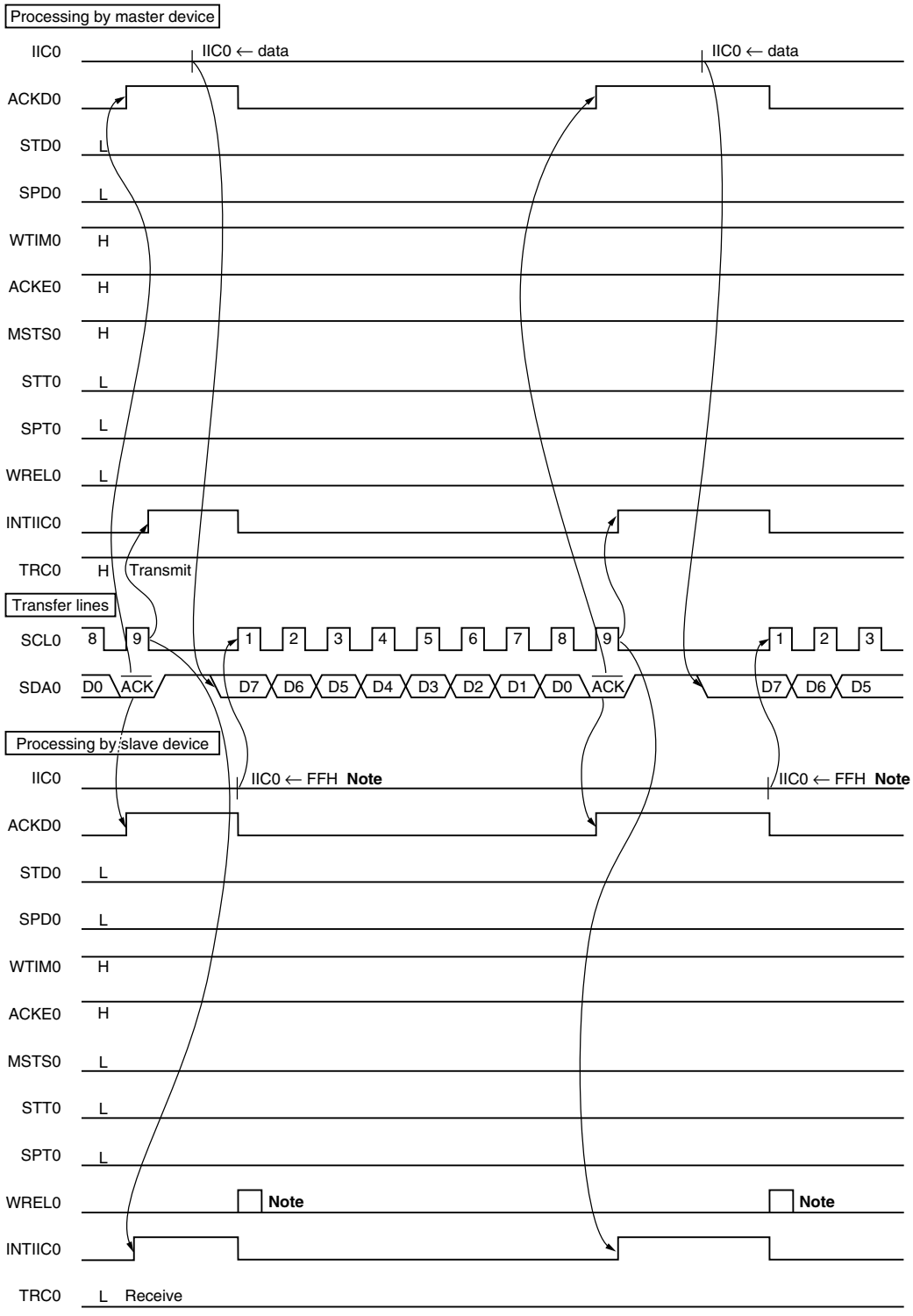
Figure 19-20. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel slave wait, write FFH to IIC0 or set WREL0.

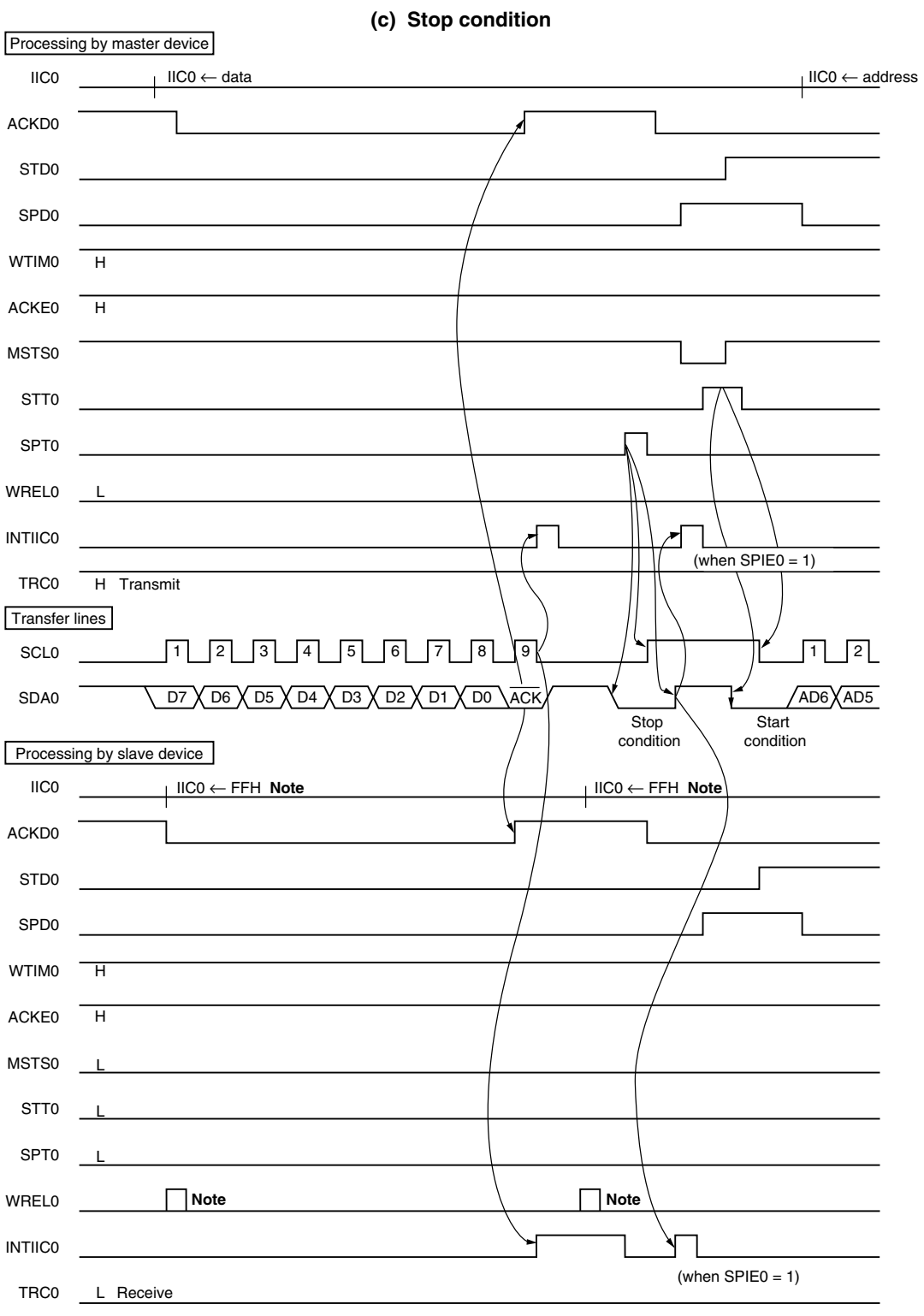
Figure 19-20. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

(b) Data



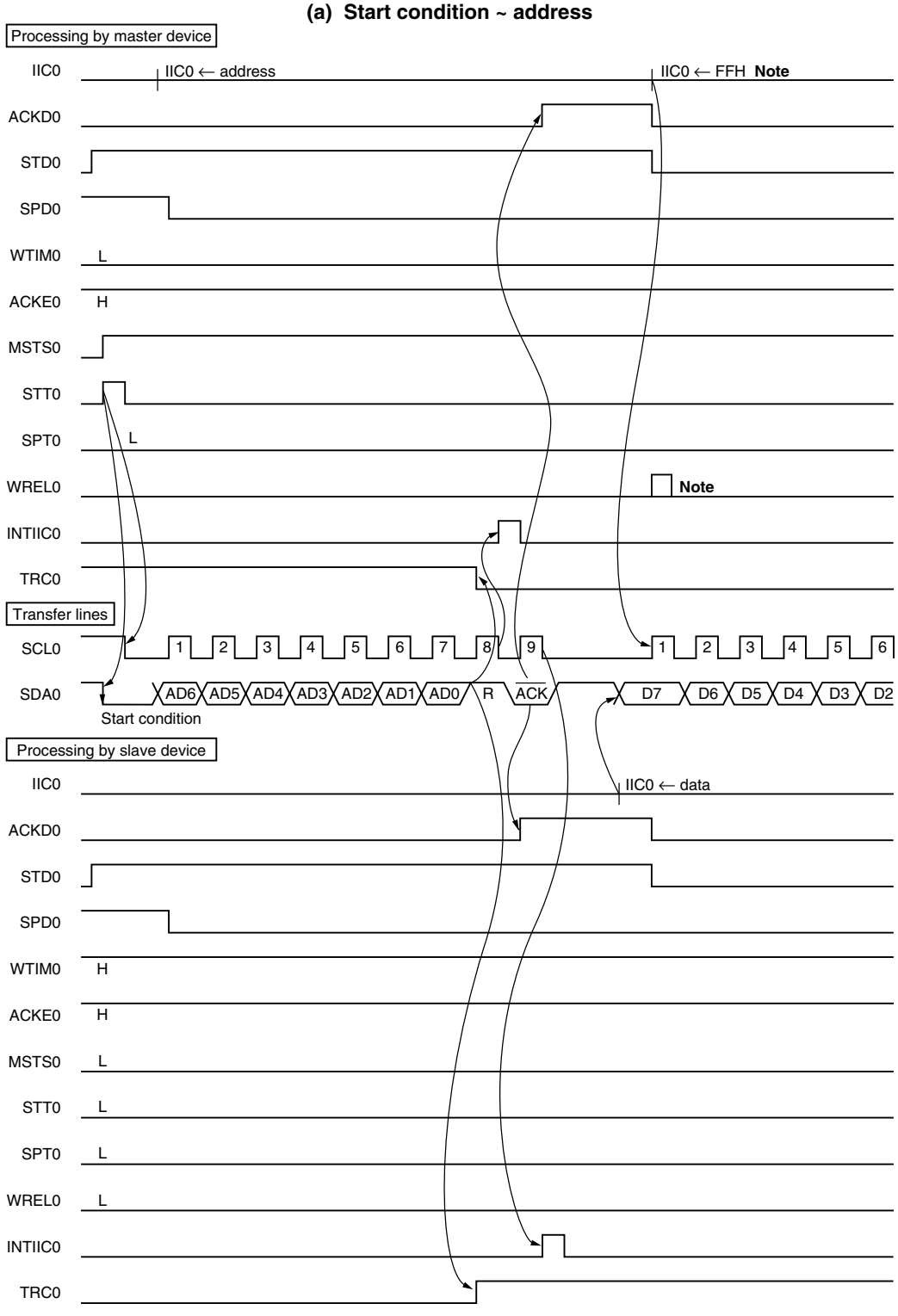
Note To cancel slave wait, write FFH to IIC0 or set WREL0.

Figure 19-20. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)



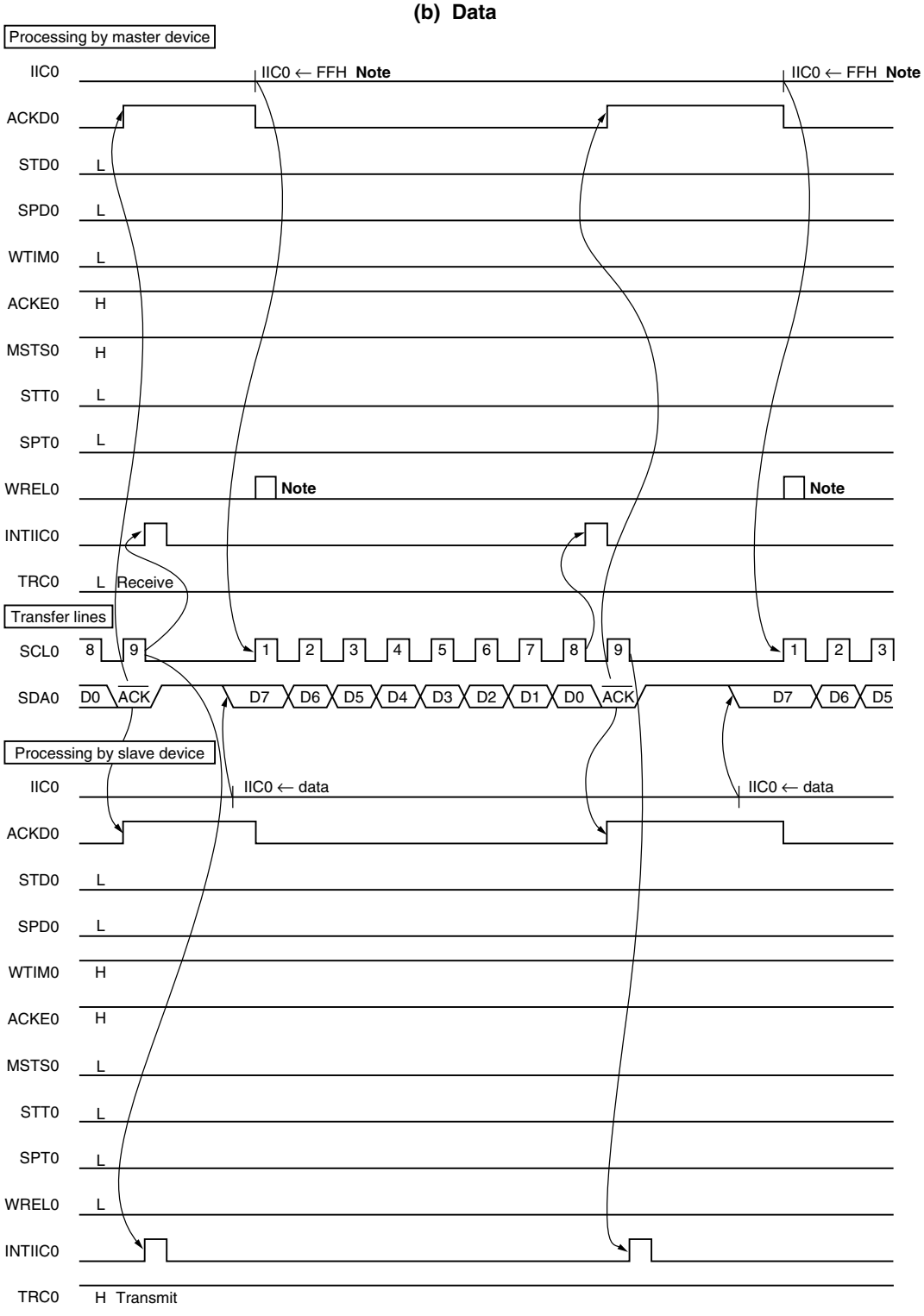
Note To cancel slave wait, write FFH to IIC0 or set WREL0.

Figure 19-21. Example of Slave to Master Communication
(When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected) (1/3)



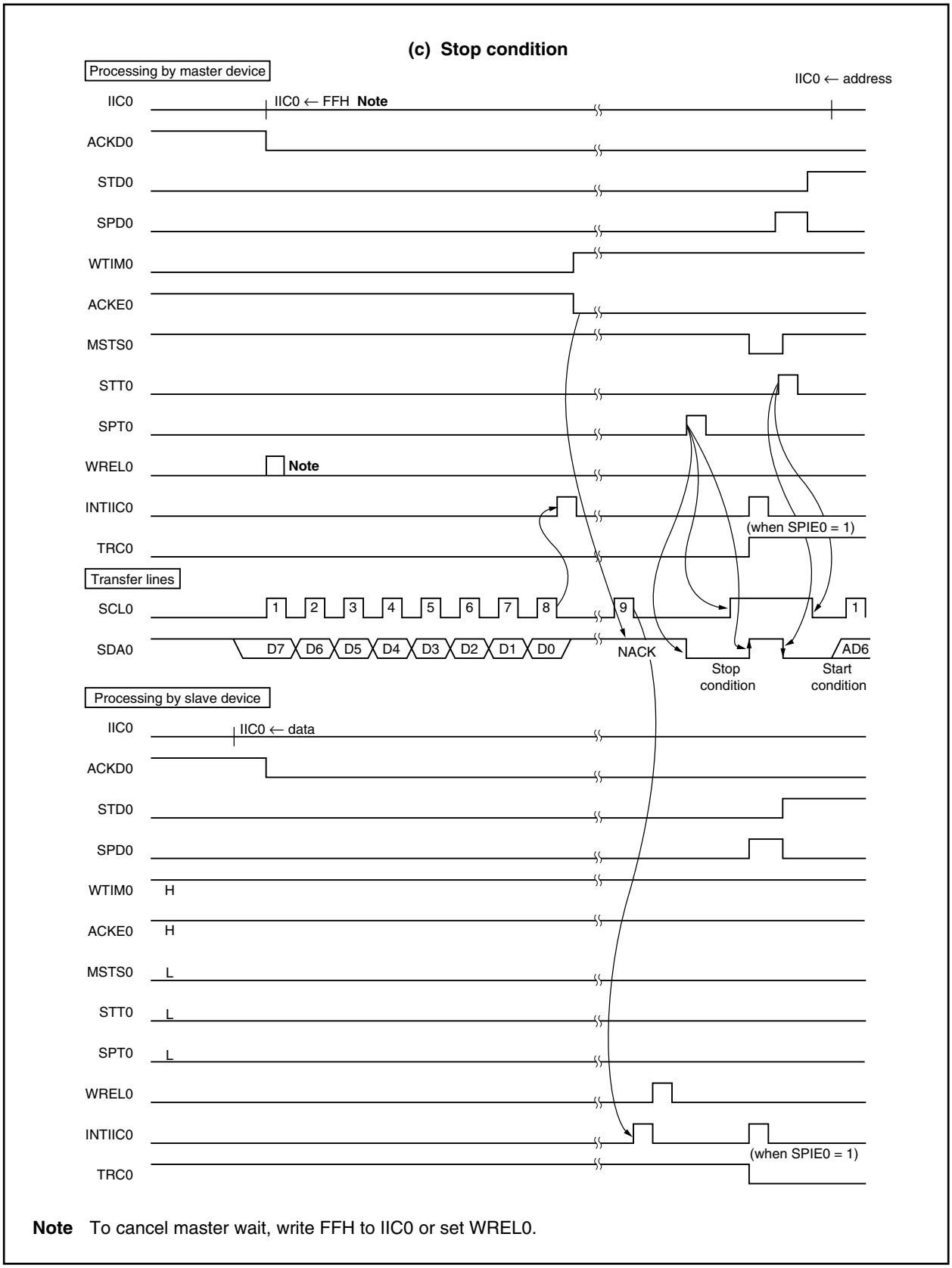
Note To cancel master wait, write FFH to IIC0 or set WREL0.

Figure 19-21. Example of Slave to Master Communication
(When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected) (2/3)



Note To cancel master wait, write FFH to IIC0 or set WREL0.

Figure 19-21. Example of Slave to Master Communication
(When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected) (3/3)



Note To cancel master wait, write FFH to IIC0 or set WREL0.

CHAPTER 20 DMA FUNCTION (DMA CONTROLLER)

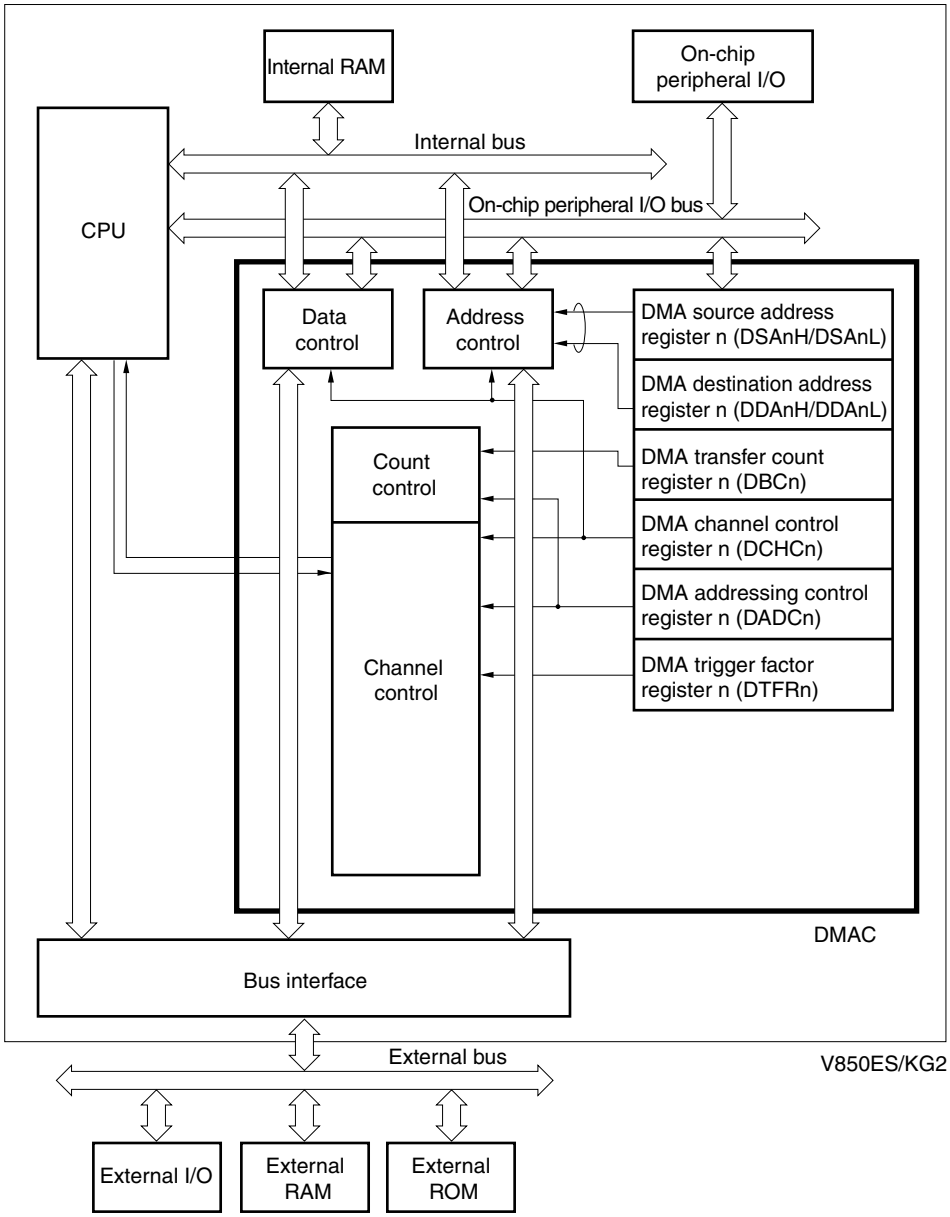
The V850ES/KG2 includes a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer.

The DMAC controls data transfer between memory and I/O, between memories, or between I/Os based on DMA requests issued by the on-chip peripheral I/O (serial interface, timer/counter, and A/D converter), interrupts from external input pins, or software triggers (memory refers to internal RAM or external memory).

20.1 Features

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})
- Transfer type: Two-cycle transfer
- Transfer mode: Single transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, A/D converter) or interrupts from external input pin
  - Requests by software trigger
- Transfer targets
  - Internal RAM ↔ Peripheral I/O
  - Peripheral I/O ↔ Peripheral I/O
  - Internal RAM ↔ External memory
  - External memory ↔ Peripheral I/O
  - External memory ↔ External memory

20.2 Configuration



Remark n = 0 to 3

20.3 Registers

(1) DMA source address registers 0 to 3 (DSA0 to DSA3)

The DSA0 to DSA3 registers set the DMA source addresses (26 bits each) for DMA channel n (n = 0 to 3).

These registers are divided into two 16-bit registers, DSAnH and DSAnL.

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DSA0H FFFFF082H, DSA1H FFFFF08AH, DSA2H FFFFF092H, DSA3H FFFFF09AH, DSA0L FFFFF080H, DSA1L FFFFF088H, DSA2L FFFFF090H, DSA3L FFFFF098H

DSAnH (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRn	0	0	0	0	0	SAn25	SAn24	SAn23	SAn22	SAn21	SAn20	SAn19	SAn18	SAn17	SAn16

DSAnL (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAn15	SAn14	SAn13	SAn12	SAn11	SAn10	SAn9	SAn8	SAn7	SAn6	SAn5	SAn4	SAn3	SAn2	SAn1	SAn0

IRn	Specification of DMA transfer source
0	External memory or on-chip peripheral I/O
1	Internal RAM

SAn25 to SAn16	Set the address (A25 to A16) of the DMA transfer source (default value is undefined). During DMA transfer, the next DMA transfer source address is held. When DMA transfer is completed, the DMA address set first is held.

SAn15 to SAn0	Set the address (A15 to A0) of the DMA transfer source (default value is undefined). During DMA transfer, the next DMA transfer source address is held. When DMA transfer is completed, the DMA address set first is held.

Cautions 1. Be sure to clear bits 14 to 10 of the DSAnH register to 0.

2. Set the DSAnH and DSAnL registers at the following timing while DMA is not in progress.

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

3. When the value of the DSAn register is read, two 16-bit registers, DSAnH and DSAnL, are read. If reading and updating conflict, the value being updated may be read (refer to 20.13 Cautions).

(2) DMA destination address registers 0 to 3 (DDA0 to DDA3)

The DDA0 to DDA3 registers set the DMA destination address (26 bits each) for DMA channel n (n = 0 to 3). These registers are divided into two 16-bit registers, DDAnH and DDAnL.

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DDA0H FFFFF086H, DDA1H FFFFF08EH, DA2H FFFFF096H, DDA3H FFFFF09EH, DDA0L FFFFF084H, DDA1L FFFFF08CH, DDA2L FFFFF094H, DDA3L FFFFF09CH

DDAnH (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRn	0	0	0	0	0	DAn25	DAn24	DAn23	DAn22	DAn21	DAn20	DAn19	DAn18	DAn17	DAn16

DDAnL (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAn15	DAn14	DAn13	DAn12	DAn11	DAn10	DAn9	DAn8	DAn7	DAn6	DAn5	DAn4	DAn3	DAn2	DAn1	DAn0

IRn	Specification of DMA transfer destination
0	External memory or on-chip peripheral I/O
1	Internal RAM

DAn25 to DAn16	Set an address (A25 to A16) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

DAn15 to DAn0	Set an address (A15 to A0) of DMA transfer destination (default value is undefined). During DMA transfer, the next DMA transfer destination address is held. When DMA transfer is completed, the DMA transfer source address set first is held.

Cautions 1. Be sure to clear bits 14 to 10 of the DDAnH register to 0.

2. Set the DDAnH and DDAnL registers at the following timing while DMA is not in progress.

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

3. When the value of the DDAn register is read, two 16-bit registers, DDAnH and DDAnL, are read. If reading and updating conflict, a value being updated may be read (refer to 20.13 Cautions).

(3) DMA byte count registers 0 to 3 (DBC0 to DBC3)

The DBC0 to DBC3 registers are 16-bit registers that set the byte transfer count for DMA channel n (n = 0 to 3).

These registers hold the remaining transfer count during DMA transfer.

These registers are decremented by 1 per one transfer regardless of the transfer data unit (8/16 bits), and the transfer is terminated if a borrow occurs.

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DBC0 FFFFF0C0H, DBC1 FFFFF0C2H, DBC2 FFFFF0C4H, DBC3 FFFFF0C6H

DBCn (n = 0 to 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCn15	BCn14	BCn13	BCn12	BCn11	BCn10	BCn9	BCn8	BCn7	BCn6	BCn5	BCn4	BCn3	BCn2	BCn1	BCn0

BCn15 to BCn0	Byte transfer count setting or remaining byte transfer count during DMA transfer
0000H	Byte transfer count 1 or remaining byte transfer count
0001H	Byte transfer count 2 or remaining byte transfer count
:	:
FFFFH	Byte transfer count 65,536 (2^{16}) or remaining byte transfer count
The number of transfer data set first is held when DMA transfer is complete.	

Caution Set the DBCn register at the following timing while DMA is not in progress.

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

(4) DMA addressing control registers 0 to 3 (DADC0 to DADC3)

The DADC0 to DADC3 registers are 16-bit registers that control the DMA transfer mode for DMA channel n (n = 0 to 3).

These registers can be read or written in 16-bit units.

Reset input clears these registers to 0000H.

After reset: 0000H R/W Address: DADC0 FFFFF0D0H, DADC1 FFFFF0D2H, DADC2 FFFFF0D4H, DADC3 FFFFF0D6H

DADCn (n = 0 to 3)

15	14	13	12	11	10	9	8
0	DSn0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
SADn1	SADn0	DADn1	DADn0	0	0	0	0

DSn0	Setting of transfer data size
0	8 bits
1	16 bits

SADn1	SADn0	Setting of count direction of the transfer source address
0	0	Increment
0	1	Decrement
1	0	Fixed
1	1	Setting prohibited

DADn1	DADn0	Setting of count direction of the destination address
0	0	Increment
0	1	Decrement
1	0	Fixed
1	1	Setting prohibited

Cautions 1. Be sure to clear bits 15, 13 to 8, and 3 to 0 of the DADCn register to "0".

2. Set the DADCn register at the following timing while DMA is not in progress.

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

3. The DSn0 bit specifies the size of the transfer data, and does not control bus sizing. If 8-bit data (DSn0 bit = 0) is set, therefore, the lower data bus is not always used.

4. If the transfer data size is set to 16 bits (DSn0 bit = 1), transfer cannot be started from an odd address. Transfer is always started from an address with the first bit of the lower address aligned to 0.

5. If DMA transfer is executed on an on-chip peripheral I/O register (as the transfer source or destination), be sure to specify the same transfer size as the register size. For example, to execute DMA transfer on an 8-bit register, be sure to specify 8-bit transfer.

(5) DMA channel control registers 0 to 3 (DCHC0 to DCHC3)

The DCHC0 to DCHC3 registers are 8-bit registers that control the DMA transfer operating mode for DMA channel n.

These registers can be read or written in 8-bit or 1-bit units (however, bit 7 is read-only and bits 1 and 2 are write-only. If bit 1 or 2 is read, the read value is always 0).

Reset input clears these registers to 00H.

After reset: 00H R/W Address: DCHC0 FFFFF0E0H, DCHC1 FFFFF0E2H, DCHC2 FFFFF0E4H, DCHC3 FFFFF0E6H

	<7>	6	5	4	3	<2>	<1>	<0>
DCHCn	TCn Note 1	0	0	0	0	INITn Note 2	STGn Note 2	Enn

(n = 0 to 3)

TCn Note 1	Status flag indicates whether DMA transfer through DMA channel n has completed or not
0	DMA transfer had not completed.
1	DMA transfer had completed.
It is set to 1 on the last DMA transfer and cleared to 0 when it is read.	

INITn Note 2	If the INITn bit is set to 1 with DMA transfer disabled (Enn bit = 0), the DMA transfer status can be initialized. When re-setting the DMA transfer status (re-setting the DDAnH, DDAnL, DSAnH, DSAnL, DBCn, and DADCn registers) before DMA transfer is completed (before the TCn bit is set to 1), be sure to initialize the DMA channel. When initializing the DMA controller, however, be sure to observe the procedure described in **20.13 Cautions**.

STGn Note 2	This is a software startup trigger of DMA transfer. If this bit is set to 1 in the DMA transfer enable state (TCn bit = 0, Enn bit = 1), DMA transfer is started.

Enn	Setting of whether DMA transfer through DMA channel n is to be enabled or disabled
0	DMA transfer disabled
1	DMA transfer enabled
DMA transfer is enabled when the Enn bit is set to 1. When DMA transfer is completed (when a terminal count is generated), this bit is automatically cleared to 0. To abort DMA transfer, clear the Enn bit to 0 by software. To resume, set the Enn bit to 1 again. When aborting or resuming DMA transfer, however, be sure to observe the procedure described in **20.13 Cautions**.	

Notes 1. The TCn bit is read-only.

2. The INITn and STGn bits are write-only.

Cautions 1. Be sure to clear bits 6 to 3 of the DCHCn register to 0.

2. When DMA transfer is completed (when a terminal count is generated), the Enn bit is cleared to 0 and then the TCn bit is set to 1. If the DCHCn register is read while its bits are being updated, a value indicating "transfer not completed and transfer is disabled" (TCn bit = 0 and Enn bit = 0) may be read.

(6) DMA trigger factor registers 0 to 3 (DTFR0 to DTFR3)

The DTFR0 to DTFR3 registers are 8-bit registers that control the DMA transfer start trigger via interrupt request signals from on-chip peripheral I/O.

The interrupt request signals set by these registers serve as DMA transfer start factors.

These registers can be read or written in 8-bit units. However, only the DFn bit can be read or written in 1-bit units.

Reset input clears these registers to 00H.

After reset: 00H R/W Address: DTFR0 FFFFF810H, DTFR1 FFFFF812H, DTFR2 FFFFF814H, DTFR3 FFFFF816H

	<7>	6	5	4	3	2	1	0
DTFRn	DFn	0	IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0

(n = 0 to 3)

DFn[Note]	DMA transfer request flag
0	No DMA transfer request
1	DMA transfer request

Note The DFn bit can write 0 only. Write 0 to this bit to clear a DMA transfer request if an interrupt that is specified as the cause of starting DMA transfer occurs while DMA transfer is disabled.

Cautions 1. Set the IFCn5 to IFCn0 bits at the following timing while DMA is not in progress.

- **Period from after reset to start of first DMA transfer**
- **Period from after channel initialization by DCHCn.INITn bit to start of DMA transfer**
- **Period from after completion of DMA transfer (DCHCn.TCn bit = 1) to start of the next DMA transfer**

2. An interrupt request that is generated in the standby mode (IDLE, STOP, or sub-IDLE mode) does not start the DMA transfer cycle (nor is the DFn bit set to 1).

3. If a DMA start factor is selected by the IFCn5 to IFCn0 bits, the DFn bit is set to 1 when an interrupt occurs from the selected on-chip peripheral I/O, regardless of whether the DMA operation is enabled or disabled. If DMA is enabled in this status, DMA transfer is immediately started.

Remark For the IFCn5 to IFCn0 bits, refer to **Table 20-1 DMA Start Factors**.

Table 20-1. DMA Start Factors

IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0	Interrupt Source
0	0	0	0	0	0	DMA request by interrupt disabled
0	0	0	0	0	1	INTWDTM1
0	0	0	0	1	0	INTP0
0	0	0	0	1	1	INTP1
0	0	0	1	0	0	INTP2
0	0	0	1	0	1	INTP3
0	0	0	1	1	0	INTP4
0	0	0	1	1	1	INTP5
0	0	1	0	0	0	INTP6
0	0	1	0	0	1	INTTM000
0	0	1	0	1	0	INTTM001
0	0	1	0	1	1	INTTM010
0	0	1	1	0	0	INTTM011
0	0	1	1	0	1	INTTM50
0	0	1	1	1	0	INTTM51
0	0	1	1	1	1	INTCSI00
0	1	0	0	0	0	INTCSI01
0	1	0	0	0	1	INTSRE0
0	1	0	0	1	0	INTSR0
0	1	0	0	1	1	INTST0
0	1	0	1	0	0	INTSRE1
0	1	0	1	0	1	INTSR1
0	1	0	1	1	0	INTST1
0	1	0	1	1	1	INTTMH0
0	1	1	0	0	0	INTTMH1
0	1	1	0	0	1	INTCSIA0
0	1	1	0	1	0	INTIIC0[Note]
0	1	1	0	1	1	INTAD
0	1	1	1	0	0	INTKR
0	1	1	1	0	1	INTWTI
0	1	1	1	1	0	INTWT
0	1	1	1	1	1	INTBRG
1	0	0	0	0	0	INTTM020
1	0	0	0	0	1	INTTM021
1	0	0	0	1	0	INTTM030
1	0	0	0	1	1	INTTM031
1	0	0	1	0	0	INTCSIA1
1	0	1	0	1	0	INTSRE2
1	0	1	0	1	1	INTSR2
1	0	1	1	0	0	INTST2
1	0	1	1	1	1	INTP7
1	1	0	0	0	0	INTTP0OV
1	1	0	0	0	1	INTTP0CC0
1	1	0	0	1	0	INTTP0CC1
Other than above						Setting prohibited

Remark n = 0 to 3

20.4 Transfer Targets

Table 20-2 shows the relationship between the transfer targets (√: Transfer enabled, ×: Transfer disabled).

Table 20-2. Relationship Between Transfer Targets

		Transfer Destination			
		Internal ROM	On-Chip Peripheral I/O	Internal RAM	External Memory
Source	On-chip peripheral I/O	×	√	√	√
	Internal RAM	×	√	×	√
	External memory	×	√	√	√
	Internal ROM	×	×	×	×

Caution The operation is not guaranteed for combinations of transfer destination and source marked with "×" in Table 20-2.

20.5 Transfer Modes

Single transfer is supported as the transfer mode.

In single transfer mode, the bus is released at each byte/halfword transfer. If there is a subsequent DMA transfer request, transfer is performed again once. This operation continues until a terminal count occurs.

When the DMAC has released the bus, if another higher priority DMA transfer request is issued, the higher priority DMA request always takes precedence.

If a new transfer request of the same channel and a transfer request of another channel with a lower priority are generated in a transfer cycle, DMA transfer of the channel with the lower priority is executed after the bus is released to the CPU (the new transfer request of the same channel is ignored in the transfer cycle).

20.6 Transfer Types

As a transfer type, the 2-cycle transfer is supported.

In two-cycle transfer, data transfer is performed in two cycles, a read cycle and a write cycle.

In the read cycle, the transfer source address is output and reading is performed from the source to the DMAC. In the write cycle, the transfer destination address is output and writing is performed from the DMAC to the destination.

An idle cycle of one clock is always inserted between a read cycle and a write cycle. If the data bus width differs between the transfer source and destination for DMA transfer of two cycles, the operation is performed as follows.

<16-bit data transfer>

<1> Transfer from 32-bit bus → 16-bit bus
A read cycle (the higher 16 bits are in a high-impedance state) is generated, followed by generation of a write cycle (16 bits).

<2> Transfer from 16-/32-bit bus to 8-bit bus
A 16-bit read cycle is generated once, and then an 8-bit write cycle is generated twice.

<3> Transfer from 8-bit bus to 16-/32-bit bus
An 8-bit read cycle is generated twice, and then a 16-bit write cycle is generated once.

<4> Transfer between 16-bit bus and 32-bit bus
A 16-bit read cycle is generated once, and then a 16-bit write cycle is generated once.

For DMA transfer executed to an on-chip peripheral I/O register (transfer source/destination), be sure to specify the same transfer size as the register size. For example, for DMA transfer to an 8-bit register, be sure to specify byte (8-bit) transfer.

Remark The bus width of each transfer target (transfer source/destination) is as follows.

- On-chip peripheral I/O: 16-bit bus width
- Internal RAM: 32-bit bus width
- External memory: 8-bit or 16-bit bus width

20.7 DMA Channel Priorities

The DMA channel priorities are fixed as follows.

DMA channel 0 > DMA channel 1 > DMA channel 2 > DMA channel 3

The priorities are checked for every transfer cycle.

20.8 Time Related to DMA Transfer

The time required to respond to a DMA request, and the minimum number of clocks required for DMA transfer are shown below.

Single transfer: DMA response time (<1>) + Transfer source memory access (<2>) + 1[Note 1] + Transfer destination memory access (<2>)

DMA Cycle		Minimum Number of Execution Clocks
<1> DMA request response time		4 clocks (MIN.) + Noise elimination time[Note 2]
<2> Memory access	External memory access	Depends on connected memory.
	Internal RAM access	2 clocks[Note 3]
	Peripheral I/O register access	3 clocks + Number of wait cycles specified by VSWC register[Note 4]

Notes 1. One clock is always inserted between a read cycle and a write cycle in DMA transfer.

2. If an external interrupt (INTPn) is specified as the trigger to start DMA transfer, noise elimination time is added (n = 0 to 7).

3. Two clocks are required for a DMA cycle.

4. More wait cycles may be necessary for accessing a special register described in **3.4.8 (1) (b)**.

20.9 DMA Transfer Start Factors

There are two types of DMA transfer start factors, as shown below.

(1) Request by software

If the DCHCn.STGn bit is set to 1 while the DCHCn.TCn bit = 0 and DCHCn.Enn bit = 1 (DMA transfer enabled), DMA transfer is started.

To request the next DMA transfer cycle immediately after that, confirm, by using the DBCn register, that the preceding DMA transfer cycle has been completed, and set the STGn bit to 1 again (n = 0 to 3).

TCn bit = 0, Enn bit = 1
↓
STGn bit = 1 … Starts the first DMA transfer.
↓
Confirm that the contents of the DBCn register have been updated.
STGn bit = 1 … Starts the second DMA transfer.
↓
:
↓
Generation of terminal count … Enn bit = 0, TCn bit = 1, and INTDMAn signal is generated.

(2) Request by on-chip peripheral I/O

If an interrupt request is generated from the on-chip peripheral I/O set by the DTFRn register when the TCn bit = 0 and Enn bit = 1 (DMA transfer enabled), DMA transfer is started.

Cautions 1. Two start factors (software trigger and hardware trigger) cannot be used for one DMA channel. If two start factors are simultaneously generated for one DMA channel, only one of them is valid. The start factor that is valid cannot be identified.

2. A new transfer request that is generated after the preceding DMA transfer request was generated or in the preceding DMA transfer cycle is ignored (cleared).

3. The transfer request interval of the same DMA channel varies depending on the setting of bus wait in the DMA transfer cycle, the start status of the other channels, or the external bus hold request. In particular, as described in Caution 2, a new transfer request that is generated for the same channel before the DMA transfer cycle or during the DMA transfer cycle is ignored. Therefore, the transfer request intervals for the same DMA channel must be sufficiently secured by the system. When the software trigger is used, completion of the DMA transfer cycle that was generated before can be checked by updating the DBCn register.

20.10 DMA Abort Factors

DMA transfer is aborted if a bus hold occurs.

The same applies if transfer is executed between the internal memory/on-chip peripheral I/O and internal memory/on-chip peripheral I/O.

When the bus hold is cleared, DMA transfer is resumed.

20.11 End of DMA Transfer

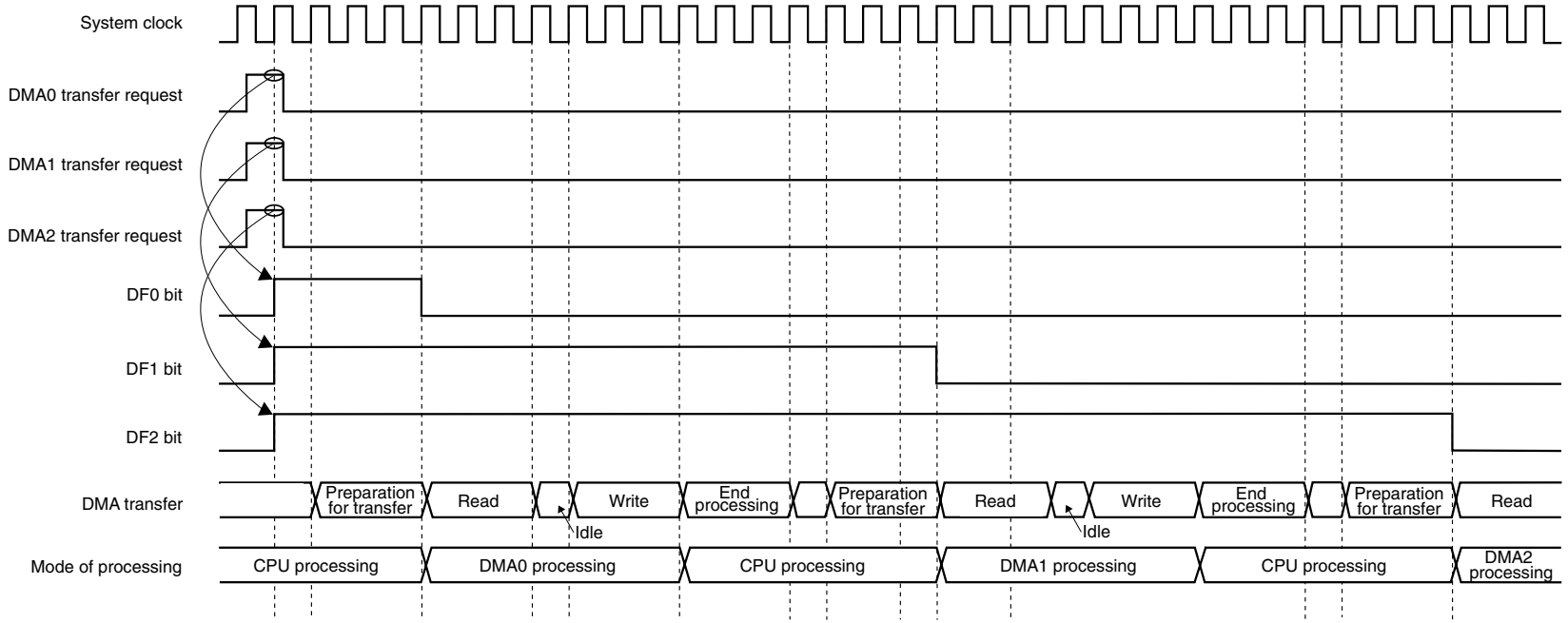
When DMA transfer has been completed the number of times set to the DBCn register and when the DCHCn.Enn bit is cleared to 0 and TCn bit is set to 1, a DMA transfer end interrupt request signal (INTDMAn) is generated for the interrupt controller (INTC) (n = 0 to 3).

The V850ES/KG2 does not output a terminal count signal to an external device. Therefore, confirm completion of DMA transfer by using the DMA transfer end interrupt or polling the TCn bit.

20.12 Operation Timing

The operation timing of DMA is as follows.

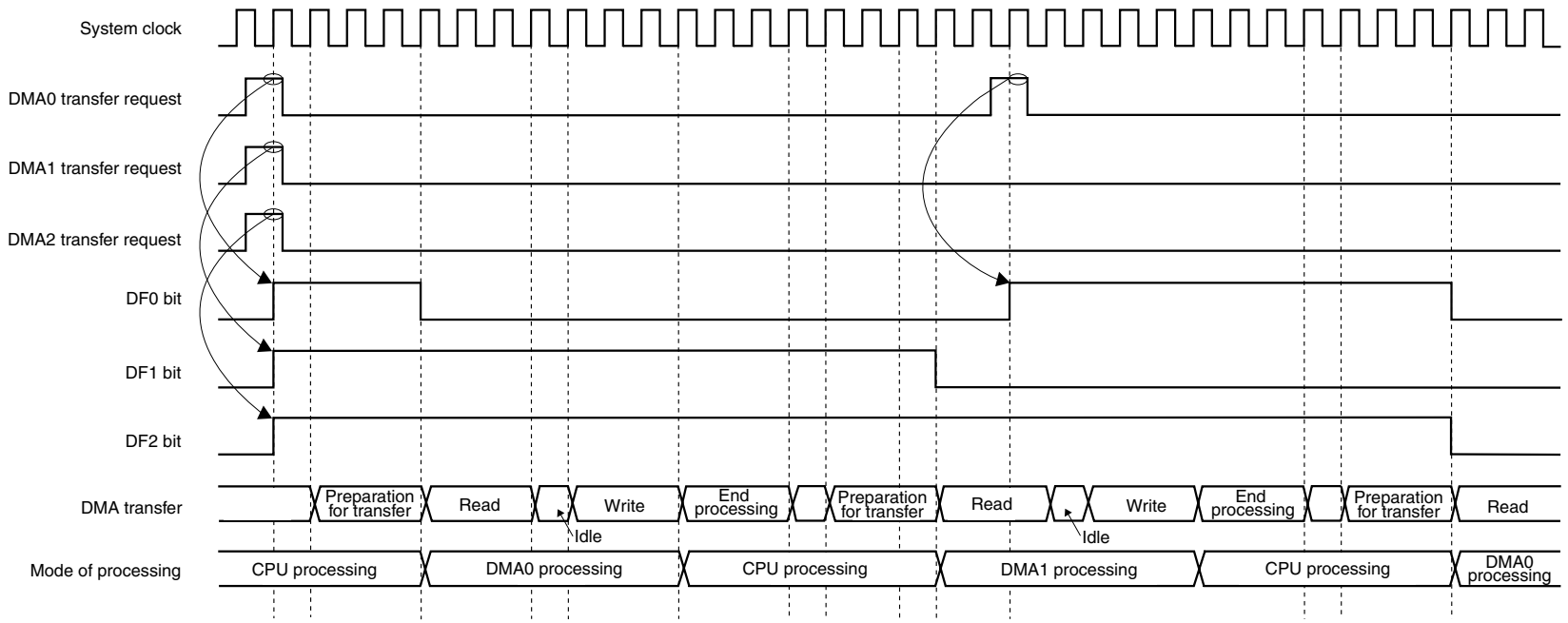
Figure 20-1. Priority of DMA (1)



Remarks 1. Transfer in the order of DMA0 → DMA1 → DMA2

2. In the case of transfer between external memory spaces (multiplex bus, no wait)

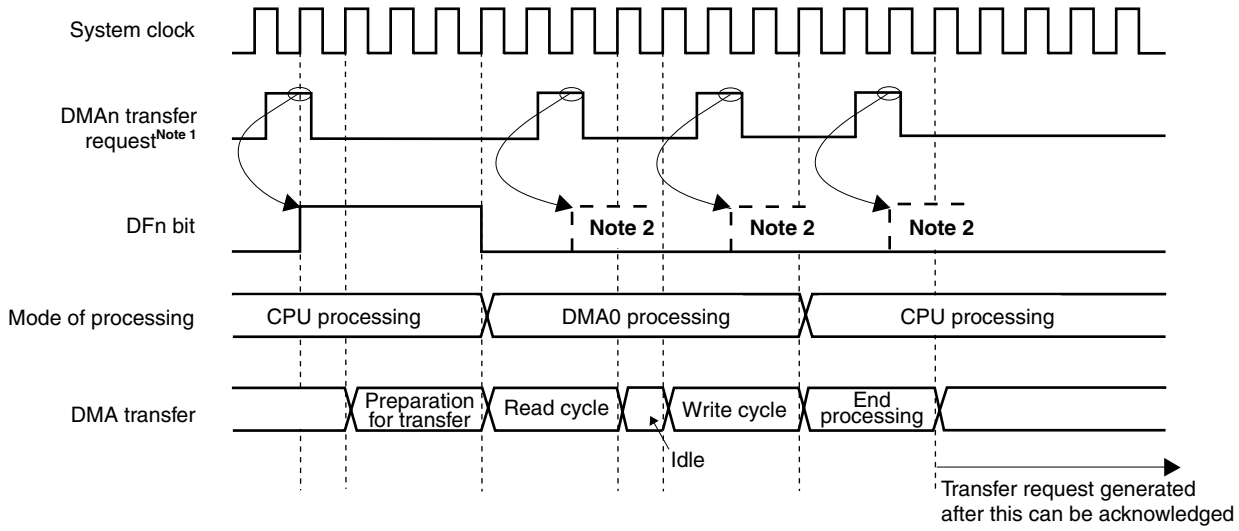
Figure 20-2. Priority of DMA (2)



Remarks 1. Transfer in the order of DMA0 → DMA1 → DMA0 (DMA2 is held pending.)

2. In the case of transfer between external memory spaces (multiplex bus, no wait)

Figure 20-3. Period in Which DMA Transfer Request Is Ignored (1)

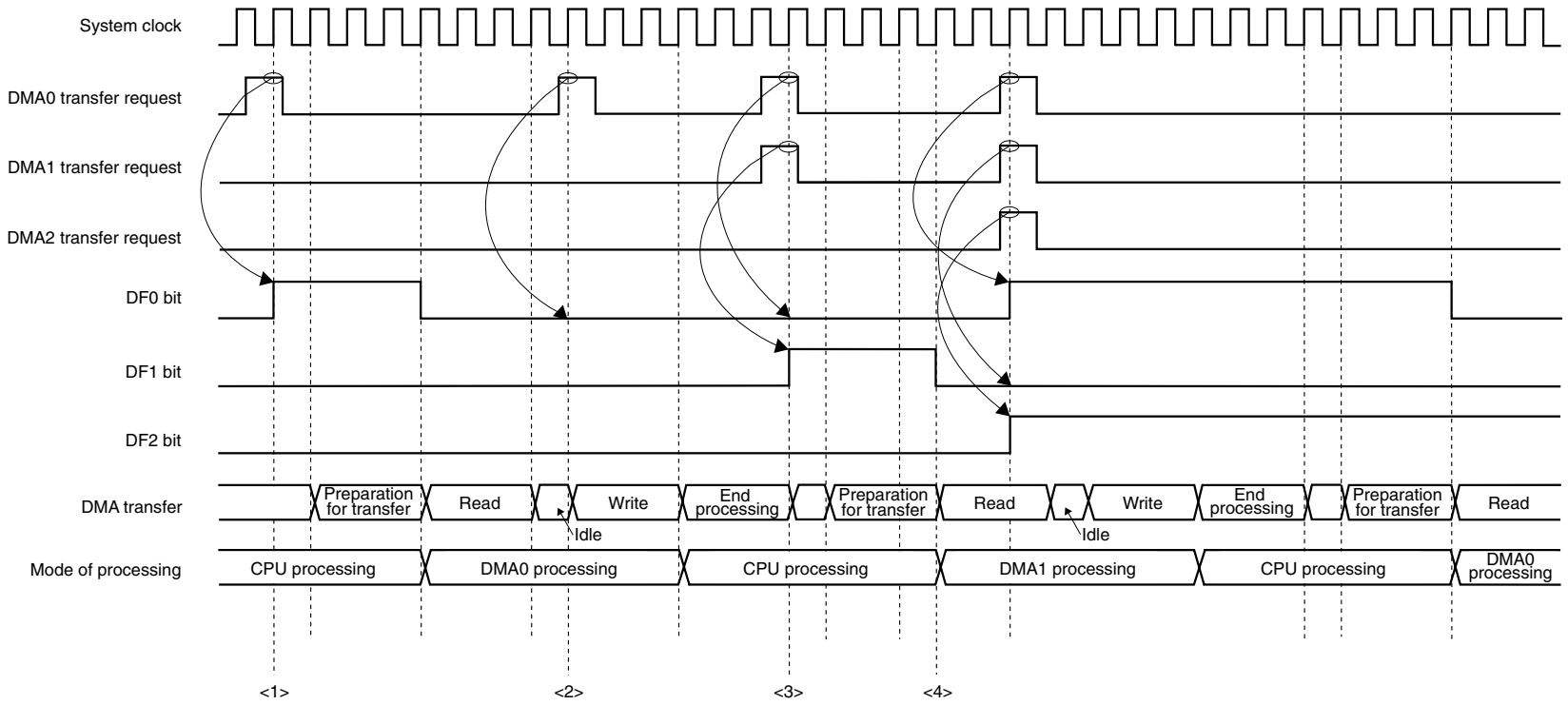


Notes 1. Interrupt from on-chip peripheral I/O, or software trigger (DCHCn.STGn bit)

2. New DMA request of the same channel is ignored between when the transfer request is generated and the end processing is complete.

Remark In the case of transfer between external memory spaces (multiplex bus, no wait)

Figure 20-4. Period in Which DMA Transfer Request Is Ignored (2)



<1> DMA0 transfer request

<2> New DMA0 transfer request is generated during DMA0 transfer.

→ A DMA transfer request of the same channel is ignored during DMA transfer.

<3> Requests for DMA0 and DMA1 are generated at the same time.

→ DMA0 request is ignored (a DMA transfer request of the same channel during transfer is ignored).

→ DMA1 request is acknowledged.

<4> Requests for DMA0, DMA1, and DMA2 are generated at the same time.

→ DMA1 request is ignored (a DMA transfer request of the same channel during transfer is ignored).

→ DMA0 request is acknowledged according to priority. DMA2 request is held pending (transfer of DMA2 occurs next).

20.13 Cautions

(1) Caution for VSWC register

When using the DMAC, be sure to set an appropriate value, in accordance with the operating frequency, to the VSWC register.

When the default value (77H) of the VSWC register is used, or if an inappropriate value is set to the VSWC register, the operation is not correctly performed (for details of the VSWC register, refer to **3.4.8 (1) (a) System wait control register (VSWC)**).

(2) Caution for DMA transfer executed on internal RAM

When executing the following instructions located in the internal RAM, do not execute a DMA transfer that transfers data to/from the internal RAM (transfer source/destination), because the CPU may not operate correctly afterward.

- Data access instruction to misaligned address located in internal RAM

Conversely, when executing a DMA transfer to transfer data to/from the internal RAM (transfer source/destination), do not execute the above instruction.

(3) Caution for reading DCHCn.TCn bit (n = 0 to 3)

The TCn bit is cleared to 0 when it is read, but it is not automatically cleared to 0 even if it is read at a specific timing. To accurately clear the TCn bit, add the following processing.

(a) When waiting for completion of DMA transfer by polling TCn bit

Confirm that the TCn bit has been set to 1 (after TCn bit = 1 is read), and then read the TCn bit three more times.

(b) When reading TCn bit in interrupt servicing routine

Execute reading the TCn bit three times.

(4) DMA transfer initialization procedure (setting DCHCn.INITn bit to 1)

Even if the INITn bit is set to 1 when the channel executing DMA transfer is to be initialized, the channel may not be initialized. To accurately initialize the channel, execute either of the following two procedures.

(a) Temporarily stop transfer of all DMA channels

Initialize the channel executing DMA transfer using the procedure in <1> to <7> below.

Note, however, that TCn bit is cleared to 0 when step <5> is executed. Make sure that the other processing programs do not expect that the TCn bit is 1.

<1> Disable interrupts (DI).

<2> Read the DCHCn.Enn bit of DMA channels other than the one to be forcibly terminated, and transfer the value to a general-purpose register.

<3> Clear the Enn bit of the DMA channels used (including the channel to be forcibly terminated) to 0. To clear the Enn bit of the last DMA channel, execute the clear instruction twice. If the target of DMA transfer (transfer source/destination) is the internal RAM, execute the instruction three times.

Example: Execute instructions in the following order if channels 0, 1, and 2 are used (if the target of transfer is not the internal RAM).

- Clear DCHC0.E00 bit to 0.
- Clear DCHC1.E11 bit to 0.
- Clear DCHC2.E22 bit to 0.
- Clear DCHC2.E22 bit to 0 again.

<4> Set the INITn bit of the channel to be forcibly terminated to 1.

<5> Read the TCn bit of each channel not to be forcibly terminated. If both the TCn bit and the Enn bit read in <2> are 1 (logical product (AND) is 1), clear the saved Enn bit to 0.

<6> After the operation in <5>, write the Enn bit value to the DCHCn register.

<7> Enable interrupts (EI).

Caution Be sure to execute step <5> above to prevent illegal setting of the Enn bit of the channels whose DMA transfer has been normally completed between <2> and <3>.

(b) Repeatedly execute setting INITn bit until transfer is forcibly terminated correctly

<1> Suppress a request from the DMA request source of the channel to be forcibly terminated (stop operation of the on-chip peripheral I/O).
<2> Check that the DMA transfer request of the channel to be forcibly terminated is not held pending, by using the DTFRn.DFn bit. If a DMA transfer request is held pending, wait until execution of the pending DMA transfer request is completed.
<3> When it has been confirmed that the DMA request of the channel to be forcibly terminated is not held pending, clear the Enn bit to 0.
<4> Again, clear the Enn bit of the channel to be forcibly terminated to 0.
If the target of transfer for the channel to be forcibly terminated (transfer source/destination) is the internal RAM, execute this operation once more.
<5> Copy the initial number of transfers of the channel to be forcibly terminated to a general-purpose register.
<6> Set the INITn bit of the channel to be forcibly terminated to 1.
<7> Read the value of the DBCn register of the channel to be forcibly terminated, and compare it with the value copied in <5>. If the two values do not match, repeat operations <6> and <7>.

Remarks 1. When the value of the DBCn register is read in <7>, the initial number of transfers is read if forced termination has been correctly completed. If not, the remaining number of transfers is read.
2. Note that method (b) may take a long time if the application frequently uses DMA transfer for a channel other than the DMA channel to be forcibly terminated.

(5) Procedure of temporarily stopping DMA transfer (clearing Enn bit)

Stop and resume the DMA transfer under execution using the following procedure.

<1> Suppress a transfer request from the DMA request source (stop the operation of the on-chip peripheral I/O).
<2> Check the DMA transfer request is not held pending, by using the DFn bit (check if the DFn bit = 0).
If a request is held pending, wait until execution of the pending DMA transfer request is completed.
<3> If it has been confirmed that no DMA transfer request is held pending, clear the Enn bit to 0 (this operation stops DMA transfer).
<4> Set the Enn bit to 1 to resume DMA transfer.
<5> Resume the operation of the DMA request source that has been stopped (start the operation of the on-chip peripheral I/O).

(6) Memory boundary

The operation is not guaranteed if the address of the transfer source or destination exceeds the area of the DMA target (external memory, internal RAM, or on-chip peripheral I/O) during DMA transfer.

(7) Transferring misaligned data

DMA transfer of misaligned data with a 16-bit bus width is not supported.
If an odd address is specified as the transfer source or destination, the least significant bit of the address is forcibly assumed to be 0.

(8) Bus arbitration for CPU

Because the DMA controller has a higher priority bus mastership than the CPU, a CPU access that takes place during DMA transfer is held pending until the DMA transfer cycle is completed and the bus is released to the CPU.

However, the CPU can access the external memory, on-chip peripheral I/O, and internal RAM to/from which DMA transfer is not being executed.

- The CPU can access the internal RAM when DMA transfer is being executed between the external memory and on-chip peripheral I/O.
- The CPU can access the internal RAM and on-chip peripheral I/O when DMA transfer is being executed between the external memory and external memory.

(9) Registers/bits that must not be rewritten during DMA operation

Set the following registers at the following timing when a DMA operation is not under execution.

[Registers]

- DSAnH, DSAnL, DDAnH, DDAnL, DBCn, and DADCn registers
- DTFRn.IFCn5 to DTFRn.IFCn0 bits

[Timing of setting]

- Period from after reset to start of the first DMA transfer
- Time after channel initialization to start of DMA transfer
- Period from after completion of DMA transfer (TCn bit = 1) to start of the next DMA transfer

(10) Be sure to set the following register bits to 0.

- Bits 14 to 10 of DSAnH register
- Bits 14 to 10 of DDAnH register
- Bits 15, 13 to 8, and 3 to 0 of DADCn register
- Bits 6 to 3 of DCHCn register

(11) DMA start factor

Do not start two or more DMA channels with the same start factor. If two or more channels are started with the same factor, a DMA channel with a lower priority may be acknowledged earlier than a DMA channel with a higher priority.

(12) Read values of DSAn and DDAn registers

Values in the middle of updating may be read from the DSAn and DDAn registers during DMA transfer (n = 0 to 3).

For example, if the DSAnH register and then the DSAnL register are read when the DMA transfer source address (DSAn register) is 0000FFFFH and the count direction is incremental (DADCn.SAD1 and DADCn.SAD0 bits = 00), the value of the DSAnL register differs as follows, depending on whether DMA transfer is executed immediately after the DSAnH register is read.

(a) If DMA transfer does not occur while DSAn register is read

<1> Read value of DSAnH register: DSAnH register = 0000H

<2> Read value of DSAnL register: DSAnL register = FFFFH

(b) If DMA transfer occurs while DSAn register is read

<1> Read value of DSAnH register: DSAnH register = 0000H

<2> Occurrence of DMA transfer

<3> Incrementing DSAn register: DSAn register = 00100000H

<4> Read value of DSAnL register: DSAnL register = 0000H

CHAPTER 21 INTERRUPT/EXCEPTION PROCESSING FUNCTION

21.1 Overview

The V850ES/KG2 is provided with a dedicated interrupt controller (INTC) for interrupt servicing and realize an interrupt function that can service interrupt requests from a total of 50 sources.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.

The V850ES/KG2 can process interrupt requests from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (fetching of an illegal op code) (exception trap).

21.1.1 Features

Interrupt Source				V850ES/KG2
Interrupt function	Non-maskable interrupt	External		1 channel (NMI pin)
		Internal		2 channels (WDT1, WDT2)
	Maskable interrupt	External		8 channels (all edge detection interrupts)
		Internal	WDT1	1 channel
			TMP	3 channels
			TM0	8 channels
			TMH	2 channels
			TM5	2 channels
			WT	2 channels
			BRG	1 channel
			UART	9 channels
			CSI0	2 channels
			CSIA	2 channels
			IIC	1 channel
			KR	1 channel
			AD	1 channel
			DMA	4 channels
			Total	39 channels
Exception function	Software exception			16 channels (TRAP00H to TRAP0FH)
				16 channels (TRAP10H to TRAP1FH)
	Exception trap			2 channels (ILGOP/DBG0)

Table 21-1 lists the interrupt/exception sources.

Table 21-1. Interrupt Source List (1/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				Internal reset input from WDT1, WDT2	WDT1 WDT2				
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	0010H	00000010H	nextPC	–
		–	INTWDT1	WDT1 overflow (when non-maskable interrupt selected)	WDT1	0020H	00000020H	**Note 1**	–
		–	INTWDT2	WDT2 overflow (when non-maskable interrupt selected)	WDT2	0030H	00000030H	**Note 1**	–
Software exception	Exception	–	TRAP0n[Note 2]	TRAP instruction	–	004nH[Note 2]	00000040H	nextPC	–
		–	TRAP1n[Note 2]	TRAP instruction	–	005nH[Note 2]	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Illegal op code/DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM1	WDT1 overflow (when interval timer selected)	WDT1	0080H	00000080H	nextPC	WDT1IC
		1	INTP0	INTP0 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin valid edge input	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTTM000	TM00 and CR000 match	TM00	0100H	00000100H	nextPC	TM0IC00
		9	INTTM001	TM00 and CR001 match	TM00	0110H	00000110H	nextPC	TM0IC01
		10	INTTM010	TM01 and CR010 match	TM01	0120H	00000120H	nextPC	TM0IC10
		11	INTTM011	TM01 and CR011 match	TM01	0130H	00000130H	nextPC	TM0IC11
		12	INTTM50	TM50 and CR50 match	TM50	0140H	00000140H	nextPC	TM5IC0
		13	INTTM51	TM51 and CR51 match	TM51	0150H	00000150H	nextPC	TM5IC1
		14	INTCSI00	CSI00 transfer completion	CSI00	0160H	00000160H	nextPC	CSI0IC0
		15	INTCSI01	CSI01 transfer completion	CSI01	0170H	00000170H	nextPC	CSI0IC1
		16	INTSRE0	UART0 reception error occurrence	UART0	0180H	00000180H	nextPC	SREIC0
		17	INTSR0	UART0 reception completion	UART0	0190H	00000190H	nextPC	SRIC0
		18	INTST0	UART0 transmission completion	UART0	01A0H	000001AH	nextPC	STIC0

Notes 1. For restoration in the case of INTWDT1 and INTWDT2, refer to **21.10 Cautions**.

2. n = 0 to FH

Table 21-1. Interrupt Source List (2/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	19	INTSRE1	UART1 reception error occurrence	UART1	01B0H	000001B0H	nextPC	SREIC1
		20	INTSR1	UART1 reception completion	UART1	01C0H	000001C0H	nextPC	SRIC1
		21	INTST1	UART1 transmission completion	UART1	01D0H	000001D0H	nextPC	STIC1
		22	INTTMH0	TMH0 and CMP00/CMP01 match	TMH0	01E0H	000001E0H	nextPC	TMHIC0
		23	INTTMH1	TMH1 and CMP10/CMP11 match	TMH1	01F0H	000001F0H	nextPC	TMHIC1
		24	INTCSIA0	CSIA0 transfer completion	CSIA0	0200H	00000200H	nextPC	CSIAIC0
		25	INTIIC0	I^2C0 transfer completion	I^2C0	0210H	00000210H	nextPC	IICIC0
		26	INTAD	A/D conversion completion	A/D	0220H	00000220H	nextPC	ADIC
		27	INTKR	Key return interrupt	KR	0230H	00000230H	nextPC	KRIC
		28	INTWTI	Watch timer interval	WT	0240H	00000240H	nextPC	WTIIC
		29	INTWT	Watch timer reference time	WT	0250H	00000250H	nextPC	WTIC
		30	INTBRG	8-bit counter of prescaler 3 and PRSCM match	Prescaler 3	0260H	00000260H	nextPC	BRGIC
		31	INTTM020	TM02 and CR020 match	TM02	0270H	00000270H	nextPC	TM0IC20
		32	INTTM021	TM02 and CR021 match	TM02	0280H	00000280H	nextPC	TM0IC21
		33	INTTM030	TM03 and CR030 match	TM03	0290H	00000290H	nextPC	TM0IC30
		34	INTTM031	TM03 and CR031 match	TM03	02A0H	000002A0H	nextPC	TM0IC31
		35	INTCSIA1	CSIA1 transfer completion	CSIA1	02B0H	000002B0H	nextPC	CSIAIC1
		41	INTSRE2	UART2 reception error occurrence	UART2	0310H	00000310H	nextPC	SREIC2
		42	INTSR2	UART2 reception completion	UART2	0320H	00000320H	nextPC	SRIC2
		43	INTST2	UART2 transmission completion	UART2	0330H	00000330H	nextPC	STIC2
		44	INTP7	INTP7 pin valid edge input	Pin	0390H	00000390H	nextPC	PIC7
		45	INTTP0OV	TMP0 overflow	TMP	03A0H	000003A0H	nextPC	TPOVIC
		46	INTTP0CC0	TMP0 capture 0/ compare 0 match	TMP	03B0H	000003B0H	nextPC	TPCCIC0
		47	INTTP0CC1	TMP0 capture 1/ compare 1 match	TMP	03C0H	000003C0H	nextPC	TPCCIC1
		48	INTDMA0	DMA0 transfer completion	DMAC	03D0H	000003D0H	nextPC	DMAIC0
		49	INTDMA1	DMA1 transfer completion	DMAC	03E0H	000003E0H	nextPC	DMAIC1
		50	INTDMA2	DMA2 transfer completion	DMAC	03F0H	000003F0H	nextPC	DMAIC2
		51	INTDMA3	DMA3 transfer completion	DMAC	0400H	00000400H	nextPC	DMAIC3

Remarks 1. Default priority: The priority order when two or more maskable interrupt requests with the same priority level are generated at the same time. The highest priority is 0.

The priority of non-maskable interrupt request is as follows.

INTWDT2 > INTWDT1 > NMI

Restored PC: The value of the program counter (PC) saved to EIPC, FEPC, or DBPC when interrupt/exception processing is started. The restored PC when a non-maskable or maskable interrupt is acknowledged while either of the following instructions is being executed does not become nextPC (when an interrupt is acknowledged during the execution of an instruction, the execution of that instruction is stopped and is resumed following completion of interrupt servicing).

- Load instructions (SLD.B, SLD.BU, SLD.H, SLD.HU, SLD.W)
- Divide instructions (DIV, DIVH, DIVU, DIVHU)
- PREPARE, DISPOSE instructions (only when an interrupt occurs before stack pointer update)

nextPC: The PC value at which processing is started following interrupt/exception processing.

2. The execution address of the illegal op code when an illegal op code exception occurs is calculated with (Restored PC – 4).

21.2 Non-Maskable Interrupts

Non-maskable interrupt request signals are acknowledged unconditionally, even when interrupts are disabled (DI state). Non-maskable interrupts (NMI) are not subject to priority control and take precedence over all other interrupt request signals.

The following three types of non-maskable interrupt request signals are available in the V850ES/KG2.

- NMI pin input (NMI)
- Non-maskable interrupt request signal (INTWDT1) due to overflow of watchdog timer 1
- Non-maskable interrupt request signal (INTWDT2) due to overflow of watchdog timer 2

There are four choices for the valid edge of an NMI pin, namely: rising edge, falling edge, both edges, and no edge detection.

The non-maskable interrupt request signal (INTWDT1) due to overflow of watchdog timer 1 functions by setting the WDTM1.WDTM14 and WDTM1.WDTM13 bits to 10.

The non-maskable interrupt request signal (INTWDT2) due to overflow of watchdog timer 2 functions by setting the WDTM2.WDM21 and WDTM2.WDM20 bits to 01.

When two or more non-maskable interrupts occur simultaneously, they are processed in a sequence determined by the following priority order (the interrupt request signals with low priority level are ignored).

INTWDT2 > INTWDT1 > NMI

If during NMI processing, an NMI, INTWDT1, or INTWDT2 request signal newly occurs, processing is performed as follows.

(1) If an NMI request signal newly occurs during NMI processing

The new NMI request signal is held pending regardless of the value of the PSW.NP bit. The NMI request signal held pending is acknowledged upon completion of processing of the NMI currently being executed (following RETI instruction execution).

(2) If an INTWDT1 request signal newly occurs during NMI processing

If the NP bit remains set (to 1) during NMI processing, the new INTWDT1 request signal is held pending. The INTWDT1 request signal held pending is acknowledged upon completion of processing of the NMI currently being executed (following RETI instruction execution).

If the NP bit is cleared (to 0) during NMI processing, a newly generated INTWDT1 request signal is executed (NMI processing is interrupted).

(3) If an INTWDT2 request signal newly occurs during NMI processing

A newly generated INTWDT2 request signal is executed regardless of the value of the NP bit (NMI processing is interrupted).

Caution For non-maskable interrupt servicing from non-maskable interrupt request signals (INTWDT1, INTWDT2), refer to 21.10 Cautions.

Figure 21-1. Acknowledging Non-Maskable Interrupt Request Signals (1/2)

(a) If two or more NMI request signals are simultaneously generated

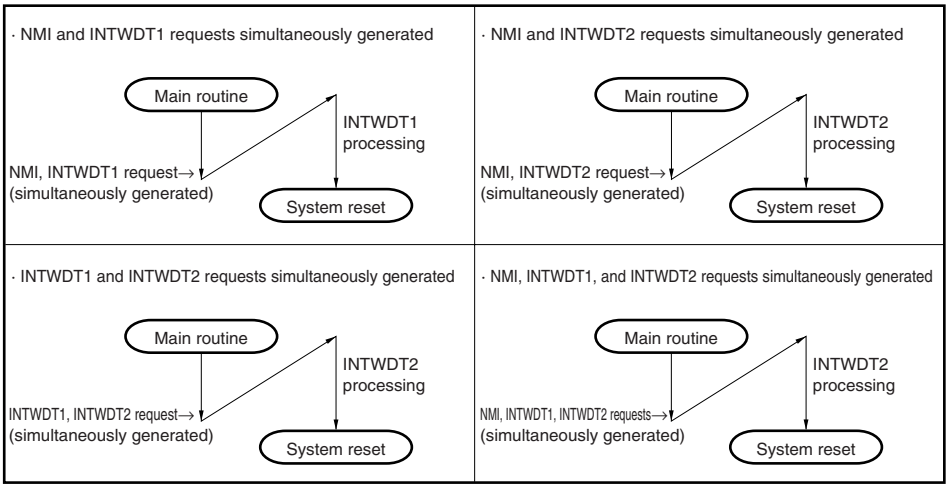
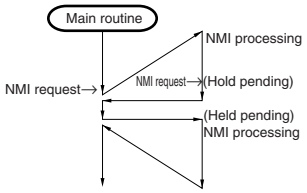
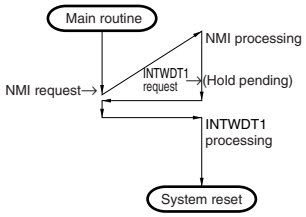
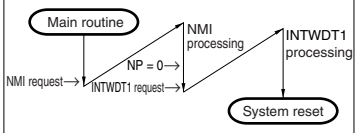
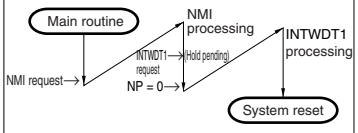
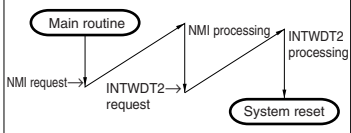
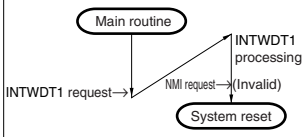
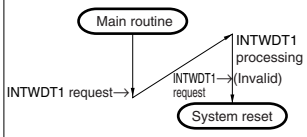
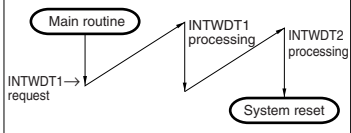
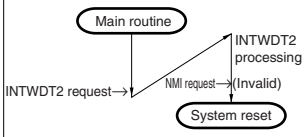
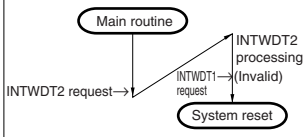
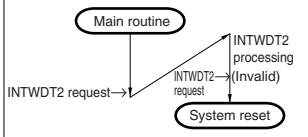


Figure 21-1. Acknowledging Non-Maskable Interrupt Request Signals (2/2)

(b) If a new non-maskable interrupt request signal is generated during a non-maskable interrupt servicing

Non-maskable interrupt currently being serviced	Non-maskable interrupt request newly generated during non-maskable interrupt servicing		
	NMI	INTWDT1	INTWDT2
NMI	· Generation of NMI request during NMI processing 	· Generation of INTWDT1 request during NMI processing (NP = 1 state prior to INTWDT1 request is maintained)  · Generation of INTWDT1 request during NMI processing (Set NP = 0 before INTWDT1 request)  · Generation of INTWDT1 request during NMI processing (Set NP = 0 after INTWDT1 request) 	· Generation of INTWDT2 request during NMI processing 
INTWDT1	· Generation of NMI request during INTWDT1 processing 	· Generation of INTWDT1 request during INTWDT1 processing 	· Generation of INTWDT2 request during INTWDT1 processing 
INTWDT2	· Generation of NMI request during INTWDT2 processing 	· Generation of INTWDT1 request during INTWDT2 processing 	· Generation of INTWDT2 request during INTWDT2 processing 

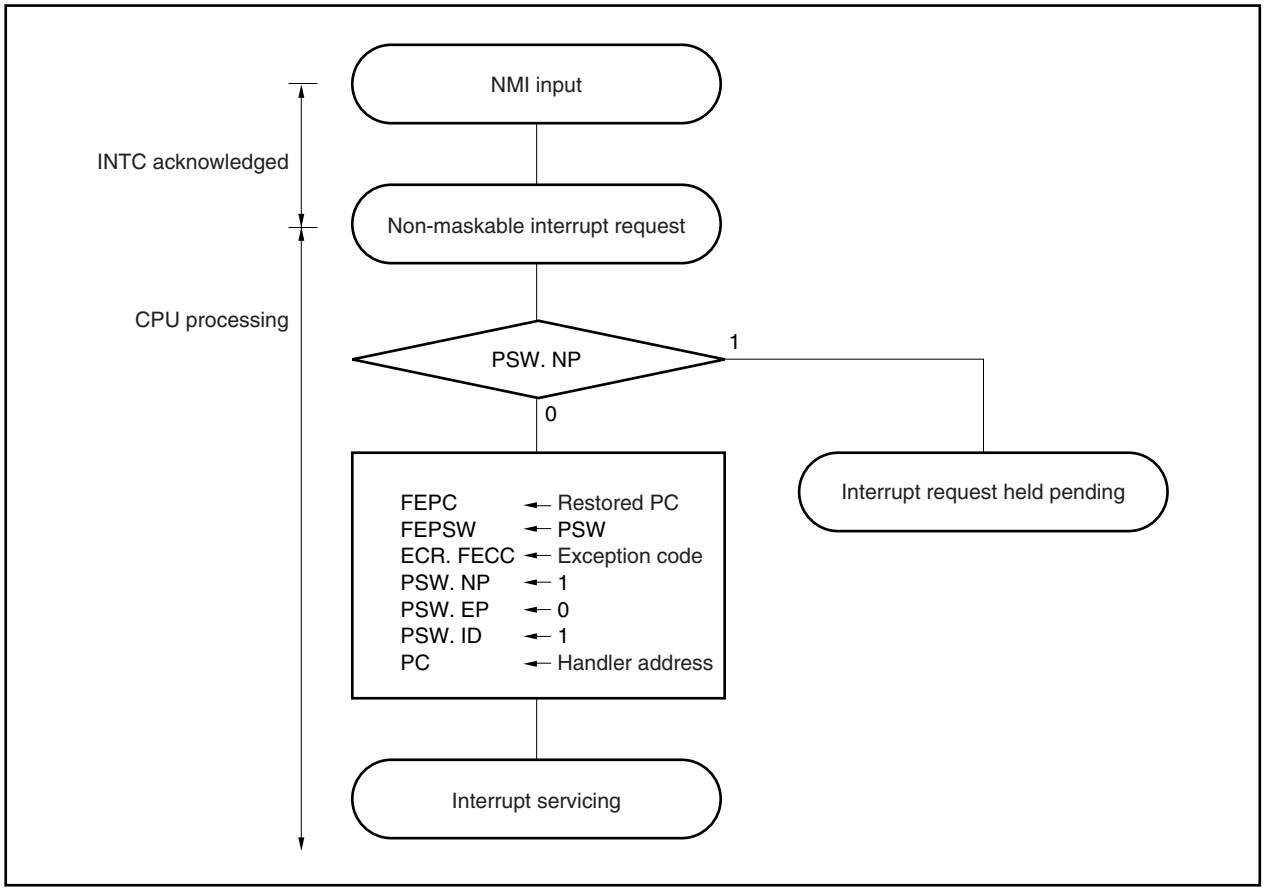
21.2.1 Operation

Upon generation of a non-maskable interrupt request signal, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to FEPC.
<2> Saves the current PSW to FEPSW.
<3> Writes the exception code (0010H, 0020H, 0030H) to the higher halfword (FECC) of ECR.
<4> Sets the PSW.NP and PSW.ID bits to 1 and clears the PSW.EP bit to 0.
<5> Loads the handler address (00000010H, 00000020H, 00000030H) of the non-maskable interrupt to the PC and transfers control.

Figure 21-2 shows the servicing flow for non-maskable interrupts.

Figure 21-2. Non-Maskable Interrupt Servicing



21.2.2 Restore

Execution is restored from non-maskable interrupt servicing by the RETI instruction.

(1) In case of NMI

Restore from NMI processing is done with the RETI instruction.

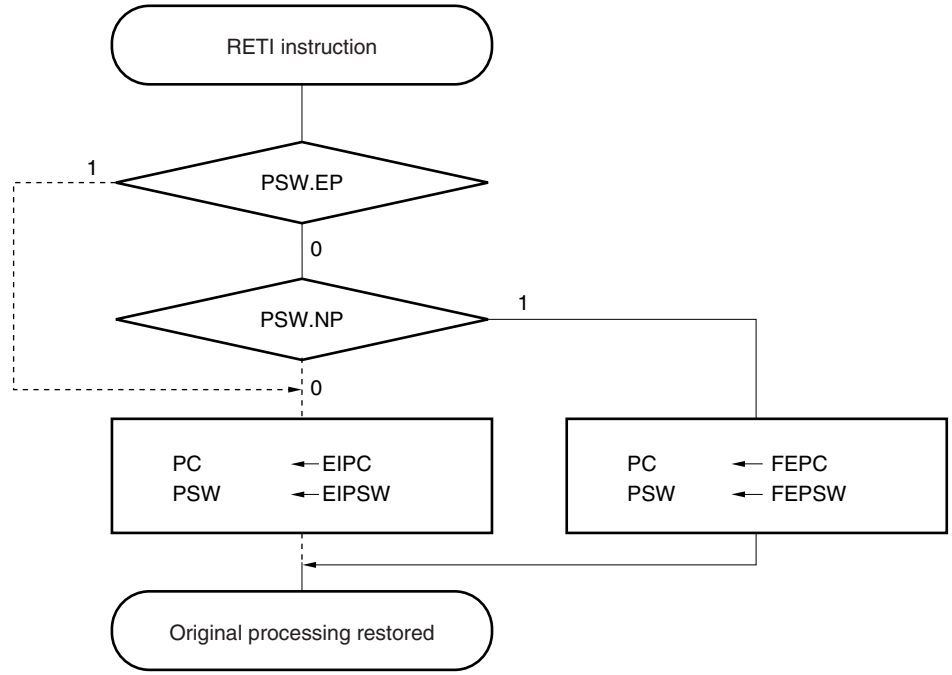
When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

(i) Loads the values of the restored PC and PSW from FEPC and FEPSW, respectively, because the PSW.EP bit and the PSW.NP bit are 0 and 1, respectively.

(ii) Transfers control back to the loaded address of the restored PC and PSW.

Figure 21-3 shows the processing flow of the RETI instruction.

Figure 21-3. RETI Instruction Processing



Caution When the EP bit and the NP bit are changed by the LDSR instruction during non-maskable interrupt servicing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to clear the EP bit back to 0 and set the NP bit back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

(2) In case of INTWDT1 and INTWDT2 signals

For non-maskable interrupt servicing by the non-maskable interrupt request signals (INTWDT1, INTWDT2), refer to **21.10 Cautions**.

21.2.3 NP flag

The NP flag is a status flag that indicates that non-maskable interrupt servicing is in progress.

This flag is set when a non-maskable interrupt request has been acknowledged, and masks all non-maskable requests to prevent multiple interrupts.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	EP	ID	SAT	CY	OV	S	Z

NP	NMI servicing status
0	No non-maskable interrupt servicing
1	Non-maskable interrupt serving in progress

21.3 Maskable Interrupts

Maskable interrupt request signals can be masked by interrupt control registers. The V850ES/KG2 has 47 maskable interrupt sources (refer to **21.1.1 Features**).

If two or more maskable interrupt request signals are generated at the same time, they are acknowledged according to the default priority. In addition to the default priority, eight levels of interrupt priorities can be specified by using the interrupt control registers, allowing programmable priority control.

When an interrupt request signal has been acknowledged, the interrupt disabled (DI) status is set and the acknowledgment of other maskable interrupt request signals is disabled.

When the EI instruction is executed in an interrupt servicing routine, the interrupt enabled (EI) status is set, which enables acknowledgment of interrupt request signals having a priority higher than that of the interrupt request signal currently in progress. Note that only interrupt request signals with a higher priority have this capability; interrupt request signals with the same priority level cannot be nested.

To use multiple interrupts, it is necessary to save EIPC and EIPSW to memory or a register before executing the EI instruction, and restore EIPC and EIPSW to the original values by executing the DI instruction before the RETI instruction.

When the WDTM1.WDTM14 bit is cleared to 0, the watchdog timer 1 overflow interrupt functions as a maskable interrupt (INTWDTM1).

21.3.1 Operation

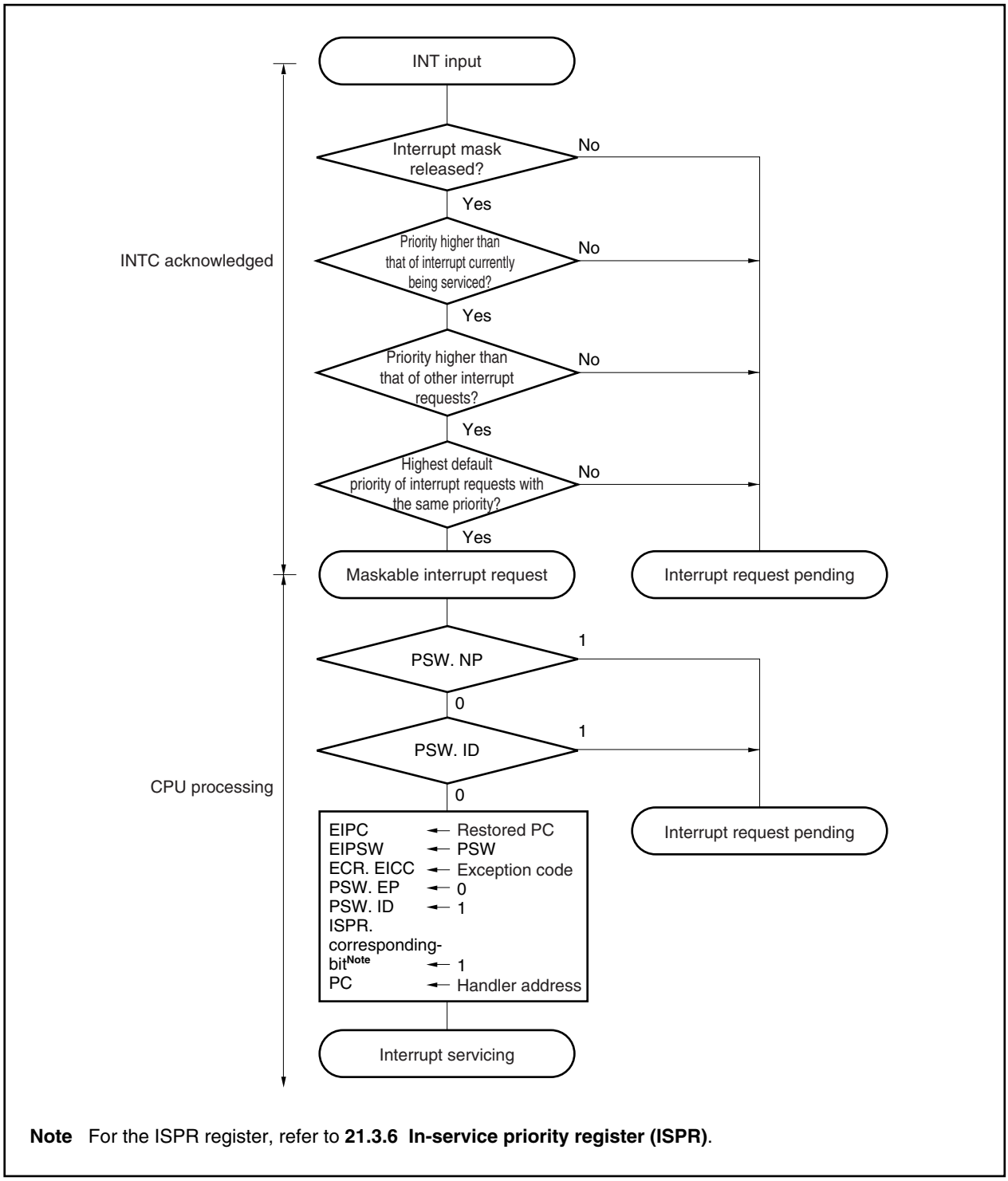
If a maskable interrupt request signal is generated, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower halfword of ECR (EICC).
<4> Sets the PSW.ID bit to 1 and clears the PSW.EP bit to 0.
<5> Loads the corresponding handler address to the PC and transfers control.

The maskable interrupt request signal masked by INTC and the maskable interrupt request signal that occurs while another interrupt is being serviced (when PSW.NP bit = 1 or ID bit = 1) are held pending internally. When the interrupts are unmasked, or when the NP bit = 0 and the ID bit = 0 by using the RETI and LDSR instructions, a new maskable interrupt servicing is started in accordance with the priority of the pending maskable interrupt request signal.

Figure 21-4 shows the servicing flow for maskable interrupts.

Figure 21-4. Maskable Interrupt Servicing



Note For the ISPR register, refer to **21.3.6 In-service priority register (ISPR)**.

21.3.2 Restore

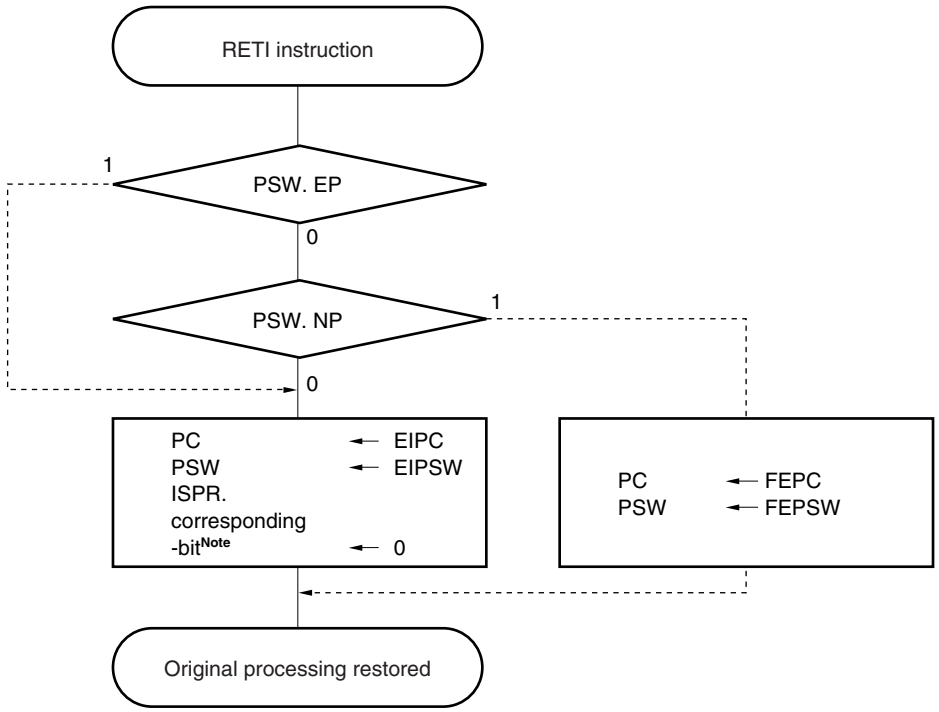
Execution is restored from maskable interrupt servicing by the RETI instruction.

When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

(1) Loads the values of the restored PC and PSW from EIPC and EIPSW because the PSW.EP bit and the PSW.NP bit are both 0.
(2) Transfers control back to the loaded address of the restored PC and PSW.

Figure 21-5 shows the processing flow of the RETI instruction.

Figure 21-5. RETI Instruction Processing



Note For the ISPR register, refer to **21.3.6 In-service priority register (ISPR)**.

Caution When the EP bit and the NP bit are changed by the LDSR instruction during maskable interrupt servicing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to clear the EP bit back to 0 and the NP bit back to 0 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

21.3.3 Priorities of maskable interrupts

INTC provides a multiple interrupt servicing in which an interrupt can be acknowledged while another interrupt is being serviced. Multiple interrupts can be controlled by priority levels.

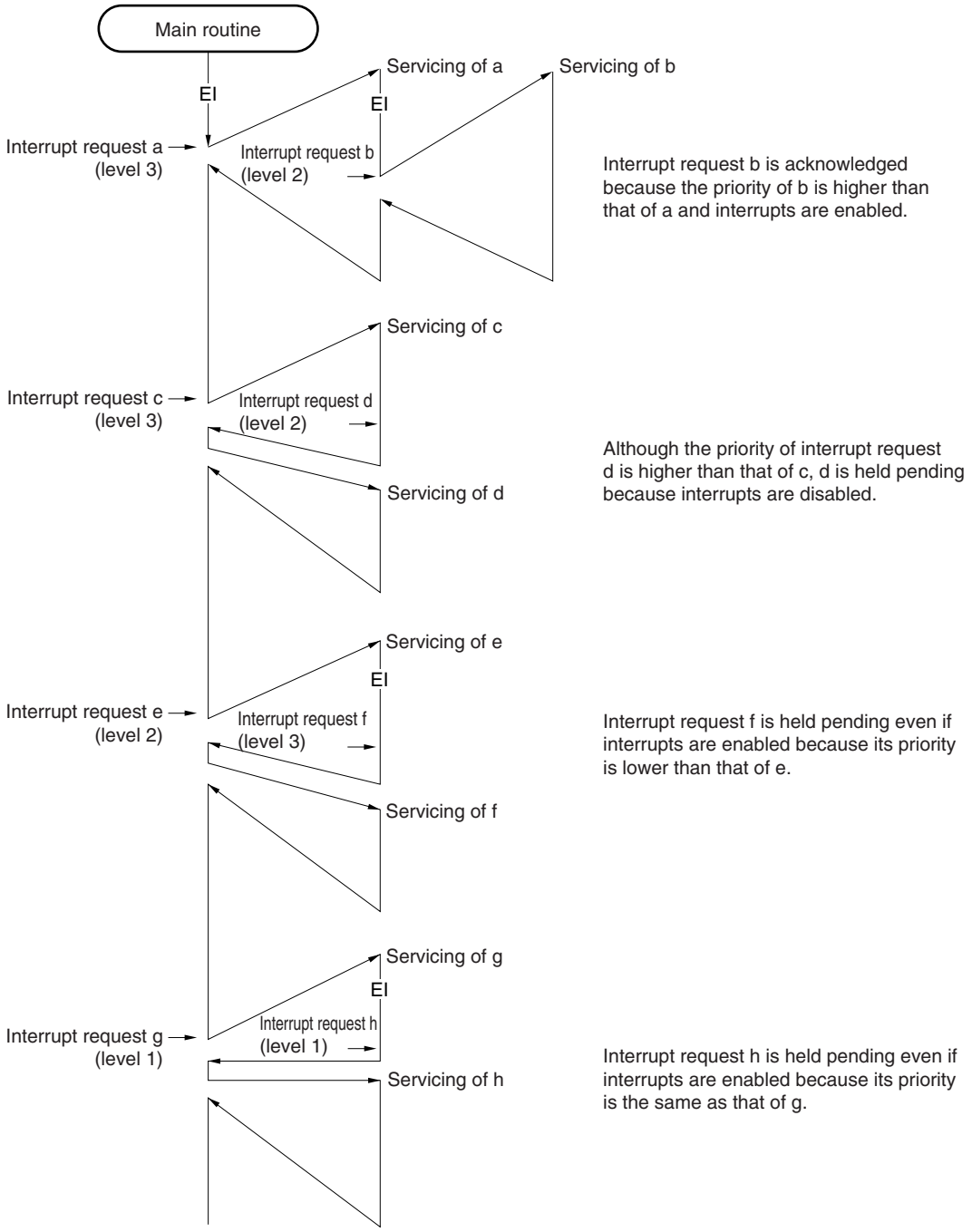
There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels specified by the interrupt priority level specification bit (xxICn.xxPRn bit). When two or more interrupts having the same priority level specified by xxPRn are generated at the same time, interrupts are serviced in order depending on the priority level allocated to each interrupt request (default priority level) beforehand. For more information, refer to **Table 21-1 Interrupt Source List**. Programmable priority control divides interrupt requests into eight levels by setting the priority level specification flag.

Note that when an interrupt request signal is acknowledged, the PSW.ID flag is automatically set (1). Therefore, when multiple interrupts are to be used, clear (0) the ID flag beforehand (for example, by placing the EI instruction into the interrupt service program) to enable interrupts.

Remark xx: Identifying name of each peripheral unit (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

n: Peripheral unit number (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

Figure 21-6. Example of Interrupt Nesting (1/2)

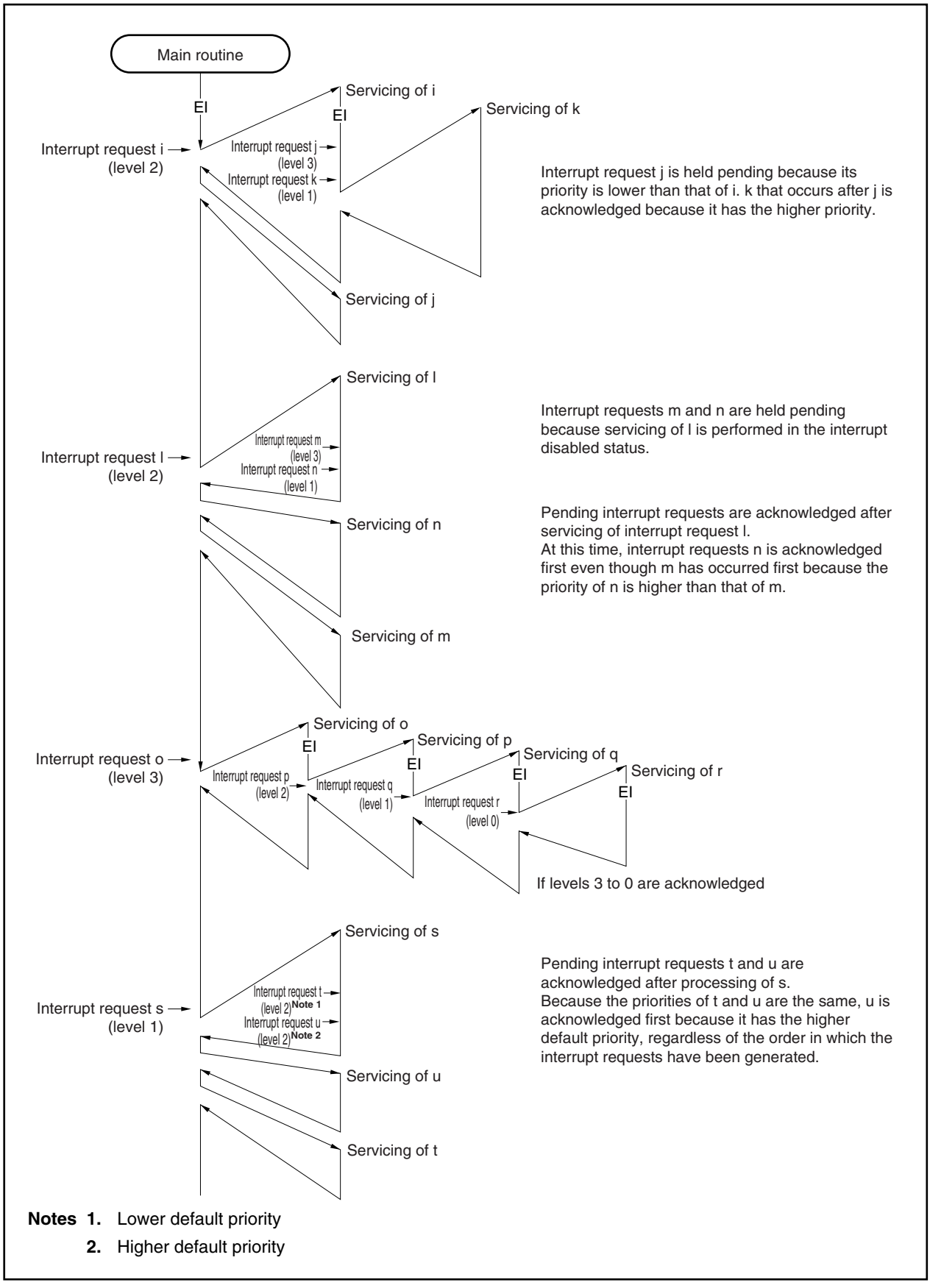


Caution The values of EIPC and EIPSW must be saved before executing multiple interrupts.

Remarks 1. a to u in the figure are the names of interrupt request signals shown for the sake of explanation.

2. The default priority in the figure indicates the relative priority between two interrupt request signals.

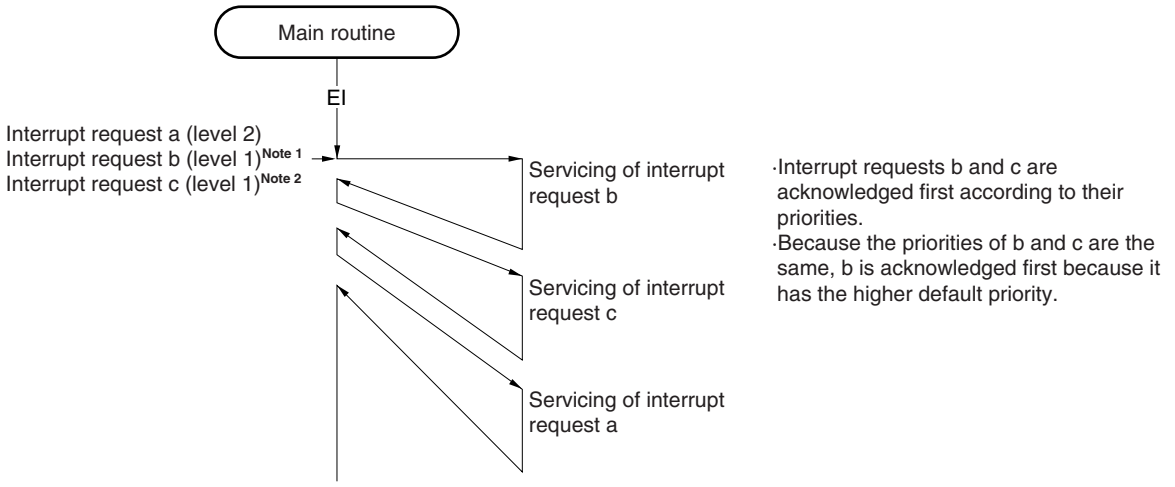
Figure 21-6. Example of Interrupt Nesting (2/2)



Notes 1. Lower default priority

2. Higher default priority

Figure 21-7. Example of Servicing Simultaneously Generated Interrupt Request Signals



Notes 1. Higher default priority

2. Lower default priority

21.3.4 Interrupt control register (xxICn)

An interrupt control register is assigned to each maskable interrupt and sets the control conditions for each maskable interrupt request.

The interrupt control registers can be read or written in 8-bit or 1-bit units.

Reset sets xxICn to 47H.

Caution Be sure to read the xxICn.xxIFn bit while interrupts are disabled (DI). If the xxIFn bit is read while interrupts are enabled (EI), an incorrect value may be read if there is a conflict between acknowledgment of the interrupt and reading of the bit.

After reset: 47H R/W Address: FFFFF110H to FFFFF168H

	<7>	<6>	5	4	3	2	1	0
xxICn	xxIFn	xxMKn	0	0	0	xxPRn2	xxPRn1	xxPRn0

xxIFn	Interrupt request flag[Note]
0	Interrupt request not generated
1	Interrupt request generated

xxMKn	Interrupt mask flag
0	Enables interrupt servicing
1	Disables interrupt servicing (pending)

xxPRn2	xxPRn1	xxPRn0	Interrupt priority specification bit
0	0	0	Specifies level 0 (highest)
0	0	1	Specifies level 1
0	1	0	Specifies level 2
0	1	1	Specifies level 3
1	0	0	Specifies level 4
1	0	1	Specifies level 5
1	1	0	Specifies level 6
1	1	1	Specifies level 7 (lowest)

Note Automatically reset by hardware when interrupt request is acknowledged.

Remark xx: Identifying name of each peripheral unit (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

n: Peripheral unit number (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

Following tables list the addresses and bits of the interrupt control registers.

Table 21-2. Interrupt Control Registers (xxICn) (1/2)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF110H	WDT1IC	WDT1IF	WDT1MK	0	0	0	WDT1PR2	WDT1PR1	WDT1PR0
FFFFF112H	PIC0	PIF0	PMK0	0	0	0	PPR02	PPR01	PPR00
FFFFF114H	PIC1	PIF1	PMK1	0	0	0	PPR12	PPR11	PPR10
FFFFF116H	PIC2	PIF2	PMK2	0	0	0	PPR22	PPR21	PPR20
FFFFF118H	PIC3	PIF3	PMK3	0	0	0	PPR32	PPR31	PPR30
FFFFF11AH	PIC4	PIF4	PMK4	0	0	0	PPR42	PPR41	PPR40
FFFFF11CH	PIC5	PIF5	PMK5	0	0	0	PPR52	PPR51	PPR50
FFFFF11EH	PIC6	PIF6	PMK6	0	0	0	PPR62	PPR61	PPR60
FFFFF120H	TM0IC00	TM0IF00	TM0MK00	0	0	0	TM0PR002	TM0PR001	TM0PR000
FFFFF122H	TM0IC01	TM0IF01	TM0MK01	0	0	0	TM0PR012	TM0PR011	TM0PR010
FFFFF124H	TM0IC10	TM0IF10	TM0MK10	0	0	0	TM0PR102	TM0PR101	TM0PR100
FFFFF126H	TM0IC11	TM0IF11	TM0MK11	0	0	0	TM0PR112	TM0PR111	TM0PR110
FFFFF128H	TM5IC0	TM5IF0	TM5MK0	0	0	0	TM5PR02	TM5PR01	TM5PR00
FFFFF12AH	TM5IC1	TM5IF1	TM5MK1	0	0	0	TM5PR12	TM5PR11	TM5PR10
FFFFF12CH	CSI0IC0	CSI0IF0	CSI0MK0	0	0	0	CSI0PR02	CSI0PR01	CSI0PR00
FFFFF12EH	CSI0IC1	CSI0IF1	CSI0MK1	0	0	0	CSI0PR12	CSI0PR11	CSI0PR10
FFFFF130H	SREIC0	SREIF0	SREMK0	0	0	0	SREPR02	SREPR01	SREPR00
FFFFF132H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF134H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF136H	SREIC1	SREIF1	SREMK1	0	0	0	SREPR12	SREPR11	SREPR10
FFFFF138H	SRIC1	SRIF1	SRMK1	0	0	0	SRPR12	SRPR11	SRPR10
FFFFF13AH	STIC1	STIF1	STMK1	0	0	0	STPR12	STPR11	STPR10
FFFFF13CH	TMHIC0	TMHIF0	TMHMK0	0	0	0	TMHPR02	TMHPR01	TMHPR00
FFFFF13EH	TMHIC1	TMHIF1	TMHMK1	0	0	0	TMHPR12	TMHPR11	TMHPR10
FFFFF140H	CSIAIC0	CSIAIF0	CSIAMK0	0	0	0	CSIAPR02	CSIAPR01	CSIAPR00
FFFFF142H	IICIC0	IICIF0	IICMK0	0	0	0	IICPR02	IICPR01	IICPR00
FFFFF144H	ADIC	ADIF	ADMK	0	0	0	ADPR2	ADPR1	ADPR0
FFFFF146H	KRIC	KRIF	KRMK	0	0	0	KRPR2	KRPR1	KRPR0
FFFFF148H	WTIIC	WTIIF	WTIMK	0	0	0	WTIPR2	WTIPR1	WTIPR0
FFFFF14AH	WTIC	WTIF	WTMK	0	0	0	WTPR2	WTPR1	WTPR0
FFFFF14CH	BRGIC	BRGIF	BRGMK	0	0	0	BRGPR2	BRGPR1	BRGPR0
FFFFF14EH	TM0IC20	TM0IF20	TM0MK20	0	0	0	TM0PR202	TM0PR201	TM0PR200
FFFFF150H	TM0IC21	TM0IF21	TM0MK21	0	0	0	TM0PR212	TM0PR211	TM0PR210
FFFFF152H	TM0IC30	TM0IF30	TM0MK30	0	0	0	TM0PR302	TM0PR301	TM0PR300
FFFFF154H	TM0IC31	TM0IF31	TM0MK31	0	0	0	TM0PR312	TM0PR311	TM0PR310
FFFFF156H	CSIAIC1	CSIAIF1	CSIAMK1	0	0	0	CSIAPR12	CSIAPR11	CSIAPR10
FFFFF162H	SREIC2	SREIF2	SREMK2	0	0	0	SREPR22	SREPR21	SREPR20
FFFFF164H	SRIC2	SRIF2	SRMK2	0	0	0	SRPR22	SRPR21	SRPR20
FFFFF166H	STIC2	STIF2	STMK2	0	0	0	STPR22	STPR21	STPR20
FFFFF172H	PIC7	PIF7	PMK7	0	0	0	PPR72	PPR71	PPR70
FFFFF174H	TP0OVIC	TP0OVIF	TP0OVMK	0	0	0	TP0OVPR2	TP0OVPR1	TP0OVPR0
FFFFF176H	TP0CCIC0	TP0CCIF0	TP0CCMK0	0	0	0	TP0CCPR02	TP0CCPR01	TP0CCPR00
FFFFF178H	TP0CCIC1	TP0CCIF1	TP0CCMK1	0	0	0	TP0CCPR12	TP0CCPR11	TP0CCPR10
FFFFF17AH	DMAIC0	DMAIF0	DMAMK0	0	0	0	DMAPR02	DMAPR01	DMAPR00

Table 21-2. Interrupt Control Registers (xxICn) (2/2)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF17CH	DMAIC1	DMAIF1	DMAMK1	0	0	0	DMAPR12	DMAPR11	DMAPR10
FFFFF17EH	DMAIC2	DMAIF2	DMAMK2	0	0	0	DMAPR22	DMAPR21	DMAPR20
FFFFF180H	DMAIC3	DMAIF3	DMAMK3	0	0	0	DMAPR32	DMAPR31	DMAPR30

21.3.5 Interrupt mask registers 0 to 3 (IMR0 to IMR3)

These registers set the interrupt mask status for maskable interrupts. The xxMKn bit of the IMR0 to IMR3 registers and the xxMKn bit of the xxICn register are respectively linked.

The IMRm register can be read or written in 16-bit units.

When the higher 8 bits of the IMRm register are used as the IMRmH register and the lower 8 bits of the IMRm register as the IMRmL register, they can be read or written in 8-bit or 1-bit units (m = 0 to 3).

Caution In the device file, the xxMKn bit of the xxICn register is defined as a reserved word. Therefore, if bit manipulation is performed using the name xxMKn, the xxICn register, not the IMRm register, is rewritten (as a result, the IMRm register is also rewritten).

After reset: FFFFH R/W Address: IMR0 FFFFF100H, IMR0L FFFFF100H, IMR0H FFFFF101H

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	CSI0MK1	CSI0MK0	TM5MK1	TM5MK0	TM0MK11	TM0MK10	TM0MK01	TM0MK00
	7	6	5	4	3	2	1	0
(IMR0L)	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	WDT1MK

After reset: FFFFH R/W Address: IMR1 FFFFF102H, IMR1L FFFFF102H, IMR1H FFFFF103H

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	TM0MK20	BRGMK	WTMK	WTIMK	KRMK	ADMK	IICMK0	CSIAMK0
	7	6	5	4	3	2	1	0
(IMR1L)	TMHMK1	TMHMK0	STMK1	SRMK1	SREMK1	STMK0	SRMK0	SREMK0

After reset: FFFFH R/W Address: IMR2 FFFFF104H, IMR2L FFFFF104H, IMR2H FFFFF105H

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	1	1	1	1	STMK2	SRMK2	SREMK2	1
	7	6	5	4	3	2	1	0
(IMR2L)	1	1	1	1	CSIAMK1	TM0MK31	TM0MK30	TM0MK21

After reset: FFFFH R/W Address: IMR3 FFFFF106H, IMR3L FFFFF106H, IMR3H FFFFF107H

	15	14	13	12	11	10	9	8
IMR3 (IMR3H[Note])	1	1	1	1	1	1	1	DMAMK3
	7	6	5	4	3	2	1	0
(IMR3L)	DMAMK2	DMAMK1	DMAMK0	TP0CCMK1	TP0CCMK2	TP0OVFMK	PMK7	1

xxMKn	Interrupt mask flag setting
0	Enables interrupt servicing
1	Disables interrupt servicing

Note When reading from or writing to bits 8 to 15 of the IMR0 to IMR3 registers in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the IMR0H to IMR3H registers.

Caution Set bits 15 to 12 and 8 to 4 of the IMR2 register and bits 15 to 9 and 0 of the IMR3 register to 1. The operation is not guaranteed if their value is changed.

Remark xx: Identifying name of each peripheral unit (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

n: Peripheral unit number (refer to **Table 21-2 Interrupt Control Registers (xxICn)**)

21.3.6 In-service priority register (ISPR)

This register holds the priority level of the maskable interrupt currently being acknowledged. When the interrupt request signal is acknowledged, the bit of this register corresponding to the priority level of that interrupt request signal is set (1) and remains set while the interrupt is being serviced.

When the RETI instruction is executed, the bit among those that are set (1) in the ISPR register that corresponds to the interrupt request signal having the highest priority is automatically cleared (0) by hardware. However, it is not cleared (0) when execution is returned from non-maskable interrupt servicing or exception processing.

This register is read-only in 8-bit or 1-bit units.

Reset sets ISPR to 00H.

Caution If an interrupt is acknowledged while the ISPR register is being read in the interrupt enabled (EI) status, the value of the ISPR register after the bits of the register have been set to 1 by acknowledging the interrupt may be read. To accurately read the value of the ISPR register before an interrupt is acknowledged, read the register while interrupts are disabled (DI status).

After reset: 00H R Address: FFFFF1FAH

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
ISPR	ISPR7	ISPR6	ISPR5	ISPR4	ISPR3	ISPR2	ISPR1	ISPR0

ISPRn	Priority of interrupt currently being acknowledged
0	Interrupt request with priority n is not acknowledged
1	Interrupt request with priority n is being acknowledged

Remark n = 0 to 7 (priority level)

21.3.7 ID flag

The interrupt disable flag (ID) is allocated to the PSW and controls the maskable interrupt's operating state, and stores control information regarding enabling/disabling reception of interrupt request signals.

Reset sets this flag to 00000020H.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	EP	ID	SAT	CY	OV	S	Z

ID	Maskable interrupt servicing specification[Note]
0	Maskable interrupt request signal acknowledgment enabled
1	Maskable interrupt request signal acknowledgment disabled

Note Interrupt disable flag (ID) function

ID is set (1) by the DI instruction and cleared (0) by the EI instruction. Its value is also modified by the RETI instruction or LDSR instruction when referencing the PSW.

Non-maskable interrupt request signals and exceptions are acknowledged regardless of this flag. When a maskable interrupt request signal is acknowledged, the ID flag is automatically set (1) by hardware.

An interrupt request signal generated during the acknowledgment disabled period (ID flag = 1) can be acknowledged when the xxICn.xxIFn bit is set (1), and the ID flag is cleared (0).

21.3.8 Watchdog timer mode register 1 (WDTM1)

This register is a special register that can be written to only in a special sequence. To generate a maskable interrupt (INTWDT1), clear the WDTM14 bit to 0.

This register can be read or written in 8-bit or 1-bit units (for details, refer to **CHAPTER 12 WATCHDOG TIMER FUNCTIONS**).

After reset: 00H R/W Address: FFFFF6C2H

	<7>	6	5	4	3	2	1	0
WDTM1	RUN1	0	0	WDTM14	WDTM13	0	0	0

RUN1	Watchdog timer operation mode selection[Note 1]
0	Stop count operation
1	Clear counter and start count operation

WDTM14	WDTM13	Watchdog timer operation mode selection[Note 2]
0	0	Interval timer mode (Generate maskable interrupt INTWDTM1 when overflow occurs)
0	1	
1	0	Watchdog timer mode 1[Note 3] (Generate non-maskable interrupt INTWDT1 when overflow occurs)
1	1	Watchdog timer mode 2 (Start WDTRES2 reset operation when overflow occurs)

Notes 1. Once the RUN1 bit has been set (1), it cannot be cleared (0) by software. Therefore, once counting starts, it cannot be stopped except reset.

2. Once the WDTM14 and WDTM13 bits have been set (1), they cannot be cleared (0) by software. Reset is the only way to clear these bits.

3. For non-maskable interrupt servicing due to a non-maskable interrupt request signal (INTWDT1), refer to **21.10 Cautions**.

21.4 External Interrupt Request Input Pins (NMI, INTP0 to INTP7)

21.4.1 Noise elimination

(1) Noise elimination for NMI pin

The NMI pin includes a noise eliminator that operates using analog delay. Therefore, a signal input to the NMI pin is not detected as an edge unless it maintains its input level for a certain period. The edge is detected only after a certain period has elapsed.

The NMI pin is used for releasing the STOP mode. In the STOP mode, noise elimination using the system clock is not performed because the internal system clock is stopped.

(2) Noise elimination for INTP0 to INTP2 and INTP4 to INTP7 pins

The INTP0 to INTP2 and INTP4 to INTP7 pins include a noise eliminator that operates using analog delay. Therefore, a signal input to each pin is not detected as an edge unless it maintains its input level for a certain period. The edge is detected only after a certain period has elapsed.

(3) Noise elimination for INTP3 pin

The INTP3 pin has a digital/analog noise eliminator that can be selected by the NFC.NFEN bit.

The number of times the digital noise eliminator samples signals can be selected by the NFC.NFSTS bit from three or two. The sampling clock can be selected by the NFC.NFC2 to NFC.NFC0 bits from $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$, $f_{XX}/512$, $f_{XX}/1024$, and f_{XT}. If the sampling clock is set to $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$, $f_{XX}/512$, or $f_{XX}/1024$, the sampling clock stops in the IDLE/STOP mode. It cannot therefore be used to release the standby mode. To release the standby mode, select f_{XT} as the sampling clock or select the analog noise eliminator.

(a) Digital noise elimination control register (NFC)

The NFC register controls elimination of noise on the INTP3 pin. If f_{XT} is used as the noise elimination clock, the external interrupt function of the INTP3 pin can be used even in the IDLE/STOP mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets NFC to 00H.

After reset: 00H R/W Address: FFFFF318H

	7	6	5	4	3	2	1	0
NFC	NFEN	NFSTS	0	0	0	NFC2	NFC1	NFC0

NFEN	Setting of INTP3 pin noise elimination
0	Analog noise elimination
1	Digital noise elimination

NFSTS	Setting of number of samplings of digital noise elimination
0	Number of samplings = 3 times
1	Number of samplings = 2 times

NFC2	NFC1	NFC0	Selection of sampling clock
0	0	0	$f_{XX}/64$
0	0	1	$f_{XX}/128$
0	1	0	$f_{XX}/256$
0	1	1	$f_{XX}/512$
1	0	0	$f_{XX}/1024$
1	0	1	f_{XT}
Other than above			Setting prohibited

Remark f_{XX}: Main clock frequency

f_{XT}: Subclock frequency

<Noise elimination width>

The digital noise elimination width (t_{WIT3}) is as follows, where T is the sampling clock period and M is the number of samplings.

- $t_{WIT3} < (M - 1)T$: Accurately eliminated as noise
- $(M - 1)T \leq t_{WIT3} < MT$: May be eliminated as noise or detected as valid edge
- $t_{WIT3} \geq MT$: Accurately detected as valid edge

To detect the valid edge input to the INTP3 pin accurately, therefore, a pulse wider than MT must be input.

NFSTS	NFC2	NFC1	NFC0	Sampling Clock	Minimum Elimination Noise Width		
					f_{XX} = 20 MHz	f_{XX} = 10 MHz	f_{XX} = 8 MHz
0	0	0	0	f_{XX}/64	6.4 μs	12.8 μs	16 μs
0	0	0	1	f_{XX}/128	12.8 μs	25.6 μs	32 μs
0	0	1	0	f_{XX}/256	25.6 μs	51.2 μs	64 μs
0	0	1	1	f_{XX}/512	51.2 μs	102.4 μs	128 μs
0	1	0	0	f_{XX}/1024	102.4 μs	204.8 μs	256 μs
0	1	0	1	f_{XT} (32.768 kHz)	61.04 μs		
1	0	0	0	f_{XX}/64	3.2 μs	6.4 μs	8 μs
1	0	0	1	f_{XX}/128	6.4 μs	12.8 μs	16 μs
1	0	1	0	f_{XX}/256	12.8 μs	25.6 μs	32 μs
1	0	1	1	f_{XX}/512	25.6 μs	51.2 μs	64 μs
1	1	0	0	f_{XX}/1024	51.2 μs	102.4 μs	128 μs
1	1	0	1	f_{XT} (32.768 kHz)	30.52 μs		
Other than above				Setting prohibited			

21.4.2 Edge detection

The valid edges of the NMI and INTP0 to INTP7 pins can be selected from the following four types for each pin.

- Rising edge
- Falling edge
- Both edges
- No edge detection

After reset, the edge detection for the NMI pin is set to “no edge detection”. Therefore, interrupt requests cannot be acknowledged (the NMI pin functions as a normal port) unless a valid edge is specified by the INTR0 and INTF0 registers.

When using the P02 pin as an output port, set the NMI pin valid edge to “no edge detection”.

(1) External interrupt rising and falling edge specification registers 0 (INTR0, INTF0)

These are 8-bit registers that specify detection of the rising and falling edges of the NMI and INTP0 to INTP3 pins.

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When switching to the port function from the external interrupt function (alternate function), edge detection may be performed. Therefore, set the port mode after setting the INTF0n and INTR0n bits = 00.

After reset: 00H R/W Address: INTR0 FFFFFC20H, INTF0 FFFFFC00H

	7	6	5	4	3	2	1	0
INTR0	0	INTR06	INTR05	INTR04	INTR03	INTR02	0	0
		INTP3	INTP2	INTP1	INTP0	NMI		
	7	6	5	4	3	2	1	0
INTF0	0	INTF06	INTF05	INTF04	INTF03	INTF02	0	0
		INTP3	INTP2	INTP1	INTP0	NMI		

Remark For specification of the valid edge, refer to **Table 21-3**.

Table 21-3. NMI and INTP0 to INTP3 Pins Valid Edge Specification

INTF0n	INTR0n	Valid edge specification (n = 2 to 6)
0	0	No edge detection
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Remark n = 2: Control of NMI pin

n = 3 to 6: Control of INTP0 to INTP3 pins

(2) External interrupt rising and falling edge specification registers 3 (INTR3, INTF3)

These are 8-bit registers that specify detection of the rising and falling edges of the INTP7 pin.

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When switching to the port function from the external interrupt function (alternate function), edge detection may be performed. Therefore, set the port mode after setting the INTF31 and INTR31 bits = 00.

After reset: 00H R/W Address: INTR3 FFFFFC26H, INTF3 FFFFFC06H

	7	6	5	4	3	2	1	0
INTR3	0	0	0	0	0	0	INTR31	0
							INTP7	
	7	6	5	4	3	2	1	0
INTF3	0	0	0	0	0	0	INTF31	0
							INTP7	

Remark For specification of the valid edge, refer to **Table 21-4**.

Table 21-4. INTP7 Pin Valid Edge Specification

INTF31	INTR31	Valid edge specification
0	0	No edge detection
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

(3) External interrupt rising and falling edge specification registers 9H (INTR9H, INTF9H)

These are 8-bit registers that specify detection of the rising edge of the INTP4 to INTP6 pins.

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When switching to the port function from the external interrupt function (alternate function), edge detection may be performed. Therefore, set the port mode after setting the INTF9n and INTR9n bits = 00.

After reset: 00H R/W Address: INTR9H FFFFFC33H, INTF9H FFFFFC13H

	7	6	5	4	3	2	1	0
INTR9H	INTR915	INTR914	INTR913	0	0	0	0	0
	INTP6	INTP5	INTP4					
	7	6	5	4	3	2	1	0
INTF9H	INTF915	INTF914	INTF913	0	0	0	0	0
	INTP6	INTP5	INTP4					

Remark For specification of the valid edge, refer to **Table 21-5**.

Table 21-5. INTP4 to INTP6 Pins Valid Edge Specification

INTF9n	INTR9n	Valid edge specification (n = 13 to 15)
0	0	No edge detection
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Remark n = 13 to 15: Control of INTP4 to INTP6 pins

21.5 Software Exceptions

A software exception is generated when the CPU executes the TRAP instruction. Software exceptions can always be acknowledged.

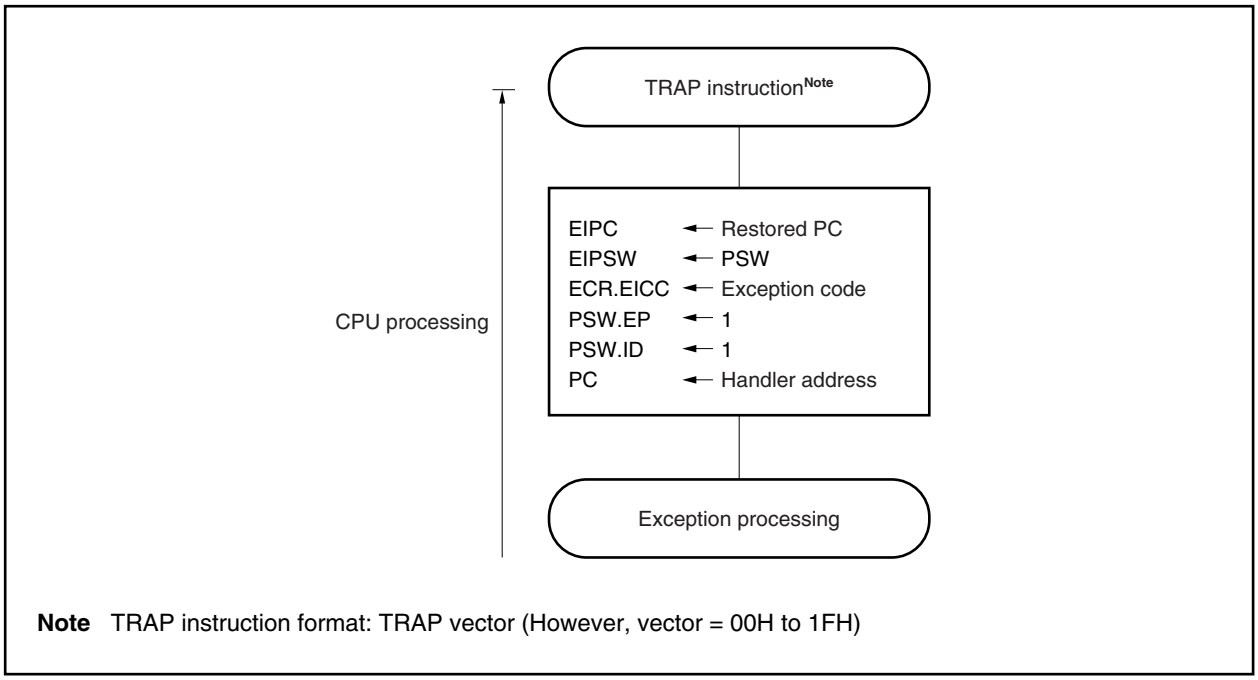
21.5.1 Operation

If a software exception occurs, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower 16 bits (EICC) of ECR (interrupt source).
<4> Sets the PSW.EP and PSW.ID bits to 1.
<5> Loads the handler address (00000040H or 00000050H) for the software exception routine to the PC and transfers control.

Figure 21-8 shows the software exception processing flow.

Figure 21-8. Software Exception Processing



Note TRAP instruction format: TRAP vector (However, vector = 00H to 1FH)

The handler address is determined by the operand (vector) of the TRAP instruction. If the vector is 00H to 1FH, the handler address is 00000040H, and if the vector is 10H to 1FH, the handler address is 00000050H.

21.5.2 Restore

Execution is restored from software exception processing by the RETI instruction.

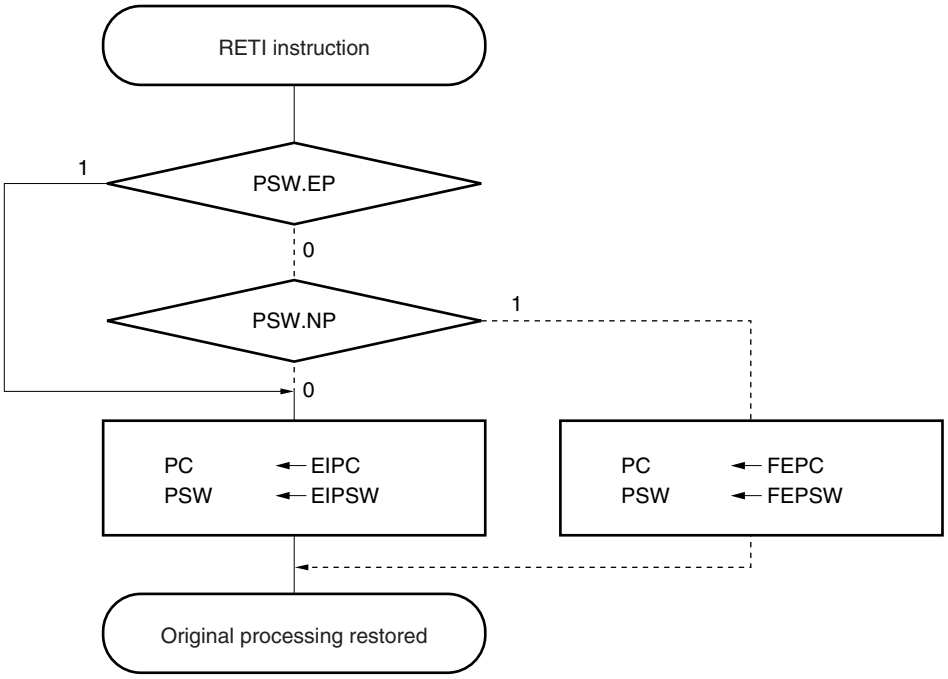
When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from EIPC and EIPSW because the PSW.EP bit is 1.

<2> Transfers control to the address of the restored PC and PSW.

Figure 21-9 shows the processing flow of the RETI instruction.

Figure 21-9. RETI Instruction Processing



Caution When the EP bit and the NP bit are changed by the LDSR instruction during software exception processing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to set the EP bit back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

21.5.3 EP flag

The EP flag is a status flag that indicates that exception processing is in progress. It is set when an exception occurs.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	EP	ID	SAT	CY	OV	S	Z

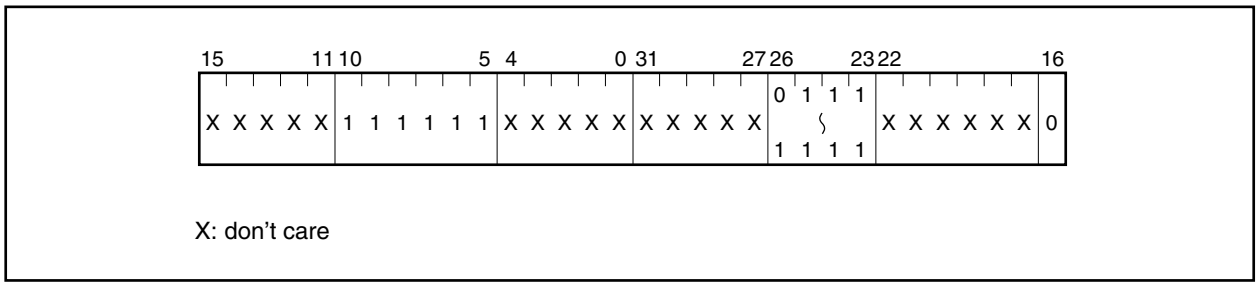
EP	Exception processing status
0	Exception processing not in progress
1	Exception processing in progress

21.6 Exception Trap

The exception trap is an interrupt that is requested when the illegal execution of an instruction takes place. In the V850ES/KG2, an illegal op code trap (ILGOP: illegal OP code trap) is considered as an exception trap.

21.6.1 Illegal op code

An illegal op code is defined as an instruction with instruction op code (bits 10 to 5) = 111111B, sub-op code (bits 26 to 23) = 0111B to 1111B, and sub-op code (bit 16) = 0B. When such an instruction is executed, an exception trap is generated.



Caution It is recommended not to use illegal op code because instructions may newly be assigned in the future.

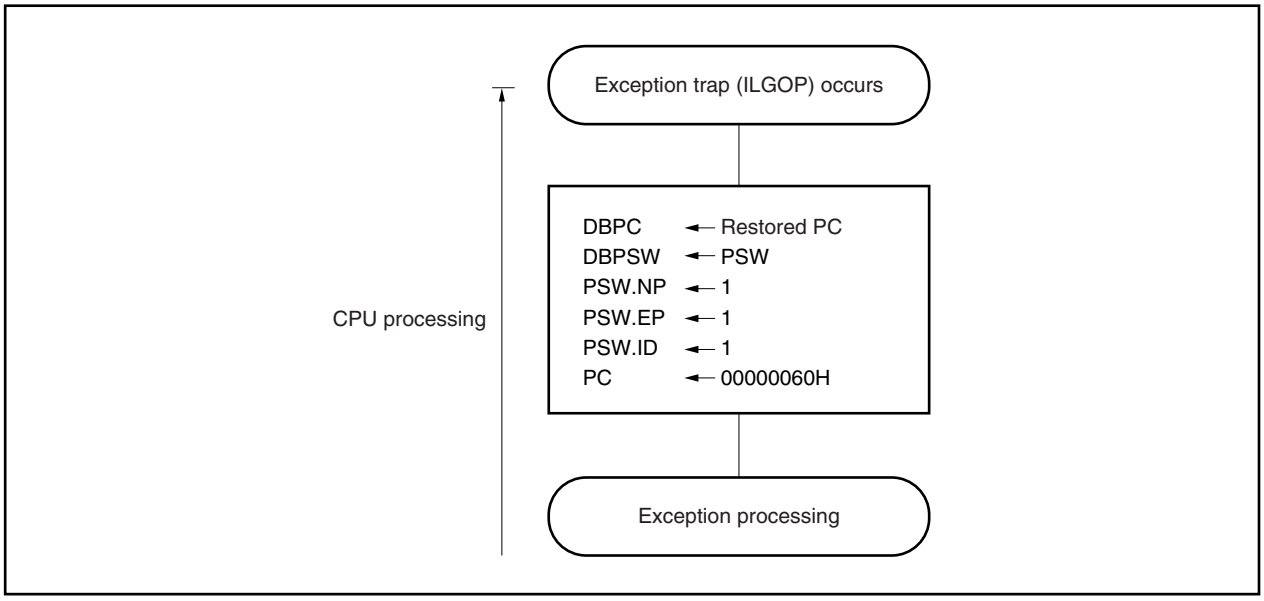
(1) Operation

Upon generation of an exception trap, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to DBPC.
<2> Saves the current PSW to DBPSW.
<3> Sets the PSW.NP, PSW.EP, and PSW.ID bits.
<4> Loads the handler address (00000060H) for the exception trap routine to the PC and transfers control.

Figure 21-10 shows the exception trap processing flow.

Figure 21-10. Exception Trap Processing



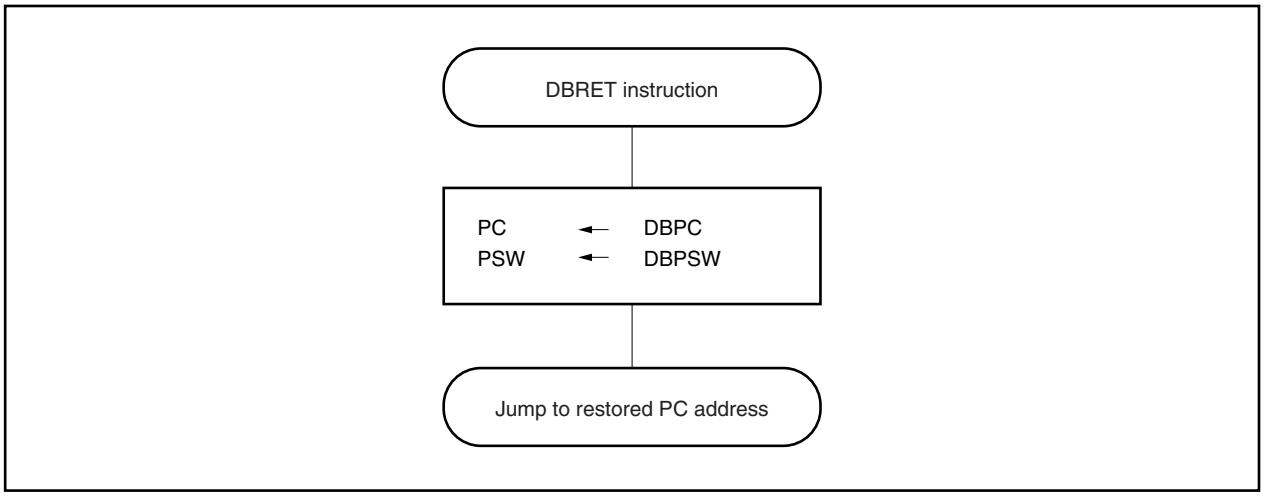
(2) Restore

Execution is restored from exception trap processing by the DBRET instruction. When the DBRET instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from DBPC and DBPSW.
<2> Transfers control to the loaded address of the restored PC and PSW.

Figure 21-11 shows the processing flow for restore from exception trap processing.

Figure 21-11. Processing Flow for Restore from Exception Trap



21.6.2 Debug trap

A debug trap is an exception that occurs upon execution of the DBTRAP instruction and that can be acknowledged at all times.

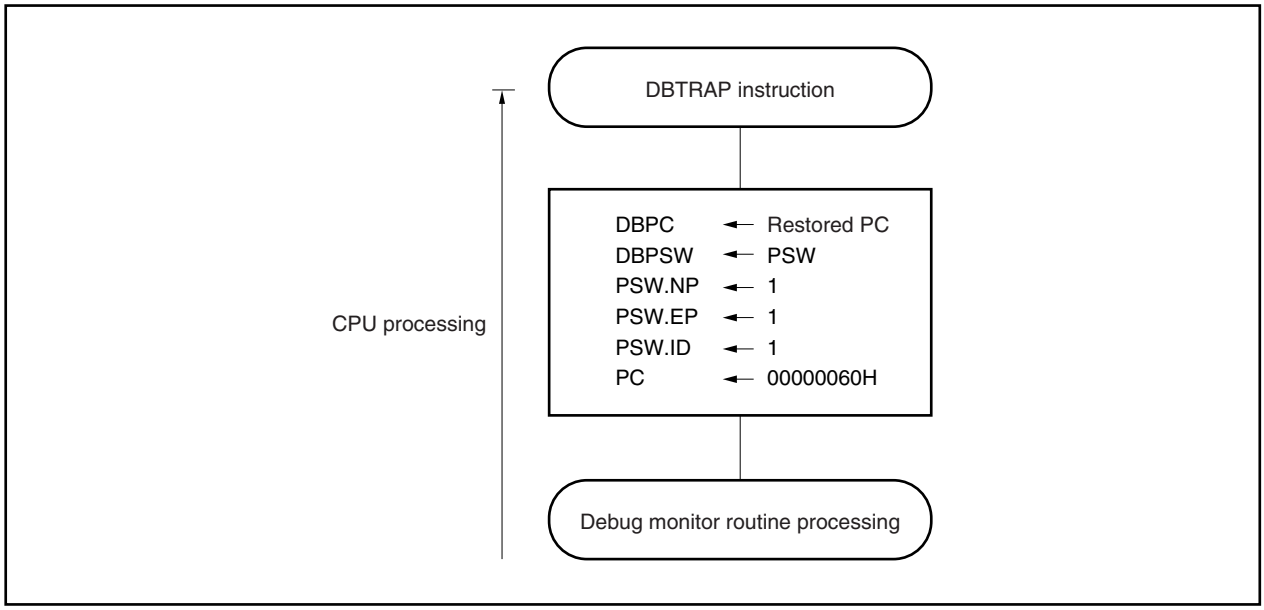
When a debug trap occurs, the CPU performs the following processing.

(1) Operation

<1> Saves the restored PC to DBPC.
<2> Saves the current PSW to DBPSW.
<3> Sets the PSW.NP, PSW.EP, and PSW.ID bits to 1.
<4> Sets the handler address (00000060H) for the debug trap routine to the PC and transfers control.

Figure 21-12 shows the debug trap processing flow.

Figure 21-12. Debug Trap Processing



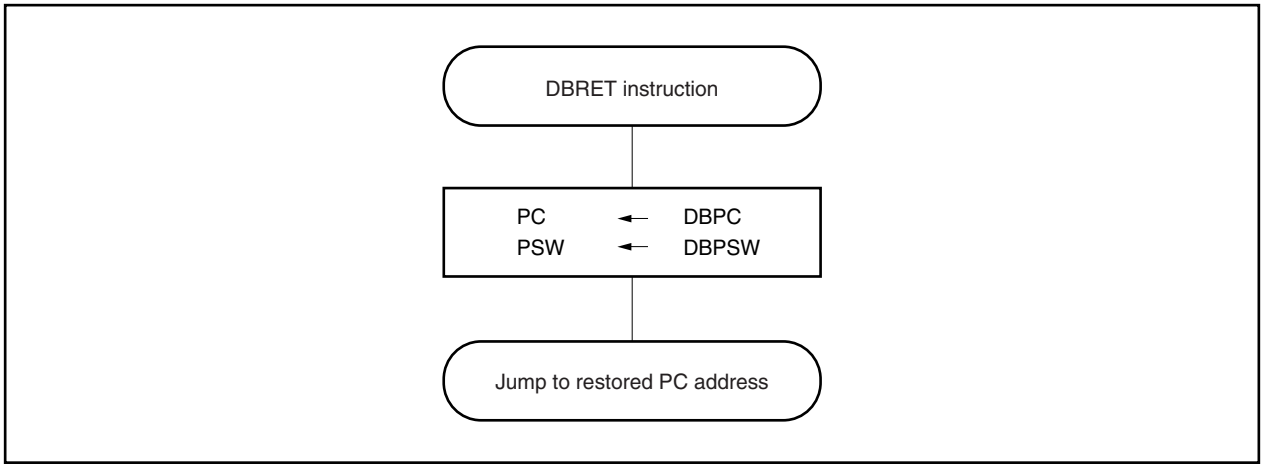
(2) Restore

Execution is restored from debug trap processing by the DBRET instruction. When the DBRET instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from DBPC and DBPSW.
<2> Transfers control to the loaded address of the restored PC and PSW.

Figure 21-13 shows the processing flow for restore from debug trap processing.

Figure 21-13. Processing Flow for Restore from Debug Trap



21.7 Multiple Interrupt Servicing Control

Multiple interrupt servicing control is a function that stops an interrupt service routine currently in progress if a higher priority interrupt request signal is generated, and processes the acknowledgment operation of the higher priority interrupt request signal.

If an interrupt request signal with a lower or equal priority is generated and a service routine is currently in progress, the later interrupt request signal will be held pending.

Multiple interrupt servicing control is performed when interrupts are enabled (PSW.ID bit = 0). Even in an interrupt servicing routine, multiple interrupt control must be performed while interrupts are enabled (ID bit = 0). If a maskable interrupt or software exception is generated in a maskable interrupt or software exception service program, EIPC and EIPSW must be saved.

The following example illustrates the procedure.

(1) To acknowledge maskable interrupt request signals in service program

Service program for maskable interrupt or exception

```
    …
    …
• EIPC saved to memory or register
• EIPSW saved to memory or register
• EI instruction (enables interrupt acknowledgment)
    …
    …                          ←Acknowledges maskable interrupt
    …
    …
• DI instruction (disables interrupt acknowledgment)
• Saved value restored to EIPSW
• Saved value restored to EIPC
• RETI instruction
```

(2) To generate exception in service program

Service program for maskable interrupt or exception

…
…
- EIPC saved to memory or register
- EIPSW saved to memory or register

…
- TRAP instruction ←Acknowledges exceptions such as TRAP instruction.

…
- Saved value restored to EIPSW
- Saved value restored to EIPC
- RETI instruction

Priorities 0 to 7 (0 is the highest) can be set for each maskable interrupt request in multiple interrupt servicing control by software. To set a priority level, write values to the xxICn.xxPRn0 to xxICn.xxPRn2 bits corresponding to each maskable interrupt request. After reset, interrupt requests are masked by the xxICn.xxMKn bit, and the priority is set to level 7 by the xxPRn0 to xxPRn2 bits.

Priorities of maskable interrupts are as follows.

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

Interrupt servicing that has been suspended as a result of multiple interrupt servicing control is resumed after the interrupt servicing of the higher priority has been completed and the RETI instruction has been executed.
A pending interrupt request signal is acknowledged after the current interrupt servicing has been completed and the RETI instruction has been executed.

Caution In a non-maskable interrupt servicing routine (in the time until the RETI instruction is executed), maskable interrupts are not acknowledged and held pending.

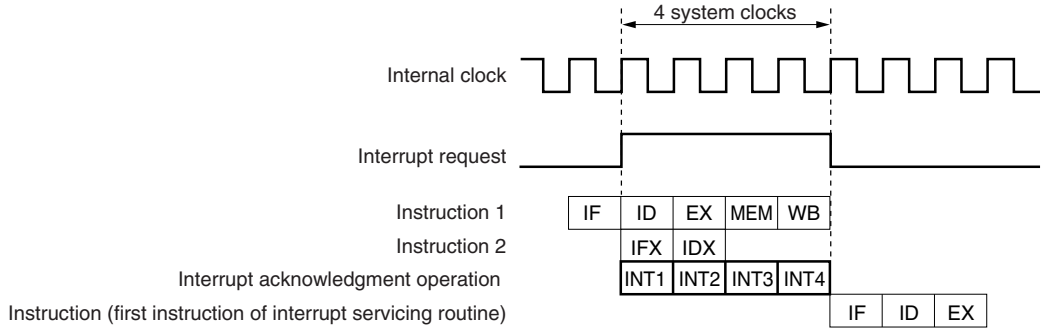
21.8 Interrupt Response Time

Except in the following cases, the CPU interrupt response time is a minimum of 4 clocks. If inputting consecutive interrupt request signals, at least 4 clocks must be placed between each interrupt request signal.

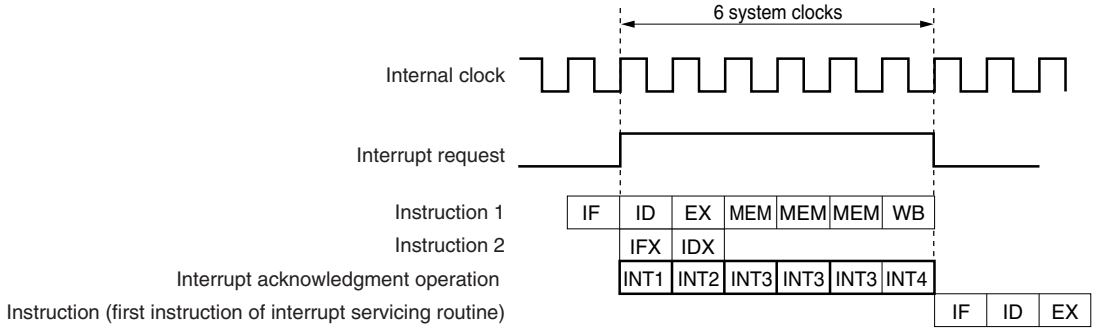
- IDLE/STOP mode
- External bus access
- Consecutive interrupt request non-sample instruction (refer to **21.9 Periods in Which Interrupts Are Not Acknowledged by CPU**)
- Access to interrupt control register
- Access to peripheral I/O register

Figure 21-14. Pipeline Operation During Interrupt Request Signal Acknowledgment (Outline)

(1) Minimum interrupt response time



(2) Maximum interrupt response time



Remark INT1 to INT4: Interrupt acknowledgment processing
IFX: Invalid instruction fetch
IDX: Invalid instruction decode

Interrupt response time (internal system clock)			Condition
	Internal interrupt	External interrupt	
Min.	4	4 + analog delay	The following cases are excluded. • IDLE/STOP mode • External bus access • Consecutive interrupt request non-sample instruction • Access to interrupt control register • Access to peripheral I/O register
Max.	6	6 + analog delay	

21.9 Periods in Which Interrupts Are Not Acknowledged by CPU

Interrupts are acknowledged by the CPU while an instruction is being executed. However, no interrupt is acknowledged between an interrupt request non-sample instruction and the next instruction.

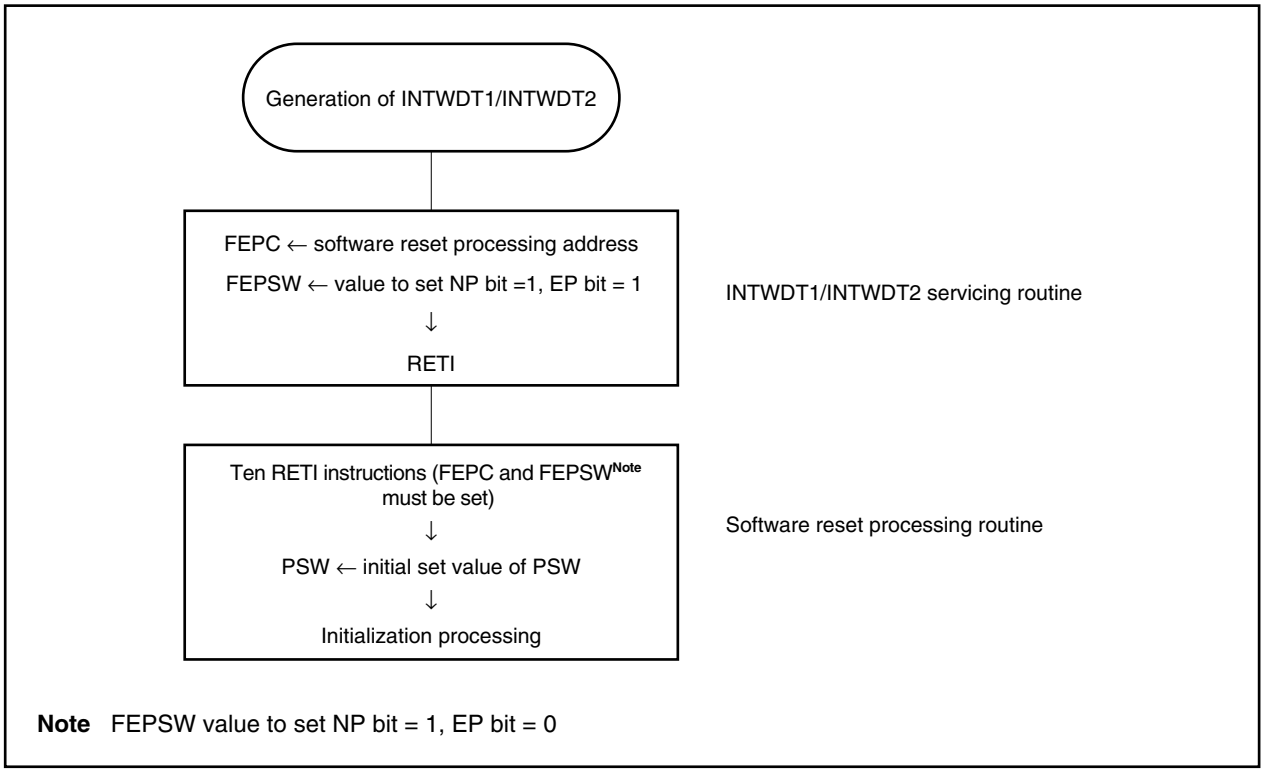
The following instructions are interrupt request non-sample instructions.

- EI instruction
- DI instruction
- LDSR reg2, 0x5 instructions (vs. PSW)
- Store instruction for the PRCMD register
- Store instruction and bit manipulation instruction for the following registers
  - Interrupt-related registers:
    Interrupt control register (xxICn), interrupt mask registers 0 to 3 (IMR0 to IMR3)

21.10 Cautions

Design the system so that restoring by the RETI instruction is as follows after a non-maskable interrupt triggered by a non-maskable interrupt request signal (INTWDT1/INTWDT2) is serviced.

Figure 21-15. Restoring by RETI Instruction



Note FEPSW value to set NP bit = 1, EP bit = 0

CHAPTER 22 KEY INTERRUPT FUNCTION

22.1 Function

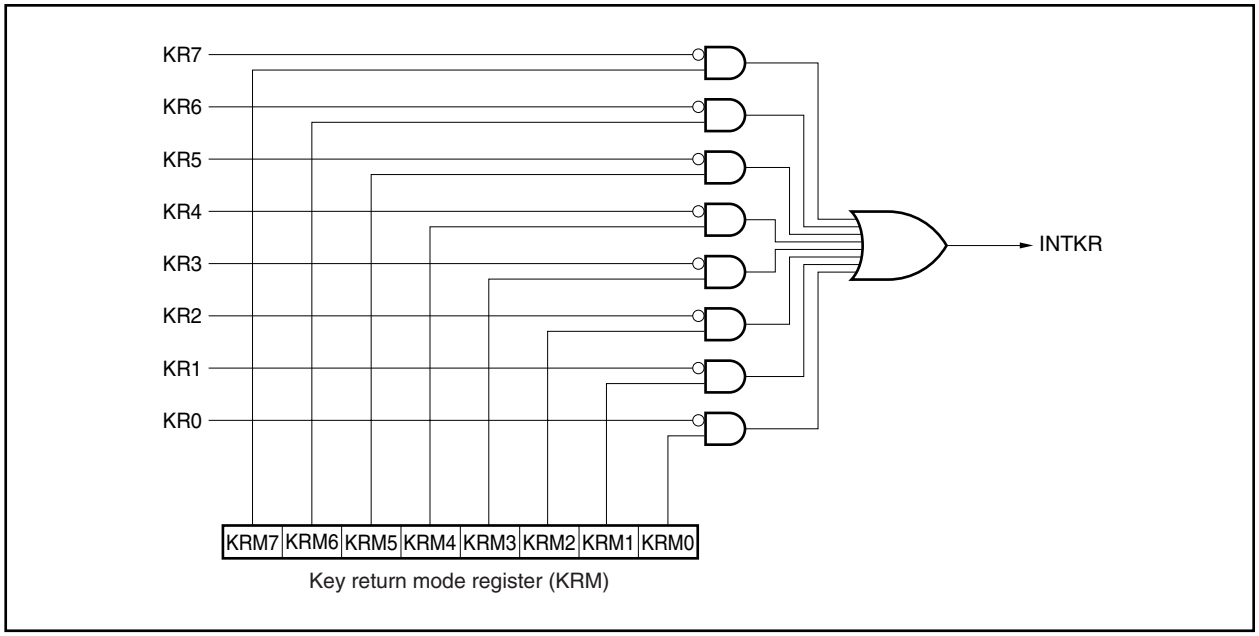
A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the KRM register.

Caution If any of the KR0 to KR7 pins is at low level, the INTKR signal is not generated even if a falling edge is input to another pin.

Table 22-1. Assignment of Key Return Detection Pins

Flag	Pin Description
KRM0	Controls KR0 signal in 1-bit units
KRM1	Controls KR1 signal in 1-bit units
KRM2	Controls KR2 signal in 1-bit units
KRM3	Controls KR3 signal in 1-bit units
KRM4	Controls KR4 signal in 1-bit units
KRM5	Controls KR5 signal in 1-bit units
KRM6	Controls KR6 signal in 1-bit units
KRM7	Controls KR7 signal in 1-bit units

Figure 22-1. Key Return Block Diagram



22.2 Register

(1) Key return mode register (KRM)

The KRM register controls the KRM0 to KRM7 bits using the KR0 to KR7 signals.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF300H

	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key return mode control
0	Does not detect key return signal
1	Detects key return signal

Caution If the KRM register is changed, an interrupt request signal (INTKR) may be generated. To prevent this, change the KRM register after disabling interrupts (DI), and then enable interrupts (EI) after clearing the interrupt request flag (KRIC.KRIF bit) to 0.

Remark For the alternate-function pin settings, refer to **Table 4-16 Settings When Port Pins Are Used for Alternate Functions**.

CHAPTER 23 STANDBY FUNCTION

23.1 Overview

The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application.

The available standby modes are listed in Table 23-1.

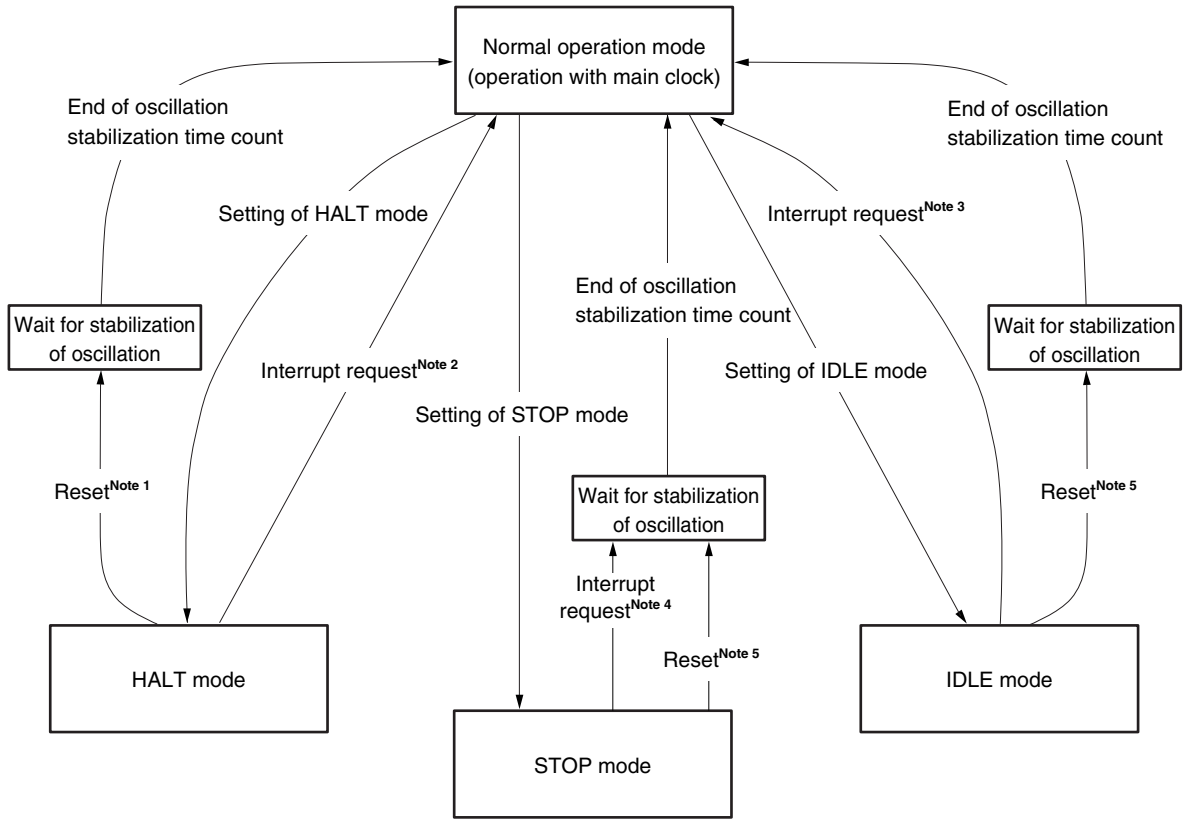
Table 23-1. Standby Modes

Mode	Functional Outline
HALT mode	Mode to stop only the operating clock of the CPU
IDLE mode	Mode to stop all the operations of the internal circuits except the oscillator[Note 1]
STOP mode	Mode to stop all the operations of the internal circuits except the subclock oscillator[Note 2]
Subclock operation mode	Mode to use the subclock as the internal system clock
Sub-IDLE mode	Mode to stop all the operations of the internal circuits, except the oscillator, in the subclock operation mode

Notes 1. The PLL does not stop. To realize low power consumption, stop the PLL and then shift to the IDLE mode.

2. Change to the clock-through mode, stop the PLL, then shift to the STOP mode. For details, refer to **CHAPTER 6 CLOCK GENERATION FUNCTION**.

Figure 23-1. Status Transition (1/2)



Notes 1. Reset by $\overline{\text{RESET}}$ pin input, watchdog timer 1 overflow (WDTRES1), or watchdog timer 2 overflow (WDTRES2).

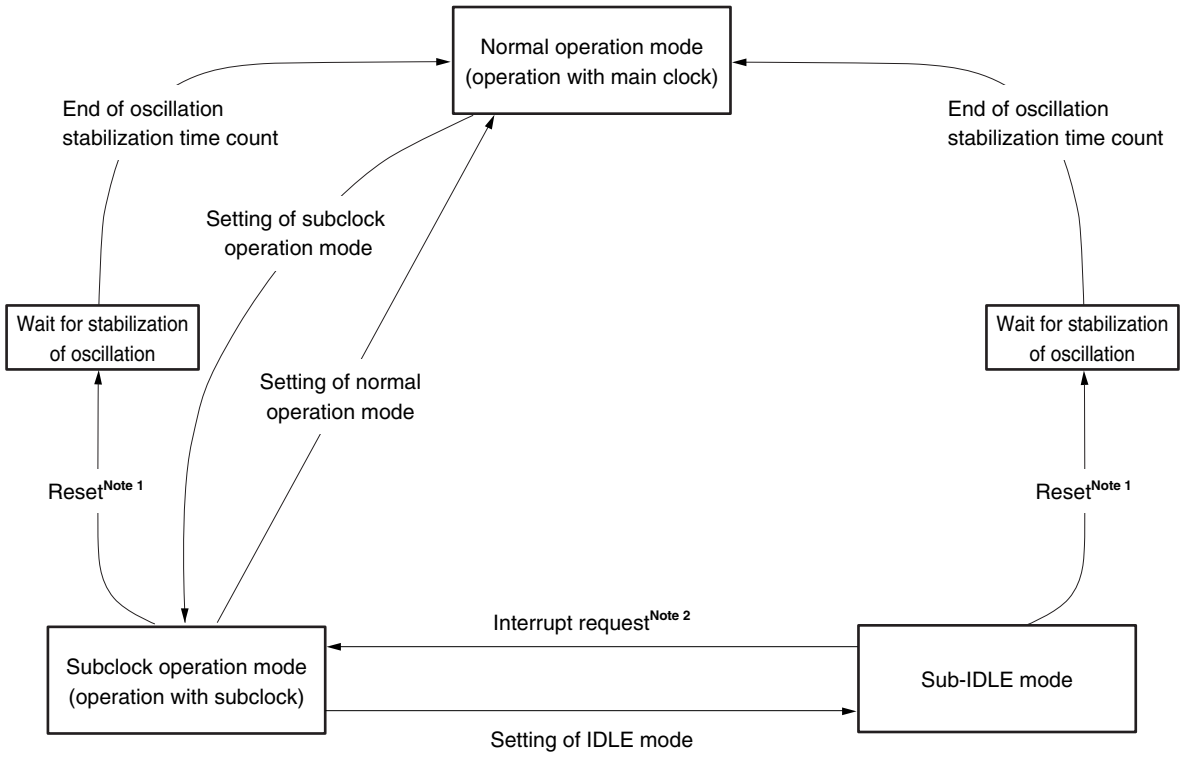
2. Non-maskable interrupt request signal (NMI, INTWDT1, INTWDT2) or unmasked maskable interrupt request signal.

3. Non-maskable interrupt request signal (NMI pin input, INTWDT2 (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), or unmasked internal interrupt request signal from peripheral functions operable in IDLE mode.

4. Non-maskable interrupt request signal (NMI pin input, INTWDT2 (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), or unmasked internal interrupt request signal from peripheral functions operable in STOP mode.

5. Reset by $\overline{\text{RESET}}$ pin input or watchdog timer 2 (when the CPU is operating on the subclock) overflow (WDTRES2).

Figure 23-1. Status Transition (2/2)



Notes 1. Reset by $\overline{\text{RESET}}$ pin input or watchdog timer 2 overflow (WDTRES2).

2. Non-maskable interrupt request signal (NMI pin input, INTWDT2 (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), or unmasked internal interrupt request signal from peripheral functions operable in sub-IDLE mode.

23.2 Registers

(1) Power save control register (PSC)

This is an 8-bit register that controls the standby function. The STP bit of this register is used to specify the standby mode. The PSC register is a special register that can be written to only in a special sequence (refer to **3.4.7 Special registers**).

This register can be read or written in 8-bit or 1-bit units.

Reset sets PSC to 00H.

After reset: 00H R/W Address: FFFFF1FEH

	<7>	6	<5>	<4>	3	2	<1>	0
PSC	NMI2M	0	NMI0M	INTM	0	0	STP	0

NMI2M	Control of releasing standby mode[Note] by INTWDT2 signal
0	Releasing standby mode[Note] by INTWDT2 signal enabled
1	Releasing standby mode[Note] by INTWDT2 signal disabled

NMI0M	Control of releasing standby mode[Note] by NMI pin input
0	Releasing standby mode[Note] by NMI pin input enabled
1	Releasing standby mode[Note] by NMI pin input disabled

INTM	Control of releasing standby mode[Note] by maskable interrupt request signals
0	Releasing standby mode[Note] by maskable interrupt request signals enabled
1	Releasing standby mode[Note] by maskable interrupt request signals disabled

STP	Standby mode[Note] setting
0	Normal mode
1	Standby mode[Note]

Note In this case, standby mode means the IDLE/STOP mode; it does not include the HALT mode.

Cautions 1. If the NMI2M, NMI0M, and INTM bits, and the STP bit are set to 1 at the same time, the setting of NMI2M, NMI0M, and INTM bits becomes invalid. If there is an unmasked interrupt request signal being held pending when the IDLE/STOP mode is set, set the bit corresponding to the interrupt request signal (NMI2M, NMI0M, or INTM) to 1, and then set the STP bit to 1.

2. When the IDLE/STOP mode is set, set the PSMR.PSM bit and then set the STP bit.

(2) Power save mode register (PSMR)

This is an 8-bit register that controls the operation status in the standby mode and the clock operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets PSMR to 00H.

After reset: 00H R/W After reset: FFFFF820H

	7	6	5	4	3	2	1	<0>
PSMR	XTSTP	0	0	0	0	0	0	PSM

XTSTP	Specification of subclock oscillator use
0	Subclock oscillator used
1	Subclock oscillator not used

PSM	Specification of operation in standby mode
0	IDLE mode
1	STOP mode

Cautions 1. Be sure to clear the XTSTP bit to 0 during subclock resonator connection.

2. Be sure to clear bits 1 to 6 of the PSMR register to 0.

3. The PSM bit is valid only when the PSC.STP bit is 1.

(3) Oscillation stabilization time selection register (OSTS)

The wait time until the oscillation stabilizes after the STOP mode is released is controlled by the OSTS register.

The OSTS register can be read or written in 8-bit units.

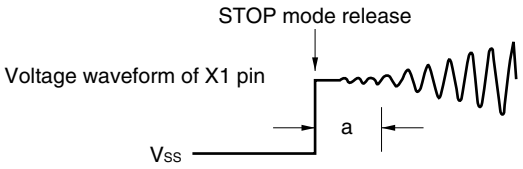
Reset sets OSTS to 01H.

After reset: 01H R/W Address: FFFFF6C0H

	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time			
				fx		
				4 MHz	5 MHz	10 MHz
0	0	0	$2^{13}/f_x$	2.048 ms	1.638 ms	0.819 ms
0	0	1	$2^{15}/f_x$	8.192 ms	6.554 ms	3.277 ms
0	1	0	$2^{16}/f_x$	16.38 ms	13.11 ms	6.554 ms
0	1	1	$2^{17}/f_x$	32.77 ms	26.21 ms	13.11 ms
1	0	0	$2^{18}/f_x$	65.54 ms	52.43 ms	26.21 ms
1	0	1	$2^{19}/f_x$	131.1 ms	104.9 ms	52.43 ms
1	1	0	$2^{20}/f_x$	262.1 ms	209.7 ms	104.9 ms
1	1	1	$2^{21}/f_x$	524.3 ms	419.4 ms	209.7 ms

Cautions 1. The wait time following release of the STOP mode does not include the time until the clock oscillation starts ("a" in the figure below) following release of the STOP mode, regardless of whether the STOP mode is released by reset or the occurrence of an interrupt request signal.



2. Be sure to clear bits 3 to 7 to "0".

3. The oscillation stabilization time following reset release is $2^{15}/f_x$ (because the initial value of the OSTS register = 01H).

4. The oscillation stabilization time is also inserted during external clock input.

Remark fx: Main clock oscillation frequency

23.3 HALT Mode

23.3.1 Setting and operation status

The HALT mode is set when a dedicated instruction (HALT) is executed in the normal operation mode.

In the HALT mode, the clock oscillator continues operating. Only clock supply to the CPU is stopped; clock supply to the other on-chip peripheral functions continues.

As a result, program execution is stopped, and the internal RAM retains the contents before the HALT mode was set. The on-chip peripheral functions that are independent of instruction processing by the CPU continue operating.

Table 23-3 shows the operation status in the HALT mode.

The average power consumption of the system can be reduced by using the HALT mode in combination with the normal operation mode for intermittent operation.

Cautions 1. Insert five or more NOP instructions after the HALT instruction.

2. If the HALT instruction is executed with an unmasked interrupt request signal held pending, the system shift to the HALT mode, but the HALT mode is immediately released by the pending interrupt request signal.

23.3.2 Releasing HALT mode

The HALT mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT1, INTWDT2 signal), an unmasked maskable interrupt request signal, and reset signal ($\overline{\text{RESET}}$ pin input, WDTRES1, WDTRES2 signal).

After the HALT mode has been released, the normal operation mode is restored.

(1) Releasing HALT mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal

The HALT mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the HALT mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

(a) If an interrupt request signal with a priority lower than that of the interrupt request currently being serviced is issued, only the HALT mode is released, and that interrupt request signal is not acknowledged. The interrupt request signal itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request signal currently being serviced is issued (including a non-maskable interrupt request signal), the HALT mode is released and that interrupt request signal is acknowledged.

Table 23-2. Operation After Releasing HALT Mode by Interrupt Request Signal

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request signal	Execution branches to the handler address	
Maskable interrupt request signal	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

(2) Releasing HALT mode by reset

The same operation as the normal reset operation is performed.

Table 23-3. Operation Status in HALT Mode

Setting of HALT Mode / Item		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
Main clock oscillator		Oscillation enabled	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Operable	
Timer P (TMP0)		Operable	
16-bit timers (TM00 to TM03)		Operable	
8-bit timers (TM50, TM51)		Operable	
Timer H (TMH0, TMH1)		Operable	
Watch timer		Operable when main clock output is selected as count clock	Operable
Watchdog timer 1		Operable	
Watchdog timer 2		Operable when main clock is selected as count clock	Operable
Serial interface	CSI00, CSI01	Operable	
	CSIA0, CSIA1	Operable	
	I^2C0	Operable	
	UART0 to UART2	Operable	
Key interrupt function		Operable	
A/D converter		Operable	
D/A converter		Operable when real-time output mode is selected	
Real-time output		Operable	
DMA		Operable	
Regulator		Operable	
Port function		Retains status before HALT mode was set.	
External bus interface		Refer to **2.2 Pin Status**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the HALT mode was set.	

23.4 IDLE Mode

23.4.1 Setting and operation status

The IDLE mode is set by clearing the PSMR.PSM bit to 0 and setting the PSC.STP bit to 1 in the normal operation mode.

In the IDLE mode, the clock oscillator continues operation but clock supply to the CPU and other on-chip peripheral functions stops.

As a result, program execution stops and the contents of the internal RAM before the IDLE mode was set are retained. The CPU and other on-chip peripheral functions stop operating. However, the on-chip peripheral functions that can operate with the subclock or an external clock continue operating.

Table 23-5 shows the operation status in the IDLE mode.

The IDLE mode can reduce the power consumption more than the HALT mode because it stops the operation of the on-chip peripheral functions. The main clock oscillator does not stop, so the normal operation mode can be restored without waiting for the oscillation stabilization time after the IDLE mode has been released, in the same manner as when the HALT mode is released.

Caution Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the IDLE mode.

23.4.2 Releasing IDLE mode

The IDLE mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT2 signal (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), unmasked internal interrupt request signal from the peripheral functions operable in the IDLE mode, or reset ($\overline{\text{RESET}}$ pin input, WDTRES2 signal (when the CPU is operating on the subclock)).

After the IDLE mode has been released, the normal operation mode is restored.

(1) Releasing IDLE mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal

The IDLE mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the IDLE mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is processed as follows.

(a) If an interrupt request signal with a priority lower than that of the interrupt request currently being serviced is issued, only the IDLE mode is released, and that interrupt request signal is not acknowledged. The interrupt request signal itself is retained.

(b) If an interrupt request signal with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request signal), the IDLE mode is released and that interrupt request signal is acknowledged.

Table 23-4. Operation After Releasing IDLE Mode by Interrupt Request Signal

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request signal	Execution branches to the handler address	
Maskable interrupt request signal	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

Caution The interrupt request signal that is disabled by setting the PSC.NMI2M, PSC.NMI0M, and PSC.INTM bits to 1 (interrupt disabled) becomes invalid and the IDLE mode is not released.

(2) Releasing IDLE mode by reset

The same operation as the normal reset operation is performed.

Table 23-5. Operation Status in IDLE Mode

Setting of IDLE Mode / Item		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
Main clock oscillator		Oscillation enabled	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Stops operation	
Timer P (TMP0)		Stops operation	
16-bit timers (TM00 to TM03)		TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock and f_{BRG} is selected as count clock of WT	TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock
8-bit timers (TM50, TM51)		• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock and TM01 is enabled in IDLE mode	
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Stops operation	Operable when f_{XT} is selected as count clock
Watch timer		Operable when main clock is selected as count clock	Operable
Watchdog timer 1		Stops operation	
Watchdog timer 2		Stops operation	Operable when f_{XT} is selected as count clock
Serial interface	CSI00, CSI01	Operable when $\overline{SCK0m}$ input clock is selected as operation clock	
	CSIA0, CSIA1	Stops operation	
	I^2C0	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART1, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation[Note]	
D/A converter		Operable However, the DACSn register cannot be updated because the CPU is stopped.	
Regulator		Operation continues	
Real-time output		Operable when INTTM5m is selected as real-time output trigger and TM5m is enabled in IDLE mode. However, the RTBH0 and RTBL0 registers cannot be updated because the CPU is stopped.	
DMA		Stops operation	
Regulator		Operation continues	
Port function		Retains status before IDLE mode was set.	
External bus interface		Refer to **2.2 Pin Status**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the IDLE mode was set.	

Note By setting the ADM.ADCS and ADM.ADCS2 bits to 00B before the IDLE mode is set, power consumption can be reduced.

Remark m = 0, 1

23.5 STOP Mode

23.5.1 Setting and operation status

The STOP mode is set when the PSMR.PSM bit is set to 1 and the PSC.STP bit is set to 1 in the normal operation mode.

In the STOP mode, the subclock oscillator continues operating but the main clock oscillator stops. Clock supply to the CPU and the on-chip peripheral functions is stopped.

As a result, program execution is stopped, and the contents of the internal RAM before the STOP mode was set are retained. The on-chip peripheral functions that operate with the clock oscillated by the subclock oscillator or an external clock continue operating.

Table 23-7 shows the operation status in the STOP mode.

Because the STOP stops operation of the main clock oscillator, it reduces the power consumption to a level lower than the IDLE mode. If the subclock oscillator and external clock are not used, the power consumption can be minimized with only leakage current flowing.

Caution Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the STOP mode.

23.5.2 Releasing STOP mode

The STOP mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT2 signal (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), unmasked internal interrupt request signal from the peripheral functions operable in the STOP mode, or reset ($\overline{\text{RESET}}$ pin input, WDTRES2 signal (when the CPU is operating on the subclock)).

After the STOP mode has been released, the normal operation mode is restored after the oscillation stabilization time has been secured.

(1) Releasing STOP mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal

The STOP mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the software STOP mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

(a) If an interrupt request signal with a priority lower than that of the interrupt request currently being serviced is issued, only the STOP mode is released, and that interrupt request signal is not acknowledged. The interrupt request signal itself is retained.

(b) If an interrupt request signal with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request signal), the STOP mode is released and that interrupt request signal is acknowledged.

Table 23-6. Operation After Releasing STOP Mode by Interrupt Request Signal

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request signal	Execution branches to the handler address	
Maskable interrupt request signal	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

Caution The interrupt request signal that is disabled by setting the PSC.NMI2M, PSC.NMI0M, and PSC.INTM bits to 1 (interrupt disabled) becomes invalid and the STOP mode is not released.

(2) Releasing STOP mode by reset

The same operation as the normal reset operation is performed.

Table 23-7. Operation Status in STOP Mode

Setting of STOP Mode / Item		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
Main clock oscillator		Oscillation stops	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Stops operation	
Timer P (TMP0)		Stops operation	
16-bit timers (TM00 to TM03)		Stops operation	TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock and f_{XT} is selected as count clock of WT
8-bit timers (TM50, TM51)		Operable when TI5m is selected as count clock	Operable when TI5m is selected as count clock or when INTTM010 is selected as count clock and TM01 is enabled in STOP mode
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Stops operation	Operable when f_{XT} is selected as count clock
Watch timer		Stops operation	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Stops operation	
Watchdog timer 2		Stops operation	Operable when f_{XT} is selected as count clock
Serial interface	CSI00, CSI01	Operable when $\overline{SCK0m}$ input clock is selected as operation clock	
	CSIA0, CSIA1	Stops operation	
	I^2C0	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART1, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation[Note]	
D/A converter		Operable However, the DACSm register cannot be updated because the CPU is stopped.	
Real-time output		Operable when INTTM5m is selected as real-time output trigger and TM5m is enabled in STOP mode. However, the RTBH0 and RTBL0 registers cannot be updated because the CPU is stopped.	
DMA		Stops operation	
Regulator		Stops operation	
Port function		Retains status before STOP mode was set.	
External bus interface		Refer to **2.2 Pin Status**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the STOP mode was set.	

Note By setting the ADM.ADCS and ADM.ADCS2 bits to 00B before the STOP mode is set, power consumption can be reduced.

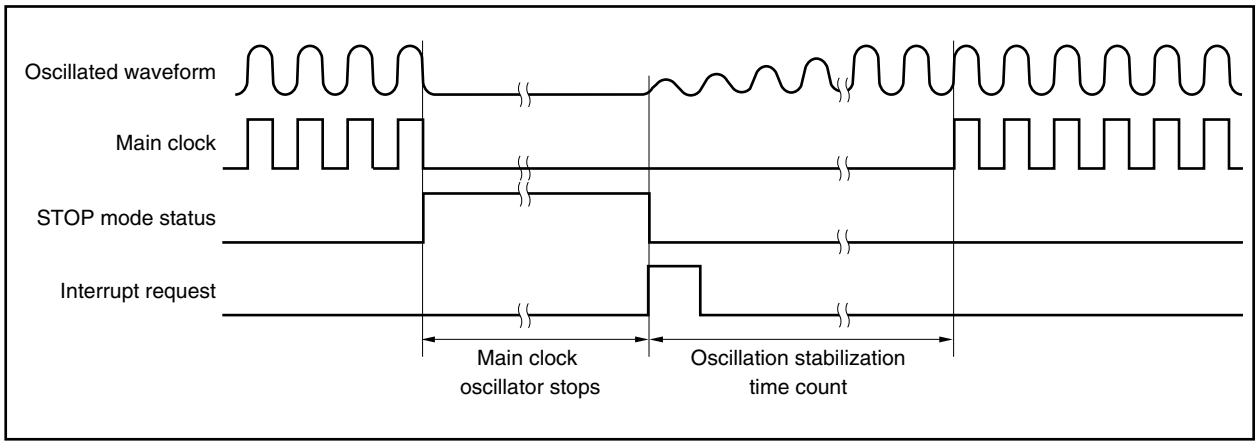
Remark m = 0, 1

23.5.3 Securing oscillation stabilization time when STOP mode is released

When the STOP mode is released, only the oscillation stabilization time set by the OSTS register elapses. If the STOP mode has been released by reset, however, the reset value of the OSTS register, 2^{15}/fx (8.192 ms at fx = 4 MHz) elapses.

The operation performed when the STOP mode is released by an interrupt request signal is shown below.

Figure 23-2. Oscillation Stabilization Time



Caution For details of the OSTS register, refer to 23.2 (3) Oscillation stabilization time selection register (OSTS).

23.6 Subclock Operation Mode

23.6.1 Setting and operation status

The subclock operation mode is set when the PCC.CK3 bit is set to 1 in the normal operation mode.

When the subclock operation mode is set, the internal system clock is changed from the main clock to the subclock.

When the PCC.MCK bit is set to 1, the operation of the main clock oscillator is stopped. As a result, the system operates only with the subclock.

Table 23-8 shows the operation status in subclock operation mode.

In the subclock operation mode, the power consumption can be reduced to a level lower than in the normal operation mode because the subclock is used as the internal system clock. In addition, the power consumption can be further reduced to the level of the STOP mode by stopping the operation of the main clock oscillator.

Cautions 1. When manipulating the CK3 bit, do not change the set values of the PCC.CK2 to PCC.CK0 bits (using a bit manipulation instruction to manipulate the bit is recommended). For details, refer to 6.3 (1) Processor clock control register (PCC).

2. If the following conditions are not satisfied, change the CK2 to CK0 bits so that the conditions are satisfied and set the subclock operation mode.

Internal system clock (f_{CLK}) > Subclock (f_{XT}: 32.768 kHz) × 4

Remark Internal system clock (f_{CLK}): Clock generated from the main clock (f_{XX}) by setting bits CK2 to CK0

23.6.2 Releasing subclock operation mode

The subclock operation mode is released when the CK3 bit is cleared to 0 or by reset ($\overline{\text{RESET}}$ pin input, WDTRES1, WDTRES2 signal). If the main clock is stopped (MCK bit = 1), set the MCK bit to 1, secure the oscillation stabilization time of the main clock by software, and clear the CK3 bit to 0.

The normal operation mode is restored when the subclock operation mode is released.

Caution When manipulating the CK3 bit, do not change the set values of the CK2 to CK0 bits (using a bit manipulation instruction to manipulate the bit is recommended). For details, refer to 6.3 (1) Processor clock control register (PCC).

Table 23-8. Operation Status in Subclock Operation Mode

Item \ Setting of Subclock Operation Mode		Operation Status	
		When Main Clock Is Oscillating	When Main Clock Is Stopped
CPU		Operable	
Subclock oscillator		Oscillation enabled	
Interrupt controller		Operable	
Timer P (TMP0)		Operable	Stops operation
16-bit timers (TM00 to TM03)		Operable	TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock and f_{XT} is selected as count clock of WT
8-bit timers (TM50, TM51)		Operable	• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock and when TM01 is enabled in subclock operation mode
Timer H (TMH0)		Operable	Stops operation
Timer H (TMH1)		Operable	Operable when f_{XT} is selected as count clock
Watch timer		Operable	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Stops operation	
Watchdog timer 2		Operable	Operable when f_{XT} is selected as count clock
Serial interface	CSI00, CSI01	Operable	Operable when $\overline{SCK0m}$ input clock is selected as operation clock
	CSIA0, CSIA1	Operable	Stops operation
	I^2C0	Operable	Stops operation
	UART0	Operable	Operable when ASCK0 is selected as count clock
	UART1, UART2	Operable	Stops operation
Key interrupt function		Operable	
A/D converter		Operable	Stops operation
D/A converter		Operable	
Real-time output		Operable	Operable when INTTM5m is selected as real-time output trigger and TI5m is selected as count clock of TM5m
DMA		Operable	
Regulator		Operation continues	
Port function		Settable	
External bus interface		Operable	
Internal data		Settable	

Remark m = 0, 1

23.7 Sub-IDLE Mode

23.7.1 Setting and operation status

The sub-IDLE mode is set when the PSMR.PSM bit is cleared to 0 and the PSC.STP bit is set to 1 in the subclock operation mode.

In this mode, the clock oscillator continues operation but clock supply to the CPU and the other on-chip peripheral functions is stopped.

As a result, program execution is stopped and the contents of the internal RAM before the sub-IDLE mode was set are retained. The CPU and the other on-chip peripheral functions are stopped. However, the on-chip peripheral functions that can operate with the subclock or an external clock continue operating.

Table 23-10 shows the operation status in the sub-IDLE mode.

Because the sub-IDLE mode stops operation of the CPU and other on-chip peripheral functions, it can reduce the power consumption more than the subclock operation mode. If the sub-IDLE mode is set after the main clock has been stopped, the power consumption can be reduced to a level as low as that in the STOP mode.

Caution Following the store instruction to set the PSC register to the sub-IDLE mode, insert five or more NOP instructions.

23.7.2 Releasing sub-IDLE mode

The sub-IDLE mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT2 signal (when the CPU is operating on the subclock)), unmasked external interrupt request signal (INTP0 to INTP7 pin input), unmasked internal interrupt request signal from the peripheral functions operable in the sub-IDLE mode, or reset ($\overline{\text{RESET}}$ pin input, WDTRES2 signal (when the CPU is operating on the subclock)).

When the sub-IDLE mode is released by an interrupt request signal, the subclock operation mode is set. If it is released by reset, the normal operation mode is restored.

(1) Releasing sub-IDLE mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal

The sub-IDLE mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the sub-IDLE mode is set in an interrupt servicing routine, however, an interrupt request signal that is issued later is serviced as follows.

(a) If an interrupt request signal with a priority lower than that of the interrupt request currently being serviced is issued, only the sub-IDLE mode is released, and that interrupt request signal is not acknowledged. The interrupt request signal itself is retained.

(b) If an interrupt request signal with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request signal), the sub-IDLE mode is released and that interrupt request signal is acknowledged.

Table 23-9. Operation After Releasing Sub-IDLE Mode by Interrupt Request Signal

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request signal	Execution branches to the handler address	
Maskable interrupt request signal	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

Caution The interrupt request signal that is disabled by setting the PSC.NMI2M, PSC.NMI0M, and PSC.INTM bits to 1 (interrupt disabled) becomes invalid and the sub-IDLE mode is not released.

(2) Releasing sub-IDLE mode by reset

The same operation as the normal reset operation is performed.

Table 23-10. Operation Status in Sub-IDLE Mode

Item \ Setting of Sub-IDLE Mode		Operation Status	
		When Main Clock Is Oscillating	When Main Clock Is Stopped
CPU		Stops operation	
Subclock oscillator		Oscillation enabled	
Interrupt controller		Stops operation	
Timer P (TMP0)		Stops operation	
16-bit timers (TM00 to TM03)		TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock	TM00, TM02, TM03: Stop operation TM01: Operable when INTWT is selected as count clock and f_{XT} is selected as count clock of WT
8-bit timers (TM50, TM51)		• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock and when TM01 is enabled in sub-IDLE mode	
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Operable when f_{XT} is selected as count clock	
Watch timer		Operable	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Stops operation	
Watchdog timer 2		Operable when f_{XT} is selected as count clock	
Serial interface	CSI00, CSI01	Operable when $\overline{SCK0m}$ input clock is selected as operation clock	
	CSIA0, CSIA1	Stops operation	
	I^2C0	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART1, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation[Note]	
D/A converter		Operable However, the DACSm register cannot be updated because the CPU is stopped.	
Real-time output		Operable when INTTM5m is selected as real-time output trigger and TM5m is set to the operable conditions of the sub-IDLE mode	
DMA		Stops operation	
Regulator		Stops operation	
Port function		Retains status before sub-IDLE mode was set.	
External bus interface		Refer to **2.2 Pin Status**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the sub-IDLE mode was set.	

Note By setting the ADM.ADCS and ADM.ADCS2 bits to 00B before the sub-IDLE mode is set, power consumption can be reduced.

Remark m = 0, 1

CHAPTER 24 RESET FUNCTION

24.1 Overview

The following reset functions are available.

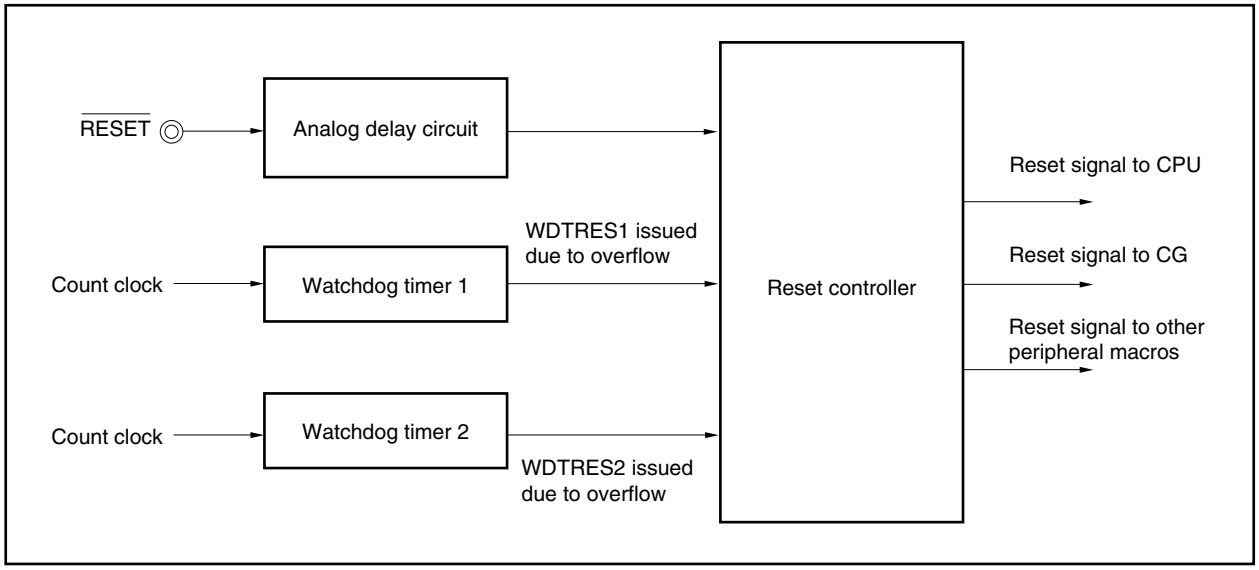
- Reset function by $\overline{\text{RESET}}$ pin input
- Reset function by overflow of watchdog timer 1 (WDTRES1)
- Reset function by overflow of watchdog timer 2 (WDTRES2)

If the $\overline{\text{RESET}}$ pin goes high, the reset status is released, and the CPU starts executing the program. Initialize the contents of each register in the program as necessary.

The $\overline{\text{RESET}}$ pin has a noise eliminator that operates by analog delay to prevent malfunction caused by noise.

24.2 Configuration

Figure 24-1. Reset Block Diagram



24.3 Operation

The system is reset, initializing each hardware unit, when a low level is input to the $\overline{\text{RESET}}$ pin or if watchdog timer 1 or watchdog timer 2 overflows (WDTRES1 or WDTRES2).

While a low level is being input to the $\overline{\text{RESET}}$ pin, the main clock oscillator stops. Therefore, the overall power consumption of the system can be reduced.

If the $\overline{\text{RESET}}$ pin goes high or if the WDTRES1 or WDTRES2 signal is received, the reset status is released.

If the reset status is released by $\overline{\text{RESET}}$ pin input or the WDTRES2 signal, the oscillation stabilization time elapses (reset value of OSTS register: $2^{15}/f_{XX}$) and then the CPU starts program execution.

If the reset status is released by the WDTRES1 signal, the oscillation stabilization time is not inserted because the main system clock oscillator does not stop.

Table 24-1. Hardware Status on $\overline{\text{RESET}}$ Pin Input or Occurrence of WDTRES2 Signal

Item	During Reset	After Reset
Main clock oscillator (f_X)	Oscillation stops	Oscillation starts
Subclock oscillator (f_{XT})	Oscillation continues	
Peripheral clock (f_{XX} to $f_{XX}/1024$)	Operation stops	Operation starts after securing oscillation stabilization time
Internal system clock (f_{CLK})	Operation stops	Operation starts after securing oscillation stabilization time (initialized to $f_{XX}/8$)
CPU clock (f_{CPU})	Operation stops	Operation starts after securing oscillation stabilization time (initialized to $f_{XX}/8$)
Watchdog timer 1 clock (f_{XW})	Operation stops	Operation starts
CPU	Initialized	Program execution starts after securing oscillation stabilization time
Internal RAM	Undefined if power-on reset or writing data to RAM (by CPU or DMA) and reset input conflict (data is damaged). Otherwise value immediately before reset input is retained.	
I/O lines	High impedance	
On-chip peripheral I/O registers	Initialized to specified status	
Watchdog timer 2	Operation stops	Operation starts after securing oscillation stabilization time
Other on-chip peripheral functions	Operation stops	Operation can be started after securing oscillation stabilization time

Table 24-2. Hardware Status on Occurrence of WDTRES1 Signal

Item	During Reset	After Reset
Main clock oscillator (f_X)	Oscillation continues	
Subclock oscillator (f_{XT})	Oscillation continues	
Peripheral clock (f_{XX} to $f_{XX}/1024$)	Operation stops	Operation starts
Internal system clock (f_{CLK})	Oscillation continues (initialized to $f_{XX}/8$)	
CPU clock (f_{CPU})	Oscillation continues (initialized to $f_{XX}/8$)	
Watchdog timer 1 clock (f_{XW})	Operation continues	
Internal RAM	Undefined if writing data to RAM (by CPU or DMA) and reset input conflict (data is damaged). Otherwise value immediately before reset input is retained.	
I/O lines	High impedance	
On-chip peripheral I/O registers	Initialized to specified status	
Watchdog timer 2	Operation stops	Operation starts
Other on-chip peripheral functions	Operation stops	Operation can be started

Figure 24-2. Hardware Status on $\overline{\text{RESET}}$ Input

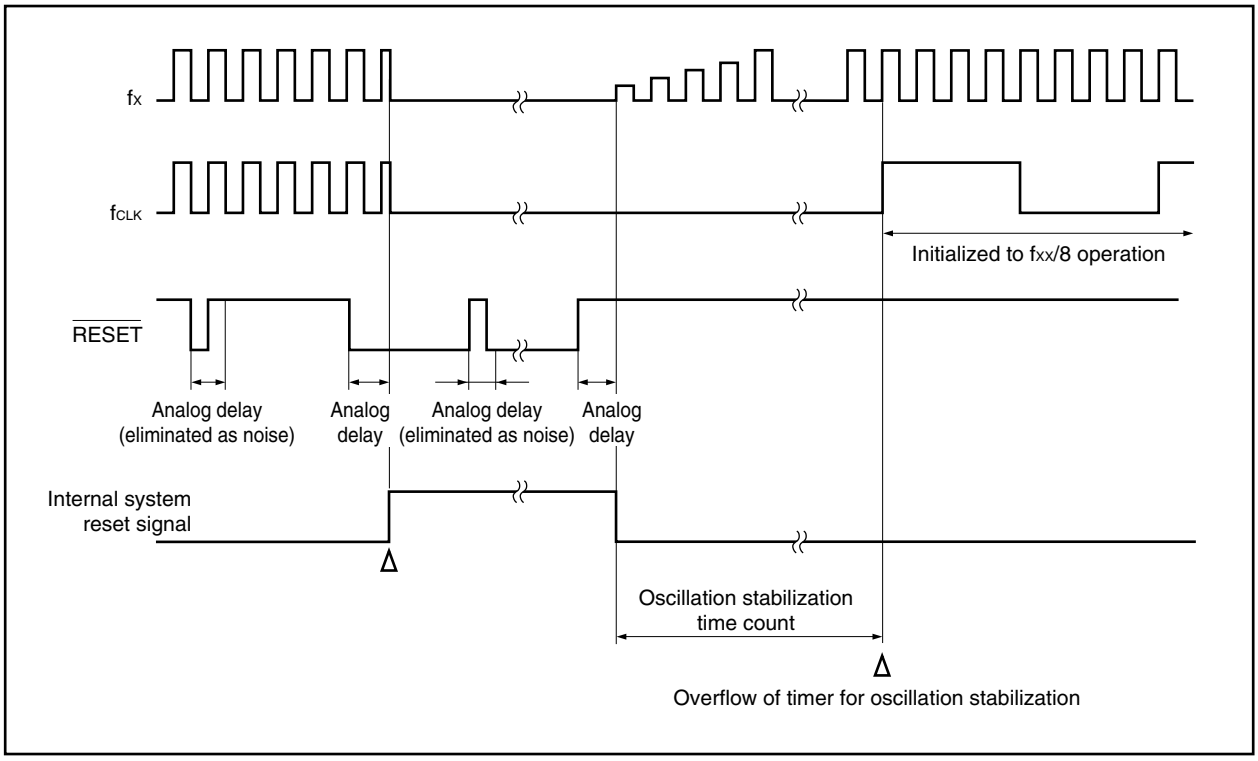


Figure 24-3. Operation on Power Application

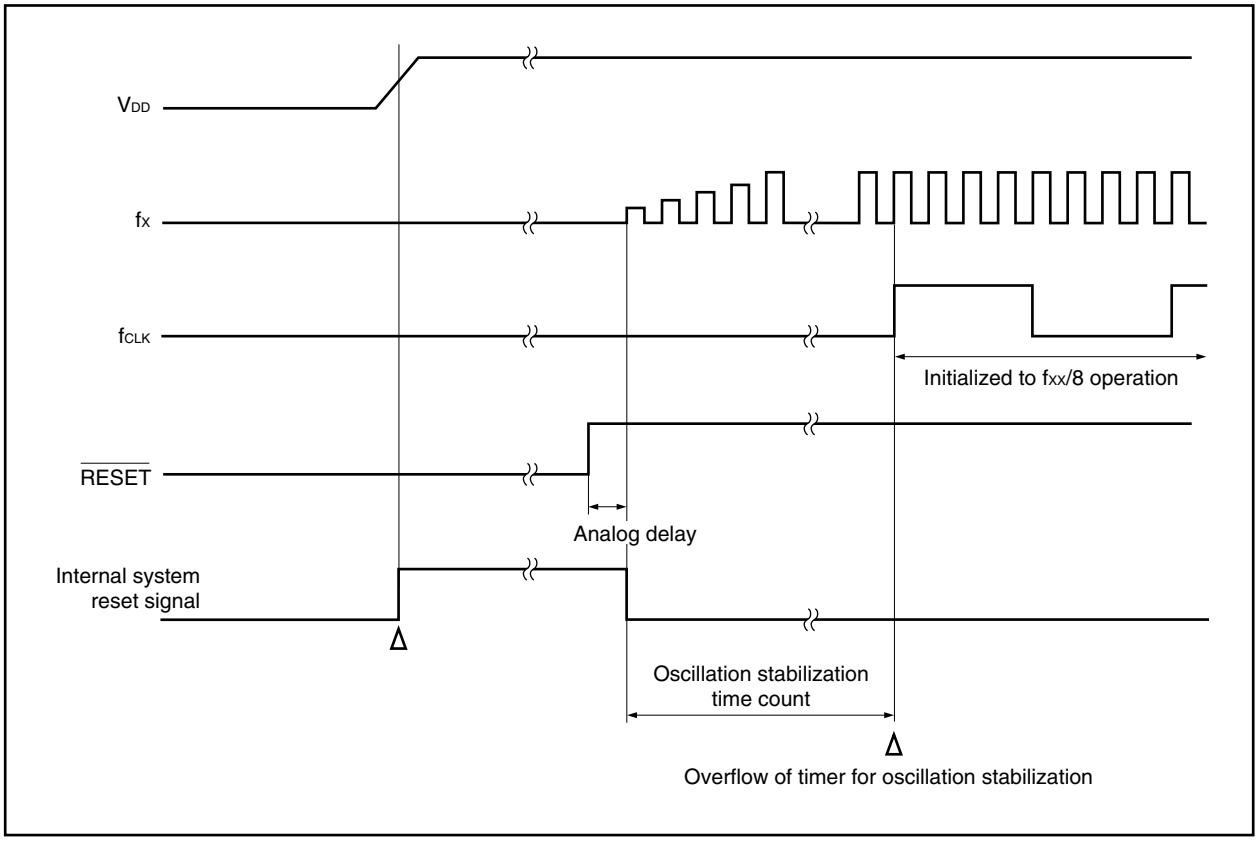


Figure 24-4. Timing of Reset Operation by Watchdog Timer 1

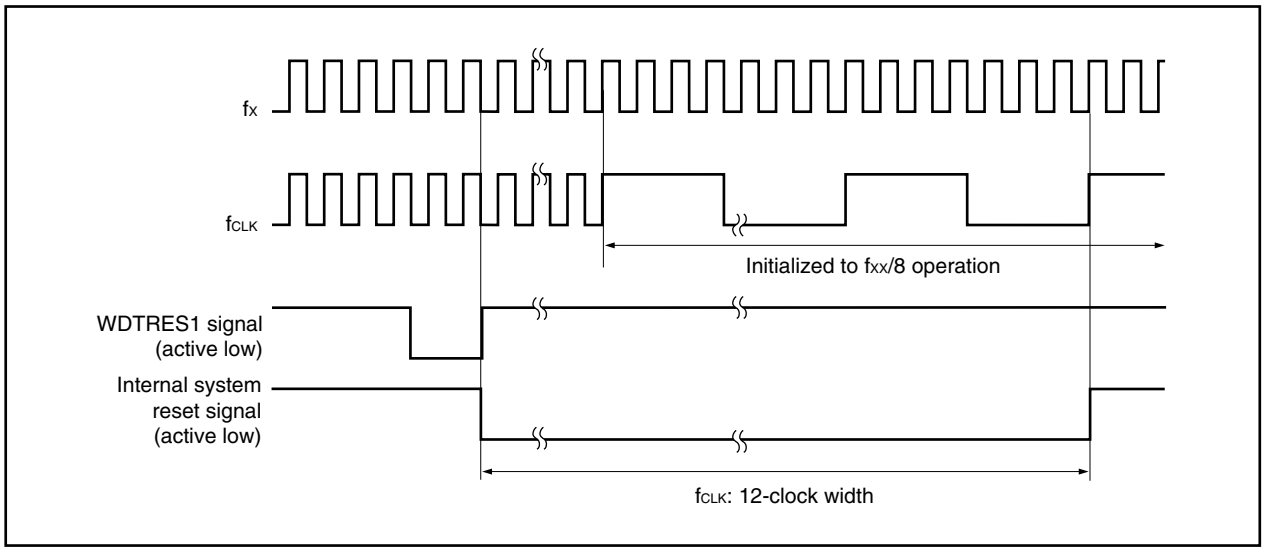
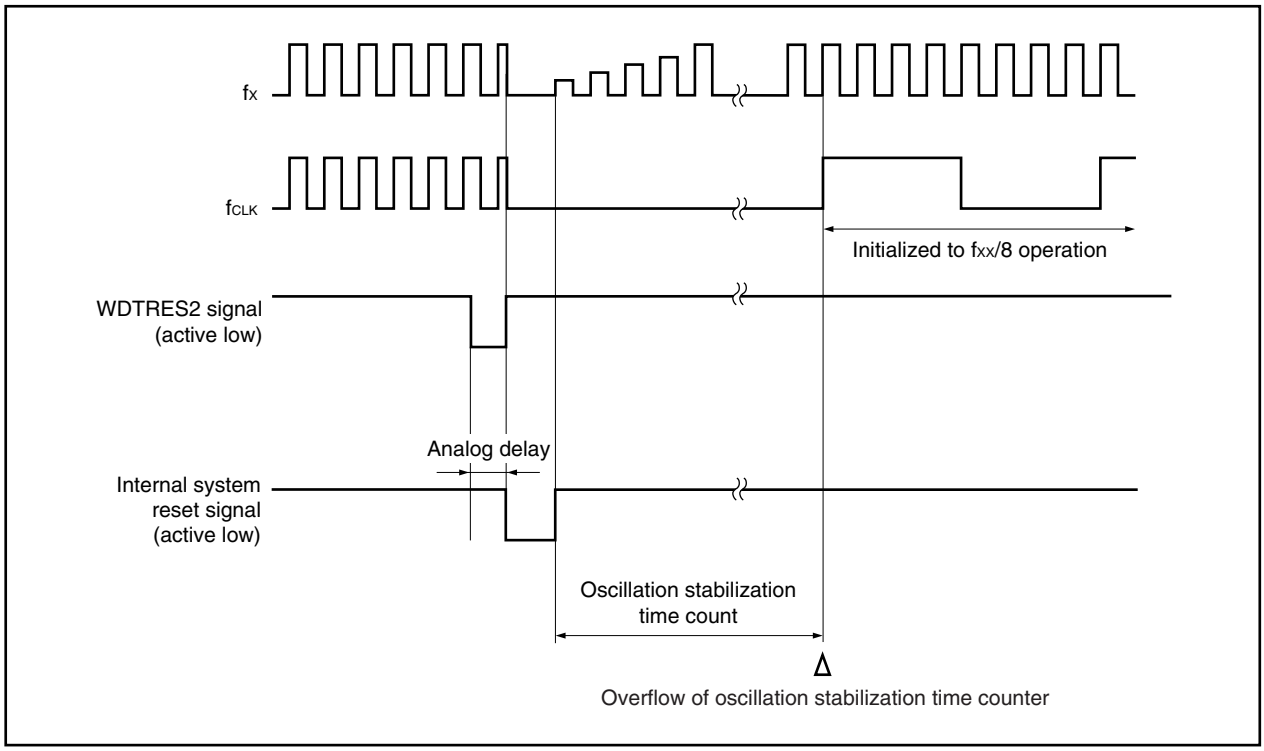


Figure 24-5. Timing of Reset Operation by Watchdog Timer 2



CHAPTER 25 REGULATOR

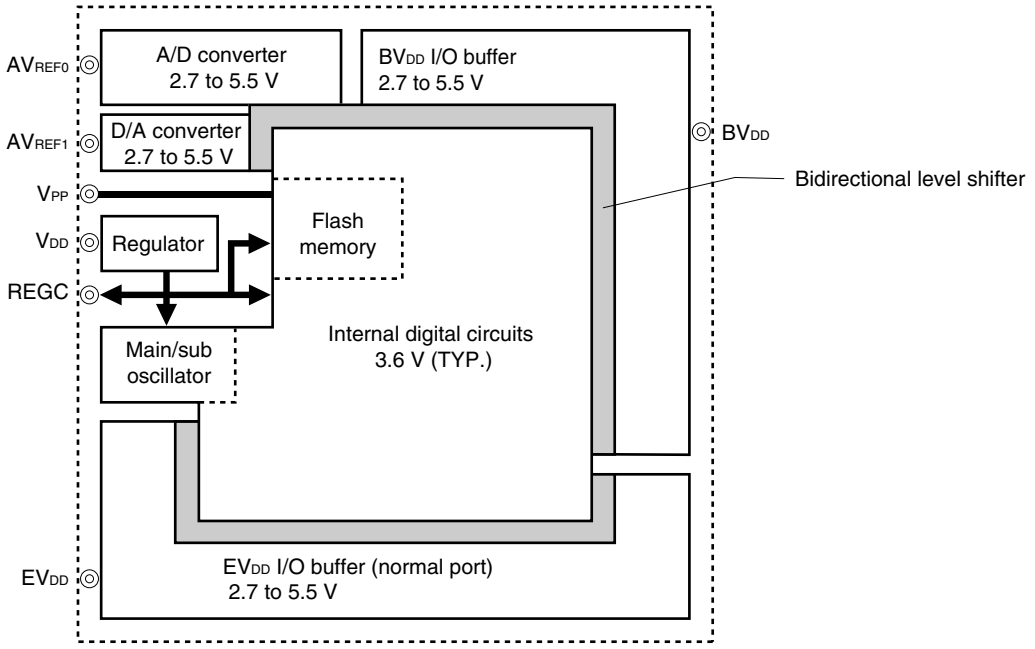
25.1 Overview

The V850ES/KG2 includes a regulator to reduce the power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits (except the A/D converter, D/A converter, and output buffer). The regulator output voltage is set to 3.6 V (TYP.).

Caution When using the regulator (REGC = 10 μF, the external clock cannot be input to the main clock oscillator or subclock oscillator.

Figure 25-1. Regulator



Caution Use the regulator with a setting of $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} \geq BV_{DD}$.

25.2 Operation

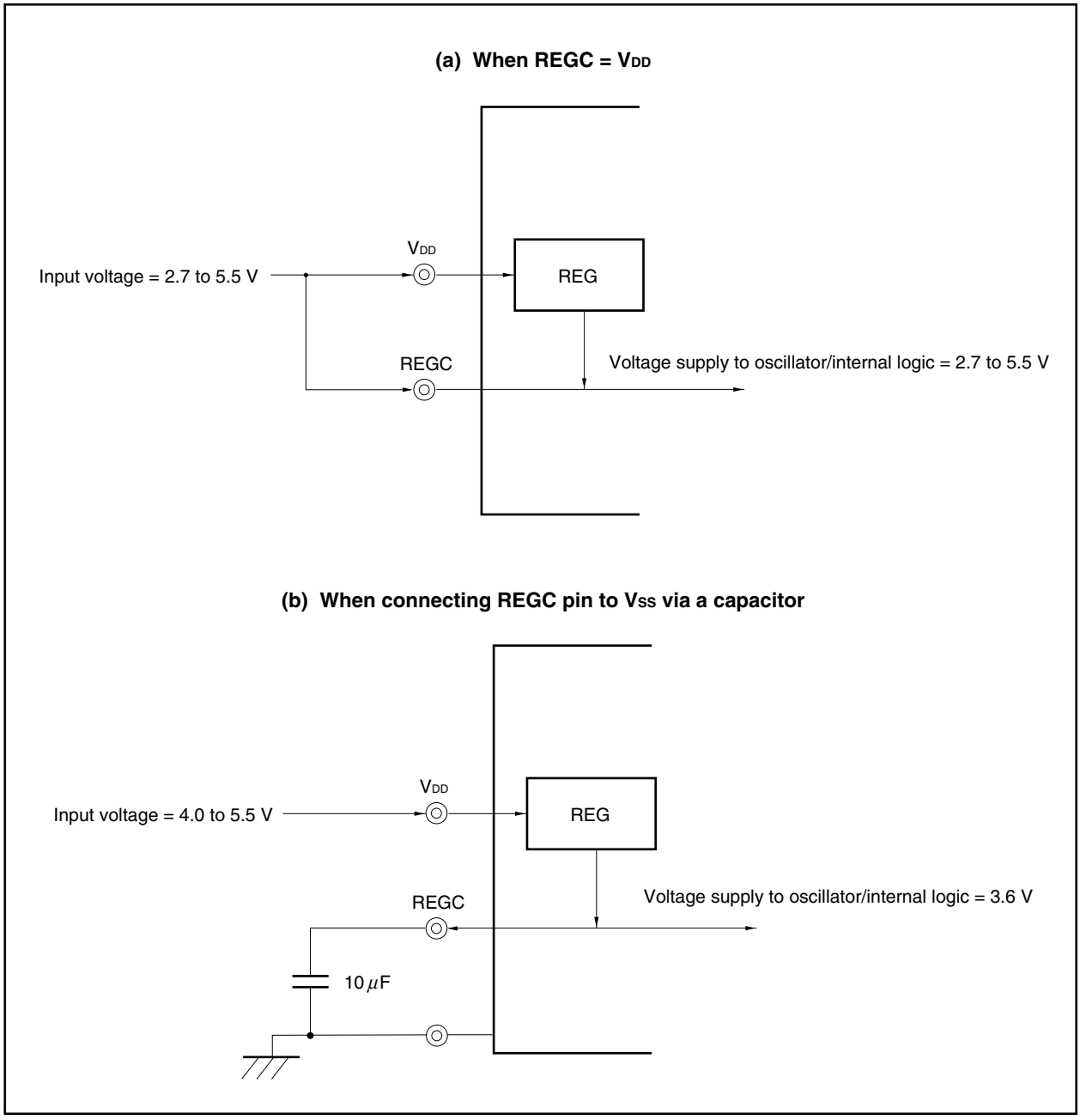
The regulator stops operating in the following modes and the supply voltage to the oscillator is V_{DD} (but only when REGC = 10 μF).

- During reset
- In STOP mode
- In sub-IDLE mode

When using the regulator, be sure to connect a capacitor (10 μF) to the REGC pin to stabilize the regulator output.

A diagram of the regulator pin connections is shown below.

Figure 25-2. REGC Pin Connection



CHAPTER 26 FLASH MEMORY

Caution For the electrical specifications related to the flash memory rewriting, refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS (TARGET).

Flash memory versions are commonly used in the following development environments and mass production applications.

- For altering software after the V850ES/KG2 is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

26.1 Features

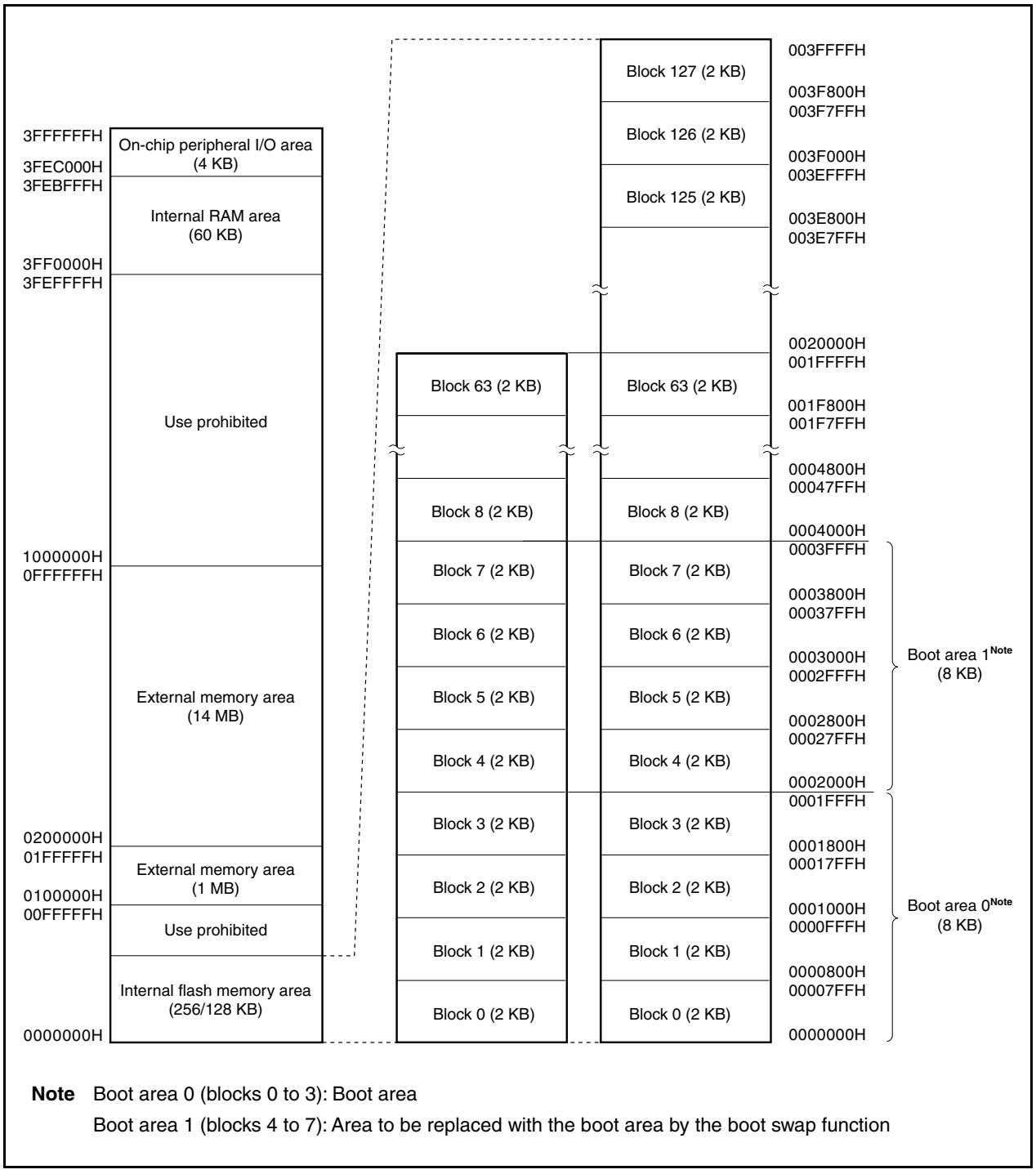
- 4-byte/1-clock access (when instruction is fetched)
- Capacity: 256/128 KB
- Write voltage: Erase/write with a single power supply
- Rewriting method
  - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

26.2 Memory Configuration

The 256/128 KB internal flash memory area is divided into 128/64 blocks and can be programmed/erased in block units. All the blocks can also be erased at once.

When the boot swap function is used, the physical memory (blocks 0 to 3) located at the addresses of boot area 0 is replaced by the physical memory (blocks 4 to 7) located at the addresses of boot area 1. For details of the boot swap function, refer to **26.5 Rewriting by Self Programming**.

Figure 26-1. Flash Memory Mapping



Note Boot area 0 (blocks 0 to 3): Boot area
Boot area 1 (blocks 4 to 7): Area to be replaced with the boot area by the boot swap function

26.3 Functional Outline

The internal flash memory of the V850ES/KG2 can be rewritten by using the rewrite function of the dedicated flash programmer, regardless of whether the V850ES/KG2 has already been mounted on the target system or not (on-board/off-board programming).

In addition, a security function that prohibits rewriting the user program written to the internal flash memory is also supported, so that the program cannot be changed by an unauthorized person.

The rewrite function using the user program (self programming) is ideal for an application where it is assumed that the program is changed after production/shipment of the target system. A boot swap function that rewrites the entire flash memory area safely is also supported. In addition, interrupt servicing is supported during self programming, so that the flash memory can be rewritten under various conditions, such as while communicating with an external device.

Table 26-1. Rewrite Method

Rewrite Method	Functional Outline	Operation Mode
On-board programming	Flash memory can be rewritten after the device is mounted on the target system, by using a dedicated flash programmer.	Flash memory programming mode
Off-board programming	Flash memory can be rewritten before the device is mounted on the target system, by using a dedicated flash programmer and a dedicated program adapter board (FA series).	
Self programming	Flash memory can be rewritten by executing a user program that has been written to the flash memory in advance by means of on-board/off-board programming. (During self-programming, instructions cannot be fetched from or data access cannot be made to the internal flash memory area. Therefore, the rewrite program must be transferred to the internal RAM or external memory in advance).	Normal operation mode

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Table 26-2. Basic Functions

Function	Functional Outline	Support (○: Supported, ×: Not supported)	
		On-Board/Off-Board Programming	Self Programming
Block erasure	The contents of specified memory blocks are erased.	○	○
Chip erasure	The contents of the entire memory area are erased all at once.	○	×
Write	Writing to specified addresses, and a verify check to see if write level is secured are performed.	○	○
Verify/checksum	Data read from the flash memory is compared with data transferred from the flash programmer.	○	× (Can be read by user program)
Blank check	The erasure status of the entire memory is checked.	○	○
Security setting	Use of the block erase command, chip erase command, and program command can be prohibited.	○	× (Supported only when setting is changed from enable to disable)

The following table lists the security functions. The block erase command prohibit, chip erase command prohibit, and program command prohibit functions are enabled by default after shipment, and security can be set by rewriting via on-board/off-board programming. Each security function can be used in combination with the others at the same time.

Table 26-3. Security Functions

Function	Function Outline	Rewriting Operation When Prohibited (○: Executable, ×: Not Executable)	
		On-Board/Off-Board Programming	Self Programming
Block erase command prohibit	Execution of a block erase command on all blocks is prohibited. Setting of prohibition can be initialized by execution of a chip erase command.	Block erase command: × Chip erase command: ○ Program command: ○	Can always be rewritten regardless of setting of prohibition
Chip erase command prohibit	Execution of block erase and chip erase commands on all the blocks is prohibited. Once prohibition is set, setting of prohibition cannot be initialized because the chip erase command cannot be executed.	Block erase command: × Chip erase command: × Program command: ○	
Program command prohibit	Write and block erase commands on all the blocks are prohibited. Setting of prohibition can be initialized by execution of the chip erase command.	Block erase command: × Chip erase command: ○ Program command: ×	

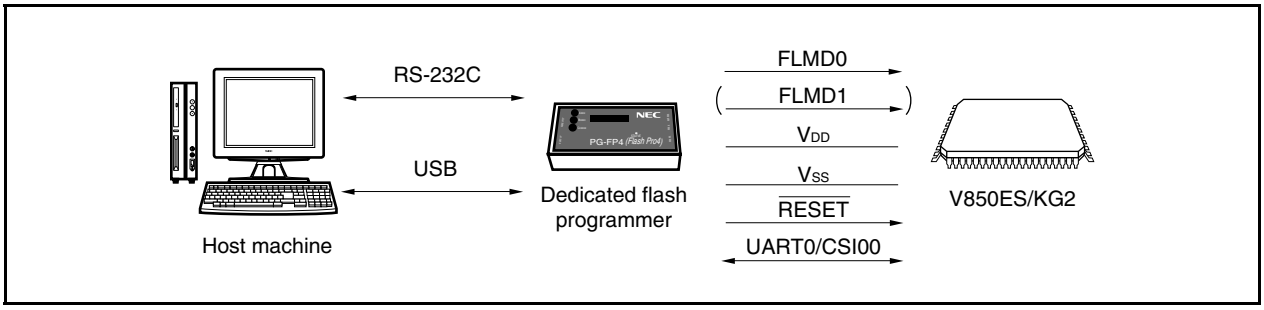
26.4 Rewriting by Dedicated Flash Programmer

The flash memory can be rewritten by using a dedicated flash programmer after the V850ES/KG2 is mounted on the target system (on-board programming). The flash memory can also be rewritten before the device is mounted on the target system (off-board programming) by using a dedicated program adapter (FA series).

26.4.1 Programming environment

The following shows the environment required for writing programs to the flash memory of the V850ES/KG2.

Figure 26-2. Environment Required for Writing Programs to Flash Memory



A host machine is required for controlling the dedicated flash programmer.

UART0 or CSI00 is used for the interface between the dedicated flash programmer and the V850ES/KG2 to perform writing, erasing, etc. A dedicated program adapter (FA series) is required for off-board writing.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

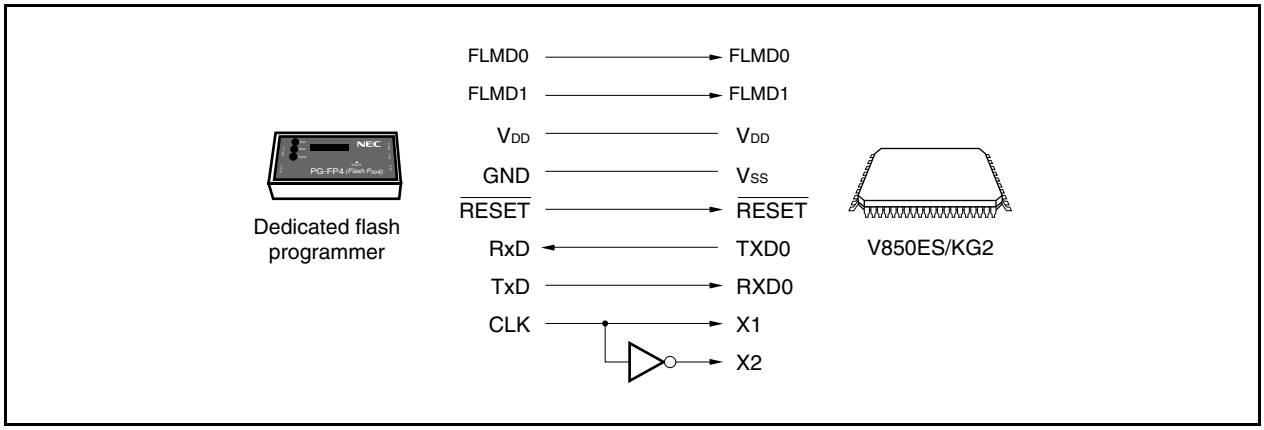
26.4.2 Communication mode

Communication between the dedicated flash programmer and the V850ES/KG2 is performed by serial communication using the UART0 or CSI00 interfaces of the V850ES/KG2.

(1) UART0

Transfer rate: 9,600 to 153,600 bps

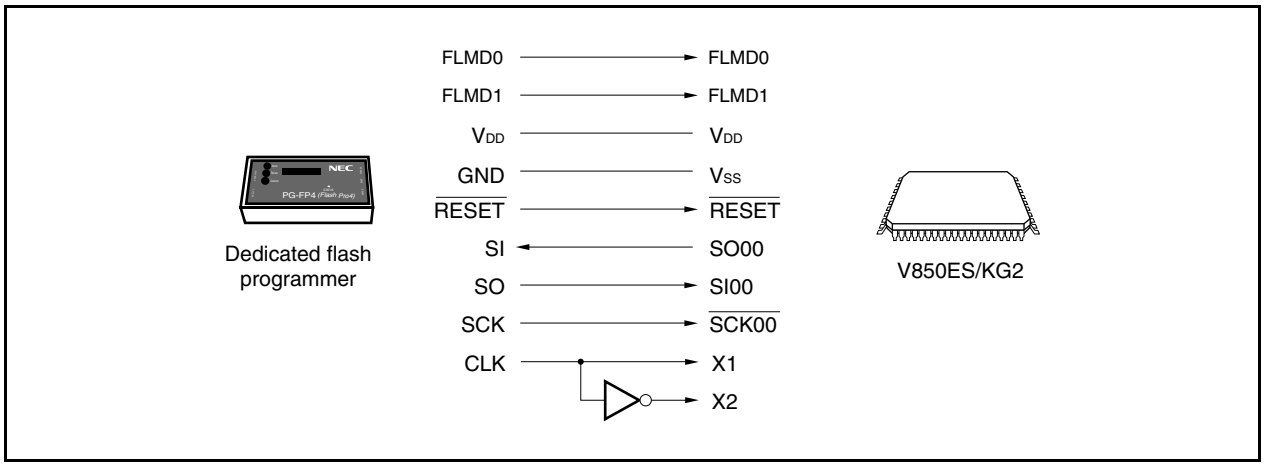
Figure 26-3. Communication with Dedicated Flash Programmer (UART0)



(2) CSI00

Serial clock: 2.4 kHz to 2.5 MHz (MSB first)

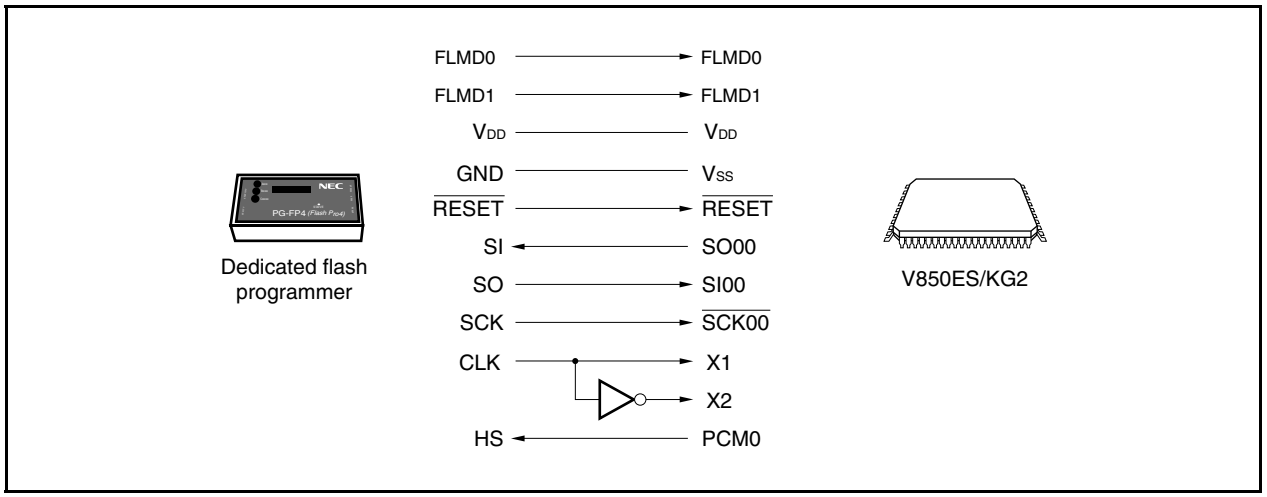
Figure 26-4. Communication with Dedicated Flash Programmer (CSI00)



(3) CSI00 + HS

Serial clock: 2.4 kHz to 2.5 MHz (MSB first)

Figure 26-5. Communication with Dedicated Flash Programmer (CSI00 + HS)



The dedicated flash programmer outputs the transfer clock, and the V850ES/KG2 operates as a slave.

When the PG-FP4 is used as the dedicated flash programmer, it generates the following signals to the V850ES/KG2. For details, refer to the **PG-FP4 User's Manual (U15260E)**.

Table 26-4. Signal Connections of Dedicated Flash Programmer (PG-FP4)

PG-FP4			V850ES/KG2	Processing for Connection		
Signal Name	I/O	Pin Function	Pin Name	UART0	CSI00	CSI00 + HS
FLMD0	Output	Write enable/disable	FLMD0	◎	◎	◎
FLMD1	Output	Write enable/disable	FLMD1	◎Note 1	◎Note 1	◎Note 1
VDD	–	V_{DD} voltage generation/voltage monitor	V_{DD}	◎	◎	◎
GND	–	Ground	V_{SS}	◎	◎	◎
CLK	Output	Clock output to V850ES/KG2	X1, X2	×Note 2	×Note 2	×Note 2
$\overline{\text{RESET}}$	Output	Reset signal	$\overline{\text{RESET}}$	◎	◎	◎
SI/RxD	Input	Receive signal	SO00	◎	◎	◎
SO/TxD	Output	Transmit signal	SI00	◎	◎	◎
SCK	Output	Transfer clock	$\overline{\text{SCK00}}$	×	◎	◎
HS	Input	Handshake signal for CSI00 + HS communication	PCM0	×	×	◎

Notes 1. Wire the pin as shown in Figure 26-6, or connect it to GND on board via a pull-down resistor.

2. Connect these pins to supply a clock from the PG-FP4 (wire as shown in Figure 26-6, or create an oscillator on board and supply the clock).

Remark ◎: Must be connected.

×: Does not have to be connected.

Table 26-5. Wiring Between V850ES/KG2 and PG-FP4

Pin Configuration of Flash Programmer (PG-FP4)			Pin Name on FA Board	With CSI00-HS			With CSI00			With UART0		
Signal Name	I/O	Pin Function		Pin Name	Pin No.		Pin Name	Pin No.		Pin Name	Pin No.	
					GC	GF		GC	GF		GC	GF
SI/RxD	Input	Receive signal	SI	P41/SO00/ TXD2	23	25	P41/SO00/ TXD2	23	25	P30/TXD0/ TO02	25	27
SO/TxD	Output	Transmit signal	SO	P40/SI00/ RXD2	22	24	P40/SI00/ RXD2	22	24	P31/RXD0/ INTP7/TO03	26	28
SCK	Output	Transfer clock	SCK	P42/$\overline{\text{SCK00}}$	24	26	P42/$\overline{\text{SCK00}}$	24	26	Not needed	Not needed	
CLK	Output	Clock to V850ES/KG2	X1	X1	12	14	X1	12	14	X1	12	14
			X2	X2[Note]	13	15	X2[Note]	13	15	X2[Note]	13	15
/RESET	Output	Reset signal	/RESET	$\overline{\text{RESET}}$	14	16	$\overline{\text{RESET}}$	14	16	$\overline{\text{RESET}}$	14	16
FLMD0	Input	Write voltage	FLMD0	FLMD0	8	10	FLMD0	8	10	FLMD0	8	10
FLMD1	Input	Write voltage	FLMD1	PDL5/AD5/ FLMD1	76	78	PDL5/AD5/ FLMD1	76	78	PDL5/AD5/ FLMD1	76	78
HS	Input	Handshake signal for CSI00 + HS communication	RESERVE/HS	PCM0/ $\overline{\text{WAIT}}$	61	63	Not needed	Not needed		Not needed	Not needed	
VDD	–	V_{DD} voltage generation/ voltage monitor	VDD	V_{DD}	9	11	V_{DD}	9	11	V_{DD}	9	11
				BV_{DD}	70	72	BV_{DD}	70	72	BV_{DD}	70	72
				EV_{DD}	34	36	EV_{DD}	34	36	EV_{DD}	34	36
				AV_{REF0}	1	3	AV_{REF0}	1	3	AV_{REF0}	1	3
				AV_{REF1}	5	7	AV_{REF1}	5	7	AV_{REF1}	5	7
GND	–	Ground	GND	V_{SS}	11	13	V_{SS}	11	13	V_{SS}	11	13
				AV_{SS}	2	4	AV_{SS}	2	4	AV_{SS}	2	4
				BV_{SS}	69	71	BV_{SS}	69	71	BV_{SS}	69	71
				EV_{SS}	33	35	EV_{SS}	33	35	EV_{SS}	33	35

Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Cautions 1. Be sure to connect the REGC pin in either of the following ways.

- **Connect to GND via a 10 μF capacitor**
- **Directly connect to V_{DD}**

2. When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.
Supply the clock by creating an oscillator on the board.

Remark GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
GF: 100-pin plastic QFP (14 × 20)

Figure 26-6. Wiring Example of V850ES/KG2 Flash Writing Adapter (FA-100GC-8EU-A) (1/2)

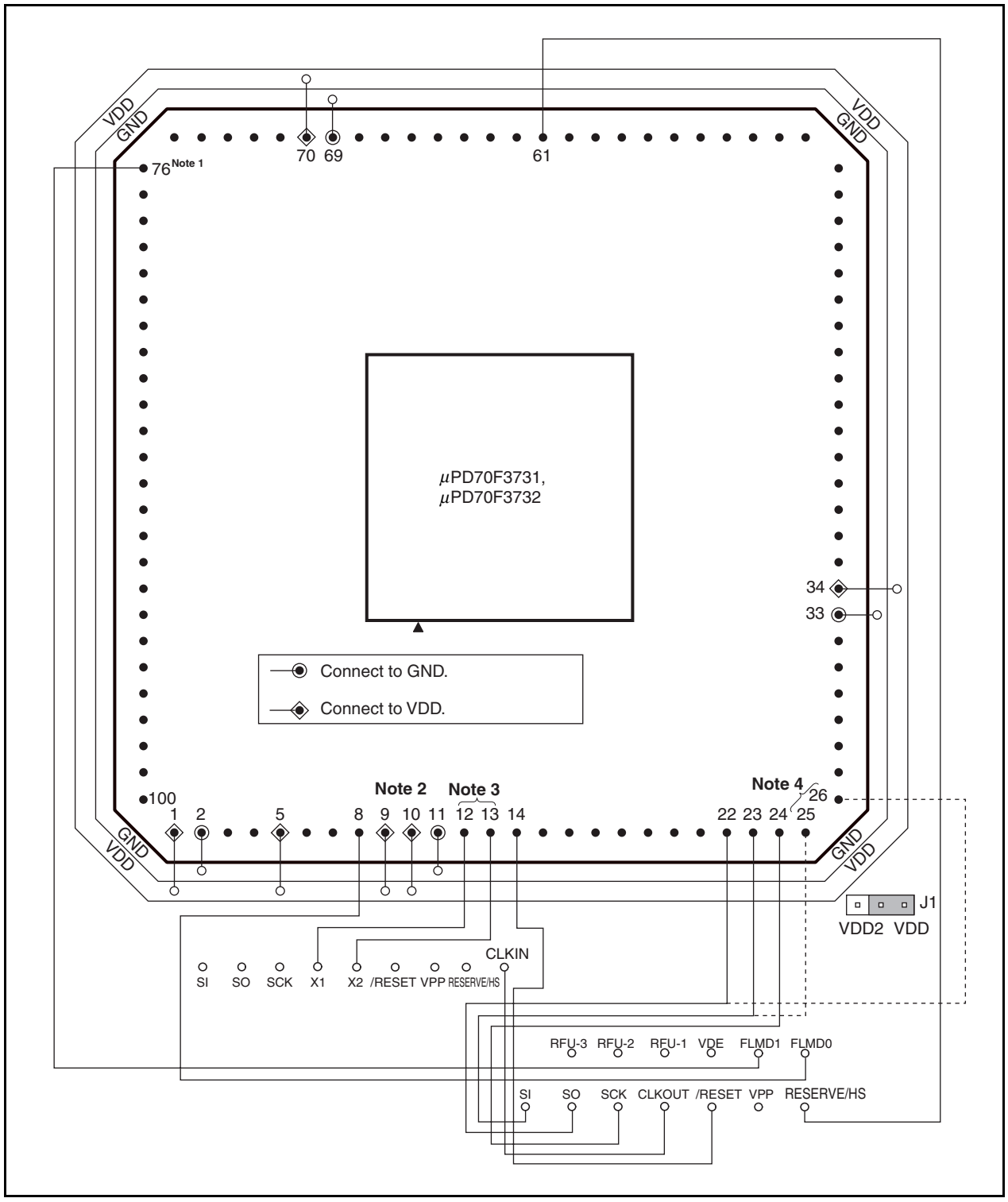


Figure 26-6. Wiring Example of V850ES/KG2 Flash Writing Adapter (FA-100GC-8EU-A) (2/2)

Notes 1. Wire the FLMD1 pin as shown in the figure, or connect it to GND on board via a pull-down resistor.

2. Be sure to connect the REGC pin in either of the following ways.

- Connect to GND via a 10 μF capacitor.
- Directly connect to V_{DD}.

When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.

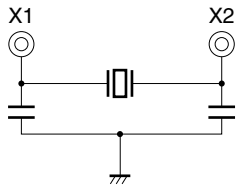
Supply the clock by creating an oscillator on the board.

3. The above figure shows an example of wiring when the clock is supplied from the PG-FP4.

Be sure to set and connect as follows when the clock is supplied from the PG-FP4.

- Set J1 of the flash adapter (FA) to the VDD side.
- Connect CLKOUT of FA to CLKIN of FA.
- Connect X1 of FA to X1 of the device.
- Connect X2 of FA to X2 of the device.

If an oscillator is created on the flash adapter and a clock is supplied, the above setting and connections will not necessary. The following shows a circuit example.



4. Corresponding pin when using UART0

Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.3 Pin I/O Circuits and Recommended Connection of Unused Pins).**

When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

2. This adapter is for a 100-pin plastic LQFP (fine pitch) package.

3. This diagram shows the wiring when using a handshake-supporting CSI.

Figure 26-7. Wiring Example of V850ES/KG2 Flash Writing Adapter (FA-100GC-3BA-A) (1/2)

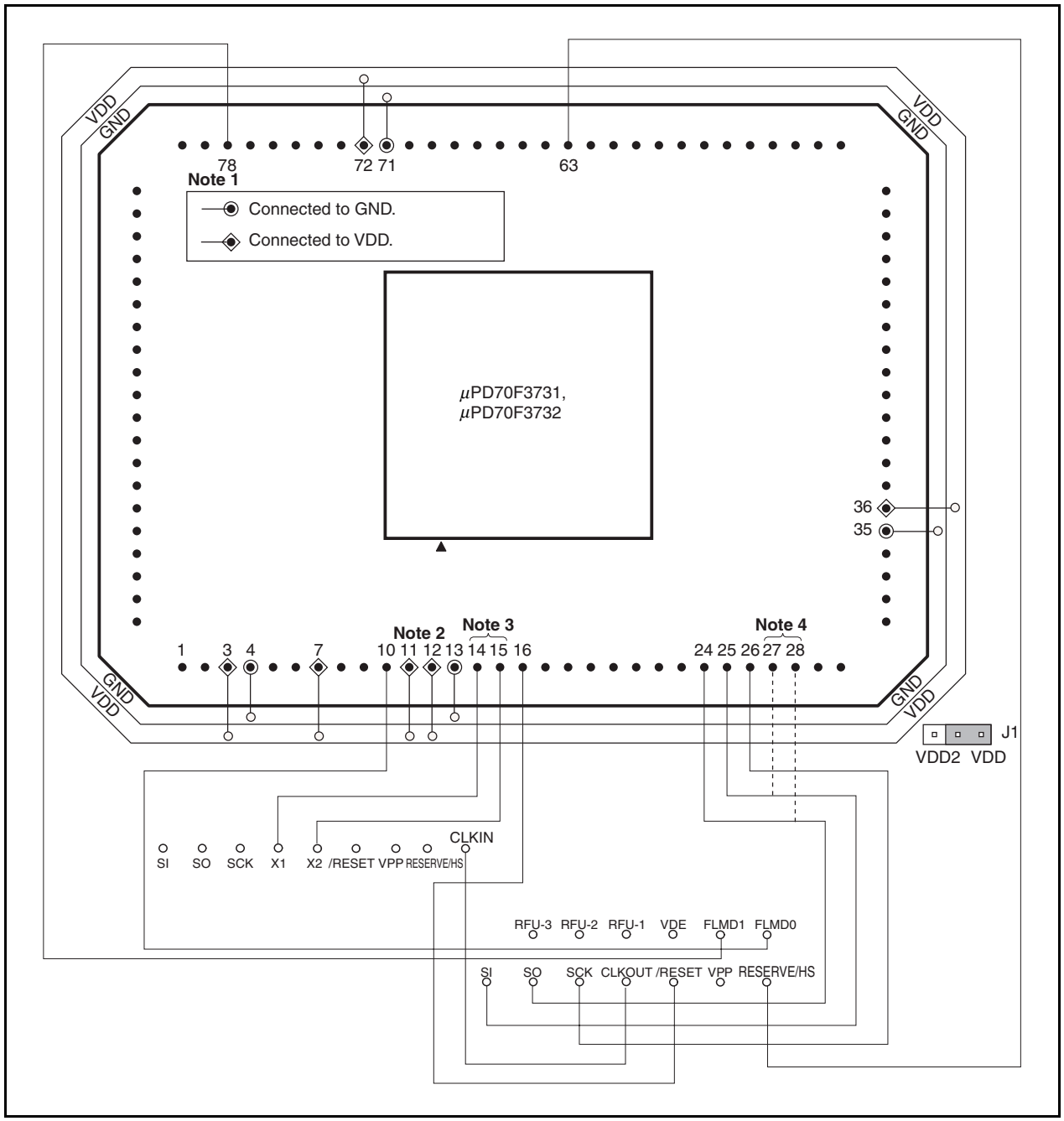


Figure 26-7. Wiring Example of V850ES/KG2 Flash Writing Adapter (FA-100GC-3BA-A) (2/2)

Notes 1. Wire the FLMD1 pin as shown in the figure, or connect it to GND on board via a pull-down resistor.

2. Be sure to connect the REGC pin in either of the following ways.

- Connect to GND via a 10 μF capacitor.
- Directly connect to V_{DD}.

When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.

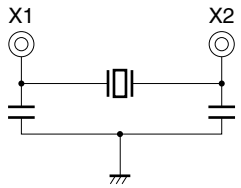
Supply the clock by creating an oscillator on the board.

3. The above figure shows an example of wiring when the clock is supplied from the PG-FP4.

Be sure to set and connect as follows when the clock is supplied from the PG-FP4.

- Set J1 of the flash adapter (FA) to the VDD side.
- Connect CLKOUT of FA to CLKIN of FA.
- Connect X1 of FA to X1 of the device.
- Connect X2 of FA to X2 of the device.

If an oscillator is created on the flash adapter and a clock is supplied, the above setting and connections will not necessary. The following shows a circuit example.



4. Corresponding pin when using UART0

Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.3 Pin I/O Circuits and Recommended Connection of Unused Pins).**

When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

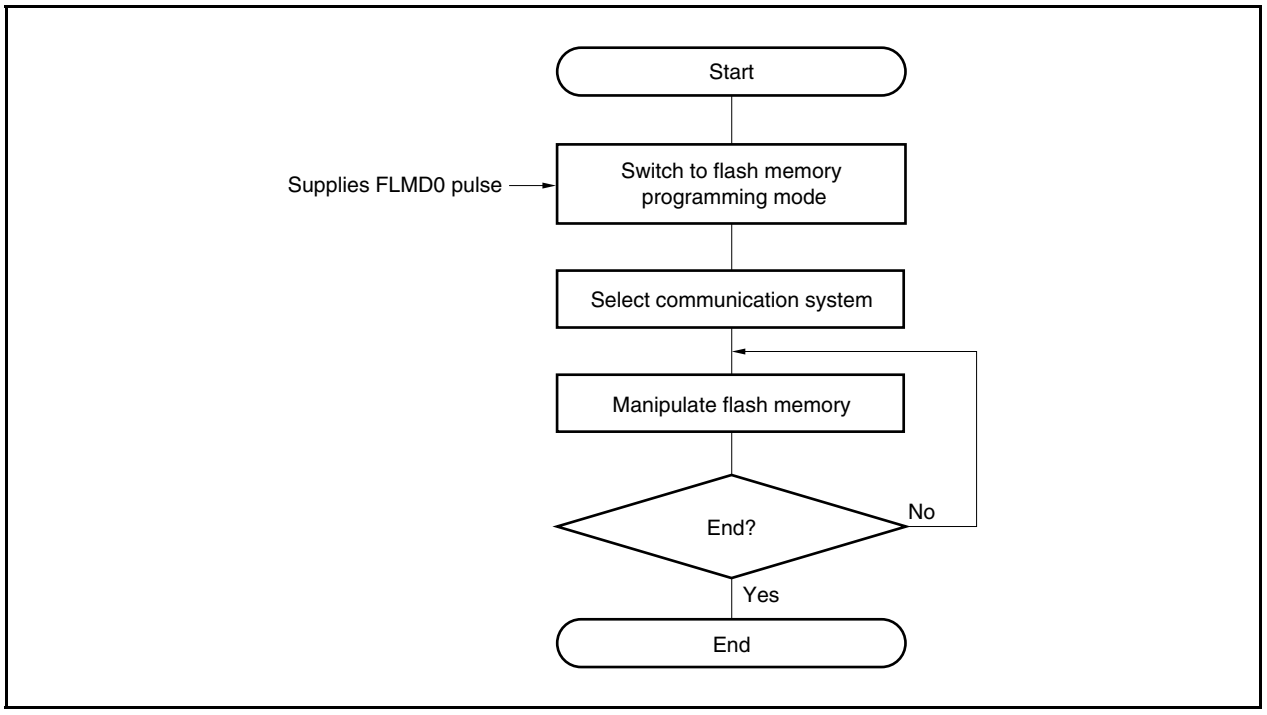
2. This adapter is for a 100-pin plastic QFP package.

3. This diagram shows the wiring when using a handshake-supporting CSI.

26.4.3 Flash memory control

The following shows the procedure for manipulating the flash memory.

Figure 26-8. Procedure for Manipulating Flash Memory

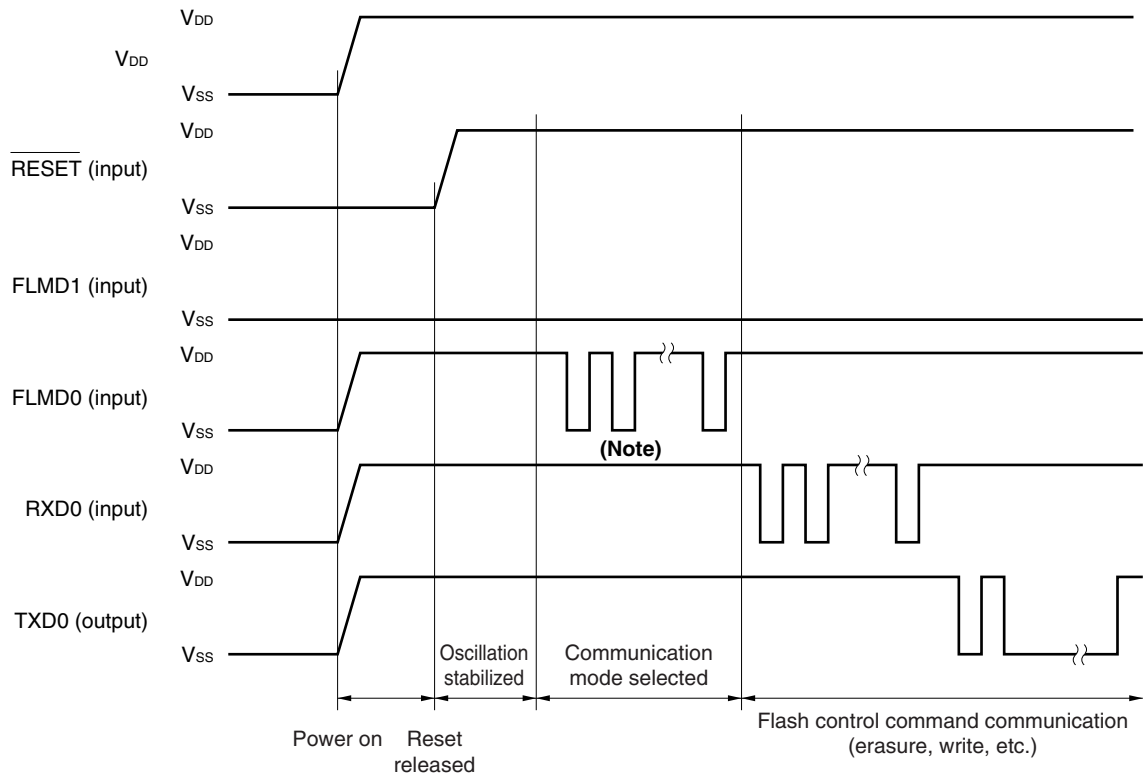


26.4.4 Selection of communication mode

In the V850ES/KG2, the communication mode is selected by inputting pulses (12 pulses max.) to the FLMD0 pin after switching to the flash memory programming mode. The FLMD0 pulse is generated by the dedicated flash programmer.

The following shows the relationship between the number of pulses and the communication mode.

Figure 26-9. Selection of Communication Mode



Note The number of clocks is as follows depending on the communication mode.

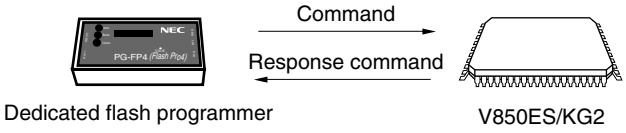
FLMD0 Pulse	Communication Mode	Remarks
0	UART0	Communication rate: 9600 bps (after reset), LSB first
8	CSI00	V850ES/KG2 performs slave operation, MSB first
11	CSI00 + HS	V850ES/KG2 performs slave operation, MSB first
Other	RFU	Setting prohibited

Caution When UART0 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash programmer after receiving the FLMD0 pulse.

26.4.5 Communication commands

The V850ES/KG2 communicates with the dedicated flash programmer by means of commands. The signals sent from the dedicated flash programmer to the V850ES/KG2 are called “commands”. The response signals sent from the V850ES/KG2 to the dedicated flash programmer are called “response commands”.

Figure 26-10. Communication Commands



The following shows the commands for flash memory control in the V850ES/KG2. All of these commands are issued from the dedicated flash programmer, and the V850ES/KG2 performs the processing corresponding to the commands.

Table 26-6. Flash Memory Control Commands

Classification	Command Name	Support			Function
		CSI00	CSI00 + HS	UART0	
Blank check	Block blank check command	○	○	○	Checks if the contents of the memory in the specified block have been correctly erased.
Erase	Chip erase command	○	○	○	Erases the contents of the entire memory.
	Block erase command	○	○	○	Erases the contents of the memory of the specified block.
Write	Write command	○	○	○	Writes the specified address range, and executes a contents verify check.
Verify	Verify command	○	○	○	Compares the contents of memory in the specified address range with data transferred from the flash programmer.
	Checksum command	○	○	○	Reads the checksum in the specified address range.
System setting, control	Silicon signature command	○	○	○	Reads silicon signature information.
	Security setting command	○	○	○	Disables the chip erase command, block erase command, and write command.

26.4.6 Pin connection

When performing on-board writing, mount a connector on the target system to connect to the dedicated flash programmer. Also, incorporate a function on-board to switch from the normal operation mode to the flash memory programming mode.

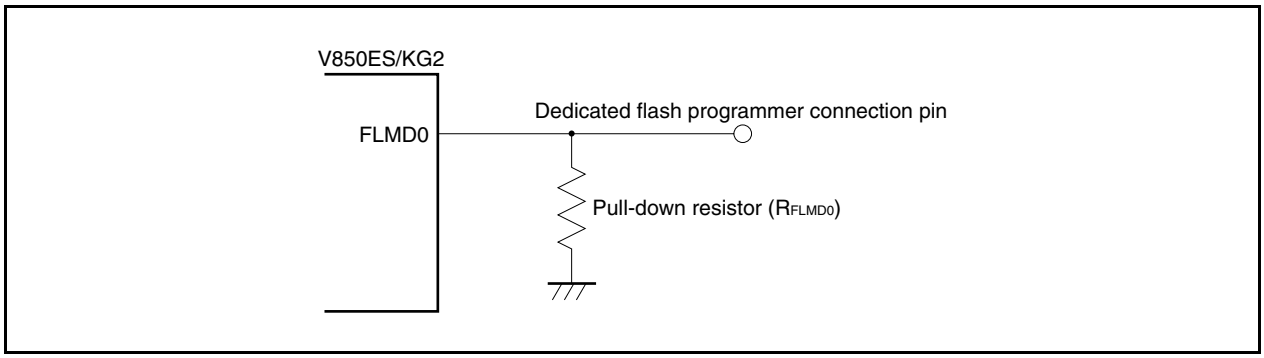
In the flash memory programming mode, all the pins not used for flash memory programming become the same status as that immediately after reset. Therefore, pin handling is required when the external device does not acknowledge the status immediately after a reset.

(1) FLMD0 pin

In the normal operation mode, input a voltage of V_{SS} level to the FLMD0 pin. In the flash memory programming mode, supply a write voltage of V_{DD} level to the FLMD0 pin.

Because the FLMD0 pin serves as a write protection pin in the self programming mode, a voltage of V_{DD} level must be supplied to the FLMD0 pin via port control, etc., before writing to the flash memory. For details, refer to **26.5.5 (1) FLMD0 pin**.

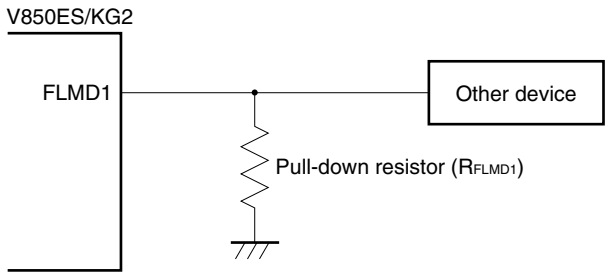
Figure 26-11. FLMD0 Pin Connection Example



(2) FLMD1 pin

When 0 V is input to the FLMD0 pin, the FLMD1 pin does not function. When V_{DD} is supplied to the FLMD0 pin, the flash memory programming mode is entered, so 0 V must be input to the FLMD1 pin. The following shows an example of the connection of the FLMD1 pin.

Figure 26-12. FLMD1 Pin Connection Example



Caution If the V_{DD} signal is input to the FLMD1 pin from another device during on-board writing and immediately after reset, isolate this signal.

Table 26-7. Relationship Between FLMD0 and FLMD1 Pins and Operation Mode When Reset Is Released

FLMD0	FLMD1	Operation Mode
0	don't care	Normal operation mode
V_{DD}	0	Flash memory programming mode
V_{DD}	V_{DD}	Setting prohibited

(3) Serial interface pin

The following shows the pins used by each serial interface.

Table 26-8. Pins Used by Serial Interfaces

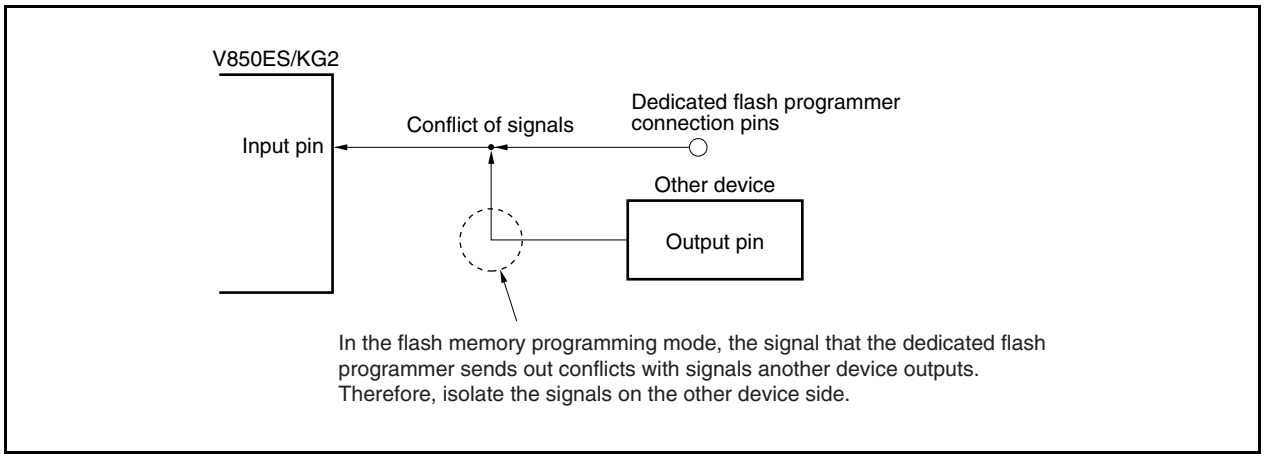
Serial Interface	Pins Used
UART0	TXD0, RXD0
CSI00	SO00, SI00, $\overline{\text{SCK00}}$
CSI00 + HS	SO00, SI00, $\overline{\text{SCK00}}$, PCM0

When connecting a dedicated flash programmer to a serial interface pin that is connected to another device on-board, care should be taken to avoid conflict of signals and malfunction of the other device.

(a) Conflict of signals

When the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the other device or set the other device to the output high-impedance status.

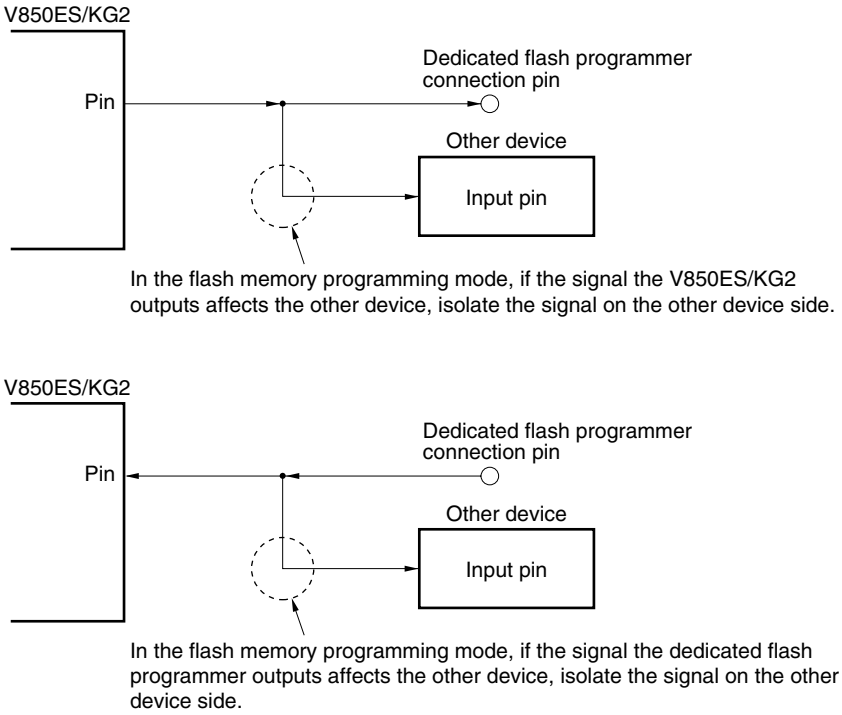
Figure 26-13. Conflict of Signals (Serial Interface Input Pin)



(b) Malfunction of other device

When the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), the signal is output to the other device, causing the device to malfunction. To avoid this, isolate the connection to the other device.

Figure 26-14. Malfunction of Other Device

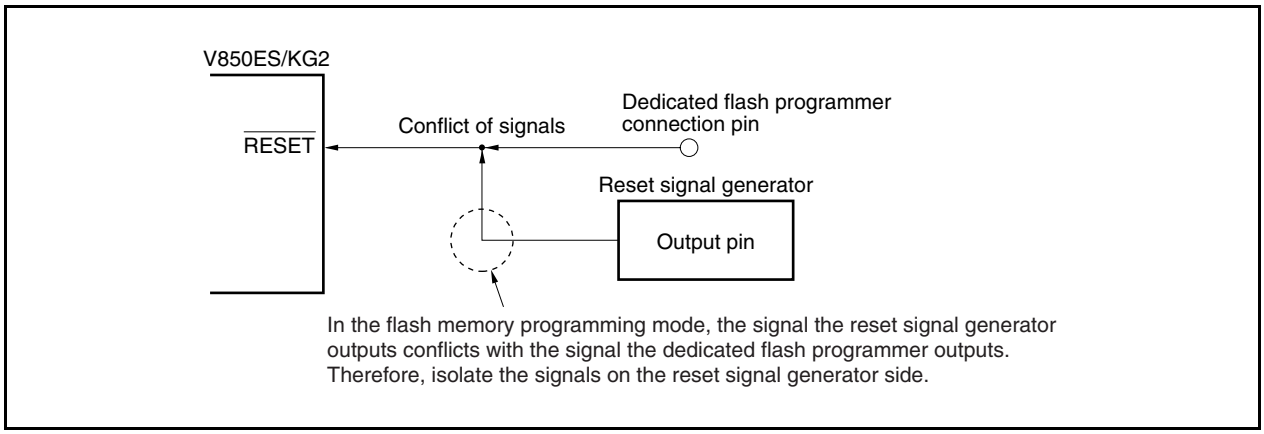


(4) $\overline{\text{RESET}}$ pin

When the reset signals of the dedicated flash programmer are connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on-board, a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the reset signal generator.

When a reset signal is input from the user system in the flash memory programming mode, the programming operation will not be performed correctly. Therefore, do not input signals other than the reset signals from the dedicated flash programmer.

Figure 26-15. Conflict of Signals ($\overline{\text{RESET}}$ Pin)



(5) Port pins (including NMI)

When the system shifts to the flash memory programming mode, all the pins that are not used for flash memory programming are in the same status as that immediately after reset. If the external device connected to each port does not recognize the status of the port immediately after reset, pins require appropriate processing, such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor.

(6) Other signal pins

Connect X1, X2, XT1, XT2, and REGC in the same status as that in the normal operation mode.

(7) Power supply

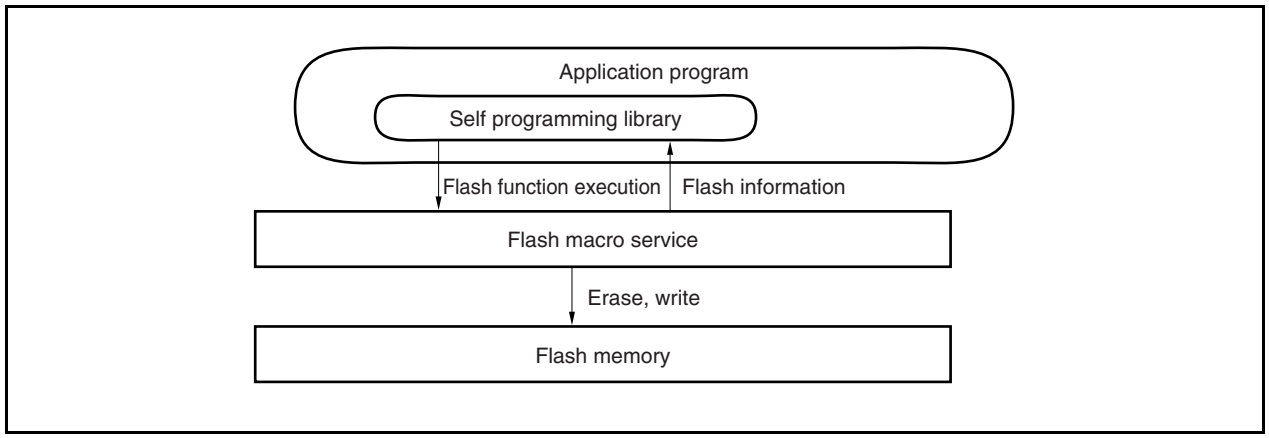
Supply the same power (V_{DD}, V_{SS}, EV_{DD}, EV_{SS}, AV_{SS}, BV_{DD}, BV_{SS}, AV_{REF0}, AV_{REF1}) as in normal operation mode.

26.5 Rewriting by Self Programming

26.5.1 Overview

The V850ES/KG2 supports a flash macro service that allows the user program to rewrite the internal flash memory by itself. By using this interface and a self programming library that is used to rewrite the flash memory with a user application program, the flash memory can be rewritten by a user application transferred in advance to the internal RAM or external memory. Consequently, the user program can be upgraded and constant data can be rewritten in the field.

Figure 26-16. Concept of Self Programming

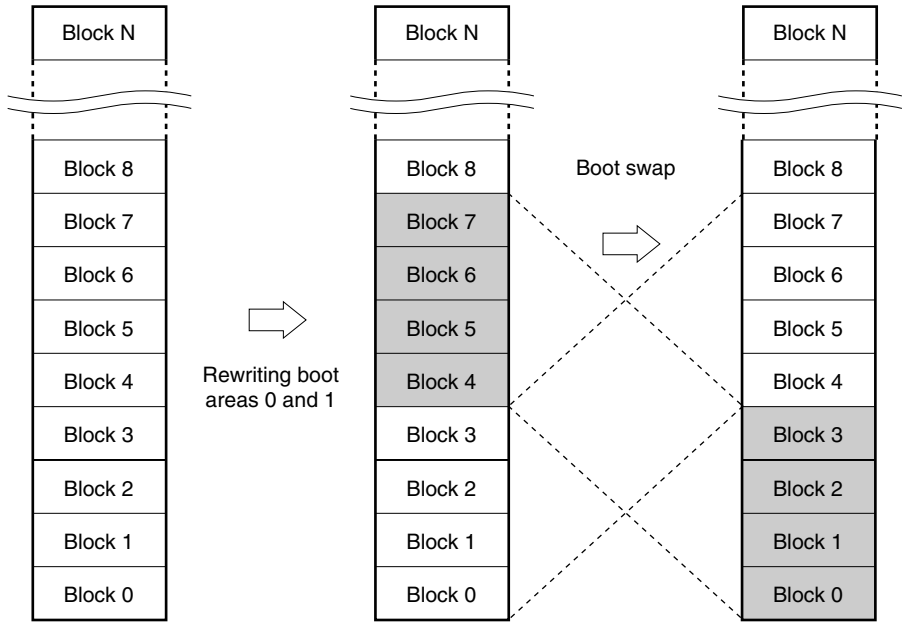


26.5.2 Features

(1) Secure self programming (boot swap function)

The V850ES/KG2 supports a boot swap function that can exchange the physical memory (blocks 0 to 3) of boot area 0 with the physical memory (blocks 4 to 7) of boot area 1. By writing the start program to be rewritten to boot area 1 in advance and then swapping the physical memory, the entire area can be safely rewritten even if a power failure occurs during rewriting because the correct user program always exists in boot area 0.

Figure 26-17. Rewriting Entire Memory Area (Boot Swap)



Remark 256 KB products: N = 127
128 KB products: N = 63

(2) Interrupt support

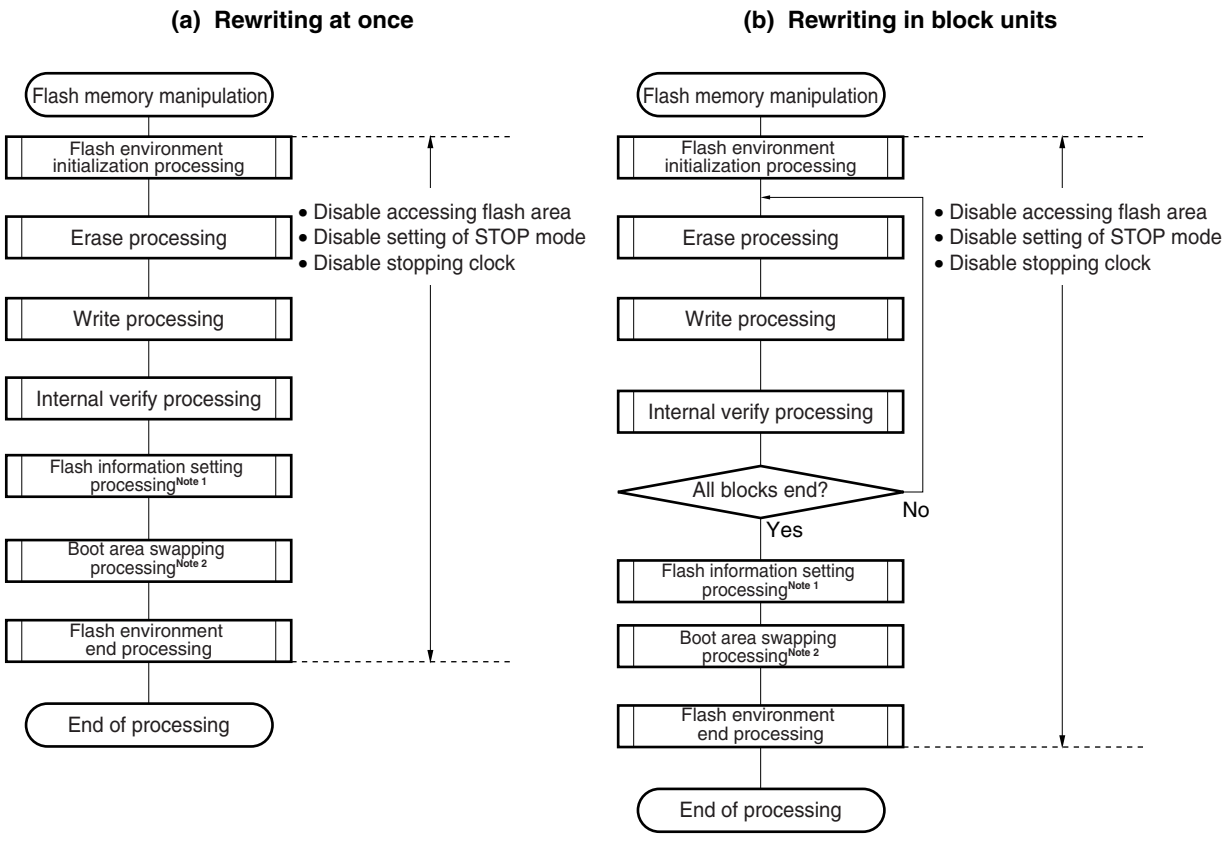
Instructions cannot be fetched from the flash memory during self programming. Conventionally, therefore, a user handler written to the flash memory could not be used even if an interrupt occurred. Therefore, in the V850ES/KG2, to use an interrupt during self programming, processing transits to the specific address[Note] in the internal RAM. Allocate the jump instruction that transits processing to the user interrupt servicing at the specific address[Note] in the internal RAM.

Note NMI interrupt: Start address of internal RAM
Maskable interrupt: Start address of internal RAM + 4 addresses

26.5.3 Standard self programming flow

The entire processing to rewrite the flash memory by flash self programming is illustrated below.

Figure 26-18. Standard Self Programming Flow



Notes 1. If a security setting is not performed, flash information setting processing does not have to be executed.

2. If boot swap is not used, flash information setting processing and boot area swap processing do not have to be executed.

26.5.4 Flash functions

Table 26-9. Main Flash Function List

Function Name	Outline	Support
FlashEnv	Initialization of flash control macro	√
FlashBlockErase	Erasure of only specified one block	√
FlashWordWrite	Writing from specified address	√
FlashBlockIVerify	Internal verification of specified block	√
FlashBlockBlankCheck	Blank check of specified block	√
FlashFLMDCheck	Check of FLMD pin	√
FlashGetInfo	Reading of flash information	√
FlashSetInfo	Setting of flash information	√
FlashBootSwap	Swapping of boot area	√
FlashWordRead	Reading data from specified address	√

Remark For details, refer to the **V850 Series Flash Memory Self Programming (Single Power Supply Flash Memory) User's Manual**.
Contact an NEC Electronics sales representative for the above manual.

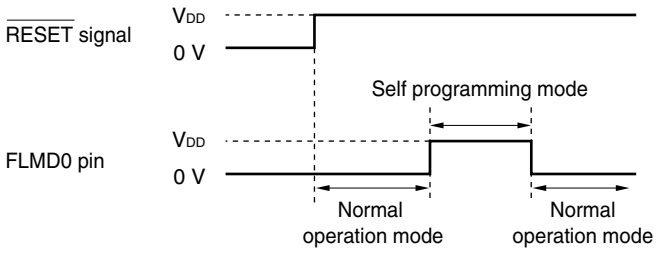
26.5.5 Pin processing

(1) FLMD0 pin

The FLMD0 pin is used to set the operation mode when reset is released and to protect the flash memory from being written during self rewriting. It is therefore necessary to keep the voltage applied to the FLMD0 pin at 0 V when reset is released and a normal operation is executed. It is also necessary to apply a voltage of V_{DD} level to the FLMD0 pin during the self programming mode period via port control before the memory is rewritten.

When self programming has been completed, the voltage on the FLMD0 pin must be returned to 0 V.

Figure 26-19. Mode Change Timing



Caution Make sure that the FLMD0 pin is at 0 V when reset is released.

26.5.6 Internal resources used

The following table lists the internal resources used for self programming. These internal resources can also be used freely for purposes other than self programming.

Table 26-10. Internal Resources Used

Resource Name	Description
Entry RAM area (internal RAM/external RAM size: 136 bytes)	Routines and parameters used for the flash macro service are located in this area. The entry program and default parameters are copied by calling a library initialization function.
Stack area (stack size: 600 bytes)	An extension of the stack used by the user is used by the library (can be used in both the internal RAM and external RAM).
Library code (code size: Approx. 1600 bytes)	Program entity of library (can be used anywhere other than the flash memory block to be manipulated).
Application program	Executed as user application. Calls flash functions.
Maskable interrupt	Can be used in user application execution status or self programming status. To use this interrupt in the self-programming status, since the processing transits to the address of the internal RAM start address + 4 addresses (3FFB004H), allocate the jump instruction that transits the processing to the user interrupt servicing at the address of the internal RAM start address + 4 addresses (3FFB004H) in advance.
NMI interrupt	Can be used in user application execution status or self programming status. To use this interrupt in the self-programming status, since the processing transits to the address of the internal RAM start address (3FFB000H), allocate the jump instruction that transits the processing to the user interrupt servicing at the internal RAM start address (3FFB000H) in advance.
TM50, TM51	Because TM50 and TM51 are used in the flash macro service, do not use them in the self programming status. When using TM50 and TM51 after self programming, set them again.

Remark For details, refer to the **V850 Series Flash Memory Self Programming (Single Power Supply Flash Memory) User's Manual**.

Contact an NEC Electronics sales representative for the above manual.

CHAPTER 27 ON-CHIP DEBUG FUNCTION

The V850ES/KG2 is not provided with an on-chip debug function. However, a pseudo on-chip debug function can be realized by using the on-chip debug emulator (MINICUBE) and debug adapter (QB-V850ESKX1H-DA).

27.1 ROM Security Function

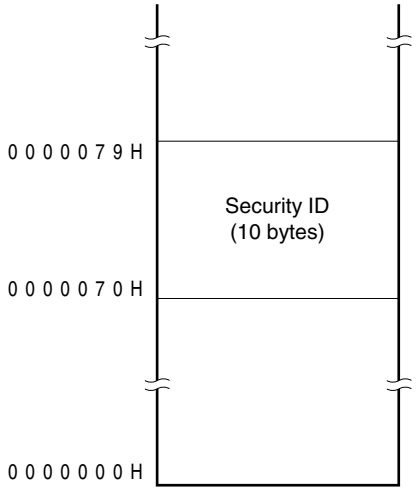
27.1.1 Security ID

The flash memory versions of the V850ES/KG2 perform authentication using a 10-byte ID code to prevent the contents of the flash memory from being read by an unauthorized person during on-chip debugging by the on-chip debug emulator.

Set the ID code in the 10-byte on-chip flash memory area from 0000070H to 0000079H to allow the debugger perform ID authentication.

If the IDs match, the security is released and reading flash memory and using the on-chip debug emulator are enabled.

- Set the 10-byte ID code to 0000070H to 0000079H.
- Bit 7 of 0000079H is the on-chip debug emulator enable flag.
  (0: Disable, 1: Enable)
- When the on-chip debug emulator is started, the debugger requests ID input. When the ID code input on the debugger and the ID code set in 0000070H to 0000079H match, the debugger starts.
- Debugging cannot be performed if the on-chip debug emulator enable flag is 0, even if the ID codes match.



Caution When the data in the flash memory has been deleted, all the bits are set to 1.

27.1.2 Setting

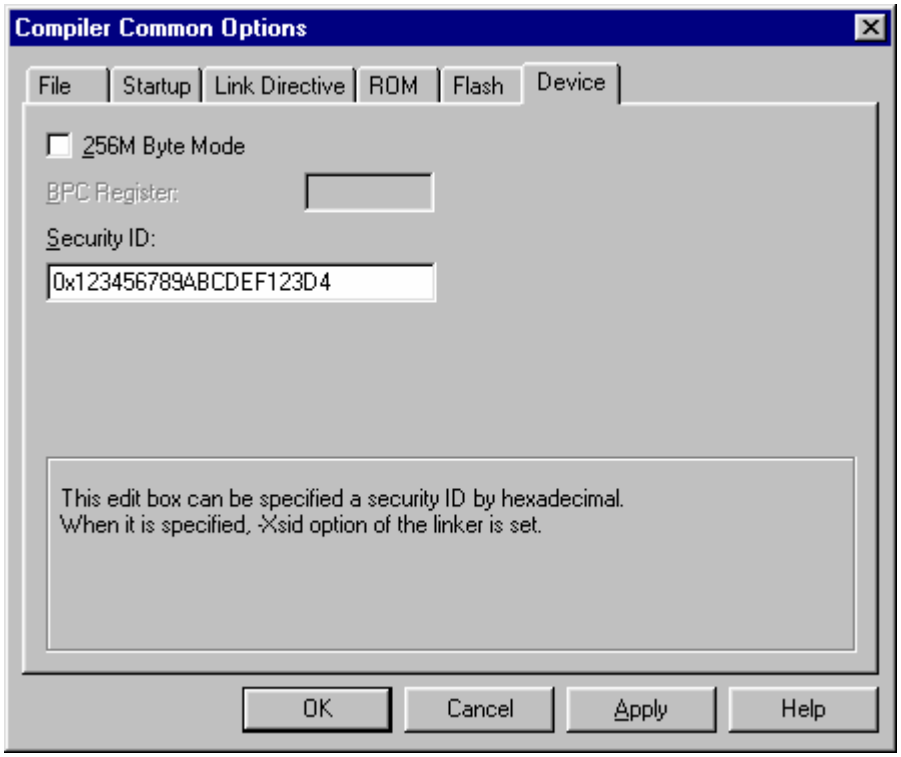
The following shows how to set the ID code as shown in Table 27-1.

When the ID code is set as shown in Table 27-1, the ID code input in the configuration dialog box of the ID850QB is “123456789ABCDEF123D4”.

Table 27-1. ID Code

Address	Value
0x70	0x12
0x71	0x34
0x72	0x56
0x73	0x78
0x74	0x9A
0x75	0xBC
0x76	0xDE
0x77	0XF1
0x78	0x23
0x79	0xD4

The ID code can be specified for the device file that supports the CA850 Ver. 2.60 or later and the security ID by the PM+ linker option setting.



[Program example (when using CA850 Ver. 2.60 or later)]

```
#---------------------------------------
#       SECURITYID (continue ILGOP  handler)
#---------------------------------------
        .section    "SECURITY_ID"   --Interrupt handler address 0x70
        .word       0x78563412      --0-3 byte code
        .word       0xF1DEBC9A      --4-7 byte code
        .hword      0xD423          --8-9 byte code
```

Remark Add the above program example to the startup files.

27.2 Cautions

(1) If a reset signal is input (from the target system or a reset signal from an internal reset source) during RUN (program execution), the break function may malfunction.

(2) Even if the reset signal is masked by the mask function, the I/O buffer (port pin) may be reset if a reset signal is input from a pin.

(3) Because a software breakpoint set in the internal flash memory is realized by the ROM correction function, it is made temporarily invalid by target reset or internal reset generated by watchdog timer 2. The breakpoint becomes valid again when a hardware break or forced break occurs, but a software break does not occur until then.

(4) Pin reset during a break is masked and the CPU and peripheral I/O are not reset. If pin reset or internal reset is generated as soon as the flash memory is rewritten by DMA or read by the RAM monitor function while the user program is being executed, the CPU and peripheral I/O may not be correctly reset.

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	BV_{DD}	$BV_{DD} \leq V_{DD}$	−0.3 to V_{DD} + 0.3[Note]	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF1}	$AV_{REF1} \leq V_{DD}$ (D/A output mode) $AV_{REF1} = AV_{REF0} = V_{DD}$ (port mode)	−0.3 to V_{DD} + 0.3[Note]	V
	V_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	AV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	BV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	EV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P90 to P915, $\overline{\text{RESET}}$, FLMD0	−0.3 to EV_{DD} + 0.3[Note]	V
	V_{I2}	PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15, PDH0 to PDH5	−0.3 to BV_{DD} + 0.3[Note]	V
	V_{I3}	P10, P11	−0.3 to AV_{REF1} + 0.3[Note]	V
	V_{I4}	P36, P37	−0.3 to +13	V
	V_{I5}	X1, X2, XT1, XT2	−0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{IAN}	P70 to P77	−0.3 to AV_{REF0} + 0.3[Note]	V

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	**Note**	Per pin	20	mA
		P36 to P39		30	mA
		P00 to P06, P30 to P39, P40 to P42	Total of all pins: 70 mA	35	mA
		P50 to P55, P90 to P915		35	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT7	Total of all pins: 70 mA	35	mA
		PDL0 to PDL15, PDH0 to PDH5		35	mA
Output current, high	I_{OH}	**Note**	Per pin	−10	mA
		P00 to P06, P30 to P35, P40 to P42	Total of all pins: −60 mA	−30	mA
		P50 to P55, P90 to P915		−30	mA
		PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT7	Total of all pins: −60 mA	−30	mA
		PDL0 to PDL15, PDH0 to PDH5		−30	mA
Operating ambient temperature	T_A	Normal operation mode		−40 to +85	°C
		Flash programming mode		−40 to +85	°C
Storage temperature	T_{stg}			−40 to +125	°C

Note P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P90 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15, PDH0 to PDH5

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_X = 1 MHz Unmeasured pins returned to 0 V	P70 to P77			15	pF
I/O capacitance	C_{IO}		**Note**			15	pF
			P36 to P39			20	pF

Note P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P90 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15, PDH0 to PDH5

Remark f_X: Main clock oscillation frequency

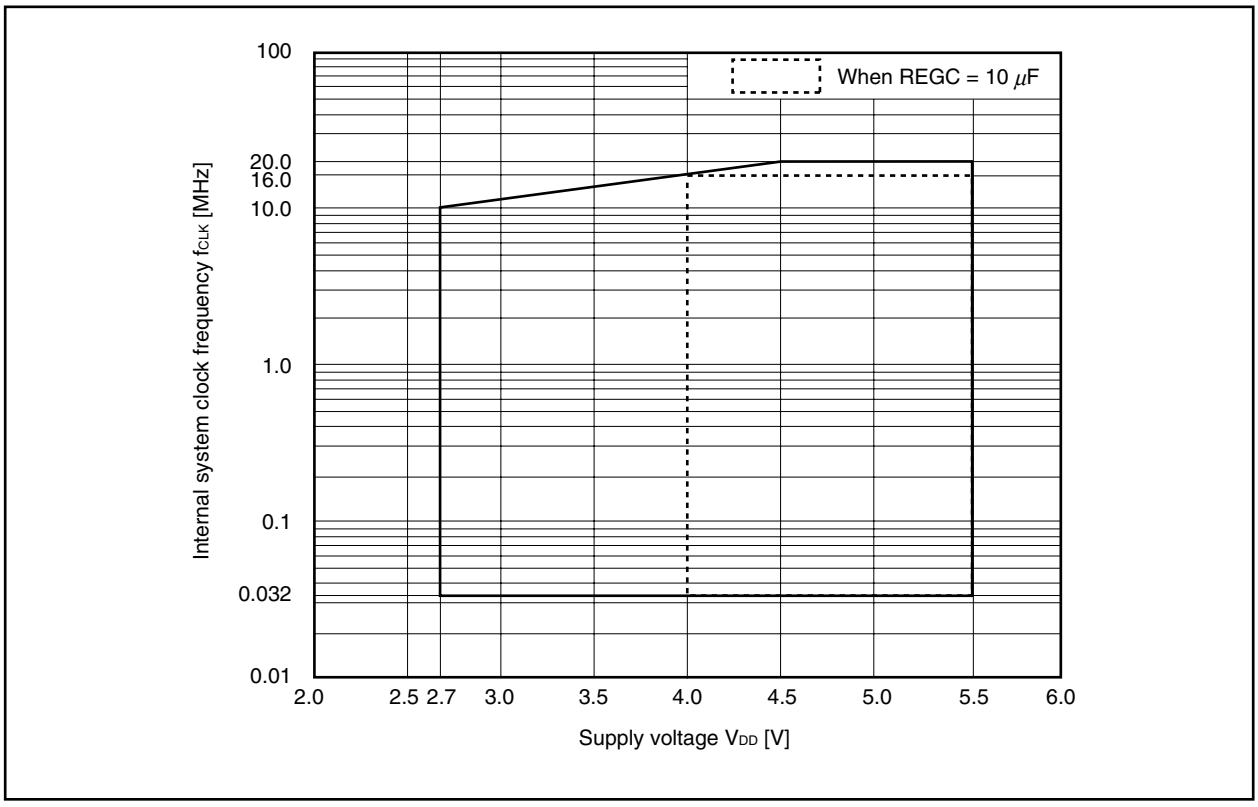
Operating Conditions

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	In PLL mode	REGC = V_{DD} = 4.5 to 5.5 V	0.25		20	MHz
			REGC = V_{DD} = 4.0 to 5.5 V	0.25		16	MHz
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	0.25		16	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	0.25		10	MHz
		In clock-through mode	REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	0.0625		10	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	0.0625		10	MHz
		Operating with subclock	**Note**		32.768		kHz

Note REGC = V_{DD} = 2.7 to 5.5 V or REGC = 10 μF, V_{DD} = 4.0 to 5.5 V

Internal System Clock Frequency vs. Supply Voltage



PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_X		2		5	MHz
Output frequency	f_{XX}		8		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches 2.7 V (MIN.)			200	μs

Operating Conditions for EEPROM Emulation

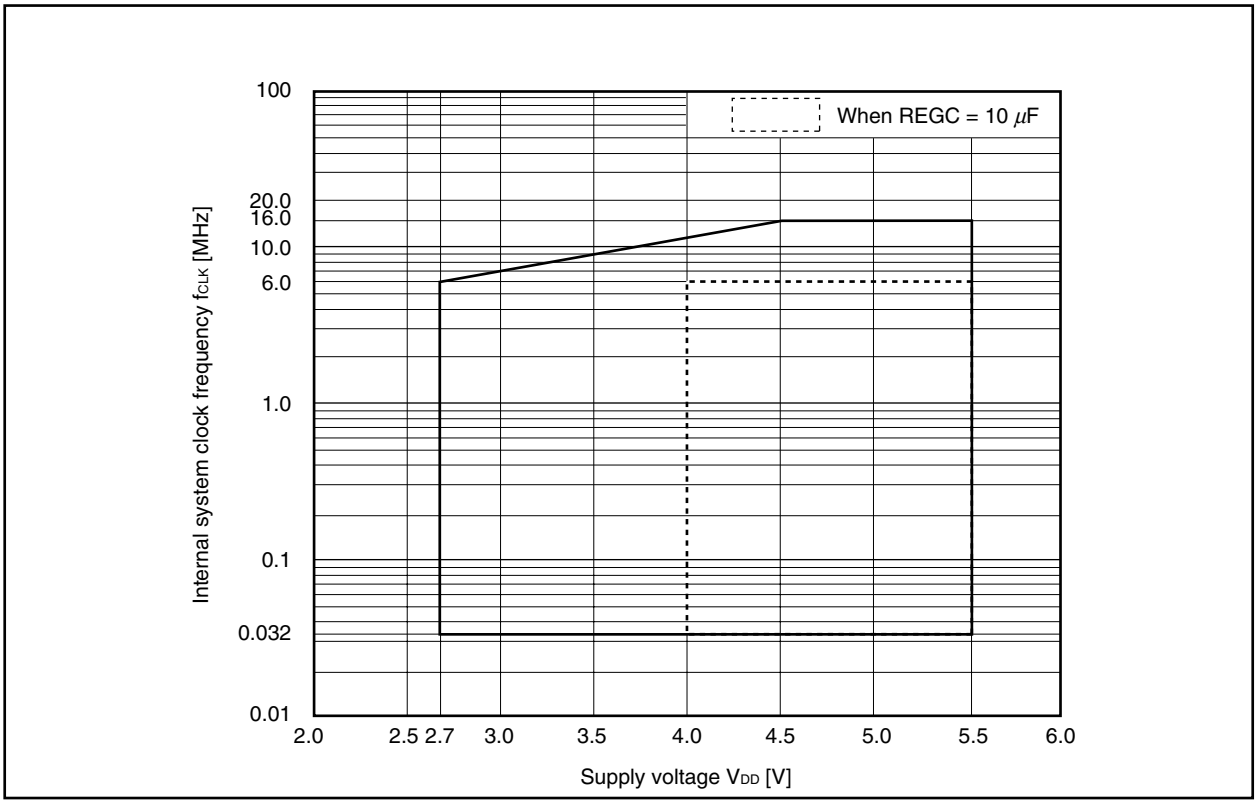
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	In PLL mode	REGC = V_{DD} = 4.5 to 5.5 V	0.25		16	MHz
			REGC = V_{DD} = 4.0 to 5.5 V	0.25		12	MHz
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	0.25		6	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	0.25		6	MHz
		In clock-through mode	REGC = V_{DD} = 4.0 to 5.5 V	0.0625		10	MHz
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	0.0625		6	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	0.0625		6	MHz
		Operating with subclock	**Notes 1, 2**		32.768		kHz

Notes 1. REGC = V_{DD} = 2.7 to 5.5 V or REGC = 10 μF, V_{DD} = 4.0 to 5.5 V

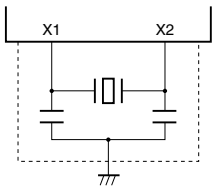
2. Do not stop the main clock.

Internal System Clock Frequency vs. Supply Voltage



Main Clock Oscillator Characteristics

(1) Crystal resonator, ceramic resonator (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

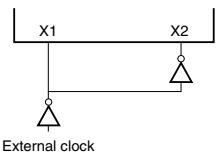
Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
	Oscillation frequency (f_X)[Note 1]	In PLL mode	REGC = V_{DD} = 4.5 to 5.5 V	2		5	MHz
			REGC = V_{DD} = 4.0 to 5.5 V	2		4	MHz
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	2		4	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	2		2.5	MHz
		In clock through mode	REGC = V_{DD} = 2.7 to 5.5 V	2		10	MHz
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	2		10	MHz
	Oscillation stabilization time[Note 2]	After reset is released	OSTS0 = 1		$2^{15}/f_X$		s
		After STOP mode is released			**Note 3**		s

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the resonator after reset or STOP mode is released.

3. The value differs depending on the OSTS register settings.

(2) External clock (T_A = –40 to +85°C, REGC = V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Recommended Circuit	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
	X1, X2 input frequency (f_X)[Note]	In PLL mode	REGC = V_{DD} = 4.5 to 5.5 V	2		5	MHz
			REGC = V_{DD} = 4.0 to 5.5 V	2		4	MHz
			REGC = V_{DD} = 2.7 to 5.5 V	2		2.5	MHz
		In clock through mode	REGC = V_{DD} = 2.7 to 5.5 V	2		10	MHz

Note The duty ratio of the input waveform must be within 50% ±5%.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

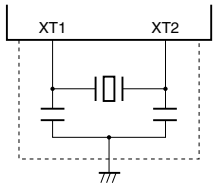
2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

3. When REGC = 10 μF, the supply voltage to the oscillator is the on-chip regulator output (3.6 V (TYP.)). However, the supply voltage to the oscillator is V_{DD} in the following modes.

- **After reset (except during WDTRES1 and oscillation stabilization time)**
- **In STOP mode**
- **In Sub-IDLE mode**

Subclock Oscillator Characteristics

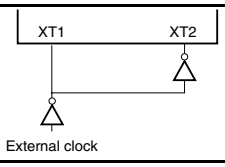
(1) Crystal resonator (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
	Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
	Oscillation stabilization timeNote 2			10		s

Notes 1. Indicates only oscillator characteristics.

2. Time required from when V_{DD} reaches oscillation voltage range (2.7 V (MIN.)) to when the crystal resonator stabilizes.

(2) External clock (T_A = –40 to +85°C, REGC = V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
	Input frequency (f_{XT})Note	REGC = V_{DD} = 2.7 to 5.5 V	32		35	kHz

Note The duty ratio of the input waveform must be within 50% ±5%.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

3. When REGC = 10 μF, the supply voltage to the oscillator is the on-chip regulator output (3.6 V (TYP.)). However, the supply voltage to the oscillator is V_{DD} in the following modes.

- **After reset (except during WDTRES1 and oscillation stabilization time)**
- **In STOP mode**
- **In Sub-IDLE mode**

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions		MAX.	Unit
Output current, high	I_{OH1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P90 to P915		–5.0	mA
		Total of P00 to P06, P30 to P35, P40 to P42	EV_{DD} = 4.0 to 5.5 V	–30	mA
			EV_{DD} = 2.7 to 5.5 V	–15	mA
		Total of P50 to P55, P90 to P915	EV_{DD} = 4.0 to 5.5 V	–30	mA
			EV_{DD} = 2.7 to 5.5 V	–15	mA
	I_{OH2}	Per pin for PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDH0 to PDH5, PDL0 to PDL15		–5.0	mA
		Total of PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6	BV_{DD} = 4.0 to 5.5 V	–30	mA
			BV_{DD} = 2.7 to 5.5 V	–15	mA
		Total of PDL0 to PDL15, PDH0 to PDH5	BV_{DD} = 4.0 to 5.5 V	–30	mA
			BV_{DD} = 2.7 to 5.5 V	–15	mA
Output current, low	I_{OL1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P90 to P915		10	mA
		Per pin for P36 to P39	EV_{DD} = 4.0 to 5.5 V	15	mA
			EV_{DD} = 2.7 to 5.5 V	8	mA
		Total of P00 to P06, P30 to P37, P40 to P42		30	mA
		Total of P38, P39, P50 to P55, P90 to P915		30	mA
	I_{OL2}	Per pin for PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDH0 to PDH5, PDL0 to PDL15		10	mA
		Total of PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6		30	mA
		Total of PDL0 to PDL15, PDH0 to PDH5		30	mA

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (2/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	**Note 2**	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	**Note 3**	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P77	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	P10, P11[Note 4]	0.7AV_{REF1}		AV_{REF1}	V
	V_{IH6}	P36, P37	0.7EV_{DD}		12[Note 5]	V
	V_{IH7}	X1, X2, XT1, XT2	V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	**Note 2**	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	**Note 3**	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P77	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	P10, P11[Note 4]	AV_{SS}		0.3AV_{REF1}	V
	V_{IL6}	P36, P37	EV_{SS}		0.3EV_{DD}	V
	V_{IL7}	X1, X2, XT1, XT2	V_{SS}		0.4	V

Notes 1. P00, P01, P30, P41, P98, P911 and their alternate-function pins.

2. $\overline{\text{RESET}}$, P02 to P06, P31 to P35, P38, P39, P40, P42, P50 to P55, P90 to P97, P99, P910, P912 to P915 and their alternate-function pins.

3. PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15, PDH0 to PDH5 and their alternate-function pins.

4. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

5. When an on-chip pull-up resistor is not specified by a mask option. EV_{DD} when a pull-up resistor is specified.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (3/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	**Note 1**	I_{OH} = –2.0 mA, EV_{DD} = 4.0 to 5.5 V	EV_{DD} – 1.0		EV_{DD}	V
		Note 2	I_{OH} = –0.1 mA, EV_{DD} = 2.7 to 5.5 V	EV_{DD} – 0.5		EV_{DD}	V
	V_{OH2}	**Note 3**	I_{OH} = –2.0 mA, BV_{DD} = 4.0 to 5.5 V	BV_{DD} – 1.0		BV_{DD}	V
		Note 4	I_{OH} = –0.1 mA, BV_{DD} = 2.7 to 5.5 V	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P10, P11[Note 5]	I_{OH} = –2.0 mA	AV_{REF1} – 1.0		AV_{REF1}	V
			I_{OH} = –0.1 mA	AV_{REF1} – 0.5		AV_{REF1}	V
Output voltage, low	V_{OL1}	**Note 6**	I_{OL} = 2.0 mA[Note 7]	0		0.8	V
	V_{OL2}	**Note 8**	I_{OL} = 2.0 mA[Note 7]	0		0.8	V
	V_{OL3}	P10, P11[Note 5]	I_{OL} = 2 mA	0		0.8	V
	V_{OL4}	P36 to P39	I_{OL} = 15 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 8 mA, EV_{DD} = 3.0 to 5.5 V	0		1.0	V
			I_{OL} = 5 mA, EV_{DD} = 2.7 to 5.5 V	0		1.0	V
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}				3.0	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V				–3.0	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3.0	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3.0	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Notes 1. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –30 mA, total of P50 to P55, P90 to P915 and their alternate-function pins: I_{OH} = –30 mA.

2. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –15 mA, total of P50 to P55, P90 to P915 and their alternate-function pins: I_{OH} = –15 mA.

3. Total of PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6: I_{OH} = –30 mA, total of PDH0 to PDH5, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –30 mA.

4. Total of PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6: I_{OH} = –15 mA, total of PDH0 to PDH5, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –15 mA.

5. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

6. Total of P00 to P06, P30 to P37, P40 to P42 and their alternate-function pins: I_{OL} = 30 mA, total of P38, P39, P50 to P55, P90 to P915 and their alternate-function pins: I_{OL} = 30 mA.

7. Refer to I_{OL1} for I_{OL} of P36 to P39.

8. Total of PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6 and their alternate-function pins: I_{OL} = 30 mA, total of PDH0 to PDH5, PDL0 to PDL15 and their alternate-function pins: I_{OL} = 30 mA.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (4/4)

Parameter	Symbol	Conditions	MIN.	TYP.[Note 2]	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Normal operation mode (all peripheral functions operating)				
		f_{XX} = 20 MHz (f_X = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		55	75	mA
		f_{XX} = 16 MHz (f_X = 4 MHz) (in PLL mode) V_{DD} = 5 V ±10%, REGC = 10 μF		34	50	mA
		f_{XX} = 10 MHz (in clock-through mode) REGC = V_{DD} = 3 V ±10%		18	37	mA
	I_{DD2}	HALT mode (all peripheral functions operating)				
		f_{XX} = 20 MHz (f_X = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		29	43	mA
		f_{XX} = 16 MHz (f_X = 4 MHz) (in PLL mode) V_{DD} = 5 V ±10%, REGC = 10 μF		17	31	mA
		f_{XX} = 10 MHz (in clock-through mode) REGC = V_{DD} = 3 V ±10%		10	17	mA
	I_{DD3}	IDLE mode (watch timer operating)				
		f_X = 5 MHz (when PLL mode off) REGC = V_{DD} = 5 V ±10%		2.1	3.3	mA
		f_X = 4 MHz (when PLL mode off) V_{DD} = 5 V ±10%, REGC = 10 μF		1.5	2.7	mA
		f_X = 10 MHz (in clock-through mode) REGC = V_{DD} = 3 V ±10%		1.5	2.7	mA
	I_{DD4}	Subclock operation mode (f_{XT} = 32.768 kHz) Main oscillation stopped		250	420	μA
	I_{DD5}	Sub-IDLE mode (f_{XT} = 32.768 kHz) Watch timer operating, main oscillation stopped		20	75	μA
	I_{DD6}	STOP mode				
		Subclock oscillating		15	60	μA
		Subclock stopped (XT1 = V_{SS}, PSMR.XTSTP bit = 1)		0.1	30	μA
	I_{DD7}	Flash memory erase/write (T_A = –40 to +85°C)				
		f_{XX} = 20 MHz (f_X = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		55	75	mA
		f_{XX} = 16 MHz (f_X = 4 MHz) (in PLL mode) V_{DD} = 5 V ±10%, REGC = 10 μF		34	50	mA
		f_{XX} = 10 MHz (in clock-through mode) REGC = V_{DD} = 3 V ±10%		18	37	mA

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped). AV_{REF0} and AV_{REF1} are not included.

2. TYP. value of V_{DD} is as follows.

V_{DD} = 5.0 V when V_{DD} = 5 V ±10%

V_{DD} = 3.0 V when V_{DD} = 3 V ±10%

Remark f_{XX}: Main clock frequency

f_X: Main clock oscillation frequency

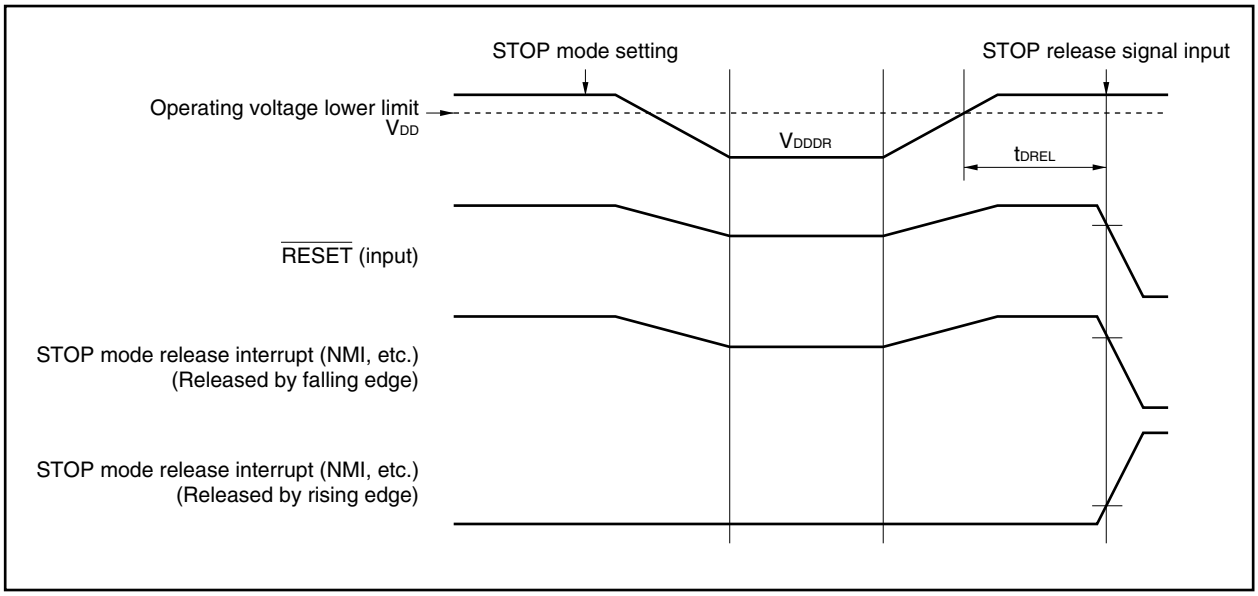
f_{XT}: Subclock frequency

Data Retention Characteristics

STOP Mode (T_A = –40 to +85°C)

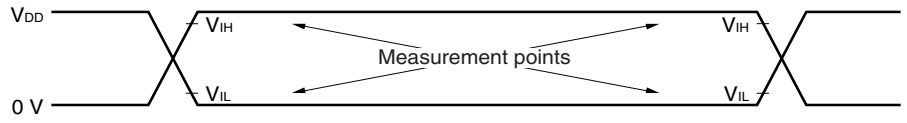
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.0		5.5	V
STOP release signal input time	t_{DREL}		0			μs

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

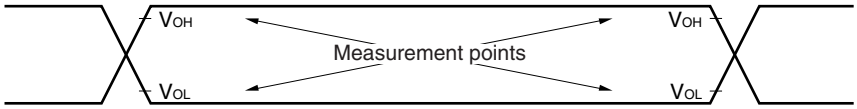


AC Characteristics

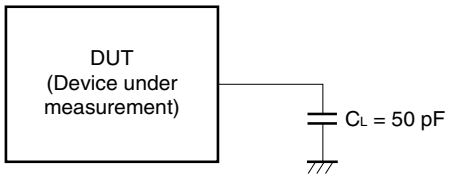
AC Test Input Measurement Points (V_{DD}, AV_{REF0}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



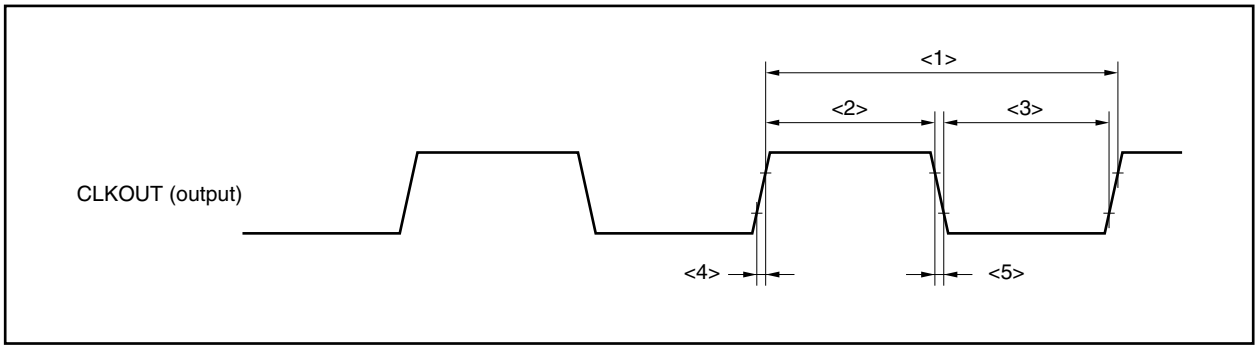
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

CLKOUT Output Timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}	<1>		50 ns	30.6 μs	
High-level width	t_{WKH}	<2>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 17		ns
			V_{DD} = 2.7 to 5.5 V	t_{CYK}/2 – 26		ns
Low-level width	t_{WKL}	<3>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 17		ns
			V_{DD} = 2.7 to 5.5 V	t_{CYK}/2 – 26		ns
Rise time	t_{KR}	<4>	V_{DD} = 4.0 to 5.5 V		17	ns
			V_{DD} = 2.7 to 5.5 V		26	ns
Fall time	t_{KF}	<5>	V_{DD} = 4.0 to 5.5 V		17	ns
			V_{DD} = 2.7 to 5.5 V		26	ns

Clock Timing



Bus Timing

(1) In multiplex bus mode

(a) Read/write cycle (CLKOUT asynchronous)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<6>		$(0.5 + t_{ASW})T - 23$		ns
Address hold time (from ASTB↓)	t_{HSTA}	<7>		$(0.5 + t_{AHW})T - 15$		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}	<8>			16	ns
Data input setup time from address	t_{SAID}	<9>			$(2 + n + t_{ASW} + t_{AHW})T - 40$	ns
Data input setup time from $\overline{RD}$↓	t_{SRID}	<10>			$(1 + n)T - 25$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$	<11>		$(0.5 + t_{AHW})T - 20$		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}	<12>		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}	<13>		$(1 + i)T - 16$		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$	<14>		$0.5T - 10$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}	<15>		$(1.5 + i + t_{ASW})T - 10$		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}	<16>		$(1 + n)T - 10$		ns
ASTB high-level width	t_{WSTH}	<17>		$(1 + i + t_{ASW})T - 25$		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}	<18>			20	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}	<19>		$(1 + n)T - 25$		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}	<20>		$T - 15$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<21>	n ≥ 1		$(1.5 + t_{ASW} + t_{AHW})T - 45$	ns
	t_{SAWT2}	<22>			$(1.5 + n + t_{ASW} + t_{AHW})T - 45$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<23>	n ≥ 1	$(0.5 + n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}	<24>		$(1.5 + n + t_{ASW} + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<25>	n ≥ 1		$(1 + t_{AHW})T - 32$	ns
	t_{SSTWT2}	<26>			$(1 + n + t_{AHW})T - 32$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<27>	n ≥ 1	$(n + t_{AHW})T$		ns
	t_{HSTWT2}	<28>		$(1 + n + t_{AHW})T$		ns

Remarks 1. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

2. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

3. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

4. m = 0, 1

5. i: Number of idle states inserted after a read cycle (0 or 1)

6. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<6>		$(0.5 + t_{ASW})T - 42$		ns
Address hold time (from ASTB↓)	t_{HSTA}	<7>		$(0.5 + t_{AHW})T - 30$		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}	<8>			32	ns
Data input setup time from address	t_{SAID}	<9>			$(2 + n + t_{ASW} + t_{AHW})T - 72$	ns
Data input setup time from $\overline{RD}$↓	t_{SRID}	<10>			$(1 + n)T - 40$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$	<11>		$(0.5 + t_{AHW})T - 35$		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}	<12>		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}	<13>		$(1 + i)T - 32$		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$	<14>		$0.5T - 20$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}	<15>		$(1.5 + i + t_{ASW})T - 20$		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}	<16>		$(1 + n)T - 20$		ns
ASTB high-level width	t_{WSTH}	<17>		$(1 + i + t_{ASW})T - 50$		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}	<18>			35	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}	<19>		$(1 + n)T - 40$		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}	<20>		$T - 30$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<21>	n ≥ 1		$(1.5 + t_{ASW} + t_{AHW})T - 80$	ns
	t_{SAWT2}	<22>			$(1.5 + n + t_{ASW} + t_{AHW})T - 80$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<23>	n ≥ 1	$(0.5 + n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}	<24>		$(1.5 + n + t_{ASW} + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<25>	n ≥ 1		$(1 + t_{AHW})T - 60$	ns
	t_{SSTWT2}	<26>			$(1 + n + t_{AHW})T - 60$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<27>	n ≥ 1	$(n + t_{AHW})T$		ns
	t_{HSTWT2}	<28>		$(1 + n + t_{AHW})T$		ns

Caution Set the following in accordance with the usage conditions of the CPU operating clock frequency (k = 0 to 3).

- **70 ns < 1/f_{CPU} < 84 ns**
  Set an address setup wait (AWC.ASWk bit = 1).
- **62.5 ns < 1/f_{CPU} < 70 ns**
  Set an address setup wait (ASWk bit = 1) and address hold wait (AWC.AHWk bit = 1).

Remarks 1. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

2. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

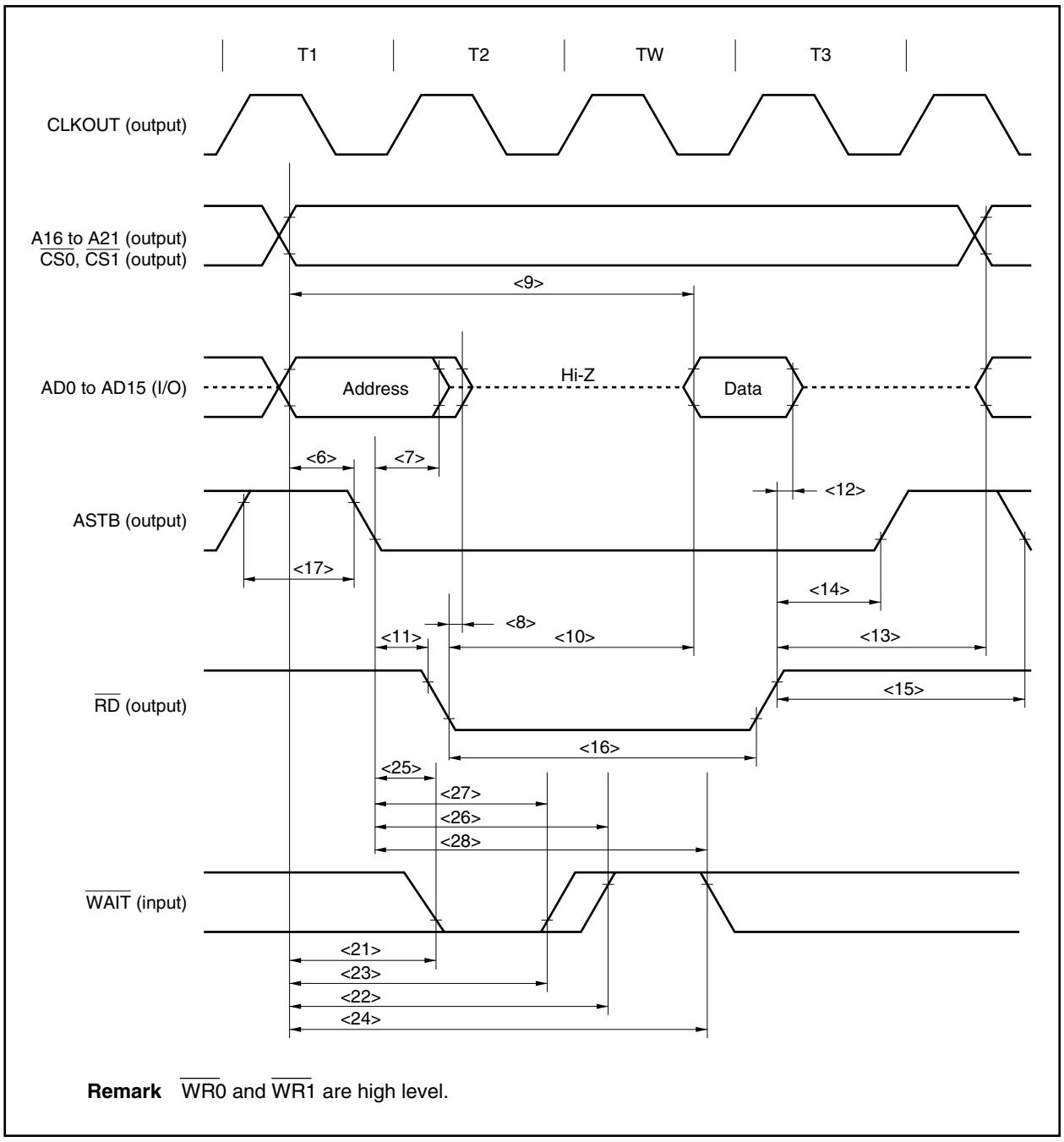
3. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

4. m = 0, 1

5. i: Number of idle states inserted after a read cycle (0 or 1)

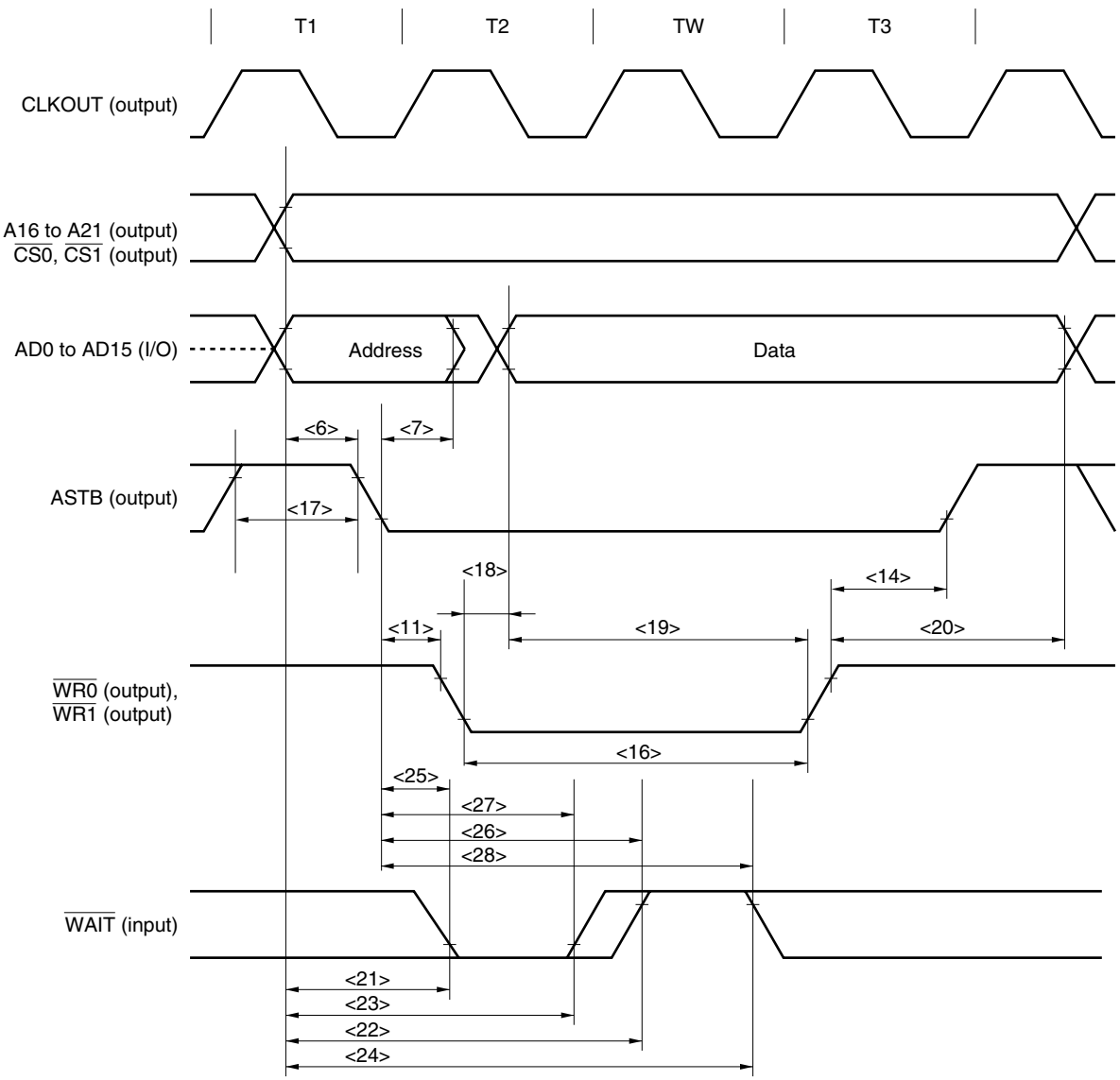
6. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Asynchronous): In Multiplex Bus Mode



Remark WR0 and WR1 are high level.

Write Cycle (CLKOUT Asynchronous): In Multiplex Bus Mode



Remark $\overline{RD}$ is high level.

(b) Read/write cycle (CLKOUT synchronous): In multiplex bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<29>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<30>		0	14	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<31>		0	23	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}	<32>		–22	0	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<33>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<34>		0		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<35>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<36>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<37>		0		ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

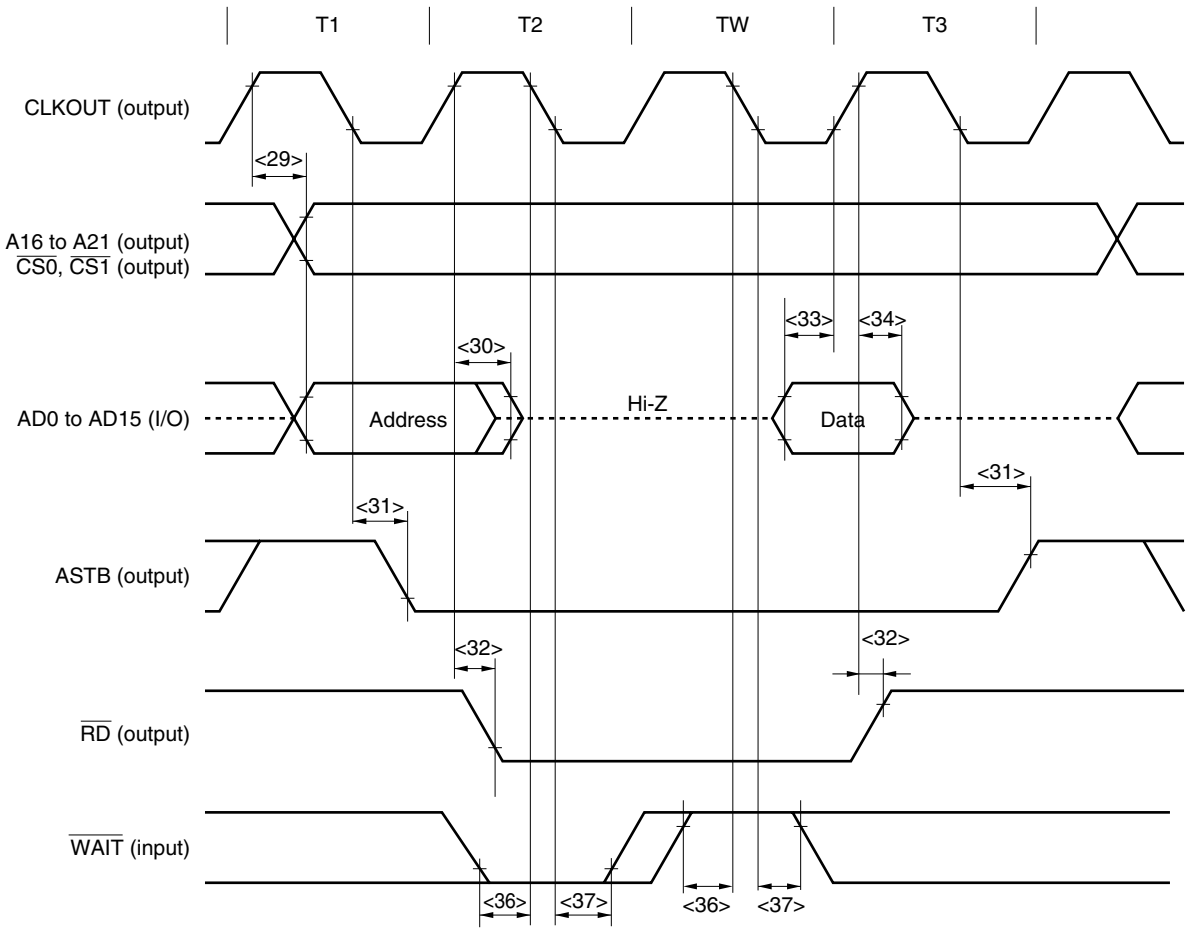
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<29>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<30>		0	18	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<31>		0	55	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}	<32>		–22	0	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<33>		30		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<34>		0		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<35>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<36>		25		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<37>		0		ns

Remarks 1. m = 0, 1

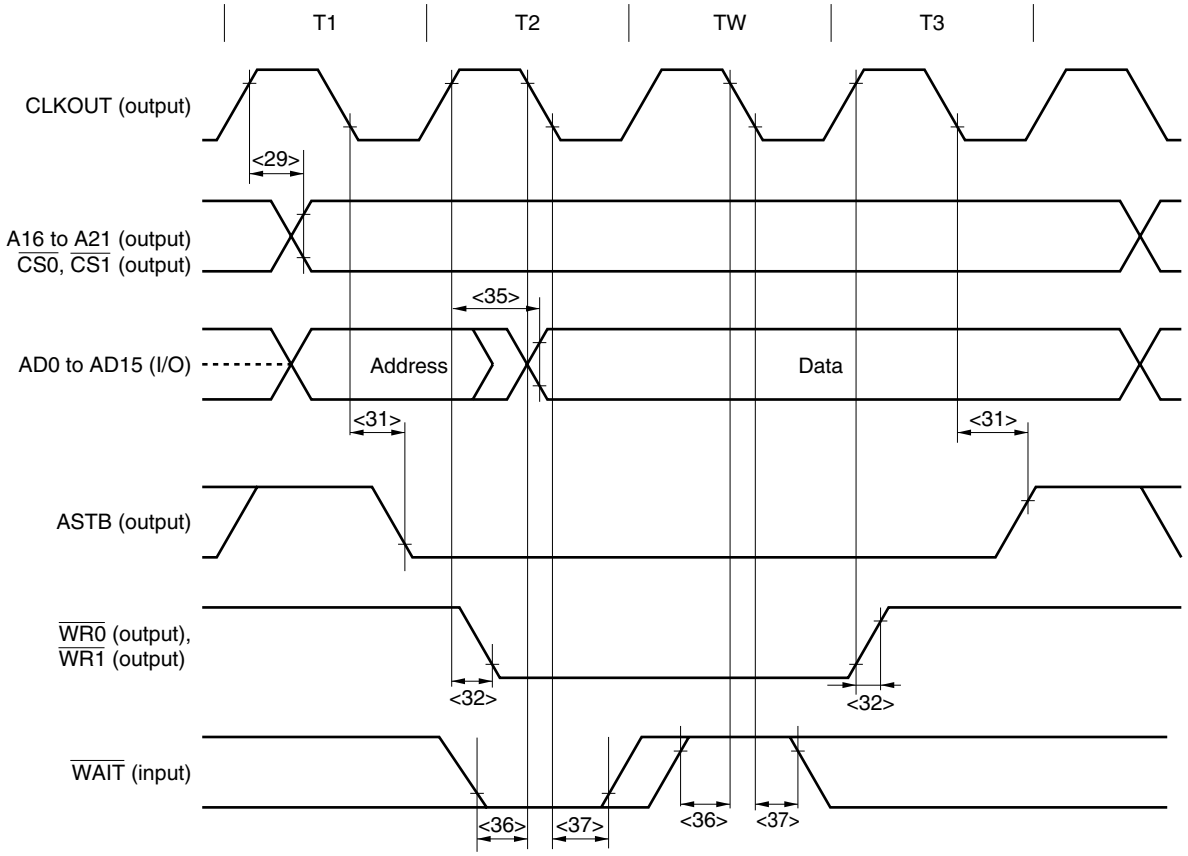
2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Synchronous): In Multiplex Bus Mode



Remark WR0 and WR1 are high level.

Write Cycle (CLKOUT Synchronous): In Multiplex Bus Mode



Remark $\overline{RD}$ is high level.

(2) In separate bus mode

(a) Read cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{RD}$↓)	t_{SARD}	<38>		$(0.5 + t_{ASW})T - 50$		ns
Address hold time (from $\overline{RD}$↑)	t_{HARD}	<39>		$iT - 13$		ns
$\overline{RD}$ low-level width	t_{WRDL}	<40>		$(1.5 + n + t_{AHW})T - 15$		ns
Data setup time (to $\overline{RD}$↑)	t_{SISD}	<41>		30		ns
Data hold time (from $\overline{RD}$↑)	t_{HISD}	<42>		0		ns
Data setup time (to address)	t_{SAID}	<43>			$(2 + n + t_{ASW} + t_{AHW})T - 65$	ns
$\overline{WAIT}$ setup time (to $\overline{RD}$↓)	t_{SRDWT1}	<44>	n ≥ 1		$(0.5 + t_{AHW})T - 32$	ns
	t_{SRDWT2}	<45>			$(0.5 + n + t_{AHW})T - 32$	ns
$\overline{WAIT}$ hold time (from $\overline{RD}$↓)	t_{HRDWT1}	<46>	n ≥ 1	$(n - 0.5 + t_{AHW})T$		ns
	t_{HRDWT2}	<47>		$(n + 0.5 + t_{AHW})T$		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<48>	n ≥ 1		$(1 + t_{ASW} + t_{AHW})T - 65$	ns
	t_{SAWT2}	<49>			$(1 + n + t_{ASW} + t_{AHW})T - 65$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<50>	n ≥ 1	$(n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}	<51>		$(1 + n + t_{ASW} + t_{AHW})T$		ns

Caution Set the following in accordance with the usage conditions of the CPU operating clock frequency (k = 0 to 3).

- **$1/f_{CPU}$ < 100 ns**

  Set an address setup wait (ASWk bit = 1).

Remarks 1. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

2. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

3. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted

4. i: Number of idle states inserted after a read cycle (0 or 1)

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{RD}$↓)	t_{SARD}	<38>		(0.5 + t_{ASW})T – 100		ns
Address hold time (from $\overline{RD}$↑)	t_{HARD}	<39>		iT – 26		ns
$\overline{RD}$ low-level width	t_{WRDL}	<40>		(1.5 + n + t_{AHW})T – 30		ns
Data setup time (to $\overline{RD}$↑)	t_{SISD}	<41>		60		ns
Data hold time (from $\overline{RD}$↑)	t_{HISD}	<42>		0		ns
Data setup time (to address)	t_{SAID}	<43>			(2 + n + t_{ASW} + t_{AHW})T – 120	ns
$\overline{WAIT}$ setup time (to $\overline{RD}$↓)	t_{SRDWT1}	<44>	n ≥ 1		(0.5 + t_{AHW})T – 50	ns
	t_{SRDWT2}	<45>			(0.5 + n + t_{AHW})T – 50	ns
$\overline{WAIT}$ hold time (from $\overline{RD}$↓)	t_{HRDWT1}	<46>	n ≥ 1	(n – 0.5 + t_{AHW})T		ns
	t_{HRDWT2}	<47>		(n + 0.5 + t_{AHW})T		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<48>	n ≥ 1		(1 + t_{ASW} + t_{AHW})T – 130	ns
	t_{SAWT2}	<49>			(1 + n + t_{ASW} + t_{AHW})T – 130	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<50>	n ≥ 1	(n + t_{ASW} + t_{AHW})T		ns
	t_{HAWT2}	<51>		(1 + n + t_{ASW} + t_{AHW})T		ns

Caution Set the following in accordance with the usage conditions of the CPU operating clock frequency (k = 0 to 3).

- **1/f_{CPU} < 200 ns**

  Set an address setup wait (ASWk bit = 1).

Remarks 1. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

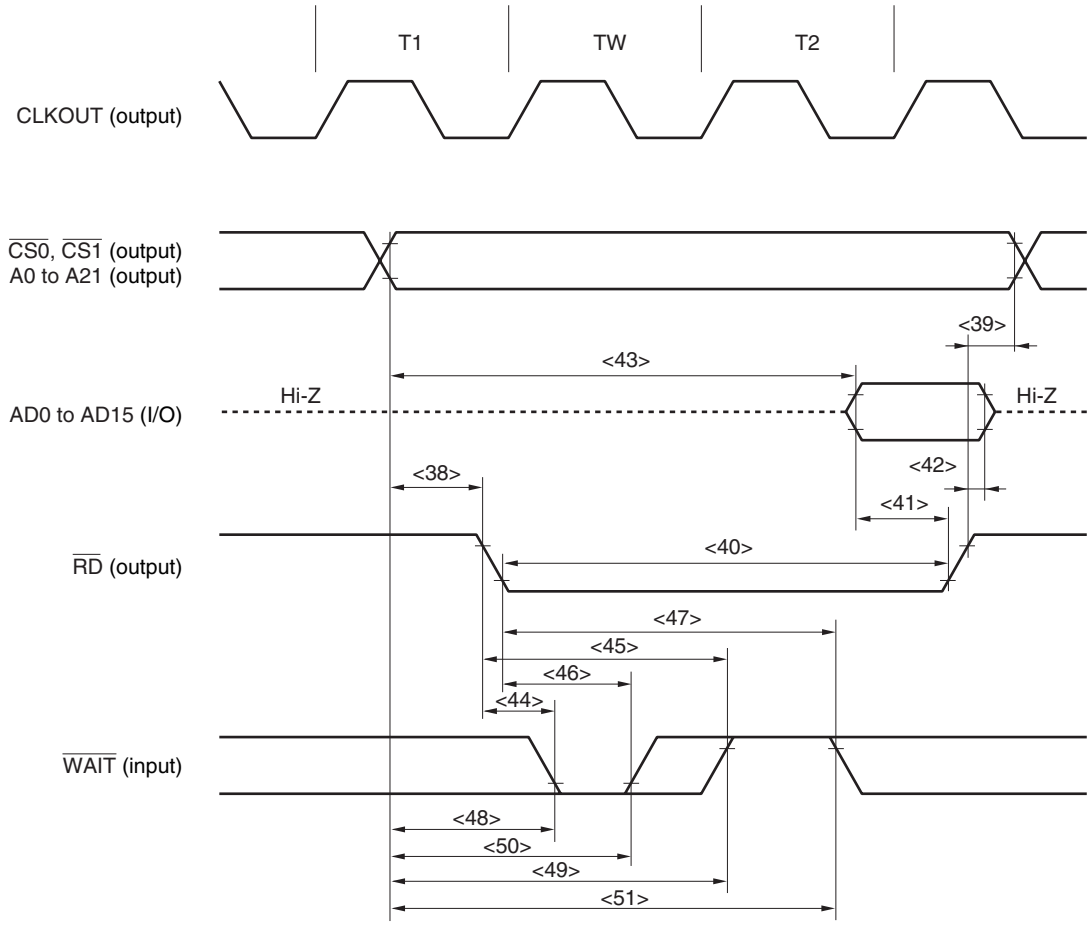
2. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

3. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

4. i: Number of idle states inserted after a read cycle (0 or 1)

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Asynchronous): In Separate Bus Mode



Remark $\overline{WR0}$ and $\overline{WR1}$ are high level.

(b) Write cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{WRm}\downarrow$)	t_{SAWR}	<52>		$(1 + t_{ASW} + t_{AHW})T - 60$		ns
Address hold time (from $\overline{WRm}\uparrow$)	t_{HAWR}	<53>		$0.5T - 10$		ns
$\overline{WRm}$ low-level width	t_{WWRL}	<54>		$(0.5 + n)T - 10$		ns
Delay time from $\overline{WRm}\downarrow$ to data output	t_{DOSDW}	<55>		–5		ns
Data setup time (to $\overline{WRm}\uparrow$)	t_{SOSDW}	<56>		$(0.5 + n)T - 20$		ns
Data hold time (from $\overline{WRm}\uparrow$)	t_{HOSDW}	<57>		$0.5T - 20$		ns
Data setup time (to address)	t_{SAOD}	<58>		$(1 + t_{ASW} + t_{AHW})T - 30$		ns
$\overline{WAIT}$ setup time (to $\overline{WRm}\downarrow$)	t_{SWRWT1}	<59>	n ≥ 1	30		ns
	t_{SWRWT2}	<60>			$nT - 30$	ns
$\overline{WAIT}$ hold time (from $\overline{WRm}\downarrow$)	t_{HWRWT1}	<61>	n ≥ 1	0		ns
	t_{HWRWT2}	<62>		nT		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<63>	n ≥ 1		$(1 + t_{ASW} + t_{AHW})T - 45$	ns
	t_{SAWT2}	<64>			$(1 + n + t_{ASW} + t_{AHW})T - 45$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<65>	n ≥ 1	$(n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}	<66>		$(1 + n + t_{ASW} + t_{AHW})T$		ns

Caution Set the following in accordance with the usage conditions of the CPU operating clock frequency (k = 0 to 3).

- **$1/f_{CPU}$ < 60 ns**
  Set an address setup wait (ASWk bit = 1).

Remarks 1. m = 0, 1

2. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

3. $T = 1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

4. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{WRm}$↓)	t_{SAWR}	<52>		$(1 + t_{ASW} + t_{AHW})T - 100$		ns
Address hold time (from $\overline{WRm}$↑)	t_{HAWR}	<53>		0.5T – 10		ns
$\overline{WRm}$ low-level width	t_{WWRL}	<54>		(0.5 + n)T – 10		ns
Delay time from $\overline{WRm}$↓ to data output	t_{DOSDW}	<55>		–5		ns
Data setup time (to $\overline{WRm}$↑)	t_{SOSDW}	<56>		(0.5 + n)T – 35		ns
Data hold time (from $\overline{WRm}$↑)	t_{HOSDW}	<57>		0.5T – 35		ns
Data setup time (to address)	t_{SAOD}	<58>		$(1 + t_{ASW} + t_{AHW})T - 55$		ns
$\overline{WAIT}$ setup time (to $\overline{WRm}$↓)	t_{SWRWT1}	<59>	n ≥ 1	50		ns
	t_{SWRWT2}	<60>			nT – 50	ns
$\overline{WAIT}$ hold time (from $\overline{WRm}$↓)	t_{HWRWT1}	<61>	n ≥ 1	0		ns
	t_{HWRWT2}	<62>		nT		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<63>	n ≥ 1		$(1 + t_{ASW} + t_{AHW})T - 100$	ns
	t_{SAWT2}	<64>			$(1 + n + t_{ASW} + t_{AHW})T - 100$	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<65>	n ≥ 1	$(n + t_{ASW} + t_{AHW})T$		ns
	t_{HAWT2}	<66>		$(1 + n + t_{ASW} + t_{AHW})T$		ns

Caution Set the following in accordance with the usage conditions of the CPU operating clock frequency (k = 0 to 3).

- **$1/f_{CPU}$ < 100 ns**

  Set an address setup wait (ASWk bit = 1).

Remarks 1. m = 0, 1

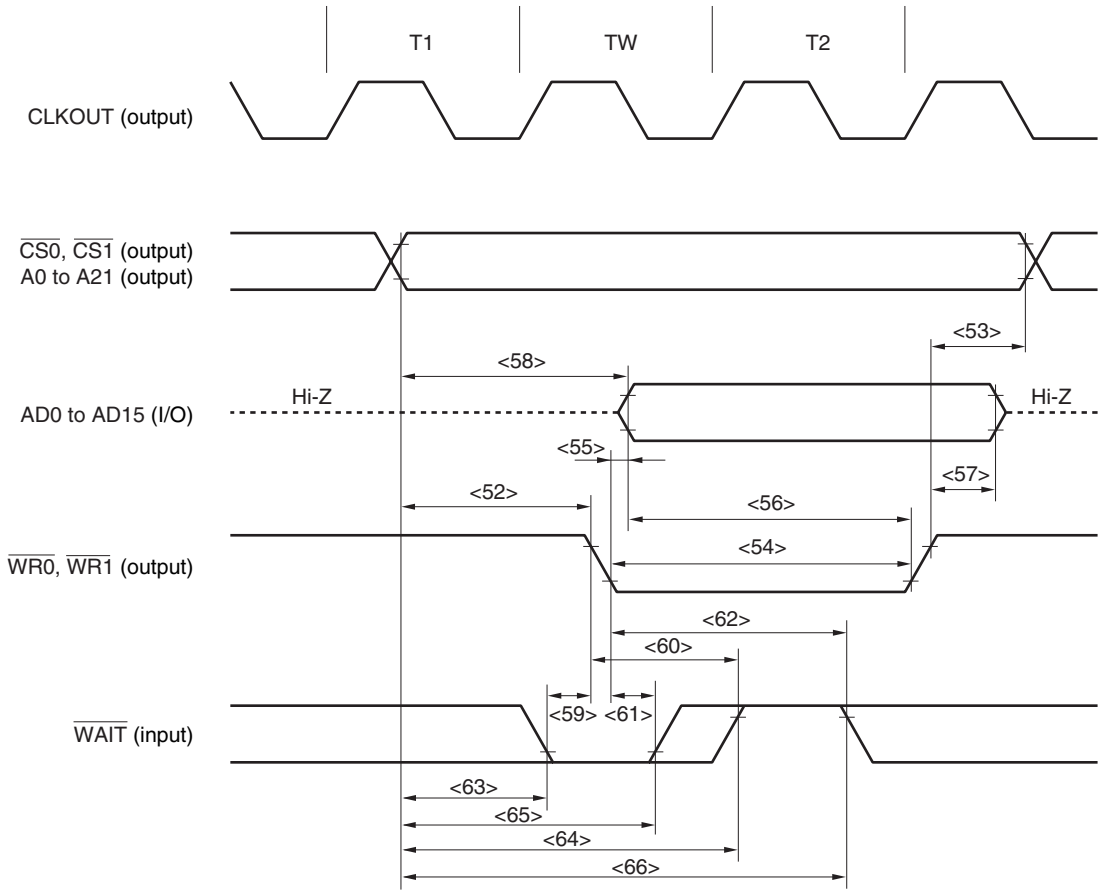
2. t_{ASW}: Number of address setup wait clocks (0 or 1)
t_{AHW}: Number of address hold wait clocks (0 or 1)

3. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

4. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Write Cycle (CLKOUT Asynchronous): In Separate Bus Mode



Remark RD is high level.

(c) Read cycle (CLKOUT synchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<67>		0	35	ns
Data input setup time (to CLKOUT↑)	t_{SISDK}	<68>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKISD}	<69>		0		ns
Delay time from CLKOUT↓↑ to $\overline{RD}$	t_{DKSR}	<70>		0	6	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<71>		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<72>		0		ns

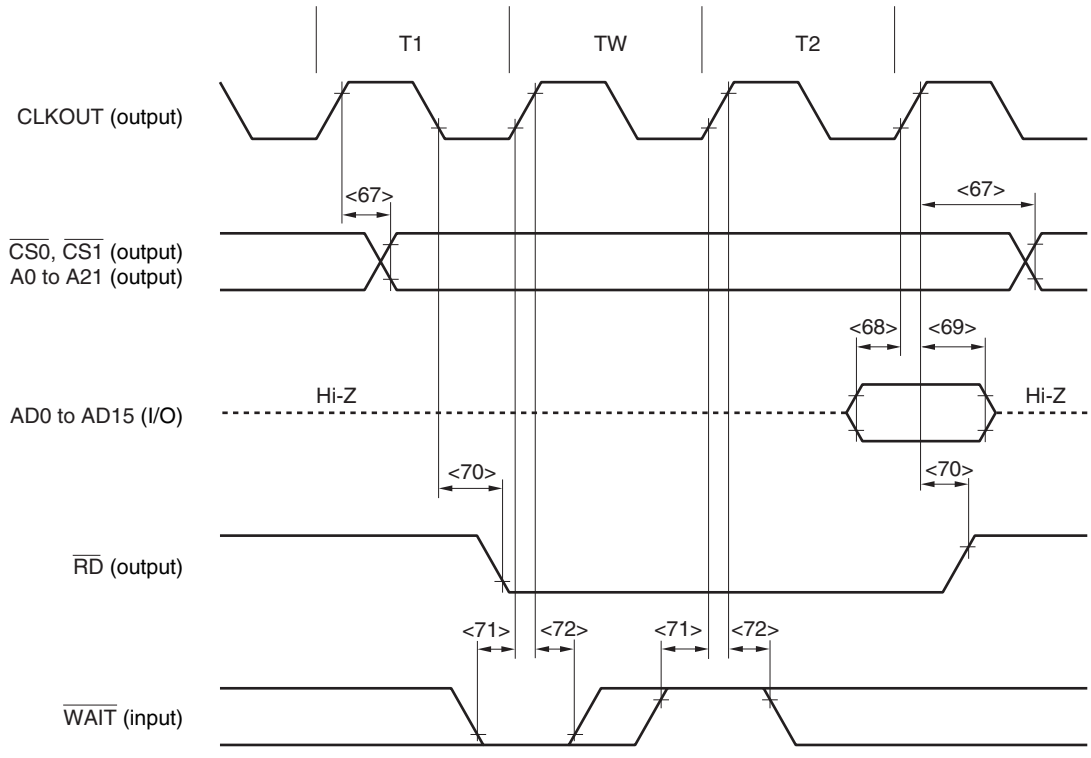
Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<67>		0	65	ns
Data input setup time (to CLKOUT↑)	t_{SISDK}	<68>		30		ns
Data input hold time (from CLKOUT↑)	t_{HKISD}	<69>		0		ns
Delay time from CLKOUT↓↑ to $\overline{RD}$	t_{DKSR}	<70>		0	10	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<71>		40		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<72>		0		ns

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Synchronous, 1 Wait): In Separate Bus Mode



Remark WR0 and WR1 are high level.

(d) Write cycle (CLKOUT synchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<73>		0	35	ns
Data output delay time from CLKOUT↑	t_{DKSD}	<74>		0	10	ns
Delay time from CLKOUT↑↓ to $\overline{WRm}$	t_{DKSW}	<75>		0	10	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<76>		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<77>		0		ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

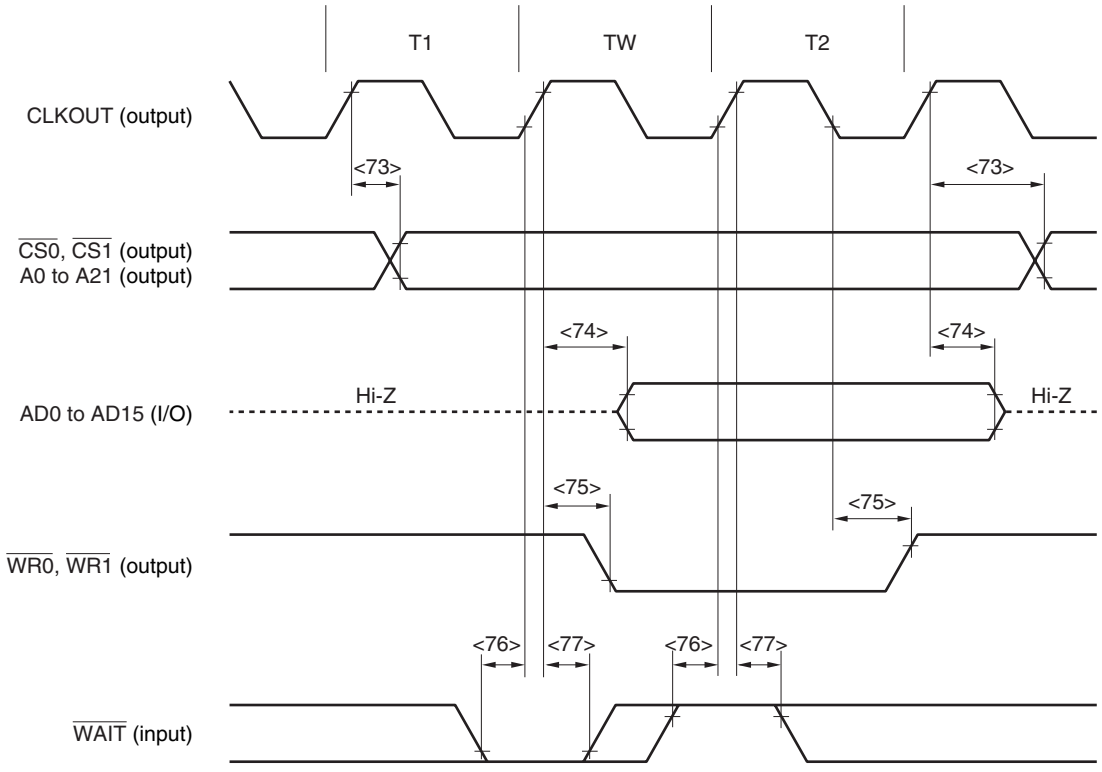
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<73>		0	65	ns
Data output delay time from CLKOUT↑	t_{DKSD}	<74>		0	15	ns
Delay time from CLKOUT↑↓ to $\overline{WRm}$	t_{DKSW}	<75>		0	15	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<76>		40		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<77>		0		ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Write Cycle (CLKOUT Synchronous): In Separate Bus Mode



Remark RD is high level.

(3) Bus hold

(a) CLKOUT asynchronous

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ high-level width	t_{WHQH}	<78>		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	t_{WHAL}	<79>		T – 15		ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	t_{DHAC}	<80>		–40		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	t_{DHQHA1}	<81>			(2n + 7.5)T + 40	ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	t_{DHQHA2}	<82>		0.5T	1.5T + 40	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

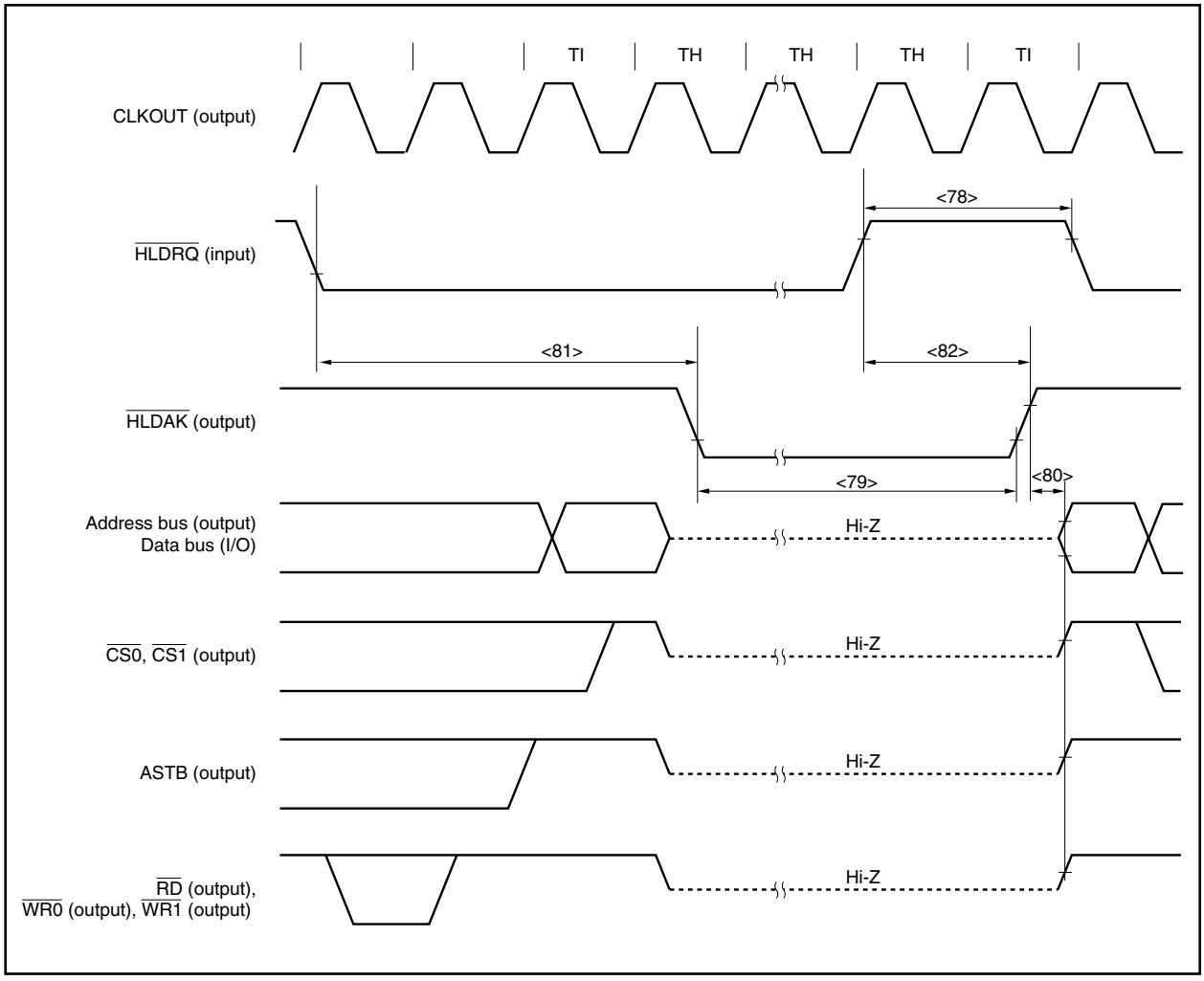
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ high-level width	t_{WHQH}	<78>		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	t_{WHAL}	<79>		T – 15		ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	t_{DHAC}	<80>		–80		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	t_{DHQHA1}	<81>			(2n + 7.5)T + 70	ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	t_{DHQHA2}	<82>		0.5T	1.5T + 70	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Bus Hold (CLKOUT Asynchronous)



(b) CLKOUT synchronous

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT↓)	t_{SHQK}	<83>		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↓)	t_{HKHQ}	<84>		0		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<85>			20	ns
Delay time from CLKOUT↑ to $\overline{\text{HLDAK}}$	t_{DKHA}	<86>			20	ns

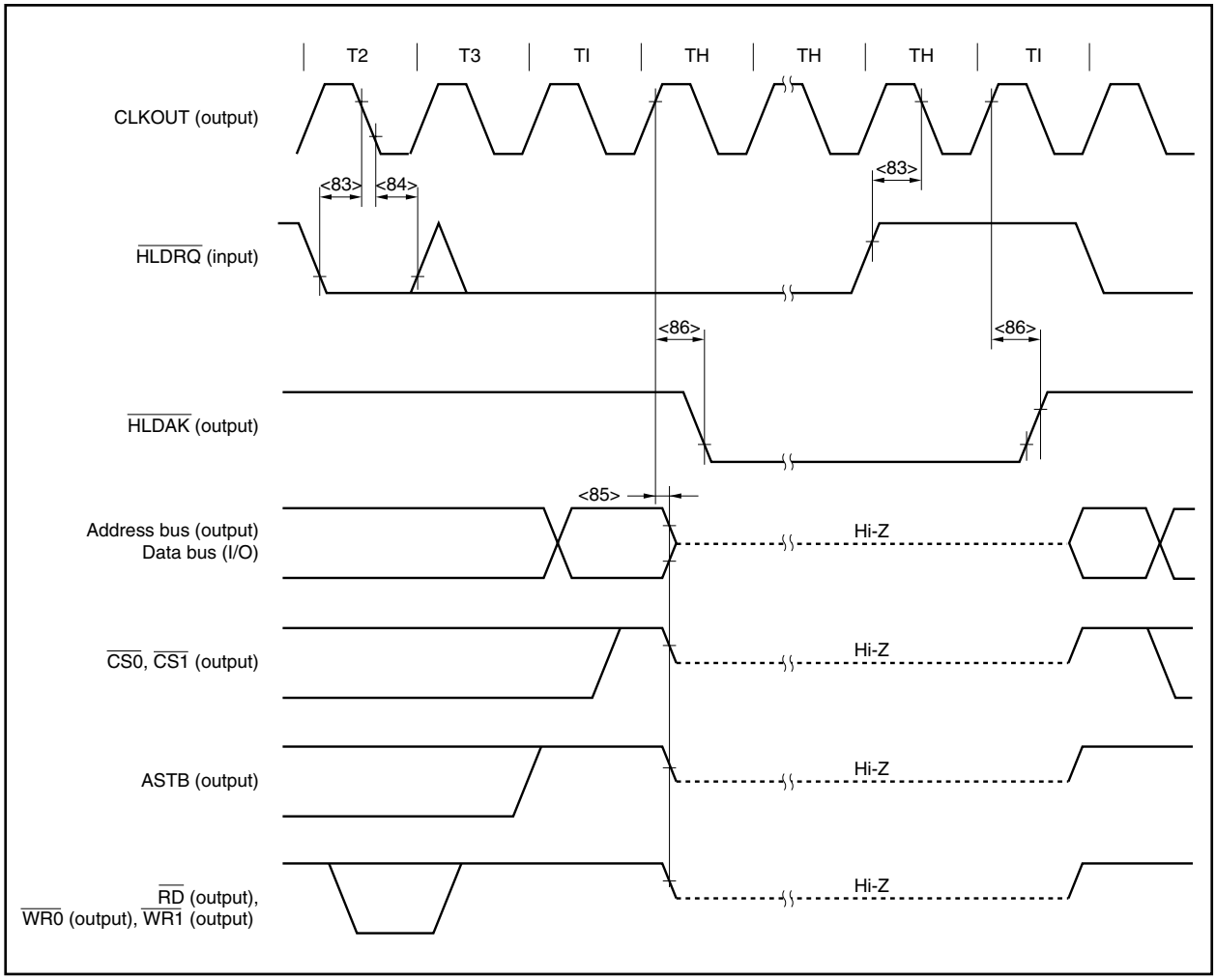
Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT↓)	t_{SHQK}	<83>		25		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↓)	t_{HKHQ}	<84>		0		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<85>			40	ns
Delay time from CLKOUT↑ to $\overline{\text{HLDAK}}$	t_{DKHA}	<86>			40	ns

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Bus Hold (CLKOUT Synchronous)



Basic Operation

(1) Reset/external interrupt timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

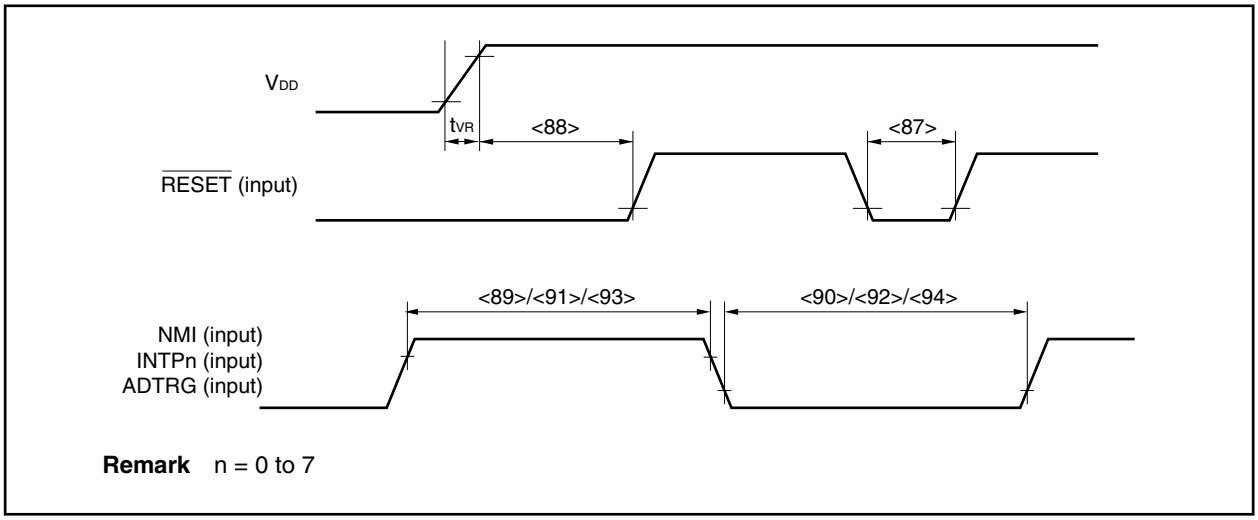
Parameter	Symbol		Conditions		MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL1}	<87>	Reset in power-on status		2		μs
	t_{WRSL2}	<88>	Power-on reset when REGC = V_{DD}		2		μs
			Note	t_{VR} > 150 μs	10		μs
				t_{VR} ≤ 150 μs	40		μs
NMI high-level width	t_{WNIH}	<89>	Analog noise elimination		1		μs
NMI low-level width	t_{WNIL}	<90>	Analog noise elimination		1		μs
INTPn high-level width	t_{WITH}	<91>	n = 0 to 7 (analog noise elimination)		600		ns
			n = 3 (when digital noise elimination selected)		Ni × t_{ISMP} + 200		ns
INTPn low-level width	t_{WITL}	<92>	n = 0 to 7 (analog noise elimination)		600		ns
			n = 3 (when digital noise elimination selected)		Ni × t_{ISMP} + 200		ns
ADTRG high-level width	t_{WADH}	<93>	REGC = V_{DD} = 4.0 to 5.5 V		T + 50		ns
			V_{DD} = 4.0 to 5.5 V, REGC = 10 μF		T + 100		ns
			REGC = V_{DD} = 2.7 to 5.5 V		T + 100		ns
ADTRG low-level width	t_{WADL}	<94>	REGC = V_{DD} = 4.0 to 5.5 V		T + 50		ns
			V_{DD} = 4.0 to 5.5 V, REGC = 10 μF		T + 100		ns
			REGC = V_{DD} = 2.7 to 5.5 V		T + 100		ns

Note Power-on reset when REGC = 10 μF

Remarks 1. t_{VR}: Time required for V_{DD} to rise from 0 V to 4.0 V (= operation lower-limit voltage)
Ni: Number of samplings set with the NFC.NFSTS bit
t_{ISMP}: Digital noise elimination sampling clock cycle of INTP3 pin
T: A/D base clock cycle (f_{AD})

2. The above specification shows the pulse width that is accurately detected as a valid edge. If a pulse narrower than the above specification is input, therefore, it may also be detected as a valid edge.

Reset/Interrupt



Remark n = 0 to 7

Timer Timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI0n high-level width	t_{TI0H}	<95>	REGC = V_{DD} = 4.5 to 5.5 V	$2T_{smp0}$ + 100 Note 1		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	$2T_{smp0}$ + 200 Note 1		ns
TI0n low-level width	t_{TI0L}	<96>	REGC = V_{DD} = 4.5 to 5.5 V	$2T_{smp0}$ + 100 Note 1		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	$2T_{smp0}$ + 200 Note 1		ns
TI5m high-level width	t_{TI5H}	<97>	REGC = V_{DD} = 4.5 to 5.5 V	50		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns
TI5m low-level width	t_{TI5L}	<98>	REGC = V_{DD} = 4.5 to 5.5 V	50		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns
TIP0m high-level width	t_{TIPH}	<99>	REGC = V_{DD} = 4.5 to 5.5 V	np × T_{smpp} + 100 Note 2		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	np × T_{smpp} + 200 Note 2		ns
TIP0m low-level width	t_{TIPL}	<100>	REGC = V_{DD} = 4.5 to 5.5 V	np × T_{smpp} + 100 Note 2		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	np × T_{smpp} + 200 Note 2		ns

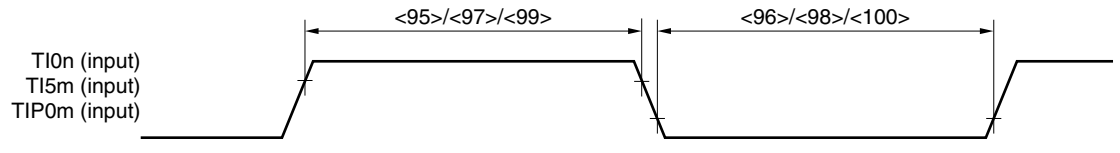
Notes 1. T_{smp0}: Timer 0 count clock cycle
However, T_{smp0} = 4/fxx when TI0n is used as an external clock.

2. np: Number of sampling clocks set by the PmNFC.PmNFSTS bit
T_{smpp}: Digital noise elimination sampling clock cycle of TIP0m pin
If TIP00 is used as an external clock or an external clear, however, T_{smpp} = 0 (digital noise is not eliminated).

Remarks 1. n = 00, 01, 10, 11, 20, 21, 30, 31
m = 0, 1

2. The above specification shows the pulse width that is accurately detected as a valid edge. If a pulse narrower than the above specification is input, therefore, it may also be detected as a valid edge.

Timer Input Timing



Remark n = 00, 01, 10, 11, 20, 21, 30, 31
m = 0, 1

UART Timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmit rate				312.5	kbps
ASCK0 frequency		REGC = V_{DD} = 4.5 to 5.5 V		12	MHz
		REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		6	MHz

CSI0 Timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY1}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH1}, t_{KL1}	<102>		t_{KCY1}/2 – 30		ns
SI0n setup time (to $\overline{SCK0n}$)	t_{SIK1}	<103>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	50		ns
SI0n hold time (from $\overline{SCK0n}$)	t_{KSI1}	<104>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	50		ns
Delay time from $\overline{SCK0n}$ to SO0n output	t_{KSO1}	<105>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		60	ns

Remark n = 0, 1

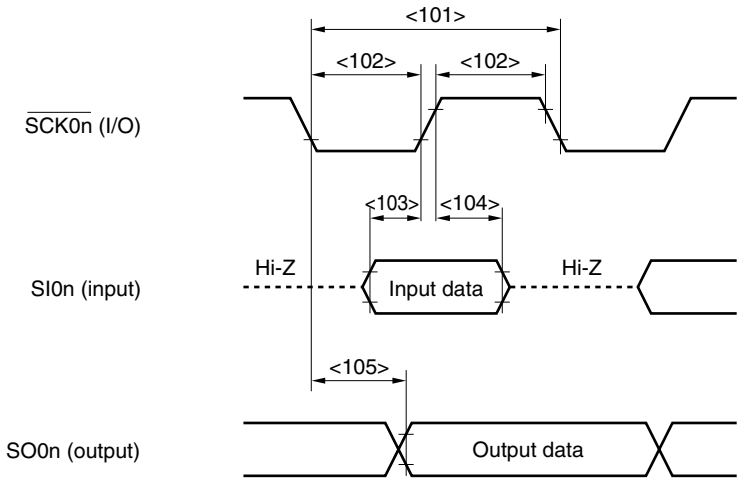
(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

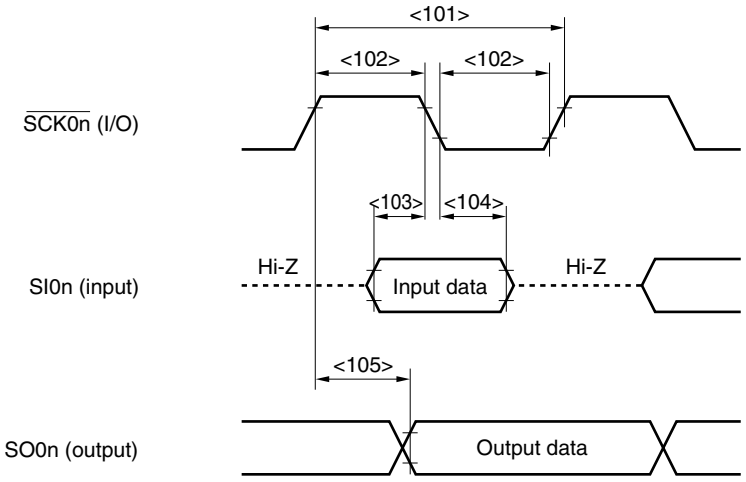
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY2}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH2}, t_{KL2}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	45		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	90		ns
SI0n setup time (to $\overline{SCK0n}$)	t_{SIK2}	<103>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
SI0n hold time (from $\overline{SCK0n}$)	t_{KSI2}	<104>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
Delay time from $\overline{SCK0n}$ to SO0n output	t_{KSO2}	<105>	REGC = V_{DD} = 4.0 to 5.5 V		50	ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		100	ns

Remark n = 0, 1

(a) CSICn.CKPn, DAPn bits = 00 or 11



(b) CSICn.CKPn, DAPn bits = 01 or 10



Remark n = 0, 1

CSIA Timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY3}	<106>	REGC = V_{DD} = 4.0 to 5.5 V	500		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	1000		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH3}, t_{KL3}	<107>		$t_{KCY3}/2 - 30$		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK3}	<108>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI3}	<109>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO3}	<110>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		60	ns

Remark n = 0, 1

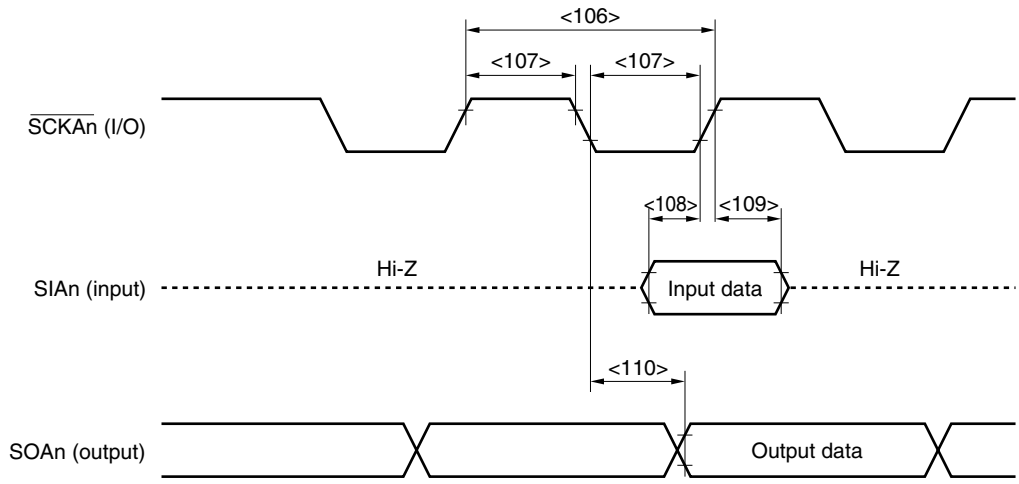
(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY4}	<106>	REGC = V_{DD} = 4.0 to 5.5 V	840		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	1700		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH4}, t_{KL4}	<107>		$t_{KCY4}/2 - 30$		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK4}	<108>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI4}	<109>	REGC = V_{DD} = 4.0 to 5.5 V	$t_{CY} \times 2 + 15$ Note		ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	$t_{CY} \times 2 + 30$ Note		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO4}	<110>	REGC = V_{DD} = 4.0 to 5.5 V		$t_{CY} \times 2 + 30$ Note	ns
			REGC = 10 μF, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		$t_{CY} \times 2 + 60$ Note	ns

Note t_{CY}: f_{SCKA} cycle

Remark n = 0, 1


<106>
<107>
<107>
SCKAn (I/O)
<108>
<109>
Hi-Z
SIAn (input)
Input data
Hi-Z
<110>
SOAn (output)
Output data

Remark n = 0, 1

I^2C Bus Mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<111>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<112>	4.0	–	0.6	–	μs
SCL0 clock low-level width		t_{LOW}	<113>	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	<114>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<115>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<116>	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<117>	250	–	100[Note 4]	–	ns
SDA0 and SCL0 signal rise time		t_R	<118>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	<119>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<120>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<121>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA0 signal (at $V_{IHmin.}$ of SCL0 signal) in order to occupy the undefined area at the falling edge of SCL0.

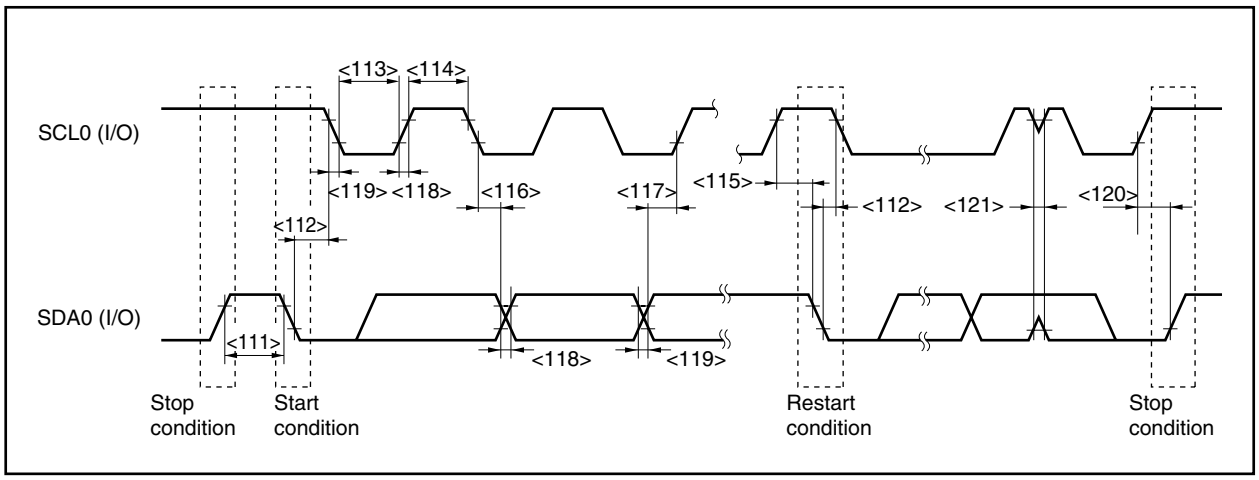
3. If the system does not extend the SCL0 signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCL0 signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL0 signal's low state hold time:
  Transmit the following data bit to the SDA0 line prior to the SCL0 line release ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

I^2C Bus Mode


SCL0 (I/O)
SDA0 (I/O)
<113>
<114>
<119>
<118>
<116>
<117>
<115>
<112>
<121>
<120>
<111>
Stop condition
Start condition
Restart condition
Stop condition

A/D Converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10	10	10	bit
Overall error[Note 1]	AINL	4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.2	±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V			±0.3	±0.6	%FSR
Conversion time	t_{CONV}	4.5 ≤ AV_{REF0} ≤ 5.5 V	High-speed mode	3.0		100	μs
			Normal mode	14.0		100	μs
		4.0 ≤ AV_{REF0} ≤ 4.5 V	High-speed mode	4.8		100	μs
			Normal mode	14.0		100	μs
		2.85 ≤ AV_{REF0} ≤ 4.0 V	High-speed mode	6.0		100	μs
			Normal mode	17.0		100	μs
		2.7 ≤ AV_{REF0} ≤ 2.85 V	High-speed mode	14.0		100	μs
			Normal mode	17.0		100	μs
Zero-scale error[Note 1]	Ezs	4.0 ≤ AV_{REF0} ≤ 5.5 V				±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V				±0.6	%FSR
Full-scale error[Note 1]	Efs	4.0 ≤ AV_{REF0} ≤ 5.5 V				±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V				±0.6	%FSR
Non-linearity error[Note 2]	ILE	4.0 ≤ AV_{REF0} ≤ 5.5 V				±2.5	LSB
		2.7 ≤ AV_{REF0} ≤ 4.0 V				±4.5	LSB
Differential linearity error[Note 2]	DLE	4.0 ≤ AV_{REF0} ≤ 5.5 V				±1.5	LSB
		2.7 ≤ AV_{REF0} ≤ 4.0 V				±2.0	LSB
Analog input voltage	V_{IAN}			0		AV_{REF0}	V
AV_{REF0} current	IA_{REF0}	When using A/D converter			1.3	2.5	mA
		When not using A/D converter[Note 3]			1.0	10	μA

Notes 1. Excluding quantization error (±0.05 %FSR).

2. Excluding quantization error (±0.5 LSB).

3. ADM.ADCS bit = 0, ADM.ADCS2 bit = 0

Remark LSB: Least Significant Bit
FSR: Full Scale Range

D/A Converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error[Notes 1, 2]		Load condition = 2 MΩ				1.2	%FSR
		Load condition = 4 MΩ				0.8	%FSR
		Load condition = 10 MΩ				0.6	%FSR
Settling time[Note 2]		C = 30 pF	V_{DD} = 4.5 to 5.5 V			10	μs
			V_{DD} = 2.7 to 4.5 V			15	μs
Output resistance[Note 3]	R_O	Output data: DACSn register = 55H			8		kΩ
AV_{REF1} current[Note 4]	IAV_{REF1}	During D/A conversion			1.5	3.0	mA
		When D/A conversion stopped			1.0	10	μA

Notes 1. Excluding quantization error (±0.2 %FSR).

2. R is the D/A converter output pin load resistance, and C is the D/A converter output pin load capacitance.

3. Value of 1 channel of D/A converter

4. Value of 2 channels of D/A converter

Remark n = 0, 1

Flash Memory Programming Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Programming operation frequency		REGC = V_{DD} = 4.5 to 5.5 V	2		20	MHz
		REGC = V_{DD} = 4.0 to 5.5 V	2		16	MHz
		REGC = 10 μF, V_{DD} = 4.0 to 5.5 V	2		16	MHz
		REGC = V_{DD} = 2.7 to 5.5 V	2		10	MHz
Supply voltage	V_{DD}		2.7		5.5	V
Number of rewrites	C_{ERWR}	**Note 1**	100			Times
Programming temperature	t_{PRG}	**Note 2**	–40		+85	°C

Notes 1. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

Shipped product ——→P→E→P→E→P: 3 rewrites

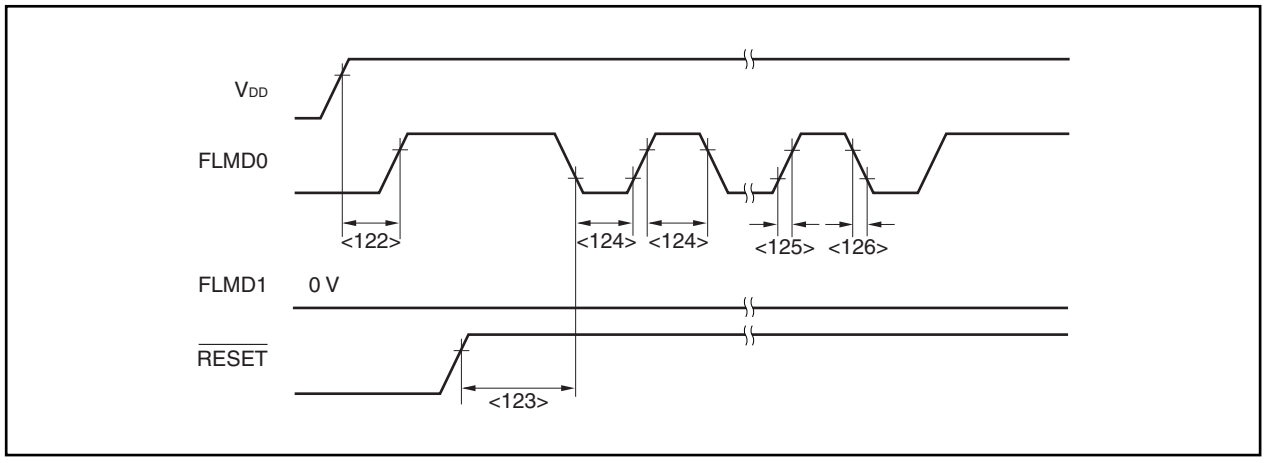
Shipped product → E→P→E→P→E→P: 3 rewrites

2. These values may change after evaluation.

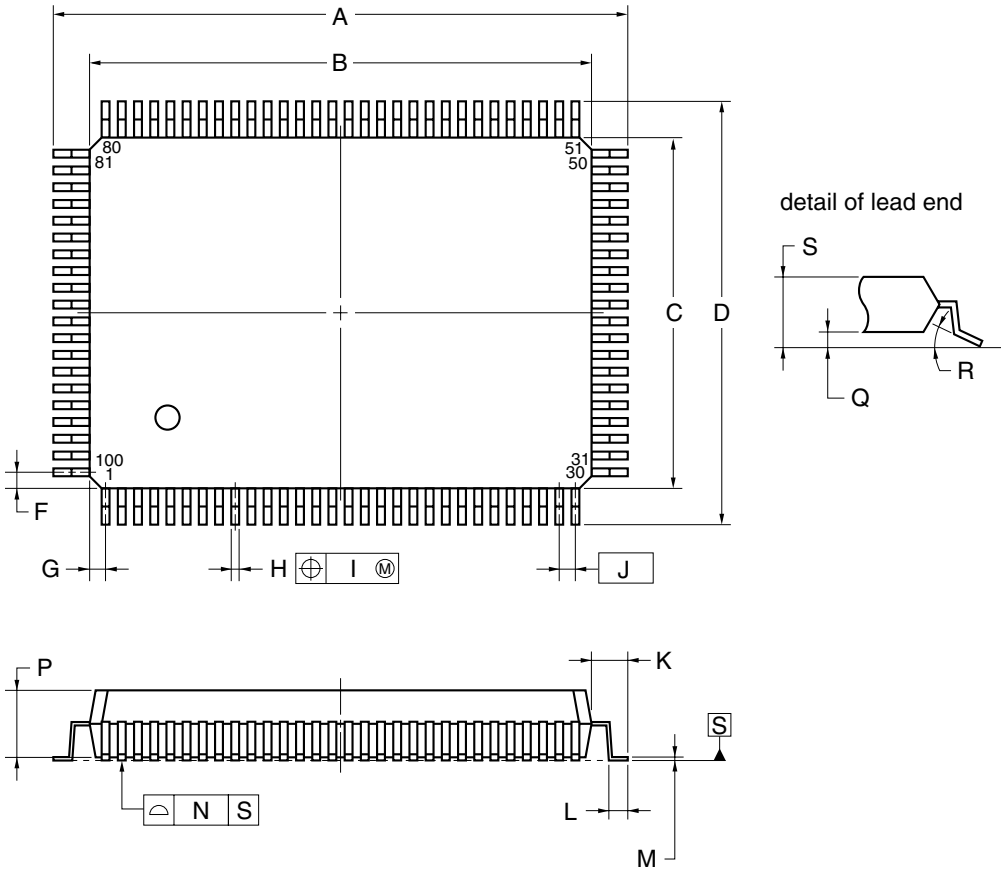
(2) Serial write operation characteristics

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Setup time from V_{DD}↑ to FLMD0↑	t_{DP}	<122>		10 ms		3 s	
Time from $\overline{\text{RESET}}$↑ to FLMD0 pulse input start	t_{RP}	<123>		66611.2/f_X			s
FLMD0 pulse high-/low-level width	t_{PW}	<124>		10		100	μs
FLMD0 pulse rise time	t_R	<125>				50	ns
FLMD0 pulse fall time	t_F	<126>				50	ns

Serial Write Operation Timing



100-PIN PLASTIC QFP (14x20)



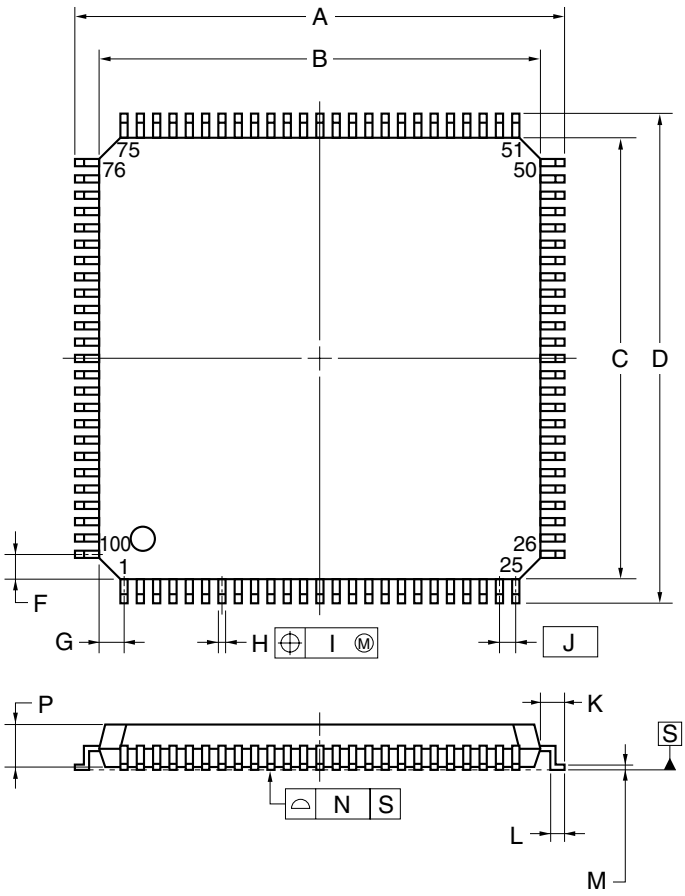
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

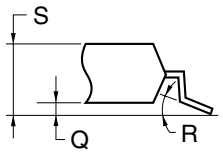
ITEM	MILLIMETERS
A	23.2±0.2
B	20.0±0.2
C	14.0±0.2
D	17.2±0.2
F	0.825
G	0.575
H	$0.32^{+0.08}_{-0.07}$
I	0.13
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.

S100GF-65-JBT-2

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

APPENDIX A INSTRUCTION SET LIST

A.1 Conventions

(1) Register symbols used to describe operands

Register Symbol	Explanation
reg1	General-purpose registers: Used as source registers.
reg2	General-purpose registers: Used mainly as destination registers. Also used as source register in some instructions.
reg3	General-purpose registers: Used mainly to store the remainders of division results and the higher 32 bits of multiplication results.
bit#3	3-bit data for specifying the bit number
immX	X bit immediate data
dispX	X bit displacement data
regID	System register number
vector	5-bit data that specifies the trap vector (00H to 1FH)
cccc	4-bit data that shows the condition codes
sp	Stack pointer (r3)
ep	Element pointer (r30)
listX	X item register list

(2) Register symbols used to describe opcodes

Register Symbol	Explanation
R	1-bit data of a code that specifies reg1 or regID
r	1-bit data of the code that specifies reg2
w	1-bit data of the code that specifies reg3
d	1-bit displacement data
I	1-bit immediate data (indicates the higher bits of immediate data)
i	1-bit immediate data
cccc	4-bit data that shows the condition codes
CCCC	4-bit data that shows the condition codes of Bcond instruction
bbb	3-bit data for specifying the bit number
L	1-bit data that specifies a program register in the register list

(3) Register symbols used in operations

Register Symbol	Explanation
←	Input for
GR [ ]	General-purpose register
SR [ ]	System register
zero-extend (n)	Expand n with zeros until word length.
sign-extend (n)	Expand n with signs until word length.
load-memory (a, b)	Read size b data from address a.
store-memory (a, b, c)	Write data b into address a in size c.
load-memory-bit (a, b)	Read bit b of address a.
store-memory-bit (a, b, c)	Write c to bit b of address a.
saturated (n)	Execute saturated processing of n (n is a 2's complement). If, as a result of calculations, n ≥ 7FFFFFFFH, let it be 7FFFFFFFH. n ≤ 80000000H, let it be 80000000H.
result	Reflects the results in a flag.
Byte	Byte (8 bits)
Halfword	Halfword (16 bits)
Word	Word (32 bits)
+	Addition
–	Subtraction
ll	Bit concatenation
×	Multiplication
÷	Division
%	Remainder from division results
AND	Logical product
OR	Logical sum
XOR	Exclusive OR
NOT	Logical negation
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

(4) Register symbols used in execution clock

Register Symbol	Explanation
i	If executing another instruction immediately after executing the first instruction (issue).
r	If repeating execution of the same instruction immediately after executing the first instruction (repeat).
l	If using the results of instruction execution in the instruction immediately after the execution (latency).

(5) Register symbols used in flag operations

Identifier	Explanation
(Blank)	No change
0	Clear to 0
X	Set or cleared in accordance with the results.
R	Previously saved values are restored.

(6) Condition codes

Condition Code (cccc)	Condition Formula	Explanation
0 0 0 0	OV = 1	Overflow
1 0 0 0	OV = 0	No overflow
0 0 0 1	CY = 1	Carry Lower (Less than)
1 0 0 1	CY = 0	No carry Not lower (Greater than or equal)
0 0 1 0	Z = 1	Zero
1 0 1 0	Z = 0	Not zero
0 0 1 1	(CY or Z) = 1	Not higher (Less than or equal)
1 0 1 1	(CY or Z) = 0	Higher (Greater than)
0 1 0 0	S = 1	Negative
1 1 0 0	S = 0	Positive
0 1 0 1	–	Always (Unconditional)
1 1 0 1	SAT = 1	Saturated
0 1 1 0	(S xor OV) = 1	Less than signed
1 1 1 0	(S xor OV) = 0	Greater than or equal signed
0 1 1 1	((S xor OV) or Z) = 1	Less than or equal signed
1 1 1 1	((S xor OV) or Z) = 0	Greater than signed

A.2 Instruction Set (in Alphabetical Order)

(1/6)

Mnemonic	Operand	Opcode	Operation		Execution Clock			Flags				
					i	r	l	CY	OV	S	Z	SAT
ADD	reg1,reg2	rrrrr001110RRRRR	GR[reg2]←GR[reg2]+GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010010iiiii	GR[reg2]←GR[reg2]+sign-extend(imm5)		1	1	1	×	×	×	×	
ADDI	imm16,reg1,reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1	×	×	×	×	
AND	reg1,reg2	rrrrr001010RRRRR	GR[reg2]←GR[reg2]AND GR[reg1]		1	1	1		0	×	×	
ANDI	imm16,reg1,reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]AND zero-extend(imm16)		1	1	1		0	×	×	
Bcond	disp9	ddddd1011dddcccc **Note 1**	if conditions are satisfied then PC←PC+sign-extend(disp9)	When conditions are satisfied	2 Note 2	2 Note 2	2 Note 2					
				When conditions are not satisfied	1	1	1					
BSH	reg2,reg3	rrrrr11111100000 wwwww01101000010	GR[reg3]←GR[reg2] (23 : 16) ll GR[reg2] (31 : 24) ll GR[reg2] (7 : 0) ll GR[reg2] (15 : 8)		1	1	1	×	0	×	×	
BSW	reg2,reg3	rrrrr11111100000 wwwww01101000000	GR[reg3]←GR[reg2] (7 : 0) ll GR[reg2] (15 : 8) ll GR [reg2] (23 : 16) ll GR[reg2] (31 : 24)		1	1	1	×	0	×	×	
CALLT	imm6	0000001000iiiiii	CTPC←PC+2(return PC) CTPSW←PSW adr←CTBP+zero-extend(imm6 logically shift left by 1) PC←CTBP+zero-extend(Load-memory(adr,Halfword))		4	4	4					
CLR1	bit#3,disp16[reg1]	10bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,0)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100100	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,0)		3 Note 3	3 Note 3	3 Note 3				×	
CMOV	cccc,imm5,reg2,reg3	rrrrr111111iiiii wwwww011000cccc0	if conditions are satisfied then GR[reg3]←sign-extended(imm5) else GR[reg3]←GR[reg2]		1	1	1					
	cccc,reg1,reg2,reg3	rrrrr111111RRRR wwwww011001cccc0	if conditions are satisfied then GR[reg3]←GR[reg1] else GR[reg3]←GR[reg2]		1	1	1					
CMP	reg1,reg2	rrrrr001111RRRRR	result←GR[reg2]–GR[reg1]		1	1	1	×	×	×	×	
	imm5,reg2	rrrrr010011iiiii	result←GR[reg2]–sign-extend(imm5)		1	1	1	×	×	×	×	
CTRET		0000011111100000 0000000101000100	PC←CTPC PSW←CTPSW		3	3	3	R	R	R	R	R
DBRET		0000011111100000 0000000101000110	PC←DBPC PSW←DBPSW		3	3	3	R	R	R	R	R

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DBTRAP		1111100001000000	DBPC←PC+2 (restored PC) DBPSW←PSW PSW.NP←1 PSW.EP←1 PSW.ID←1 PC←00000060H	3	3	3					
DI		0000011111100000 0000000101100000	PSW.ID←1	1	1	1					
DISPOSE	imm5,list12	0000011001iiiiiL LLLLLLLLLLL00000	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	imm5,list12,[reg1]	0000011001iiiiiL LLLLLLLLLLRRRRR **Note 5**	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded PC←GR[reg1]	n+3 Note 4	n+3 Note 4	n+3 Note 4					
DIV	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000000	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVH	reg1,reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1]Note 6	35	35	35		×	×	×	
	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000000	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVHU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000010	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
DIVU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000010	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
EI		1000011111100000 0000000101100000	PSW.ID←0	1	1	1					
HALT		0000011111100000 0000000100100000	Stop	1	1	1					
HSW	reg2,reg3	rrrrr11111100000 wwwww01101000100	GR[reg3]←GR[reg2](15 : 0) ll GR[reg2] (31 : 16)	1	1	1	×	0	×	×	
JARL	disp22,reg2	rrrrr11110ddddd ddddddddddddddd0 **Note 7**	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)	2	2	2					
JMP	[reg1]	00000000011RRRRR	PC←GR[reg1]	3	3	3					
JR	disp22	0000011110ddddd ddddddddddddddd0 **Note 7**	PC←PC+sign-extend(disp22)	2	2	2					
LD.B	disp16[reg1],reg2	rrrrr111000RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 11					
LD.BU	disp16[reg1],reg2	rrrrr11110bRRRRR ddddddddddddd1 **Notes 8, 10**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 11					

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Mnemonic	Operand	Opcode	Operation		Execution Clock			Flags				
					i	r	l	CY	OV	S	Z	SAT
LD.H	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Halfword))		1	1	Note 11					
LDSR	reg2,regID	rrrrr111111RRRRR 0000000000100000 **Note 12**	SR[regID]←GR[reg2]	Other than regID = PSW	1	1	1					
				regID = PSW	1	1	1	×	×	×	×	×
LD.HU	disp16[reg1],reg2	rrrrr111111RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Halfword)		1	1	Note 11					
LD.W	disp16[reg1],reg2	rrrrr111001RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr,Word)		1	1	Note 11					
MOV	reg1,reg2	rrrrr000000RRRRR	GR[reg2]←GR[reg1]		1	1	1					
	imm5,reg2	r r r r r 0 1 0 0 0 0 i i i i i	GR[reg2]←sign-extend(imm5)		1	1	1					
	imm32,reg1	00000110001RRRRR i i i i i i i i i i i i i i i i l l l l l l l l l l l l l l l l	GR[reg1]←imm32		2	2	2					
MOVEA	imm16,reg1,reg2	rrrrr110001RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+sign-extend(imm16)		1	1	1					
MOVHI	imm16,reg1,reg2	rrrrr110010RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+(imm16 ll 0^{16})		1	1	1					
MUL	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100000 **Note 14**	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	4	5					
	imm9,reg2,reg3	r r r r r 1 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 l l l l 0 0 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xsign-extend(imm9)		1	4	5					
MULH	reg1,reg2	rrrrr000111RRRRR	GR[reg2]←GR[reg2][Note 6]xGR[reg1][Note 6]		1	1	2					
	imm5,reg2	r r r r r 0 1 0 1 1 1 i i i i i	GR[reg2]←GR[reg2][Note 6]xsign-extend(imm5)		1	1	2					
MULHI	imm16,reg1,reg2	rrrrr110111RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1][Note 6]ximm16		1	1	2					
MULU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01000100010 **Note 14**	GR[reg3] ll GR[reg2]←GR[reg2]xGR[reg1]		1	4	5					
	imm9,reg2,reg3	r r r r r 1 1 1 1 1 1 i i i i i w w w w w 0 1 0 0 1 l l l l 1 0 **Note 13**	GR[reg3] ll GR[reg2]←GR[reg2]xzero-extend(imm9)		1	4	5					
NOP		0000000000000000	Pass at least one clock cycle doing nothing.		1	1	1					
NOT	reg1,reg2	rrrrr000001RRRRR	GR[reg2]←NOT(GR[reg1])		1	1	1		0	×	×	
NOT1	bit#3,disp16[reg1]	01bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100010	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,Z flag)		3 Note 3	3 Note 3	3 Note 3				×	

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
OR	reg1,reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16,reg1,reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)	1	1	1		0	×	×	
PREPARE	list12,imm5	0000011110iiiiiL LLLLLLLLLLL00001	Store-memory(sp–4,GR[reg in list12],Word) sp←sp–4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5)	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	list12,imm5, sp/imm Note 15	0000011110iiiiiL LLLLLLLLLLLff011 imm16/imm32 **Note 16**	Store-memory(sp–4,GR[reg in list12],Word) sp←sp+4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend (imm5) ep←sp/imm	n+2 Note 4 Note 17	n+2 Note 4 Note 17	n+2 Note 4 Note 17					
RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP=1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	3	3	3	R	R	R	R	R
SAR	reg1,reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr01010 1iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SASF	cccc,reg2	rrrrr1111110cccc 0000001000000000	if conditions are satisfied then GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000001H else GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000000H	1	1	1					
SATADD	reg1,reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	×	×	×	×	×
	imm5,reg2	rrrrr01000 1iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5))	1	1	1	×	×	×	×	×
SATSUB	reg1,reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16,reg1,reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16))	1	1	1	×	×	×	×	×
SATSUBR	reg1,reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc,reg2	rrrrr1111110cccc 0000000000000000	If conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 18**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 18, 20**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					

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Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	00000000010RRRRR	adr←(PC+2) + (GR [reg1] logically shift left by 1) PC←(PC+2) + (sign-extend (Load-memory (adr,Halfword)) logically shift left by 1	5	5	5					
SXB	reg1	00000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0))	1	1	1					
SXH	reg1	00000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	0 0 0 0 0 1 1 1 1 1 1 iiiii 0000000100000000	EIPC ←PC+4 (Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit (adr,bit#3))	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not (Load-memory-bit (adr,reg2))	3 Note 3	3 Note 3	3 Note 3				×	
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	00000000100RRRRR	GR[reg1]←zero-extend (GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	00000000110RRRRR	GR[reg1]←zero-extend (GR[reg1] (15 : 0))	1	1	1					

Notes 1. ddddddddd: Higher 8 bits of disp9.

2. 3 if there is an instruction that rewrites the contents of the PSW immediately before.

3. If there is no wait state (3 + the number of read access wait states).

4. n is the total number of list12 load registers. (According to the number of wait states. Also, if there are no wait states, n is the total number of list12 registers. If n = 0, same operation as when n = 1)

5. RRRRR: other than 00000.

6. The lower halfword data only are valid.

7. ddddddddddddddddddddd: The higher 21 bits of disp22.

8. ddddddddddddddd: The higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states).

10. b: bit 0 of disp16.

11. According to the number of wait states (2 if there are no wait states).

Notes 12. In this instruction, for convenience of mnemonic description, the source register is made reg2, but the reg1 field is used in the opcode. Therefore, the meaning of register specification in the mnemonic description and in the opcode differs from other instructions.

rrrrr = regID specification

RRRRR = reg2 specification

13. iiiii: Lower 5 bits of imm9.

IIII: Higher 4 bits of imm9.

14. Do not specify the same register for general-purpose registers reg1 and reg3.

15. sp/imm: specified by bits 19 and 20 of the sub-opcode.

16. ff = 00: Load sp in ep.

01: Load sign expanded 16-bit immediate data (bits 47 to 32) in ep.

10: Load 16-bit logically left shifted 16-bit immediate data (bits 47 to 32) in ep.

11: Load 32-bit immediate data (bits 63 to 32) in ep.

17. If imm = imm32, n + 3 clocks.

18. rrrrr: Other than 00000.

19. ddddddd: Higher 7 bits of disp8.

20. dddd: Higher 4 bits of disp5.

21. dddddd: Higher 6 bits of disp8.

APPENDIX B REGISTER INDEX

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Symbol	Name	Unit	Page
ADCR	A/D conversion result register	ADC	439
ADCRH	A/D conversion result register H	ADC	439
ADIC	Interrupt control register	INTC	670
ADM	A/D converter mode register	ADC	435
ADS	Analog input channel specification register	ADC	438
ADTC0	Automatic data transfer address count register 0	CSIA	525
ADTC1	Automatic data transfer address count register 1	CSIA	525
ADTI0	Automatic data transfer interval specification register 0	CSIA	531
ADTI1	Automatic data transfer interval specification register 1	CSIA	531
ADTP0	Automatic data transfer address point specification register 0	CSIA	529
ADTP1	Automatic data transfer address point specification register 1	CSIA	529
ASIF0	Asynchronous serial interface transmit status register 0	UART	471
ASIF1	Asynchronous serial interface transmit status register 1	UART	471
ASIF2	Asynchronous serial interface transmit status register 2	UART	471
ASIM0	Asynchronous serial interface mode register 0	UART	468
ASIM1	Asynchronous serial interface mode register 1	UART	468
ASIM2	Asynchronous serial interface mode register 2	UART	468
ASIS0	Asynchronous serial interface status register 0	UART	470
ASIS1	Asynchronous serial interface status register 1	UART	470
ASIS2	Asynchronous serial interface status register 2	UART	470
AWC	Address wait control register	BCU	176
BCC	Bus cycle control register	BCU	177
BRGC0	Baud rate generator control register 0	UART	489
BRGC1	Baud rate generator control register 1	UART	489
BRGC2	Baud rate generator control register 2	UART	489
BRGCA0	Divisor selection register 0	CSIA	529
BRGCA1	Divisor selection register 1	CSIA	529
BRGIC	Interrupt control register	INTC	670
BSC	Bus size configuration register	BCU	165
CKSR0	Clock select register 0	UART	488
CKSR1	Clock select register 1	UART	488
CKSR2	Clock select register 2	UART	488
CMP00	8-bit timer H compare register 00	TMH	380
CMP01	8-bit timer H compare register 01	TMH	381
CMP10	8-bit timer H compare register 10	TMH	380
CMP11	8-bit timer H compare register 11	TMH	381
CR000	16-bit timer capture/compare register 000	TM0	288
CR001	16-bit timer capture/compare register 001	TM0	289
CR010	16-bit timer capture/compare register 010	TM0	288
CR011	16-bit timer capture/compare register 011	TM0	289
CR020	16-bit timer capture/compare register 020	TM0	288
CR021	16-bit timer capture/compare register 021	TM0	289

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Symbol	Name	Unit	Page
CR030	16-bit timer capture/compare register 030	TM0	288
CR031	16-bit timer capture/compare register 031	TM0	289
CR5	16-bit timer compare register 5	TM5	362
CR50	8-bit timer compare register 50	TM5	362
CR51	8-bit timer compare register 51	TM5	362
CRC00	Capture/compare control register 00	TM0	294
CRC01	Capture/compare control register 01	TM0	294
CRC02	Capture/compare control register 02	TM0	294
CRC03	Capture/compare control register 03	TM0	294
CSI0IC0	Interrupt control register	INTC	670
CSI0IC1	Interrupt control register	INTC	670
CSIA0B0	CSIA0 buffer RAMn (n = 0 to F)	CSIA	531
CSIA0B0H	CSIA0 buffer RAMnH (n = 0 to F)	CSIA	531
CSIA0B0L	CSIA0 buffer RAMnL (n = 0 to F)	CSIA	531
CSIA1B0	CSIA1 buffer RAMn (n = 0 to F)	CSIA	531
CSIA1B0H	CSIA1 buffer RAMnH (n = 0 to F)	CSIA	531
CSIA1B0L	CSIA1 buffer RAMnL (n = 0 to F)	CSIA	531
CSIAIC0	Interrupt control register	INTC	670
CSIAIC1	Interrupt control register	INTC	670
CSIC0	Clocked serial interface clock selection register 0	CSI0	501
CSIC1	Clocked serial interface clock selection register 1	CSI0	501
CSIM00	Clocked serial interface mode register 00	CSI0	499
CSIM01	Clocked serial interface mode register 01	CSI0	499
CSIMA0	Serial operation mode specification register 0	CSIA	526
CSIMA1	Serial operation mode specification register 1	CSIA	526
CSIS0	Serial status register 0	CSIA	527
CSIS1	Serial status register 1	CSIA	527
CSIT0	Serial trigger register 0	CSIA	528
CSIT1	Serial trigger register 1	CSIA	528
CTBP	CALLT base pointer	CPU	50
CTPC	CALLT execution status saving register	CPU	49
CTPSW	CALLT execution status saving register	CPU	49
DACS0	D/A conversion value setting register 0	DAC	461
DACS1	D/A conversion value setting register 1	DAC	461
DADC0	DMA addressing control register 0	DMA	634
DADC1	DMA addressing control register 1	DMA	634
DADC2	DMA addressing control register 2	DMA	634
DADC3	DMA addressing control register 3	DMA	634
DAM	D/A converter mode register	DAC	461
DBC0	DMA byte count register 0	DMA	633
DBC1	DMA byte count register 1	DMA	633
DBC2	DMA byte count register 2	DMA	633
DBC3	DMA byte count register 3	DMA	633
DBPC	Exception/debug trap status saving register	CPU	50

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Symbol	Name	Unit	Page
DBPSW	Exception/debug trap status saving register	CPU	50
DCHC0	DMA channel control register 0	DMA	635
DCHC1	DMA channel control register 1	DMA	635
DCHC2	DMA channel control register 2	DMA	635
DCHC3	DMA channel control register 3	DMA	635
DDA0H	DMA destination address register 0H	DMA	632
DDA0L	DMA destination address register 0L	DMA	632
DDA1H	DMA destination address register 1H	DMA	632
DDA1L	DMA destination address register 1L	DMA	632
DDA2H	DMA destination address register 2H	DMA	632
DDA2L	DMA destination address register 2L	DMA	632
DDA3H	DMA destination address register 3H	DMA	632
DDA3L	DMA destination address register 3L	DMA	632
DMAIC0	Interrupt control register	INTC	670
DMAIC1	Interrupt control register	INTC	671
DMAIC2	Interrupt control register	INTC	671
DMAIC3	Interrupt control register	INTC	671
DSA0H	DMA source address register 0H	DMA	631
DSA0L	DMA source address register 0L	DMA	631
DSA1H	DMA source address register 1H	DMA	631
DSA1L	DMA source address register 1L	DMA	631
DSA2H	DMA source address register 2H	DMA	631
DSA2L	DMA source address register 2L	DMA	631
DSA3H	DMA source address register 3H	DMA	631
DSA3L	DMA source address register 3L	DMA	631
DTFR0	DMA trigger factor register 0	DMA	636
DTFR1	DMA trigger factor register 1	DMA	636
DTFR2	DMA trigger factor register 2	DMA	636
DTFR3	DMA trigger factor register 3	DMA	636
DWC0	Data wait control register 0	BCU	173
ECR	Interrupt source register	CPU	47
EIPC	Interrupt status saving register	CPU	46
EIPSW	Interrupt status saving register	CPU	46
EXIMC	External bus interface mode control register	BCU	164
FEPC	NMI status saving register	CPU	47
FEPSW	NMI status saving register	CPU	47
IIC0	IIC shift register 0	I^2C	572
IICC0	IIC control register 0	I^2C	559
IICCL0	IIC clock selection register 0	I^2C	569
IICF0	IIC flag register 0	I^2C	567
IICIC0	Interrupt control register	INTC	670
IICS0	IIC status register 0	I^2C	564
IICX0	IIC function expansion register 0	I^2C	570
IMR0	Interrupt mask register 0	INTC	671

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Symbol	Name	Unit	Page
IMR0H	Interrupt mask register 0H	INTC	671
IMR0L	Interrupt mask register 0L	INTC	671
IMR1	Interrupt mask register 1	INTC	671
IMR1H	Interrupt mask register 1H	INTC	671
IMR1L	Interrupt mask register 1L	INTC	671
IMR2	Interrupt mask register 2	INTC	671
IMR2H	Interrupt mask register 2H	INTC	671
IMR2L	Interrupt mask register 2L	INTC	671
IMR3	Interrupt mask register 3	INTC	671
IMR3H	Interrupt mask register 3H	INTC	671
IMR3L	Interrupt mask register 3L	INTC	671
INTF0	External interrupt falling edge specification register 0	INTC	679
INTF3	External interrupt falling edge specification register 3	INTC	680
INTF9H	External interrupt falling edge specification register 9H	INTC	681
INTR0	External interrupt rising edge specification register 0	INTC	679
INTR3	External interrupt rising edge specification register 3	INTC	680
INTR9H	External interrupt rising edge specification register 9H	INTC	681
ISPR	In-service priority register	INTC	673
KRIC	Interrupt control register	INTC	670
KRM	Key return mode register	KR	694
NFC	Digital noise elimination control register	INTC	677
OSTS	Oscillation stabilization time selection register	Standby	700
P0	Port 0 register	Port	90
P0NFC	TIP00 noise elimination control register	TMP	283
P1	Port 1 register	Port	92
P1NFC	TIP01 noise elimination control register	TMP	283
P3	Port 3 register	Port	95
P3H	Port 3 register H	Port	95
P3L	Port 3 register L	Port	95
P4	Port 4 register	Port	100
P5	Port 5 register	Port	103
P7	Port 7 register	Port	106
P9	Port 9 register	Port	108
P9H	Port 9 register H	Port	108
P9L	Port 9 register L	Port	108
PC	Program counter	CPU	44
PCC	Processor clock control register	CG	191
PCM	Port CM register	Port	115
PCS	Port CS register	Port	117
PCT	Port CT register	Port	119
PDH	Port DH register	Port	121
PDL	Port DL register	Port	124
PDLH	Port DL register H	Port	124
PDLL	Port DL register L	Port	124

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Symbol	Name	Unit	Page
PF3H	Port 3 function register H	Port	97
PF4	Port 4 function register	Port	102
PF5	Port 5 function register	Port	104
PF9H	Port 9 function register H	Port	111
PFC3	Port 3 function control register	Port	97
PFC4	Port 4 function control register	Port	101
PFC5	Port 5 function control register	Port	106
PFC9	Port 9 function control register	Port	111
PFC9H	Port 9 function control register H	Port	111
PFC9L	Port 9 function control register L	Port	111
PFCE3	Port 3 function control expansion register	Port	97
PFM	Power fail comparison mode register	ADC	441
PFT	Power fail comparison threshold register	ADC	441
PIC0	Interrupt control register	INTC	670
PIC1	Interrupt control register	INTC	670
PIC2	Interrupt control register	INTC	670
PIC3	Interrupt control register	INTC	670
PIC4	Interrupt control register	INTC	670
PIC5	Interrupt control register	INTC	670
PIC6	Interrupt control register	INTC	670
PIC7	Interrupt control register	INTC	670
PLLCTL	PLL control register	CG	196, 430
PM0	Port 0 mode register	Port	90
PM1	Port 1 mode register	Port	92
PM3	Port 3 mode register	Port	95
PM3H	Port 3 mode register H	Port	95
PM3L	Port 3 mode register L	Port	95
PM4	Port 4 mode register	Port	100
PM5	Port 5 mode register	Port	103
PM9	Port 9 mode register	Port	108
PM9H	Port 9 mode register H	Port	108
PM9L	Port 9 mode register L	Port	108
PMC0	Port 0 mode control register	Port	91
PMC3	Port 3 mode control register	Port	96
PMC3H	Port 3 mode control register H	Port	96
PMC3L	Port 3 mode control register L	Port	96
PMC4	Port 4 mode control register	Port	101
PMC5	Port 5 mode control register	Port	104
PMC9	Port 9 mode control register	Port	108
PMC9H	Port 9 mode control register H	Port	109
PMC9L	Port 9 mode control register L	Port	109
PMCCM	Port CM mode control register	Port	116
PMCCS	Port CS mode control register	Port	118
PMCCT	Port CT mode control register	Port	120

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Symbol	Name	Unit	Page
PMCDH	Port DH mode control register	Port	122
PMCDL	Port DL mode control register	Port	125
PMCDLH	Port DL mode control register H	Port	125
PMCDLL	Port DL mode control register L	Port	125
PMCM	Port CM mode register	Port	115
PMCS	Port CS mode register	Port	117
PMCT	Port CT mode register	Port	119
PMDH	Port DH mode register	Port	121
PMDL	Port DL mode register	Port	124
PMDLH	Port DL mode register H	Port	124
PMDLL	Port DL mode register L	Port	124
PRCMD	Command register	CPU	76
PRM00	Prescaler mode register 00	TM0	297
PRM01	Prescaler mode register 01	TM0	297
PRM02	Prescaler mode register 02	TM0	297
PRM03	Prescaler mode register 03	TM0	297
PRSCM	Interval timer BRG compare register	CG	405
PRSM	Interval timer BRG mode register	CG	404
PSC	Power save control register	Standby	698
PSMR	Power save mode register	Standby	699
PSW	Program status word	CPU	48
PU0	Pull-up resistor option register 0	Port	91
PU1	Pull-up resistor option register 1	Port	93
PU3	Pull-up resistor option register 3	Port	99
PU4	Pull-up resistor option register 4	Port	102
PU5	Pull-up resistor option register 5	Port	105
PU9	Pull-up resistor option register 9	Port	114
PU9H	Pull-up resistor option register 9H	Port	114
PU9L	Pull-up resistor option register 9L	Port	114
PUCM	Pull-up resistor option register CM	Port	116
PUCS	Pull-up resistor option register CS	Port	118
PUCT	Pull-up resistor option register CT	Port	120
PUDH	Pull-up resistor option register DH	Port	122
PUDL	Pull-up resistor option register DL	Port	125
PUDLL	Pull-up resistor option register DLL	Port	125
PUDLH	Pull-up resistor option register DLH	Port	125
r0 to r31	General-purpose registers	CPU	44
RTBH0	Real-time output buffer register H0	RTP	424
RTBL0	Real-time output buffer register L0	RTP	424
RTPC0	Real-time output port control register 0	RTP	426
RTPM0	Real-time output port mode register 0	RTP	425
RXB0	Receive buffer register 0	UART	472
RXB1	Receive buffer register 1	UART	472
RXB2	Receive buffer register 2	UART	472

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Symbol	Name	Unit	Page
SELCNT1	Selector operation control register 1	TM0	298
SIO00	Serial I/O shift register 0	CSI0	506
SIO00L	Serial I/O shift register 0L	CSI0	506
SIO01	Serial I/O shift register 1	CSI0	506
SIO01L	Serial I/O shift register 1L	CSI0	506
SIOA0	Serial I/O shift register A0	CSIA	525
SIOA1	Serial I/O shift register A1	CSIA	525
SIRB0	Clocked serial interface receive buffer register 0	CSI0	502
SIRB0L	Clocked serial interface receive buffer register 0L	CSI0	502
SIRB1	Clocked serial interface receive buffer register 1	CSI0	502
SIRB1L	Clocked serial interface receive buffer register 1L	CSI0	502
SIRBE0	Clocked serial interface read-only receive buffer register 0	CSI0	503
SIRBE0L	Clocked serial interface read-only receive buffer register 0L	CSI0	503
SIRBE1	Clocked serial interface read-only receive buffer register 1	CSI0	503
SIRBE1L	Clocked serial interface read-only receive buffer register 1L	CSI0	503
SOTB0	Clocked serial interface transmit buffer register 0	CSI0	504
SOTB0L	Clocked serial interface transmit buffer register 0L	CSI0	504
SOTB1	Clocked serial interface transmit buffer register 1	CSI0	504
SOTB1L	Clocked serial interface transmit buffer register 1L	CSI0	504
SOTBF0	Clocked serial interface initial transmit buffer register 0	CSI0	505
SOTBF0L	Clocked serial interface initial transmit buffer register 0L	CSI0	505
SOTBF1	Clocked serial interface initial transmit buffer register 1	CSI0	505
SOTBF1L	Clocked serial interface initial transmit buffer register 1L	CSI0	505
SREIC0	Interrupt control register	INTC	670
SREIC1	Interrupt control register	INTC	670
SREIC2	Interrupt control register	INTC	670
SRIC0	Interrupt control register	INTC	670
SRIC1	Interrupt control register	INTC	670
SRIC2	Interrupt control register	INTC	670
STIC0	Interrupt control register	INTC	670
STIC1	Interrupt control register	INTC	670
STIC2	Interrupt control register	INTC	670
SVA0	Slave address register 0	I^2C	572
SYS	System status register	CPU	77
TCL50	Timer clock selection register 50	TM5	363
TCL51	Timer clock selection register 51	TM5	363
TM00	16-bit timer counter 00	TM0	288
TM01	16-bit timer counter 01	TM0	288
TM02	16-bit timer counter 02	TM0	288
TM03	16-bit timer counter 03	TM0	288
TM0IC00	Interrupt control register	INTC	670
TM0IC01	Interrupt control register	INTC	670
TM0IC10	Interrupt control register	INTC	670
TM0IC11	Interrupt control register	INTC	670

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Symbol	Name	Unit	Page
TM0IC20	Interrupt control register	INTC	670
TM0IC21	Interrupt control register	INTC	670
TM0IC30	Interrupt control register	INTC	670
TM0IC31	Interrupt control register	INTC	670
TM5	16-bit timer counter 5	TM5	361
TM50	8-bit timer counter 50	TM5	361
TM51	8-bit timer counter 51	TM5	361
TM5IC0	Interrupt control register	INTC	670
TM5IC1	Interrupt control register	INTC	670
TMC00	16-bit timer mode control register 00	TM0	292
TMC01	16-bit timer mode control register 01	TM0	292
TMC02	16-bit timer mode control register 02	TM0	292
TMC03	16-bit timer mode control register 03	TM0	292
TMC50	8-bit timer mode control register 50	TM5	364
TMC51	8-bit timer mode control register 51	TM5	364
TMCYC0	8-bit timer H carrier control register 0	TMH	385
TMCYC1	8-bit timer H carrier control register 1	TMH	385
TMHIC0	Interrupt control register	INTC	670
TMHIC1	Interrupt control register	INTC	670
TMHMD0	8-bit timer H mode register 0	TMH	382
TMHMD1	8-bit timer H mode register 1	TMH	382
TOC00	16-bit timer output control register 00	TM0	295
TOC01	16-bit timer output control register 01	TM0	295
TOC02	16-bit timer output control register 02	TM0	295
TOC03	16-bit timer output control register 03	TM0	295
TP0CCIC0	Interrupt control register	INTC	670
TP0CCIC1	Interrupt control register	INTC	670
TP0CCR0	TMP0 capture/compare register 0	TMP	207
TP0CCR1	TMP0 capture/compare register 1	TMP	209
TP0CNT	TMP0 counter read buffer register	TMP	211
TP0CTL0	TMP0 control register 0	TMP	201
TP0CTL1	TMP0 control register 1	TMP	202
TP0IOC0	TMP0 I/O control register 0	TMP	203
TP0IOC1	TMP0 I/O control register 1	TMP	204
TP0IOC2	TMP0 I/O control register 2	TMP	205
TP0OPT0	TMP0 option register 0	TMP	206
TP0OVIC	Interrupt control register	INTC	670
TXB0	Transmit buffer register 0	UART	473
TXB1	Transmit buffer register 1	UART	473
TXB2	Transmit buffer register 2	UART	473
VSWC	System wait control register	CPU	78
WDCS	Watchdog timer clock selection register	WDT	415
WDT1IC	Interrupt control register	INTC	670
WDTE	Watchdog timer enable register	WDT	421

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Symbol	Name	Unit	Page
WDTM1	Watchdog timer mode register 1	WDT	416, 675
WDTM2	Watchdog timer mode register 2	WDT	420
WTIC	Interrupt control register	INTC	670
WTIIC	Interrupt control register	INTC	670
WTM	Watch timer operation mode register	WT	408