APPLICATION NOTE

AN460
Using the P82B96 for bus interface

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IC12a and IC28 Data Handbook

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The P82B96 offers many different ways in which it can be used as a bus interface. In its simplest application it can be used as an interface between bus systems operating from different supply voltages. Opto isolation between two bus systems is possible, and also the availability of the Tx and Rx signals permits interfacing of the P82B96 with other bus systems which separate the forward output path, from the backward input signal path.

The fixed, low, logic levels used at Sx imply a restriction that the I^2C bus connection on this chip should be used only with small I^2C systems, contained typically on one printed circuit board, and not connected with long wiring which could introduce noise.

It is the intention that the P82B96 be used as an interface to long or noisy bus systems so that the function of each local I^2C bus node remains within specification, and the P82B96 handles the more difficult interfacing tasks.

Series resistors in the SDA/SCL lines should also be avoided in the Sx lines at I^2C nodes that include P82B96.

A further implication of the way in which the P82B96 functions is that if two P82B96 chips have their Sx pins connected to the same I^2C node, then signals from the Rx input of one P82B96 will not propagate to Tx on the other. This is dictated by the non-latching requirement that they must not propagate back to Tx within one chip.

As the buffered output of the P82B96 has increased drive capability over the normal I^2C specification, these limitations do not present any great restriction. The buffered side can be used for interconnection, and distance.

There are also some issues which need to be considered in protecting the P82B96 from spurious signals in a bus line installed over a long distance, or where signals may be picked up which exceed the supply rail levels.

INTERFACING DIFFERENT SUPPLY/LOGIC LEVELS

Figure 1 shows P82B96 applied with the I/O pins Tx and Rx linked to provide a new bus with the same protocol and properties as I^2C but operating at different logic levels. Because Tx has an open collector output a pull-up resistor is applied.

Supply voltages in the range 2 V to 15 V are permitted, allowing interfacing from a conventional 5 V I^2C bus to 3 V logic systems or low current bus systems such as SMB with 350 μA pull-down current. It must be remembered that the input threshold at Rx on the buffered bus side is nominally at one half of the V_{CC} voltage.

Hence longer cable runs and ground potential differences can be accommodated by using a 15 V supply to improve noise immunity while retaining the simplicity of I^2C wiring.

The oscilloscope traces, Figures 2 and 3, show the waveforms at Tx, Rx, and Sx when Tx is not linked to Rx. Tx has a 330Ω pull-up to the chip supply of 10 V, Sx has a 1600Ω pull-up to a 5 V supply. There is no external capacitive bus loading. The propagation delay for signals from Sx to Tx is about 100ns, and from Rx to Sx it is about 300ns.

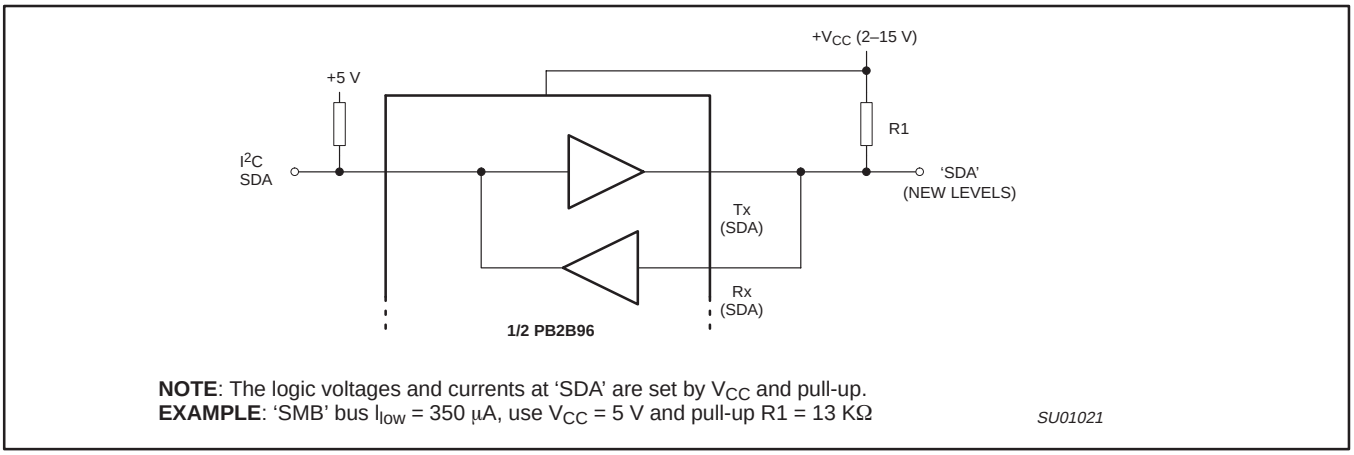


Figure 1. Interfacing an "I^2C" type of bus with different logic levels

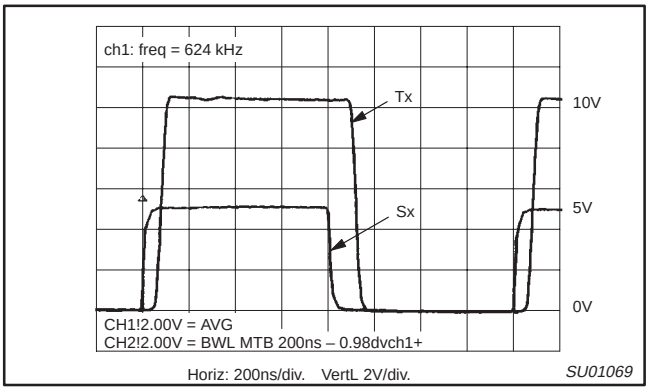


Figure 2. Propagation Sx to Tx
Sx pull-up to 5V, Tx pull-up to V_{CC} = 10V

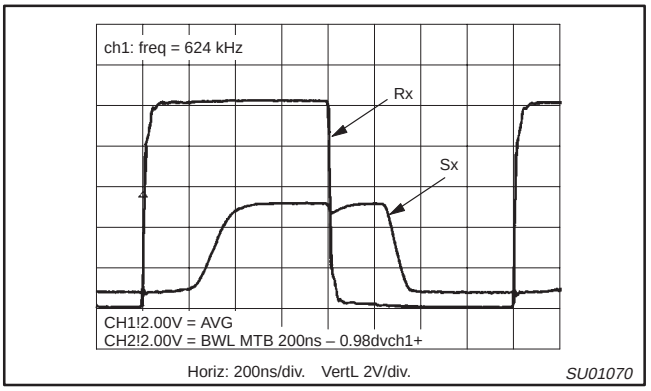


Figure 3. Propagation Rx to Sx
Sx pull-up to 5V, V_{CC} = 10V

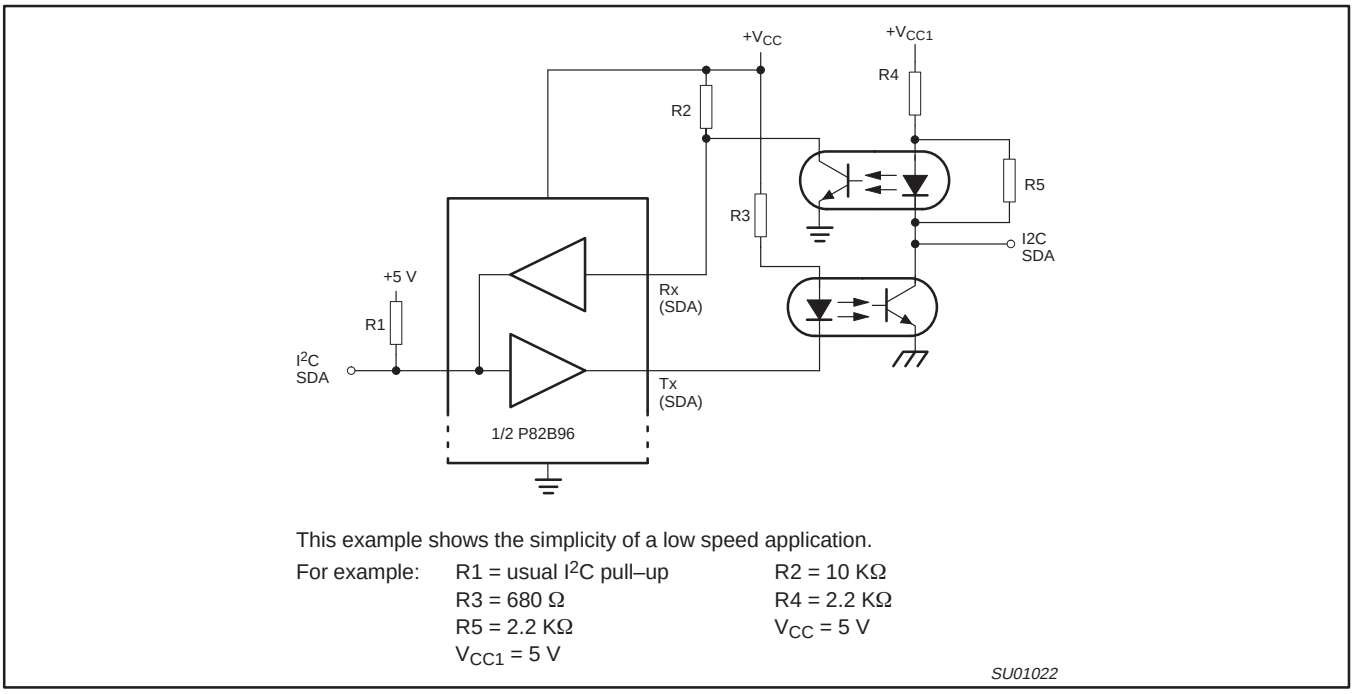
GALVANIC BUS ISOLATION

In Figure 4 the Tx and Rx signals are shown interfaced via opto-couplers to provide galvanic separation.

This simple circuit can use general purpose 4N36 opto-couplers having published switching times around 50μs for the load impedances shown. That will limit the design bus clock speed to around 5kHz. Simple circuits like this can probably reach 20kHz by changing the type of opto-coupler or the circuit values.

Low speed applications can include: Driving remote displays, security systems, access control systems, data logging, remote control of appliances or lighting. Isolation can simply be included in I^2C systems at any point on the bus where safety isolation or ground potential differences require it.

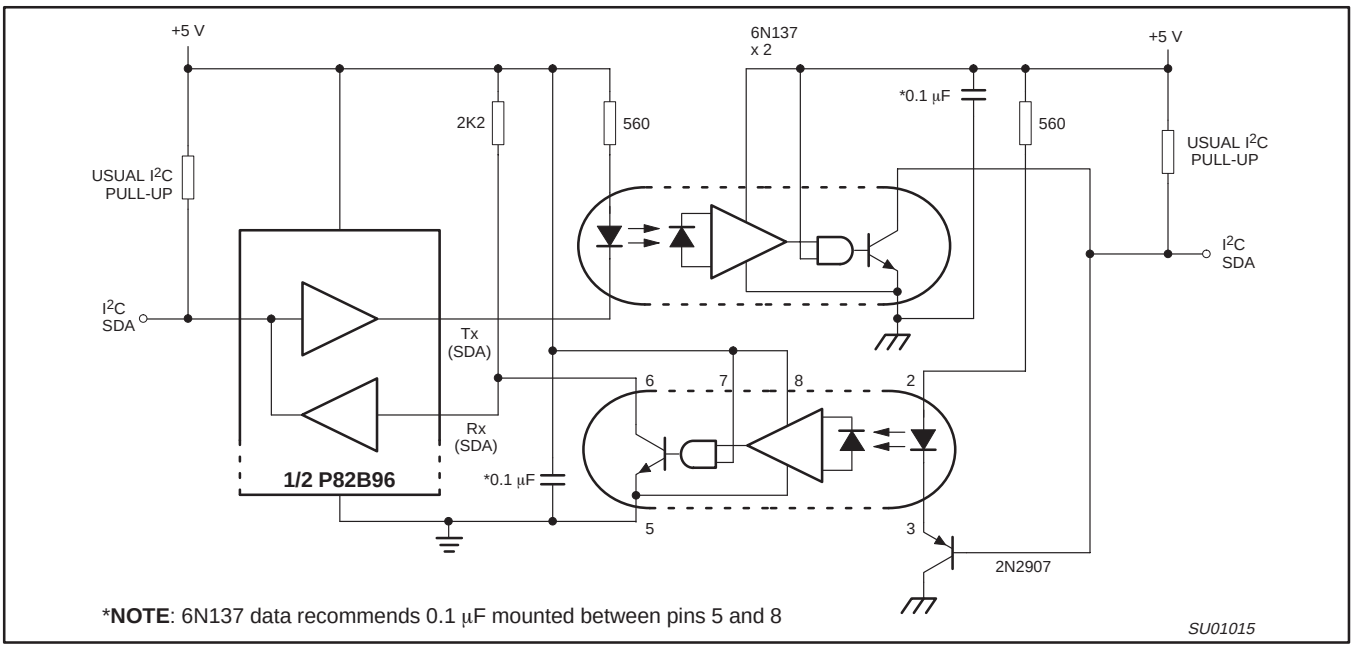
Figure 5 shows how faster opto-couplers can be applied to achieve full 100kHz clock speed.



This example shows the simplicity of a low speed application.

For example: R1 = usual I^2C pull–up; R2 = 10 KΩ; R3 = 680 Ω; R4 = 2.2 KΩ; R5 = 2.2 KΩ; V_{CC} = 5 V; V_{CC1} = 5 V

Figure 4. Galvanic isolation of I^2C nodes via opto-couplers



***NOTE**: 6N137 data recommends 0.1 μF mounted between pins 5 and 8

Figure 5. Opto-isolation of I^2C nodes via 6N137 for 100 kHz operation

LINK VIA A DIFFERENTIAL BUS

Figure 6 shows an SDA signal interfaced via P82B96 and the PCA82C250 to a balanced twisted pair bus capable of supporting over 100 nodes. In this way over 100 separate I^2C nodes can be interconnected, retaining the conventional I^2C protocol. Operation over short distances (e.g., 50 meters) at 100 kHz is possible. To meet the I^2C timing requirements for the 'acknowledge' bit it is necessary to select a lower clock speed when working with very long busses. As a minimum, the 'round trip' signal propagation delay, from any one node to another node and back again, must be less than the clock 'low' period. Signals will typically travel 1 meter in 5ns.

Note that in this example, the CAN bus hardware is only a transport medium for carrying I^2C signals. The I^2C signal format is not being converted to CAN bus software data format by the PCA82C250.

TECHNICAL ISSUES

There are a number of issues which may need to be considered in the application of the P82B96. These are discussed below.

Transient Signal Protection

The table of maximum ratings of the data sheet specifies the voltage which may be applied to any pin with respect to GND as being from -0.3 to +18 volts.

No ESD protection diodes have been applied between the input and output pins and V_{CC} as these would prevent the very useful feature of being able to operate inputs and outputs above the V_{CC} rail, up to 15 volts.

There is an internal diode from each pin to V_{EE}. This diode will conduct if negative voltages are applied to any pin. The -0.3 V rating is applied to ensure these diodes never conduct. Currents in these diodes can cause unpredictable behavior.

In applications where these voltage ratings could be exceeded, e.g. by transient signals induced into long buffered bus lines, Schottky diodes and 15 V zener diode clamps should be fitted between GND and the buffered bus pins as shown in Figure 7.

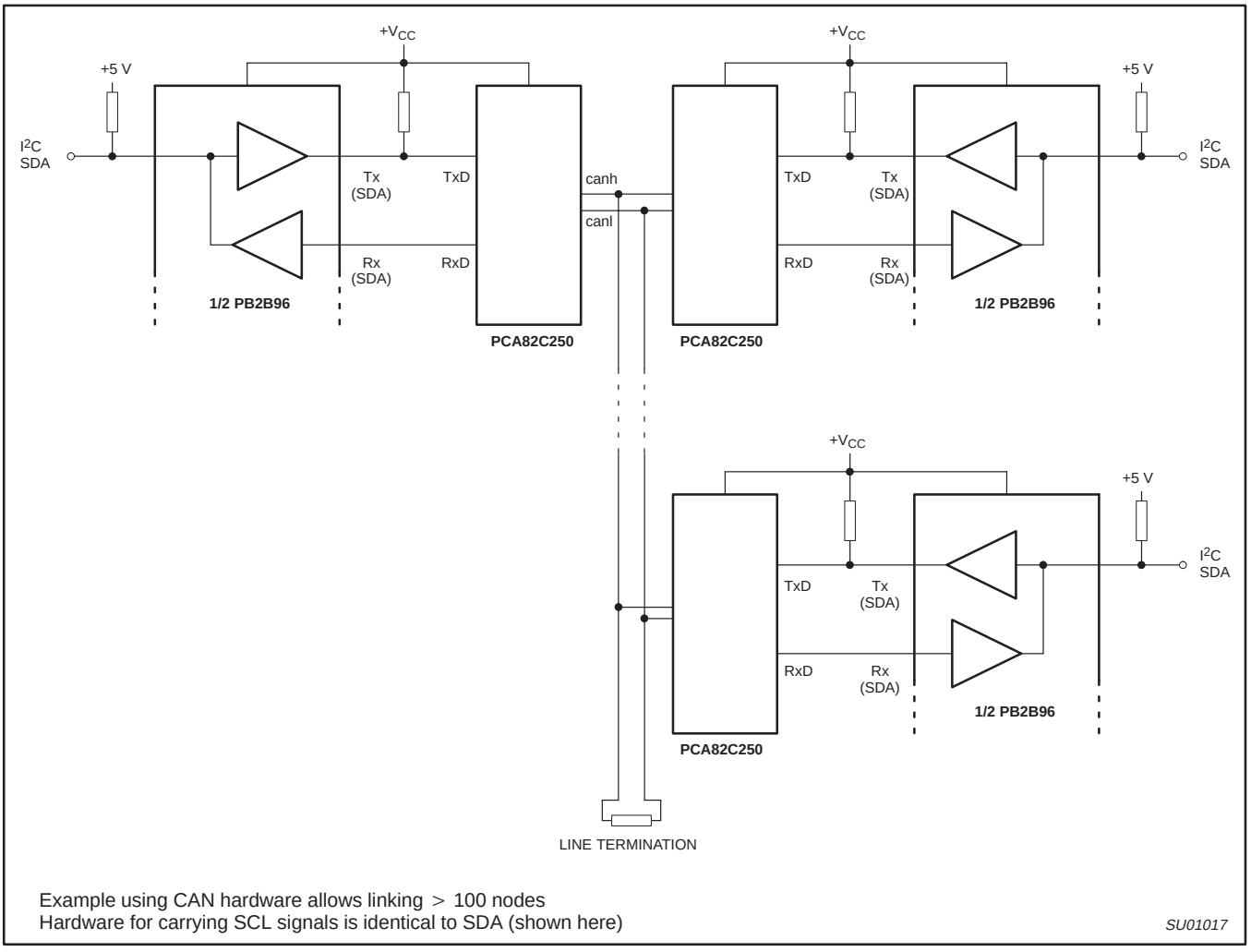


Figure 6. Linking I^2C nodes via a differential bus

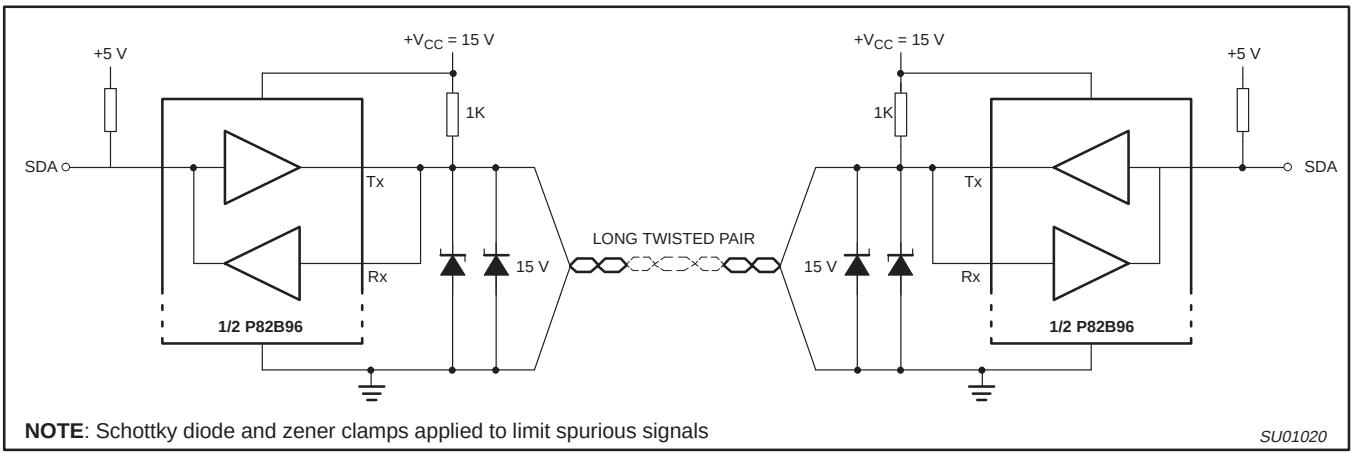


Figure 7. Driving a high voltage, low impedance "I²C" bus

Power dissipation under fault conditions

The current drive capability of the buffered Tx and Ty outputs exceeds 100 mA. If a wiring fault causes a short from these pins to V_{CC} (or to a buffered bus supply when using different supplies) then high dissipations result when Sx or Sy are driven low. The rated 300 mW dissipation can be exceeded within a very short time.

Appropriate precautions should be taken to ensure that such a short-circuit does not occur.

Bus characteristics and rise/fall times

In general terms, the rise times which will be observed on a bus driven by the P82B96 will be simply determined by the pull-up resistor used and the total capacitive load presented to the bus.

The fall time is determined mostly by the dynamic pull down current capability and the capacitive load, with some modification caused by the varying current in the bus pull up resistor.

The effective logic signal propagation time will depend on the input logic thresholds of the P82B96, and of any other devices connected to the I²C or buffered bus.

On a 2 V supply, the Sx and Sy thresholds are approaching half the supply rail. On a 5V supply their (0.65V) threshold is much closer to GND than usual for logic inputs. This causes some additional delay in the effective propagation time on falling edges, and reduces those delays on the rising edges.

For Rx and Ry, the threshold is always 50% of V_{CC} so switching levels are 'conventional' when the buffered bus pull-ups are connected to V_{CC}. However, if the buffered bus pull-ups connect to a supply voltage different to V_{CC}, the rise/fall times required to reach the Rx threshold may need to be taken into account.

P82B96 response time for propagation of low to high at Sx

With Tx connected to Rx, a low at Sx causes a low at Tx and thus to Rx. The low at Rx enables a 'clamp' at 1V, the logic low, on Sx.

So when the Sx input is released, the voltage on the I²C bus rises towards this 1V clamping level set by the return signal from Rx, which is still low.

As Sx rises past its 0.65V input threshold, the Tx output drive will be released. The Tx output voltage will begin to rise at a rate determined by its load capacitance and the pull up resistor used at Tx.

With Tx connected to Rx, when it reaches 50% of the V_{CC} supply voltage the Rx input senses that Tx has been released, and returns a 'high' signal to its output at Sx, allowing this voltage to continue its rise again towards the I²C supply. It will be recognized as high by other I²C chips when it reaches their logic threshold. Typical waveforms are shown in Figure 8.

This delay in termination of the low signal on Sx will be further extended if Tx and Rx are not directly linked and there are other delays inherent in the signal path between Tx and Rx. Including slow opto-couplers in the loop will exaggerate these delays (see Figure 4).

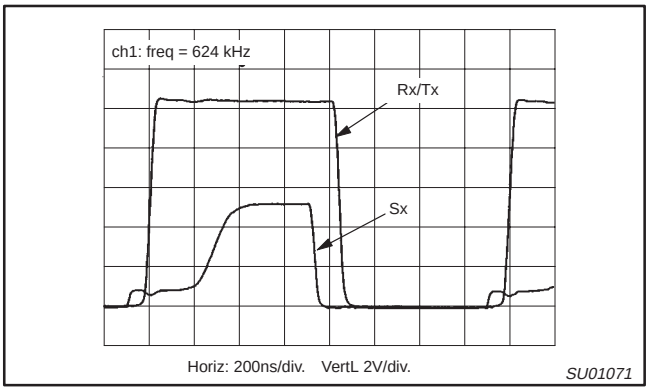


Figure 8. Low to High propagation of Sx with Tx linked to RX Sx = 5V I²C bus, Tx = buffered bus with pull-up to V_{CC} = 10V

Terminology

Because the I²C bus handles bi-directional data flow, any buffer device must be bi-directional. So inputs are also outputs. Describing a buffer operation without reference to 'input' and 'output' signals presents difficulties: forgive the occasional use of these descriptions.

We also make assumptions about the possible system connections to the chip, but these should not be taken to imply restrictions. In many of the applications described it would also be possible to exchange the terms 'I²C' and 'Buffered' bus.

Sx and Sy: the I²C side

We have named one side of the P82B96 the 'I²C' side (Sx and Sy). We intend that this I/O pin will mostly be connected to a normal 5V I²C bus comprising just a few chips and short wiring — for example a system not more complex than the I²C demonstration boards such as OM4151 or OM1016. While this I/O pin is COMPATIBLE with normal I²C signals, the logic voltage thresholds we use on this 'I²C' pin are non-standard.

Tx, Rx, and Ty, Ry: the buffered side

The other side of the chip features the separated input and output pins Tx and Rx. While that provides the possibility to include opto-couplers or to interface to other bus systems, in many applications those two pins will simply be linked together to form an I/O with properties exactly the same as any conventional I²C bus product. We refer to the linked Rx/Tx I/O as the 'buffered' bus side.

This buffered I/O is intended for connection into all the unusual bus systems — anything from 2 V to 15 V, with currents from microamps to 30 mA static sink, and conventional 0.4 V saturation. Its input logic threshold adapts to be always half the P82B96 V_{CC}.

When the buffered bus pull-ups return to V_{CC} the buffered bus is fully I²C compliant.

Comparison between the P82B96 and the P82B715 bus extender

In the P82B96 the I²C and buffered bus loads are independent. The bus loading on one input does not influence the load to be driven by devices connected to the corresponding 'buffered' output. While the I²C and buffered ports of one P82B96 share a common GND connection, opto-coupling the buffered signals allows connection to another I²C bus operating on a separate, isolated ground (Figures 4 and 5).

This is not the case in the P82B715 bus extender, which operates by providing linear x10 current amplification of the bus current sink capability in one direction only. Its two sides are linked by an internal 30 Ω resistor. This means that the loading on one side of the chip is always part of the loading seen at the other side. It does not allow different logic levels between busses having different voltages. The bus voltages on each side of P82B715 are always matched within 100 mV.

The P82B96 is not pin-compatible with the P82B715, but its 30 mA static sink capability will overlap some P82B715 applications. P82B96 can also directly drive the 10x load that P82B715 drives — and P82B96 extends operation down to 2 V supply.

P82B96 FEATURES

Buffered bus drive capability

The 30 mA buffered bus static sink capability is useful when driving opto-couplers.

It is also possible to drive low impedance, high voltage, long busses directly from the P82B96, but the overall performance will be dependent on the characteristics of the bus and it is difficult to fully address this in the specifications for the P82B96.

1. The 30 mA Tx and Ty outputs do not guarantee full 100 kHz operation when directly driving a long, high voltage bus. This is because a 15 V supply and 30 mA static drive implies a minimum pull-up resistor of 500Ω. With 500Ω, a 4 nF bus load means a time-constant of 2 μsecs., which exceeds the I²C risetime specification.

   On 5 V, the 30 mA drive permits a pull-up of 167Ω, so the time constant with a 4 nF bus load easily permits full 100 kHz operation.

   Typically, applications for long, high voltage, busses will use low speeds. For example the clock speed will usually be chosen lower than 30 kHz when working with a bus longer than 100 meters.

2. If the buffered side is used to directly drive long wires then 'ringing' on the output bus becomes a possibility, with a strong probability that the I/O pin will be driven below the ground potential.

   The P82B96 does not allow I/O pins to be driven below ground or above 15 V. Therefore for long, 'dirty' busses we recommend the use of external schottky diode and zener clamps (Figure 7).

Table 1. Table of drive capability

Type of application	Will drive bus load	To guaranteed clock
Normal 5 V I²C	All normal I²C loads	100 kHz
Low impedance 5 V	1/10 R and 10*C (4 nF)	100 kHz
3.3 V ±10% bus	All normal I²C loads	100 kHz
Low impedance 3.3 V	1/10 normal R, 10*C	100 kHz
SMB bus (350 μA)	All SMB loads	normal SMB specs
15 V bus, 500Ω	< 2 nF	100 kHz
15 V bus > 500Ω	> 2 nF	depends on capacitance

Treatment of (unused) I/O pins

In some systems, one or other side of the P82B96 might be required to be 'hot plugged' to the I^2C bus of some other separate equipment.

This will require some pull up capability to be provided on both sides of the plug.

Each input pin (Sx or Rx) is a high impedance input and cannot be left floating. Internal pull-ups have not been used because they would only pull-up to the IC supply (V_{CC}), thereby demanding that V_{CC} cannot be lower than the connected bus voltages. In the P82B96 any input may be pulled up to +15 V, independent of V_{CC}.

No currents will flow into the I/O pins (except when outputs drive a bus low). The inputs are like LM324 inputs, based on PNP input transistors, so they source tiny currents when externally driven low.

External pull up resistors fitted at Sx pins should cause the specified minimum 200 μA to flow when that input is low.

The Rx input should be treated just like any op-amp input and not left floating. A pull-up of 100 K should cope with PCB leakage in humid conditions.

Diodes have not been fitted between I/O pins and V_{CC}, to allow them to be pulled to voltages above the chip's V_{CC}. This permits, for example, use of the P82B96 on a 3 V supply, driving a 3 V buffered bus, to interface with a normal 5 V I^2C input. It also allows the I^2C busses to remain active even if the P82B96 V_{CC} fails.

Failure of V_{CC} and consequences for bus operation

The P82B96 maintains its function for V_{CC} below 2 V. At normal temperatures it starts to shut off at around 1.2 V. That means that if the normal V_{CC} supply is 5 V, and that supply was to fall to 2 V, then it just retains normal operation — it cannot 'release' the busses even though the supply is now only 40% of normal.

During failure of the V_{CC} power supply no abnormal signals are caused on any I/O until the supply falls below a value below which point there will be no signals transmitted through the chip, and all I/Os will become open circuit. That voltage is of the order of 1 V.

Margins on switching levels

There are certain constraints that determine the two low levels on the I^2C bus interface Sx and Sy. The I^2C bus must always be driven below the lowest level that guarantees a low on any bus to which it is connected.

For a normal 5 V I^2C bus the minimum low is 1.5 V. The P82B96 guaranteed low level is set well below this, at 1V maximum for the I^2C maximum allowed 3 mA. (It assumes a normal 5 V I^2C bus on the Sx/Sy side of the buffer, but this should not be taken as a restriction)

The externally connected I^2C chips must, in turn, pull the I^2C pin below the threshold required to set Tx/Ty low.

Those external chips all have a maximum static low specification of 0.4 V at 3 mA. Therefore the typical threshold for the Sx and Sy inputs is 650 mV at 25°C, with 600 mV as the minimum.

If there was not a difference between the Sx low output (the larger voltage) at the smallest permitted load current, and the Sx input threshold (a lesser voltage) the chip would latch.

As the Sx sink current decreases the output low level at Sx decreases. For this reason a minimum sink current at Sx is specified (200 μA)

The temperature coefficient on the input and output thresholds of Sx and Sy is –2 mV/K.

The other side (Tx/Rx and Ty/Ry) is designed for connection to any bus from 2 V to 15 V.

The typical threshold switching level is 50% of V_{CC}. Tolerances tighter than the normal 70/30% levels have been specified so the guaranteed noise margins, especially when working with long 15V busses, are improved.

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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