



**PRELIMINARY**

**CYM1836V33**

# 128K x 32 3.3V Static RAM Module

## Features

- High-density 3.3V 4-megabit SRAM module
- 32-bit standard footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs
- Access time of 25 ns
  - Low active power 1.6W (max.) at 20 ns
- 2.0V Data Retention ( $I_{CCDRL} = 0.8 \text{ mA, max.}$ )
- SMD technology
- TTL-compatible inputs and outputs
- Available in 64-pin SIMM, 64-pin ZIP format or 72-pin SIMM format.

## Functional Description

The CYM1836V33 is a 3.3V high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip se-

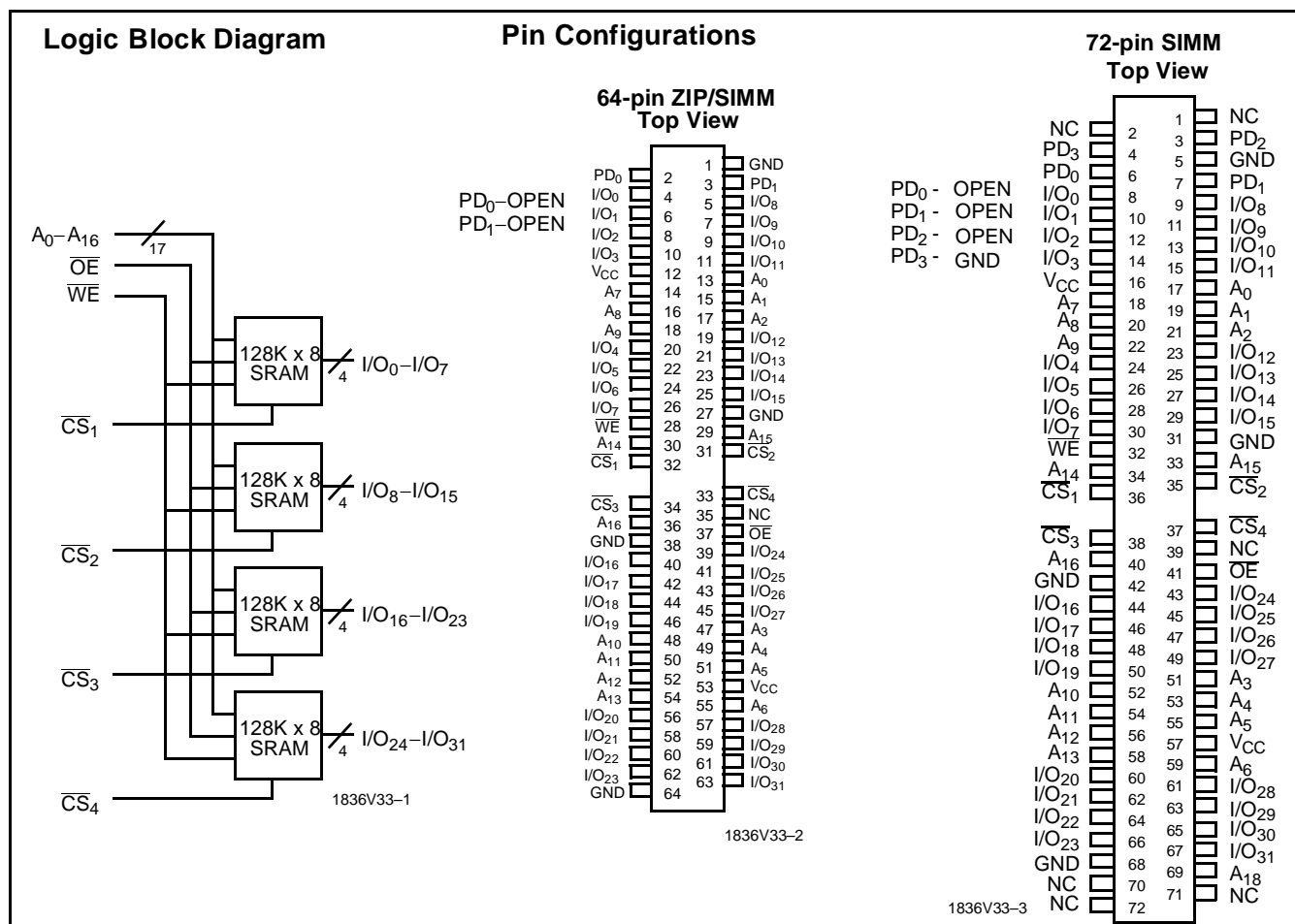
lects ( $\overline{CS}_1, \overline{CS}_2, \overline{CS}_3, \overline{CS}_4$ ) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading the device is accomplished by taking the chip select ( $\overline{CS}$ ) LOW while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins ( $PD_0$  and  $PD_1$ ) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.





**Selection Guide**

	1836V33-15	1836V33-20	1836V33-25	1836V33-30	1836V33-35	1836V33-45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	520	480	440	440	440	440
Maximum Standby Current (mA)	20	20	20	20	20	20

Shaded area contains advance information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature with

Power Applied..... -10°C to +85°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +V<sub>CC</sub> + 0.5V

DC Input Voltage..... -0.5V to +V<sub>CC</sub> + 0.5V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 300mV

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	1836V33-15		1836V33-20, 25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-4	+4	-4	+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, $\overline{CS} \leq V_{IL}$		520		480 (20ns) 440	mA
I <sub>SB1</sub>	Automatic $\overline{CS}$ Power-Down Current <sup>[1]</sup>	V <sub>CC</sub> = Max., $\overline{CS} \geq V_{IH}$ , Min. Duty Cycle = 100%		100		80	mA
I <sub>SB2</sub>	Automatic $\overline{CS}$ Power-Down Current <sup>[1]</sup>	V <sub>CC</sub> = Max., $\overline{CS} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		20		20	mA

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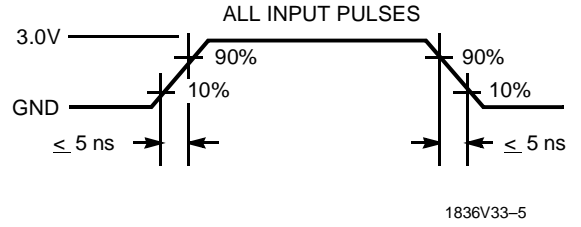
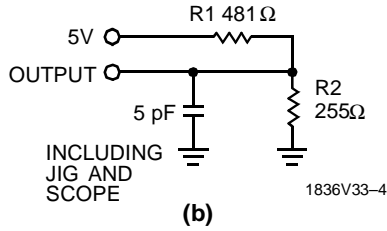
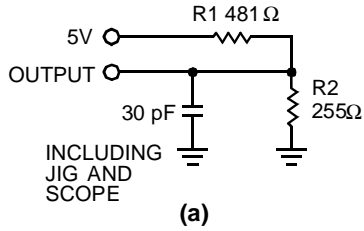
**Capacitance<sup>[2]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance <sup>[3]</sup>	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	24	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

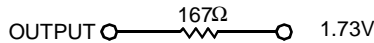
**Notes:**

1. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
2. Tested on a sample basis.
3. 20 pF on  $\overline{CS}$ , 40 pF all others.

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics** Over the Operating Range<sup>[4]</sup>

Parameter	Description	1836V33-15		1836V33-20		1836V33-25		1836V33-30		1836V33-35		1836V33-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>														
t <sub>RC</sub>	Read Cycle Time	15		20		25		30		35		45		ns
t <sub>AA</sub>	Address to Data Valid		15		20		25		30		35		45	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		3		3		3		3		3		ns
t <sub>ACS</sub>	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		7		8		8		10		12		15	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z		7		8		10		11		12		15	ns
t <sub>LZCS</sub>	$\overline{CS}$ LOW to Low Z <sup>[5]</sup>	3		3		3		3		3		3		ns
t <sub>HZCS</sub>	$\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup>		7		10		10		13		15		18	ns

Shaded area contains advance information.

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed by design and not 100% tested.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.



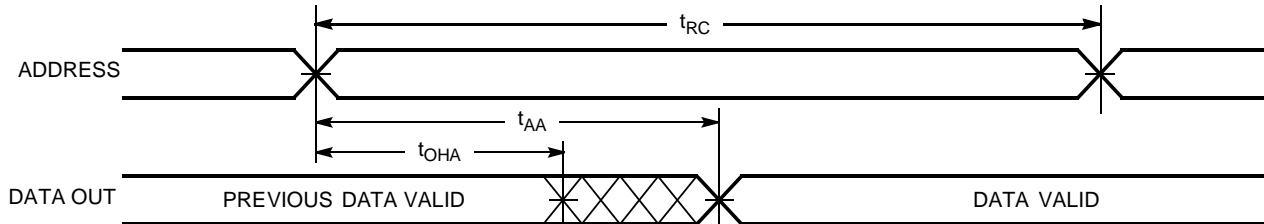
Switching Characteristics Over the Operating Range<sup>[4]</sup> (continued)

Parameter	Description	1836V33-15		1836V33-20		1836V33-25		1836V33-30		1836V33-35		1836V33-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE<sup>[7]</sup></b>														
t <sub>WC</sub>	Write Cycle Time	15		20		25		30		35		45		ns
t <sub>SCS</sub>	$\overline{CS}$ LOW to Write End	12		15		15		18		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	12		15		15		18		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	12		15		15		18		20		25		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		10		10		13		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	3		3		3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6]</sup>	0	7	0	8	0	10	0	15	0	15	0	18	ns

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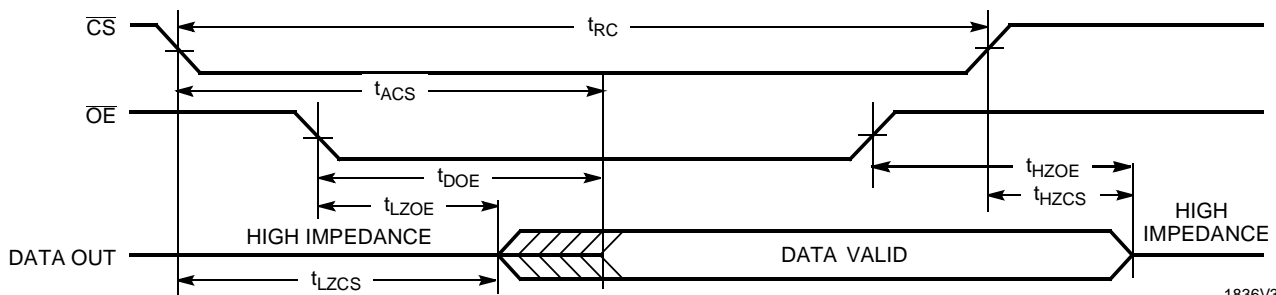
Switching Waveforms

Read Cycle No. 1<sup>[8, 9]</sup>



1836V33-6

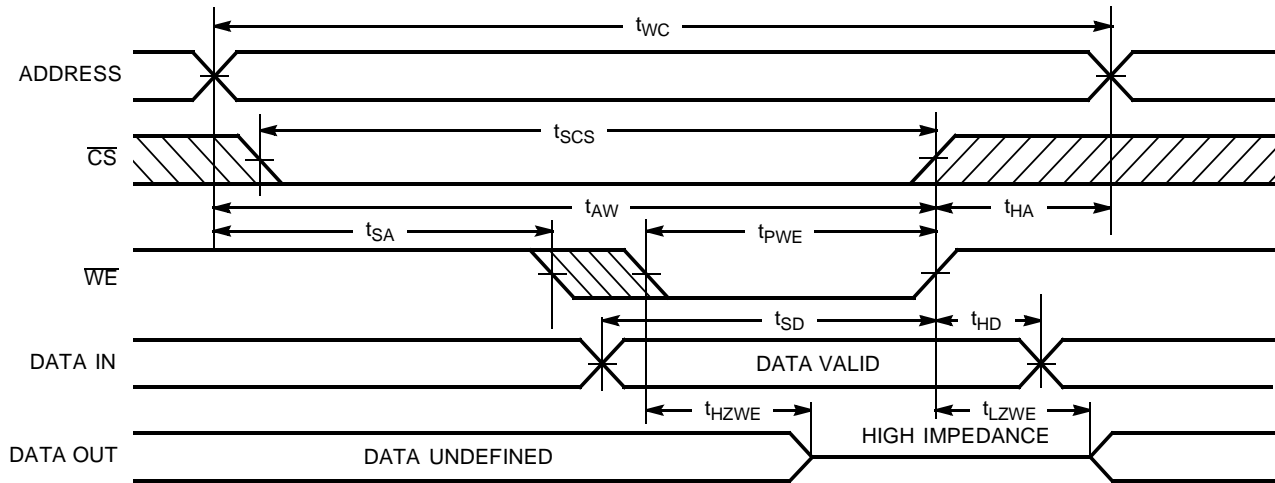
Read Cycle No. 2<sup>[8, 10]</sup>



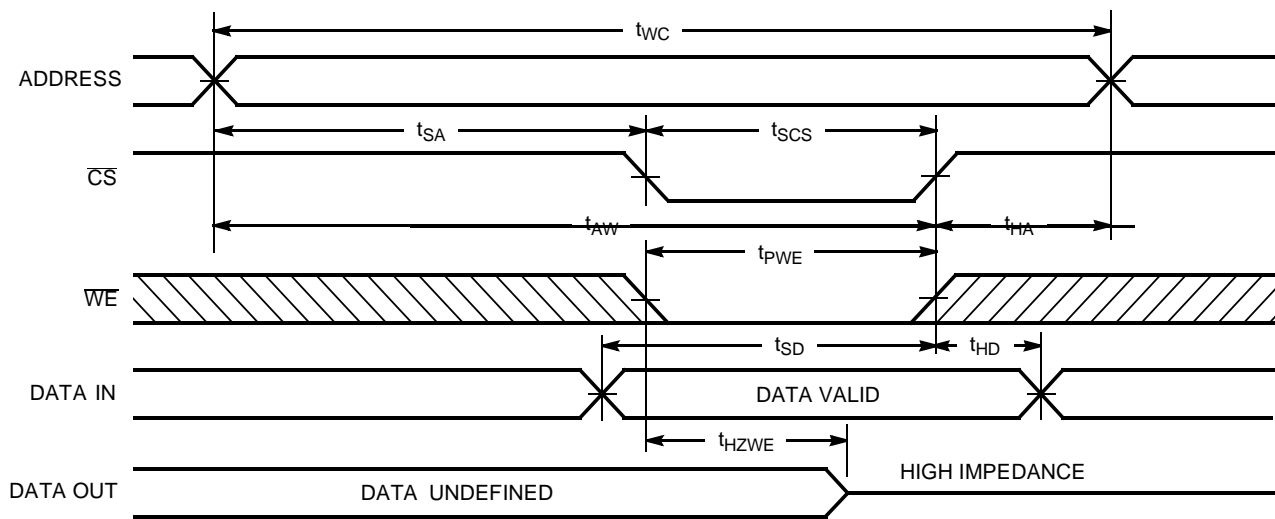
1836V33-7

Notes:

- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No.1 (WE Controlled)<sup>[7]</sup>**


1836V33-8

**Write Cycle No. 2 (CS Controlled)<sup>[7, 11]</sup>**


1836V33-9

**Note:**

 11. If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

$\overline{CS}_N$	WE	OE	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

**Ordering Information<sup>[12]</sup>**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1836V33PM-15C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-15C	PZ08	72-Pin SIMM Module (Gold Contacts)	
20	CYM1836V33PM-20C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-20C	PZ08	72-Pin SIMM Module (Gold Contacts)	
25	CYM1836V33PM-25C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-25C	PZ08	72-Pin SIMM Module (Gold Contacts)	
	CYM1836V33P8-25C	PM04	72-Pin ZIP Module (Gold Contacts)	
30	CYM1836V33PM-30C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-30C	PZ08	72-Pin SIMM Module (Gold Contacts)	
	CYM1836V33P8-25C	PM04	72-Pin ZIP Module (Gold Contacts)	
35	CYM1836V33PM-35C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-35C	PZ08	72-Pin SIMM Module (Gold Contacts)	
	CYM1836V33P8-25C	PM04	72-Pin ZIP Module (Gold Contacts)	
45	CYM1836V33PM-45C	PM03	64-Pin SIMM Module	Commercial
	CYM1836V33PZ-45C	PZ08	72-Pin SIMM Module (Gold Contacts)	
	CYM1836V33P8-25C	PM04	72-Pin ZIP Module (Gold Contacts)	

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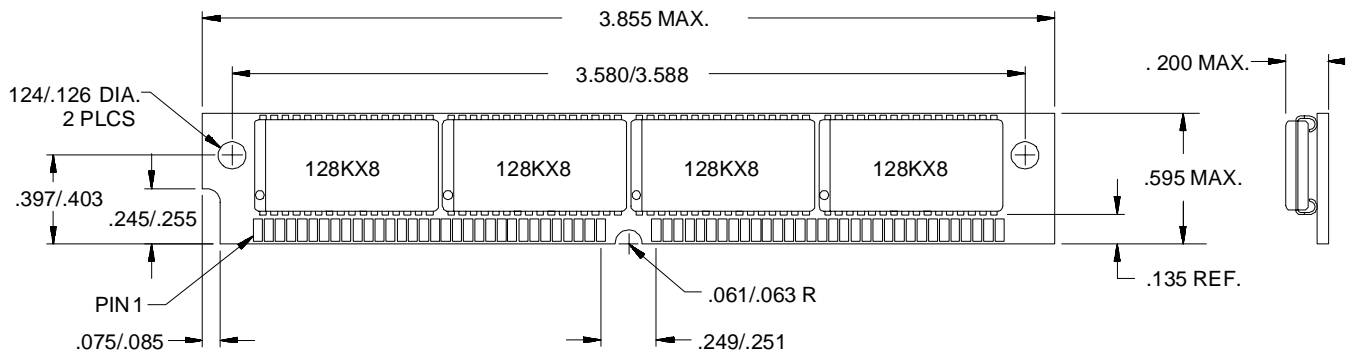
**Note:**

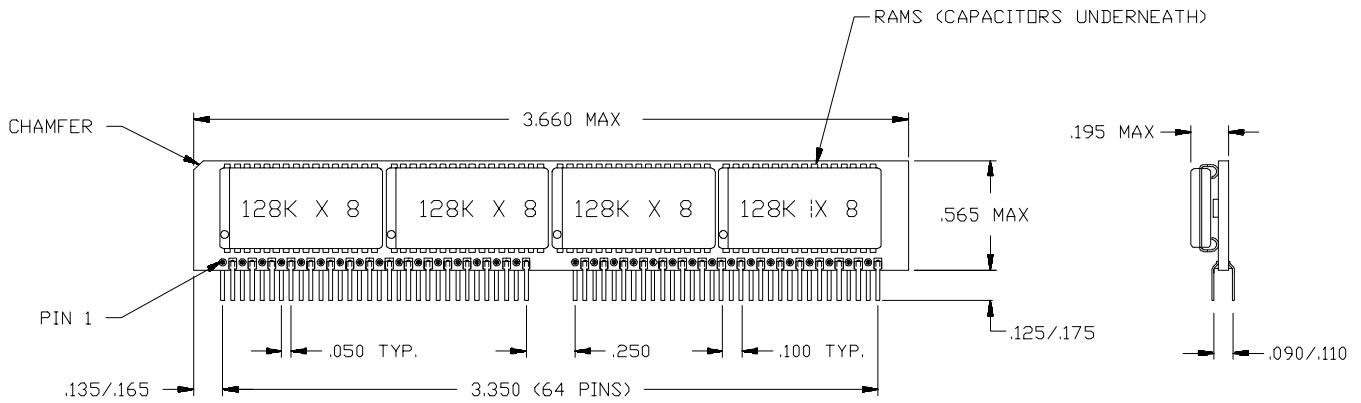
12. 64-pin SIMM suitable for use in angled SIMM applications.

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**Package Diagrams**

**64-Pin SIMM Module PM03**



**Package Diagrams (continued)**
**64-Pin ZIP Module PZ08**

**72-Pin Plastic SIMM Module PM04**
