

FMS7951

Zero Delay Clock Multiplier

Features

- Low Voltage CMOS or PECL reference input
- Up to 175 MHz of output frequency
- Nine configurable outputs
- Output enable pin
- 250 pS of output to output skew
- 300 pS of Cycle to Cycle Jitter
- V_{DD} Range of 3.3V ±0.2V
- Commercial temperature range
- Available in 32 pin TQFP

Description

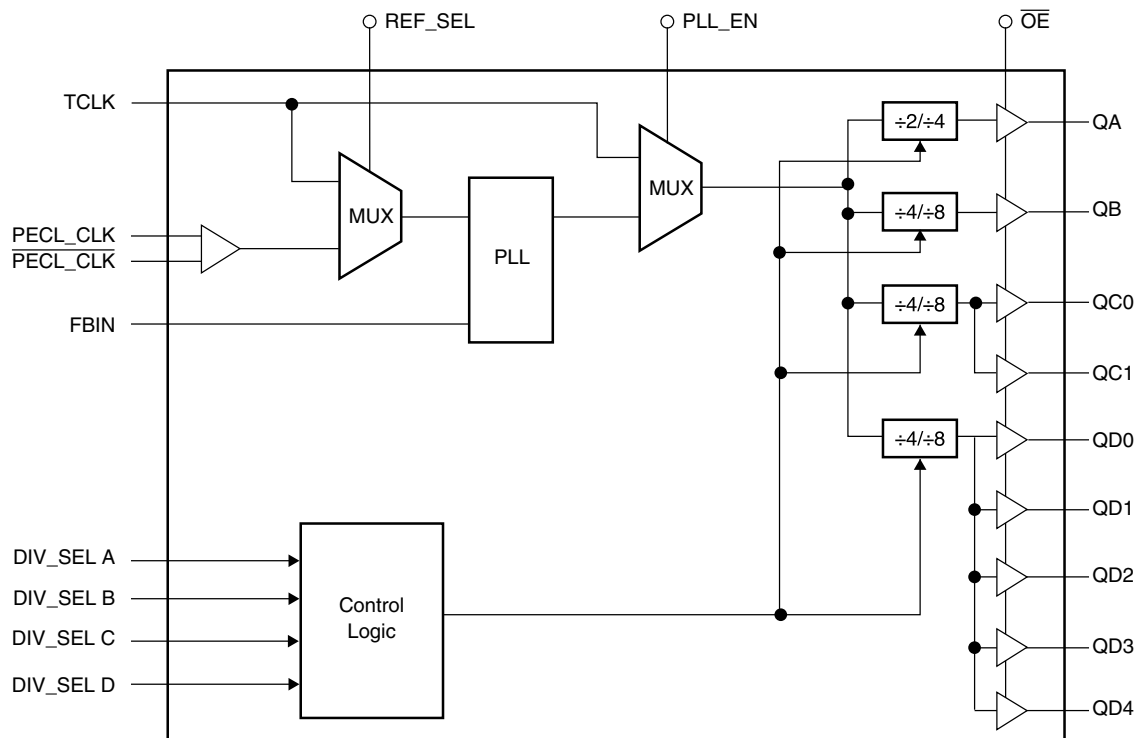
FMS7951 is a high speed, zero delay, low skew clock driver. It uses phase locked loop technology to generate frequencies up to 175 MHz.

It has four banks of configurable outputs. By externally connecting one of the outputs to FBIN, the internal PLL will lock in both phase and frequency to the incoming clock. Any changes to the input clock will be tracked by the outputs. Depending on the selected output for feedback connection, the output frequencies will be as 1X, 2X or 4X of the input.

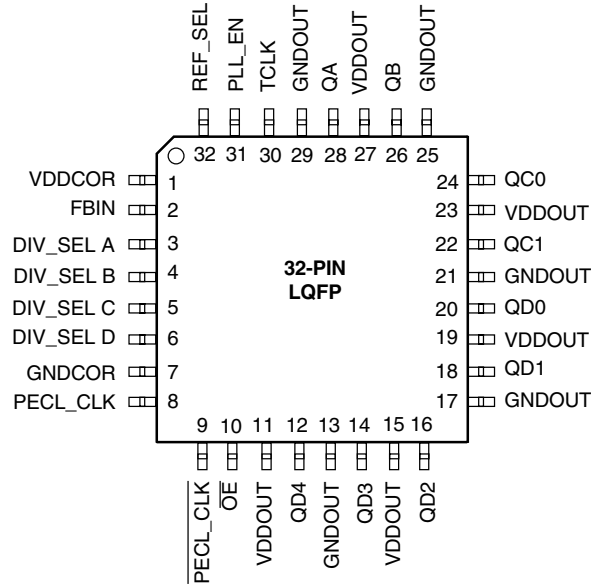
REF_SEL allows selection between PECL input or TCLK a CMOS clock driven input. Connecting PLL_EN LOW and REF_SEL HIGH will by pass the Phase locked loop. In this mode, FMS7951 will be in clock buffer mode where any clock applied to TCLK will be divided down to the four out-put banks. This is ideal for system diagnostic test. When PLL_EN is HIGH, the PLL is enabled, and any clock applied to TCLK will be locked in both phase and frequency to FBIN. PECL_CLK is activated when REF_SEL is high.

FMS7951 operates at 3.3 Volts and is available in 32 pin LQFP.

Block Diagram



Pin Assignments



Pin Description

Pin Name	Pin #	Pin Type	Description
VDDCOR	1	PWR	Power Connection. Power supply for core logic and PLL circuitry. Connect to 3.3 Volts nominal.
FBIN	2	IN	Feedback In. PLL feedback input. The user connects it to one of the outputs.
DIV_SEL(A:D)	3, 4, 5, 6	IN	Divider Select: It divides the clock to a desirable value. See table 2. No internal pull up or pull down.
GNDCOR	7	PWR	Ground Connection. Ground for core logic and PLL circuitry. Connect to the common system ground plane.
PECL_CLK/ PECL_CLK	8, 9	IN	PECL Clock Input: These are differential PECL inputs when REF_SEL is Low, they are activated.
OE	10	IN	Output Enable. When high, all outputs are in high impedance. Normal operation when asserted low.
VDDOUT	11, 15, 19, 23, 27	PWR	Power Connection. Power supply for all the output buffers. Connect to 3.3 Volts nominal.
QA; QB; QC(0:1); QD(0:4)	12, 14, 16, 18, 20, 22, 24, 26, 28	OUT	Clock Outputs. These outputs are multiple of the input.
GNDOUT	13, 17, 21, 25, 29	PWR	Ground Connection. Ground for all the outputs. Connect to common system ground plane.
TCLK	30	IN	Test Clock. When PLL-EN is low, all outputs are buffer copy of TCLK.
PLL_EN	31	IN	PLL Enable. When low, PLL is by passed.
REF_SEL	32	IN	Reference Select. When low, PECL_CLK/PECL_CLK is used for input. When high, TCLK is used for input.

Table 1. Functionality

REF_SEL	PLL_EN	\overline{OE}	PLL	All Outputs	Input
0	0	1	By Pass	Hi-Z	PECL_CLK
0	0	0	By Pass	Running	PECL_CLK
0	1	0	Enabled	Running	PECL_CLK
1	0	1	By Pass	Hi-Z	TCLK
1	0	0	By Pass	Running	TCLK
1	1	0	Enabled	Running	TCLK

Table 2. Input Versus Output Frequency

DIV_SEL A	DIV_SEL B	DIV_SEL C	DIV_SEL D	QA	QB	QC	QD
0	0	0	0	2XREF	REF	REF	REF
0	0	0	1	4XREF	2XREF	2XREF	REF
0	0	1	0	2XREF	REF	1/2REF	REF
0	0	1	1	4XREF	2XREF	REF	REF
0	1	0	0	2XREF	1/2REF	REF	REF
0	1	0	1	4XREF	REF	2XREF	REF
0	1	1	0	2XREF	1/2REF	1/2REF	REF
0	1	1	1	4XREF	REF	REF	REF
1	0	0	0	REF	REF	REF	REF
1	0	0	1	2XREF	2XREF	2XREF	REF
1	0	1	0	REF	REF	1/2REF	REF
1	0	1	1	2XREF	2XREF	REF	REF
1	1	0	0	REF	1/2REF	REF	REF
1	1	0	1	2XREF	REF	2XREF	REF
1	1	1	0	REF	1/2REF	1/2REF	REF
1	1	1	1	2XREF	REF	REF	REF

Note:

- Reference input could be either PECL_CLK or TCLK input.
- FBIN is tied to QD output for table

Table 3. Divide Select Functionality

DIV_SEL A	DIV_SEL B	DIV_SEL C	DIV_SEL D	QA	QB	QC	QD
0	0	0	0	÷2	÷4	÷4	÷4
1	1	1	1	÷4	÷8	÷8	÷8

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V _{DD} , V _{IN}	Voltage on any pin with respect to ground	-0.5 to 7.0	V
T _{STG}	Storage Temperature	-65 to 150	°C
T _B	Ambient Temperature	-55 to 125	°C
T _A	Operating Temperature	0 to 70	°C

Stresses greater than those listed in the table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may effect reliability.

DC Electrical Characteristics

T_A = 0 to 70°C; Supply Voltage 3.3 V ±0.2V (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V _{IL}	TCLK; control pins			0.8	V
Input High Voltage	V _{IH}	TCLK; control pins	2.0		3.6	V
Input Low Current	I _{IL}	V _{IN} = 0	-10		10	μA
Input High Current	I _{IH}	V _{IN} = V _{DD}	-30		30	μA
Peak to Peak Input Voltage	V _{PP}	PECL_CLK/PCL_CLK	0.3		1.0	V
Common Mode Range	V _{CMR}		V _{DD} -2.0		V _{DD} -0.6	mV
Output Low Voltage	V _{OL}	I _{OL} = 40 mA			0.5	V
Output High Voltage	V _{OH}	I _{OH} = -40mA	2.2			V
Input Capacitance ⁽¹⁾	C _{IN}				7.0	pF
Supply Current	I _{DD}	Outputs loaded		TBD	150	mA
Clock Stabilization ⁽¹⁾	T _{STAB}	From V _{DD} = 3.3V to 1% Target			10	mS

Note:

1. Guaranteed by design, not subject to 100% production testing.

AC Electrical Characteristics

T_A = 0 to 70°C; Supply Voltage V_{DD} = 3.3V ±0.2V, C_L = 10 pF (unless otherwise stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F _{IN}	Feedback Divide = 2	10		175	MHz
		Feedback Divide = 4	10		85	
		Feedback Divide = 8	10		42	
TCLK Input Rise/Fall Time ⁽¹⁾	T _{R_IN} /T _{F_IN}		–		3.0	ns
TCLK Input Duty Cycle ⁽¹⁾	D _{T_IN}		25		75	%
Output Frequency Range	F _{OUT}	Q _A ; DIV_SEL A = 0V			175	MHz
		Q _B , Q _C & Q _D ; DIV_SEL B, C, D = 0V			88	MHz
Output to Output Skew	T _{SK1}	V _{TH} = V _{DD} /2; DIV_SEL A = 0			750	pS
		V _{TH} = V _{DD} /2; DIV_SEL A = 1	-300		300	
Input to FBIN Delay	T _{SK2}	TCLK	50		400	pS
		PECL_CLK	-950		-600	

AC Electrical Characteristics (Cont.)

$T_A = 0$ to 70°C ; Supply Voltage $V_{DD} = 3.3\text{V} \pm 0.2\text{V}$, $C_L = 10\text{ pF}$ (unless otherwise stated)

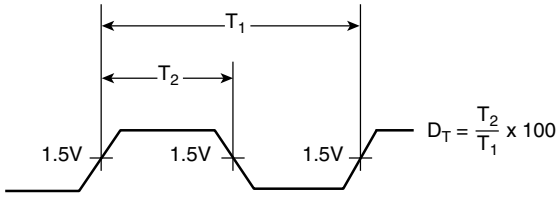
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Rise Time ⁽¹⁾	T_R	0.8 to 2.0V	0.10		1.0	nS
Fall Time ⁽¹⁾	T_F	2.0 to 0.8V	0.10		1.0	nS
Duty Cycle ⁽¹⁾	D_T	$V_{TH} = V_{DD}/2$	45		55	%
Jitter (Cycle-Cycle)	T_{JIT}	QA: DIV_SEL A = 0			450	pS
		QA: DIV_SEL A = 1			200	
		QB Output			200	
		QC(0:1) Outputs			300	
		QD(0:4) Outputs			375	

Note:

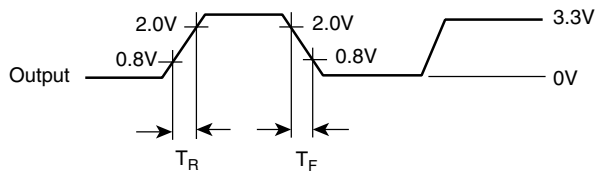
1. Guaranteed by design, not subject to 100% production testing.

Parameter Measurement Information

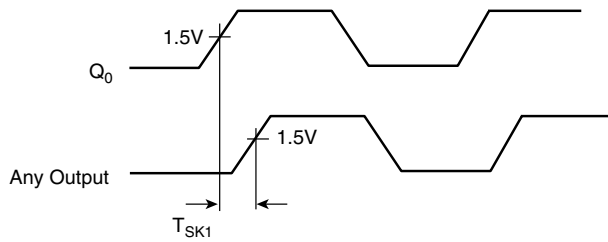
Duty Cycle (D_T)



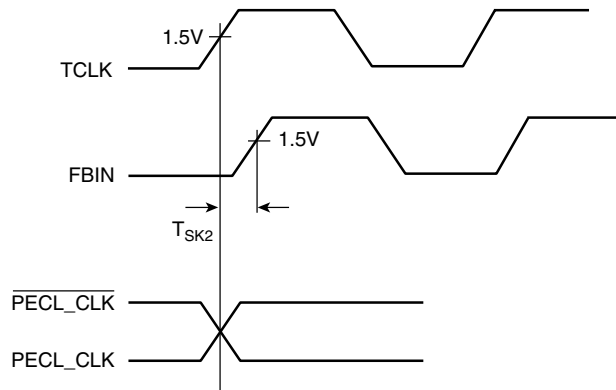
Rise/Fall Time (T_R/T_F)



Output to Output Skew (T_{SK1})



Input to Output Delay (T_{SK2})



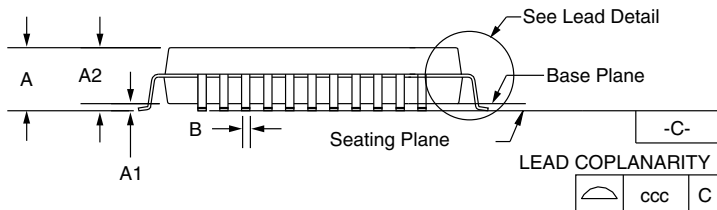
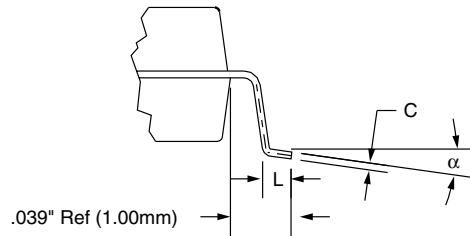
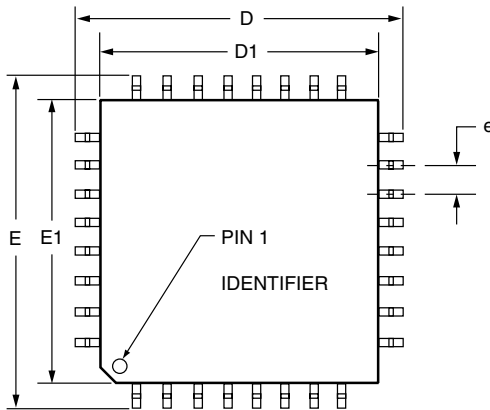
Mechanical Dimensions

32-Pin LQFP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	-	0.063	-	1.60	
A1	0.002	0.006	0.05	0.15	
A2	0.053	0.057	1.35	1.45	
B	0.012	0.018	0.30	0.45	7
C	-	0.004	-	0.10	
D/E	0.354 BSC		9.00 BSC		
D1/E1	0.276 BSC		7.00 BSC		2
e	0.032 BSC		0.800 BSC		
L	0.018	0.030	0.45	0.75	6
N	32		32		4
ND	8		8		5
α	0°	7°	0°	7°	
ccc	-	0.004	-	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.



Ordering Information

Product Number	Package Description	Package Marking
FMS7951KWC	LQFP-32	7951KWC
FMS7951KWCX	LQFP-32 w/T+R	7951KWC

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.