

SURFACE MOUNT SCR

DPAK (Plastic)	On-State Current 8 Amp	Gate Trigger Current < 200 μ A
	Off-State Voltage 200 V ÷ 600 V	
	These series of Silicon C ontrolled R ectifier use a high performance PNP technology. These parts are intended for general purpose applications where high gate sensitivity is required using surface mount technology.	

Absolute Maximum Ratings, according to IEC publication No. 134

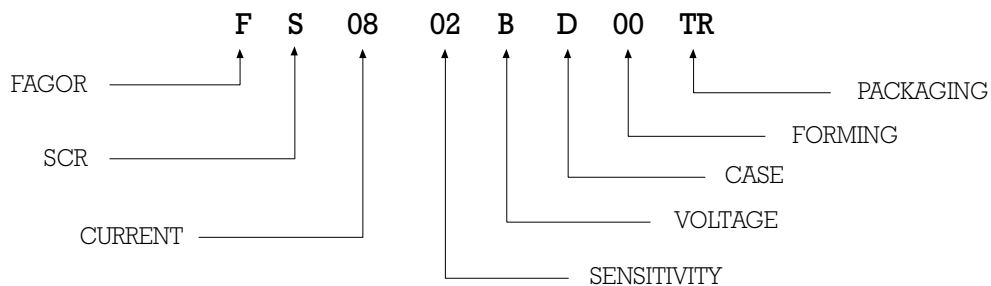
SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 110\text{ }^\circ\text{C}$		8	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $= 180^\circ$, $T_c = 110\text{ }^\circ\text{C}$		5	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz		73	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz		70	A
I^2t	Fusing Current	$t_p = 10\text{ms}$, Half Cycle		24	A^2s
V_{GRM}	Peak Reverse Gate Voltage	$I_{GR} = 10\text{ }\mu\text{A}$		8	V
I_{GM}	Peak Gate Current	20 μ s max.		4	A
P_{GM}	Peak Gate Dissipation	20 μ s max.		5	W
$P_{G(AV)}$	Gate Dissipation	20ms max.		1	W
T_j	Operating Temperature		-40	+125	$^\circ\text{C}$
T_{stg}	Storage Temperature		-40	+150	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max.		260	$^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{CK} = 1\text{ K}$	200	400	600	V

SURFACE MOUNT SCR

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY		Unit
				02		
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 140 \Omega, T_j = 25^\circ C$		MIN MAX	200	μA
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, R_{GK} = 220 \Omega, T_j = 125^\circ C$		MAX	1	mA
		$V_R = V_{RRM}, T_j = 25^\circ C$		MAX	5	μA
V_{TM}	On-state Voltage	at $I_T = 16 \text{ Amp}, t_p = 380 \mu s, T_j = 25^\circ C$		MAX	1.6	V
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 140 \Omega, T_j = 25^\circ C$		MAX	0.8	V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3K \Omega, R_{GK} = 220 \Omega, T_j = 125^\circ C$		MIN	0.1	V
I_H	Holding Current	$I_T = 50 \text{ mA}, R_{GK} = 1K \Omega, T_j = 25^\circ C$		MAX	5	mA
I_L	Latching Current	$I_G = 1 \text{ mA}, R_{GK} = 1K \Omega$		MAX	6	mA
dv / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, R_{GK} = 220 \Omega, T_j = 125^\circ C$		MIN	5	V/ μs
di / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, T_r = 100 \text{ ns}, F = 60 \text{ Hz}, T_j = 125^\circ C$		MIN	50	A/ μs
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC				20	$^\circ C/W$
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC				70	$^\circ C/W$
V_{t0}	Threshold Voltage	$T_j = 125^\circ C$		MAX	0.85	V
R_d	Dynamic resistance	$T_j = 125^\circ C$		MAX	46	m



SURFACE MOUNT SCR

Fig. 1: Maximum average power dissipation versus average on-state current.

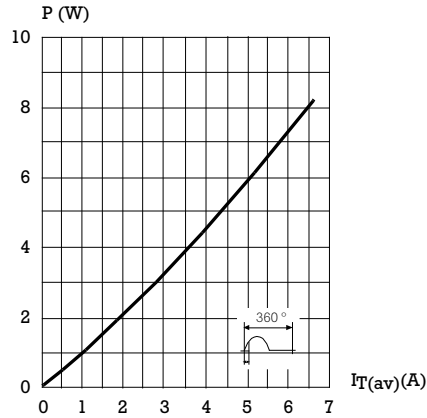


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

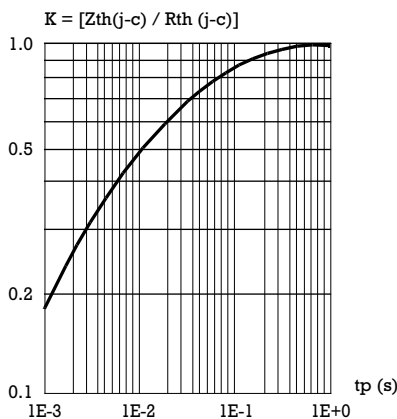


Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

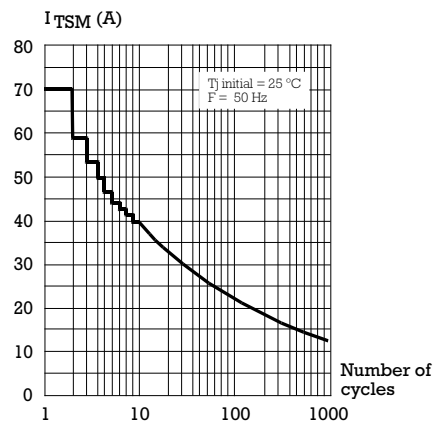


Fig. 2: Average and D.C. on-state current versus case temperature.

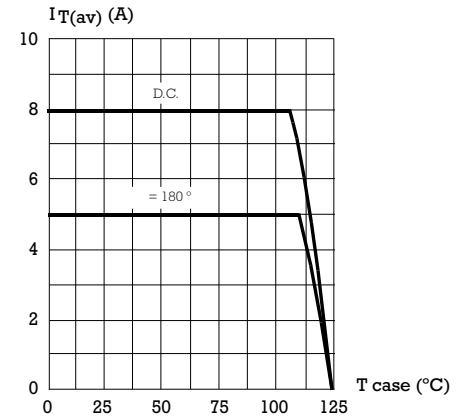
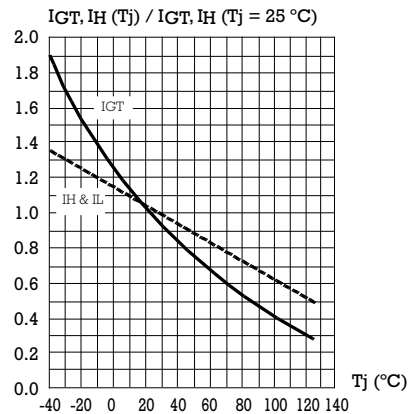
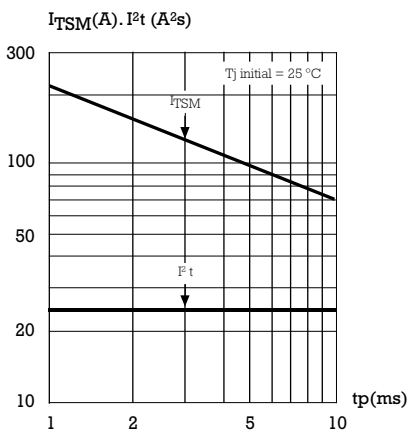
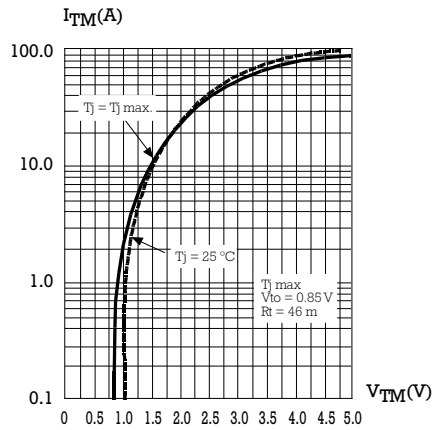


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

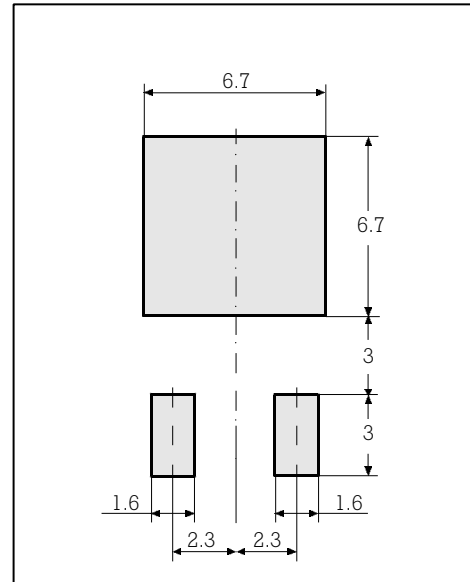

 Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10 \text{ ms}$, and corresponding value of I^2t .


SURFACE MOUNT SCR

Fig. 8: On-state characteristics (maximum values).



FOOT PRINT



PACKAGE MECHANICAL DATA DPAK TO 252-AA

REF.	DIMENSIONS		
	Millimeters		
	Min.	Nominal	Max.
A	2.18	2.3±0.18	2.39
A1	0	0.12	0.127
b	0.64	0.75±0.1	0.89
c	0.46		0.61
c1	0.46		0.56
c2		0.8±0.013	
D	5.97	6.1±0.1	6.22
D1	5.21		5.52
E	6.35	6.58±0.14	6.73
E1	5.20	5.36±0.1	5.46
e		2.28BSC	
H	9.40	9.90±0.15	10.41
L	1.40		1.78
L1	2.55	2.6±0.05	2.74
L2	0.46	0.5±0.013	0.58
L3	0.89	1.20±0.05	1.27
L4	0.64	0.83±0.1	1.02

Marking: type number
Weight: 0.2 g