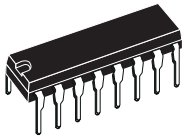
HCF40104B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

- MEDIUM SPEED OPERATION : 12 MHz (Typ.) at 10V
- FULLY STATIC OPERATION
- SYNCHRONOUS PARALLEL OR SERIAL OPERATION
- THREE-STATE OUTPUTS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

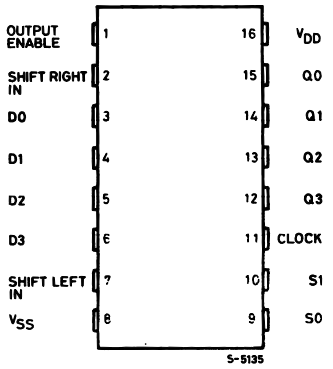
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF40104BEY	

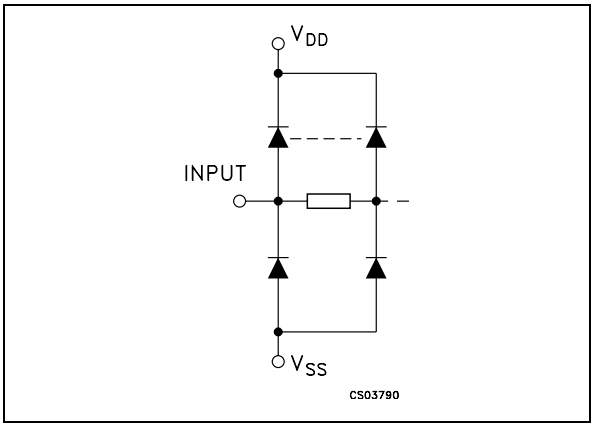
DESCRIPTION

HCF40104B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP packages.
HCF40104B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (SO and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are synchronously accomplished on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

PIN CONNECTION



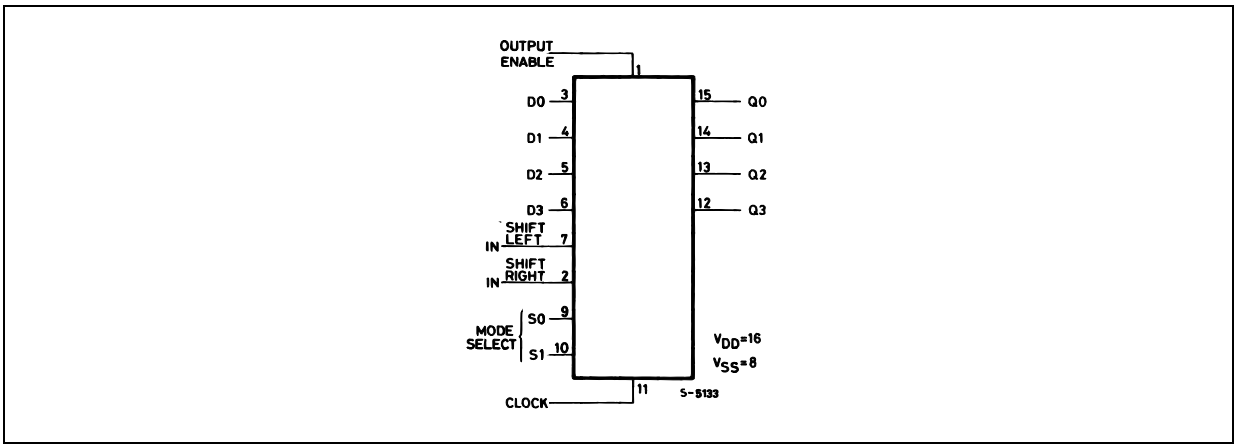
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	OUTPUT ENABLE	Output Enable
3, 4, 5, 6	D0 to D3	Inputs
15, 14, 13, 12	Q0 to Q3	Outputs
2	Shift Right IN	Shift Righ Input
7	Shift Left IN	Shift Left Input
11	CLOCK	Clock Input
9, 10	S0, S1	Input (High)
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

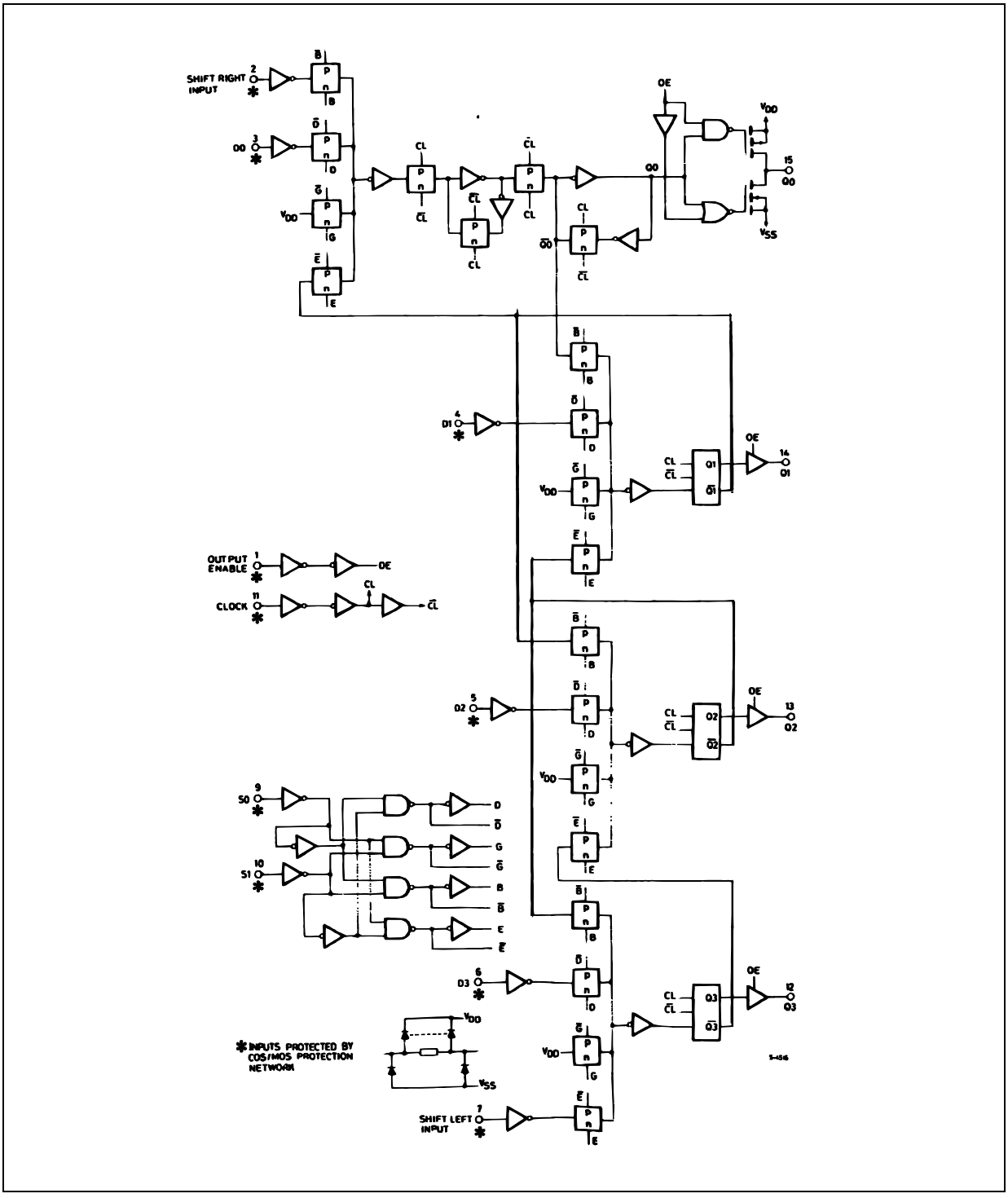


TRUTH TABLE

CLOCK	MODE SELECT		OUTPUT ENABLE	ACTION
	S0	S1		
⎍	L	L	H	RESET
⎍	H	L	H	SHIFT RIGHT (Q0 toward Q3)
⎍	L	H	H	SHIFT LEFT (Q3 toward Q0)
⎍	H	H	H	PARALLEL LOAD
X	X	X	L	Operations occur as shown above, but outputs assume high impedance

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

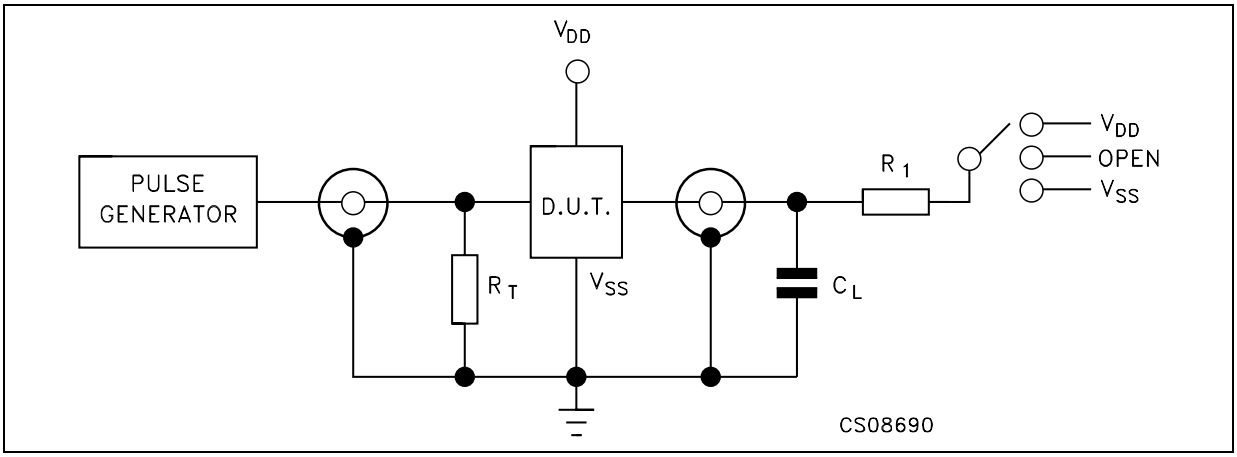
Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q	5			220	440	ns
		10			100	200	
		15			70	140	
t_{PZH},t_{PZL}, t_{PLZ}	3-State Outputs High Impedance	5			80	160	ns
		10			35	70	
		15			25	50	
t_{PHZ}		5			45	90	ns
		10			25	50	
		15			20	40	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Setup Time D0, D3, SR, SL to Clock	5			80	100	ns
		10			35	70	
		15			20	50	
	SO, S1 to Clock	5			200	400	ns
		10			110	220	
		15			65	130	
t_{hold}	Hold Time D0, D3, SR, SL to Clock	5			-65	0	ns
		10			-25	0	
		15			-15	0	
	SO, S1 to Clock	5			-170	0	ns
		10			-95	0	
		15			-55	0	
t_W	Clock Pulse Width	5			90	180	ns
		10			40	180	
		15			25	50	
f_{CL}	Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8	15		
t_r , t_f	Clock Input Rise or Fall Time	5				1000	µs
		10				100	
		15				100	

TEST CIRCUIT



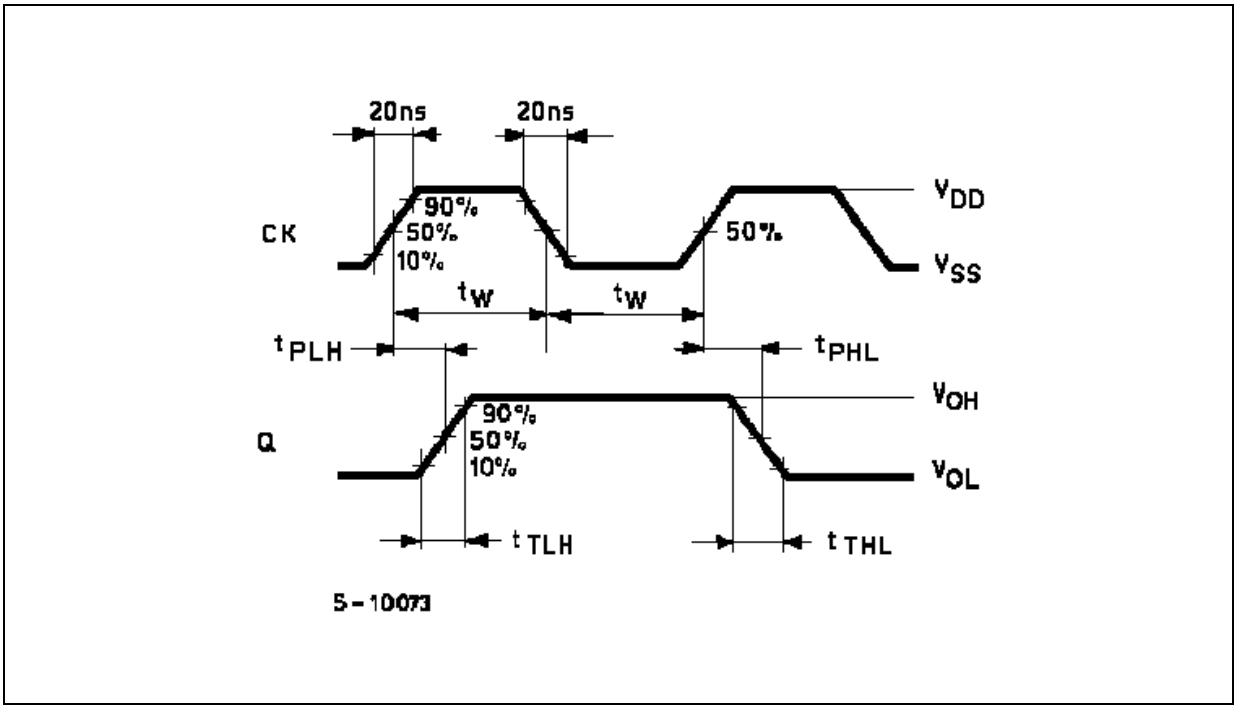
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{DD}
t_{PZH}, t_{PHZ}	V_{SS}

C_L = 50pF or equivalent (includes jig and probe capacitance)

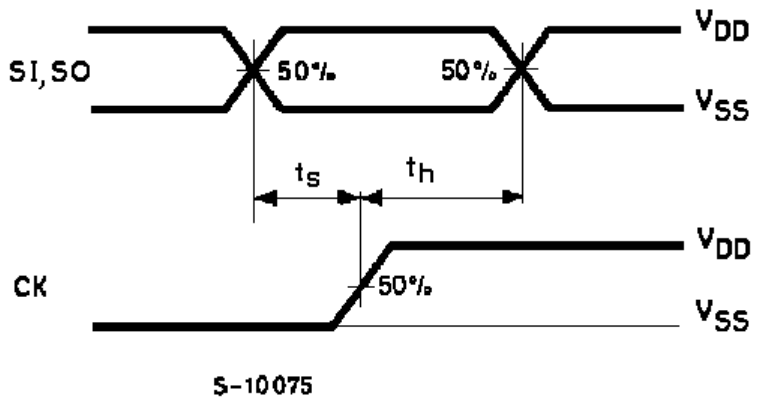
R_L = 200KΩ

R_T = Z_{OUT} of pulse generator (typically 50Ω)

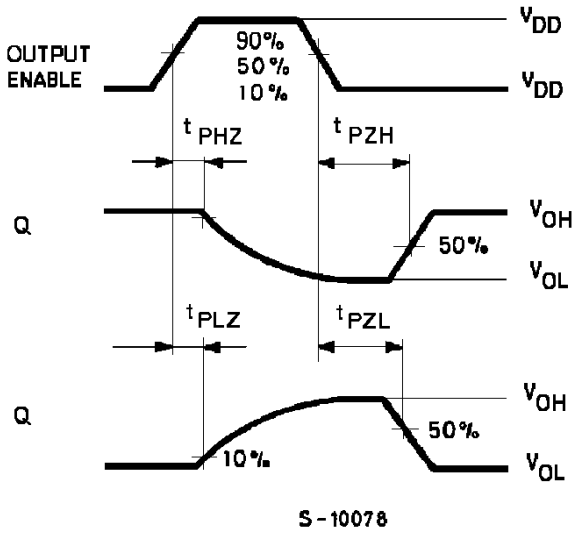
WAVEFORM 1 : CK TO Q PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2 : SI, SO SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)

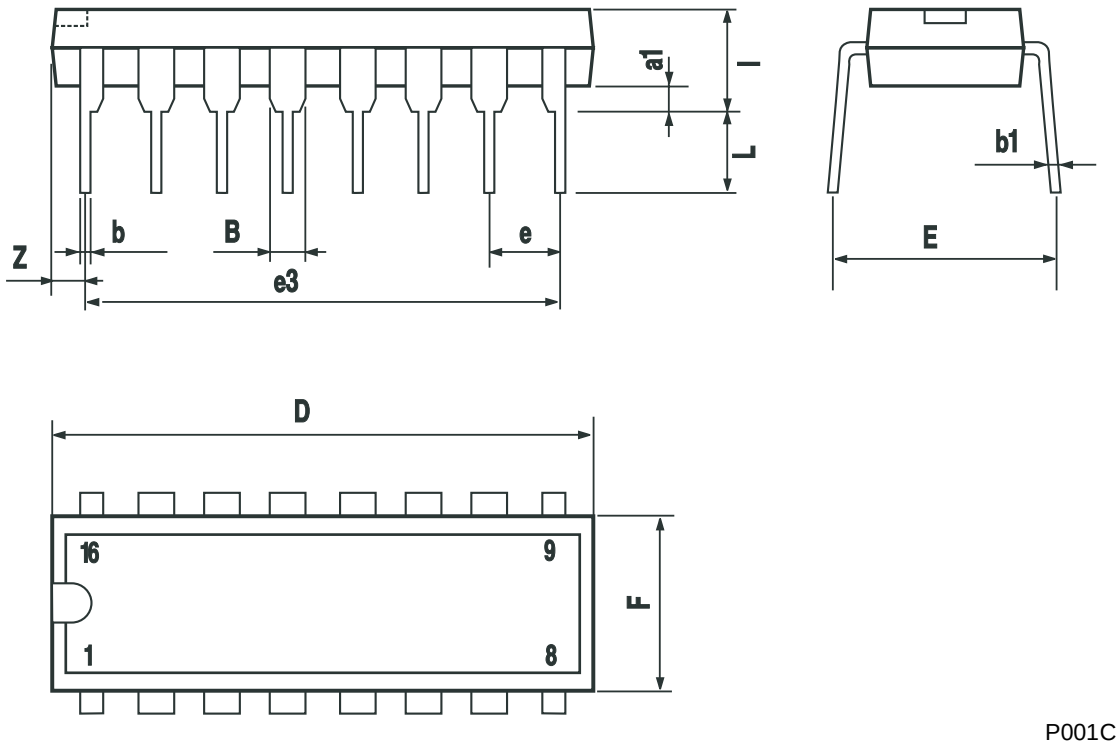


WAVEFORM 3 : OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



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