PRELIMINARY

Integrated Circuit Systems, Inc.

ICS858011

LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-CML FANOUT BUFFER

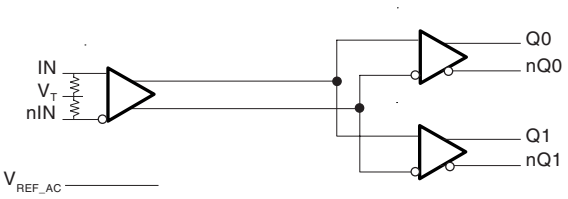
GENERAL DESCRIPTION

The ICS858011 is a high speed 1-to-2 Differential-to-CML Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS858011 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The ICS858011 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

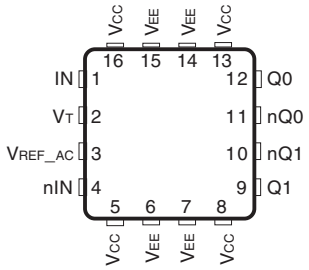
FEATURES

- 2 differential CML outputs
- 1 differential LVPECL clock input
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: > 2.5GHz (typical)
- Output skew: TBD
- Part-to-part skew: TBD
- Additive phase jitter, RMS: <100fs (design target)
- Propagation delay: 388ps (typical)
- Operating voltage supply range: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature
- Pin compatible with SY58011U

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS858011
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	IN	Input		Non-inverting LVPECL differential clock input.
2	V_T	Input		Termination input.
3	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. V_{REF_AC} = to V_{CC} - 1.38V.
4	nIN	Input		Inverting differential LVPECL clock input.
5, 8, 13, 16	V_{CC}	Power		Positive supply pins.
6, 7, 14, 15	V_{EE}	Power		Negative supply pin.
9, 10	Q1, nQ1	Output		Differential output pair. CML interface levels.
11, 12	nQ0, Q0	Output		Differential output pair. CML interface levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (CML mode, V_{EE} = 0)
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	20mA
Surge Current	40mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 2A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current			TBD		mA

TABLE 2B. DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)			100		Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current	(IN, nIN)				35	mA

NOTE 1: Refer to Parameter Measurement Information, Input Voltage Swing Diagram

TABLE 2C. CML DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.63V; V_{EE} = 0V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 0.020	V_{CC} - 0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing		325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		650	800		mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

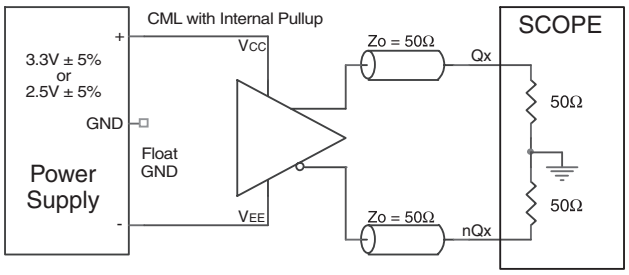
NOTE 1: Outputs terminated with 100Ω across differential output pair.

TABLE 3. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.63V TO -2.375V OR V_{CC} = 2.375 TO 3.63V; V_{EE} = 0V

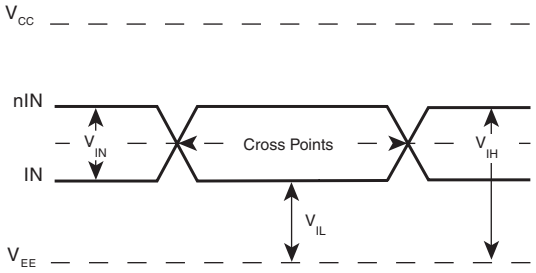
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			>2.5		GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1			388		ps
*t*sk(o)	Output Skew; NOTE 2, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			<100		fs
t_R/t_F	Output Rise/Fall Time	20% to 80%		120		ps

All parameters characterized at ≤ 1GHz unless otherwise noted.
R_L = 100Ω after each output pair.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

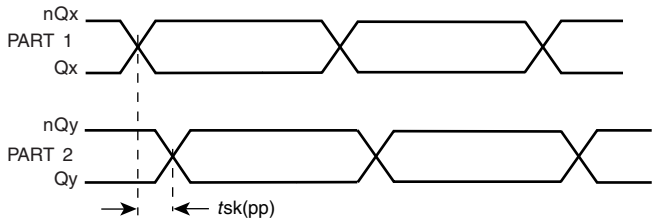
PARAMETER MEASUREMENT INFORMATION



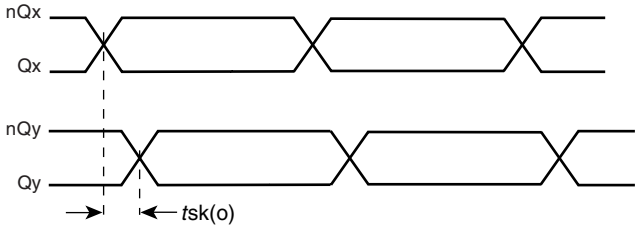
OUTPUT LOAD AC TEST CIRCUIT



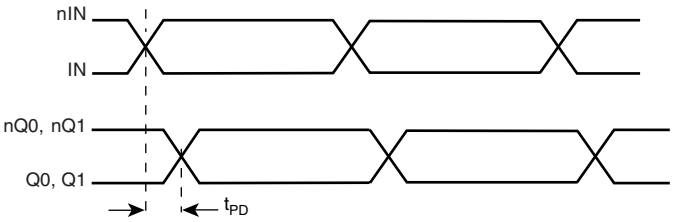
DIFFERENTIAL INPUT LEVEL



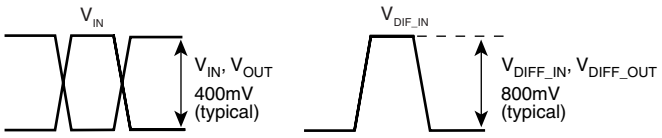
PART-TO-PART SKEW



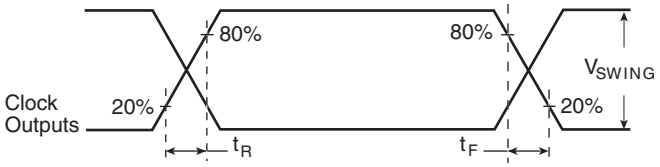
OUTPUT SKEW



PROPAGATION DELAY



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (2.5V)

The IN/nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

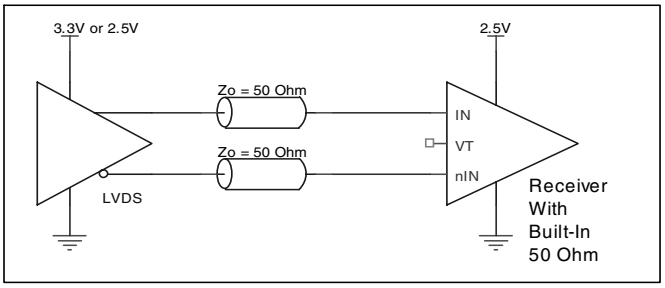


FIGURE 1A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

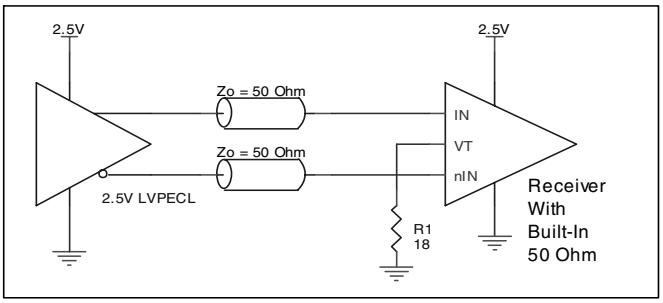


FIGURE 1B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

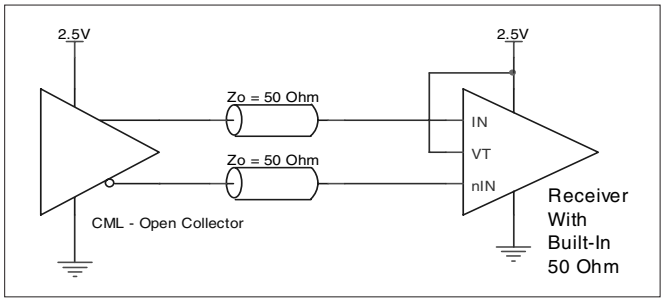


FIGURE 1C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

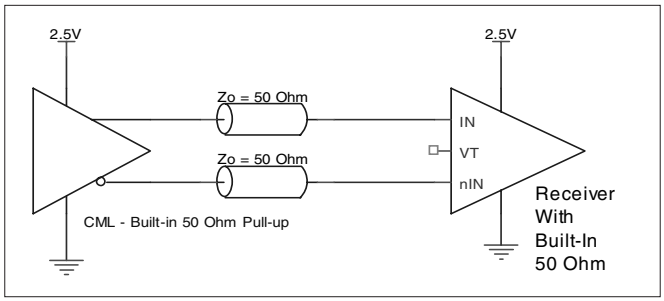


FIGURE 1D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

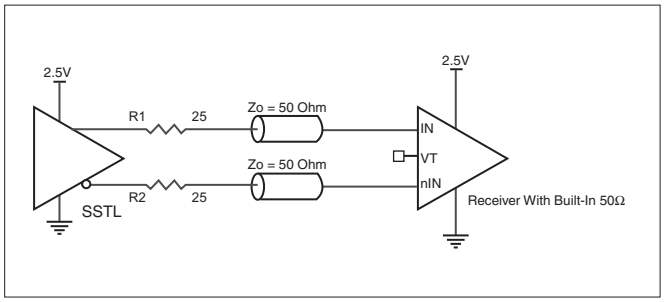


FIGURE 1E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (3.3V)

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

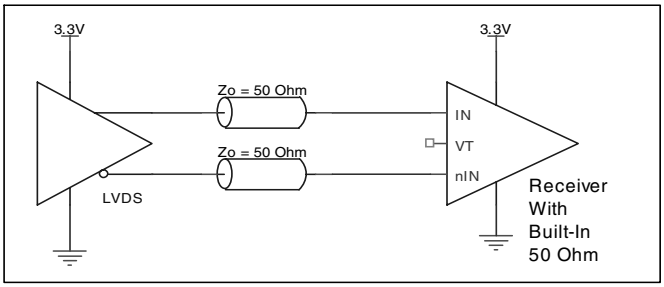


FIGURE 2A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

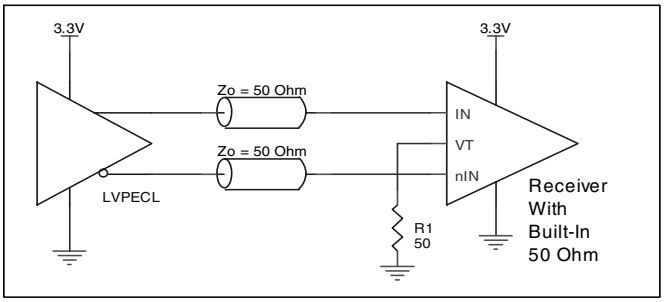


FIGURE 2B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

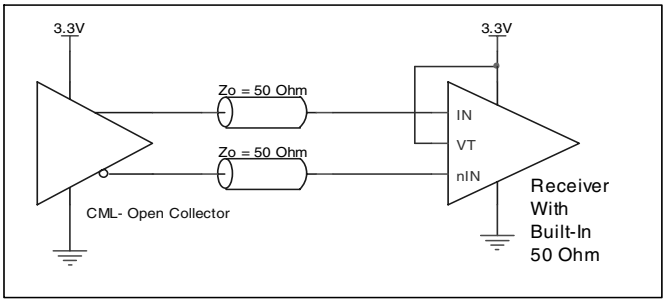


FIGURE 2C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

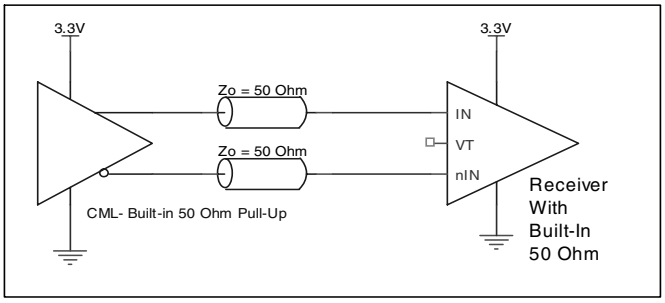


FIGURE 2D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

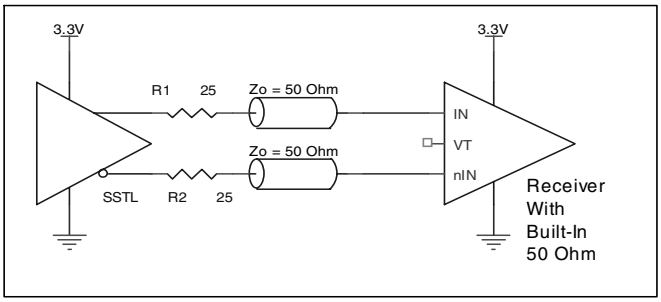


FIGURE 2E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 3.*

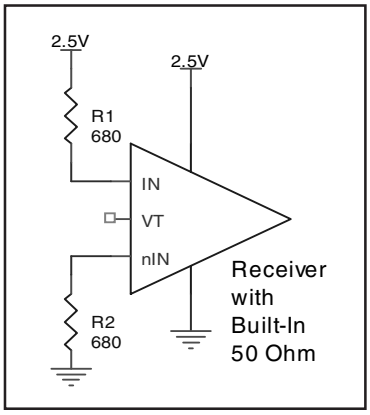


FIGURE 3. UNUSED INPUT HANDLING

3.3V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 4.*

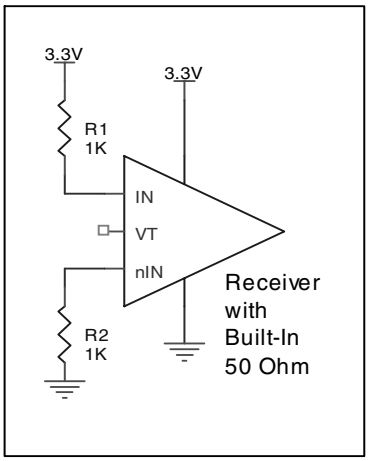


FIGURE 4. UNUSED INPUT HANDLING

SCHEMATIC EXAMPLE

Figure 5 shows a schematic example of the ICS858011. This schematic provides examples of input and output handling. The ICS858011 input has built-in 50Ω termination resistors. The input can directly accept various types of differential signal without AC couple. If AC couple termination is used, the ICS858011 also provides VREF_AC pin for proper offset level after AC couple. This example shows the ICS858011 input driven by a 2.5V LVPECL driver with AC couple. The ICS858011 outputs are CML driver with built-in 50Ω pull up resistors. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An external 100Ω resistor across the receiver input is required.

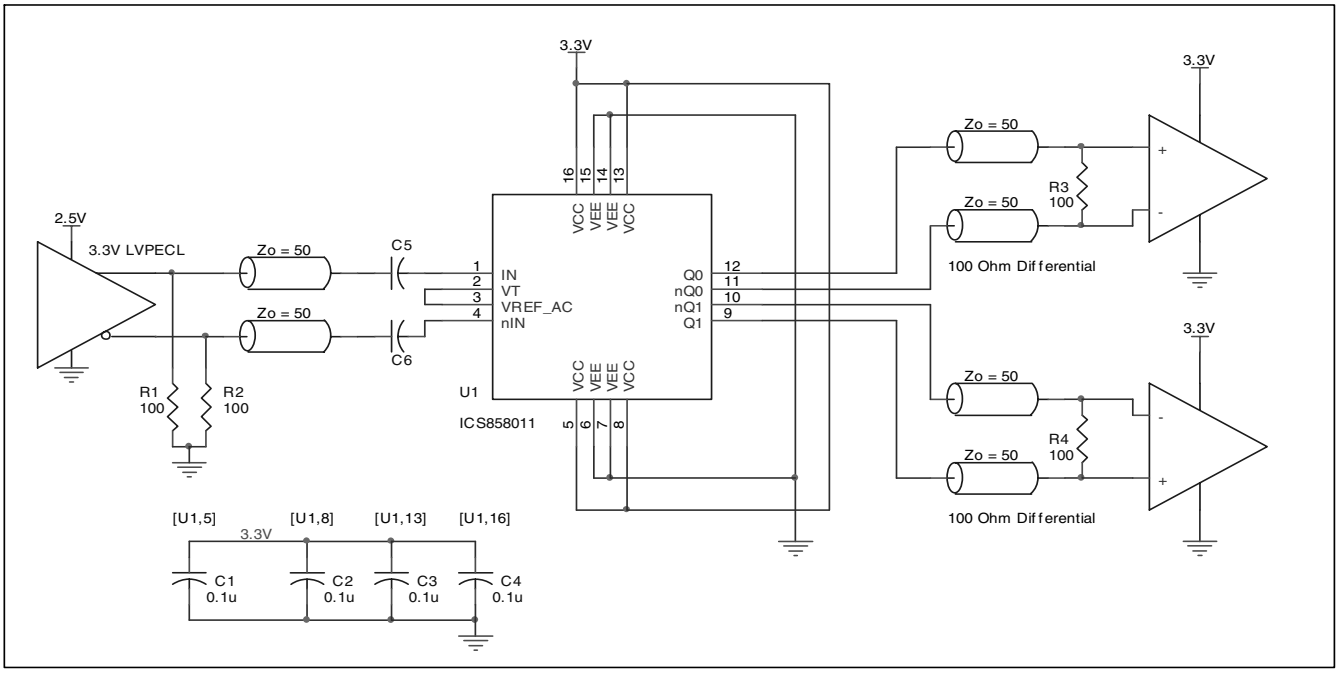


FIGURE 5. ICS858011 APPLICATION SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 4. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS858011 is: 109

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

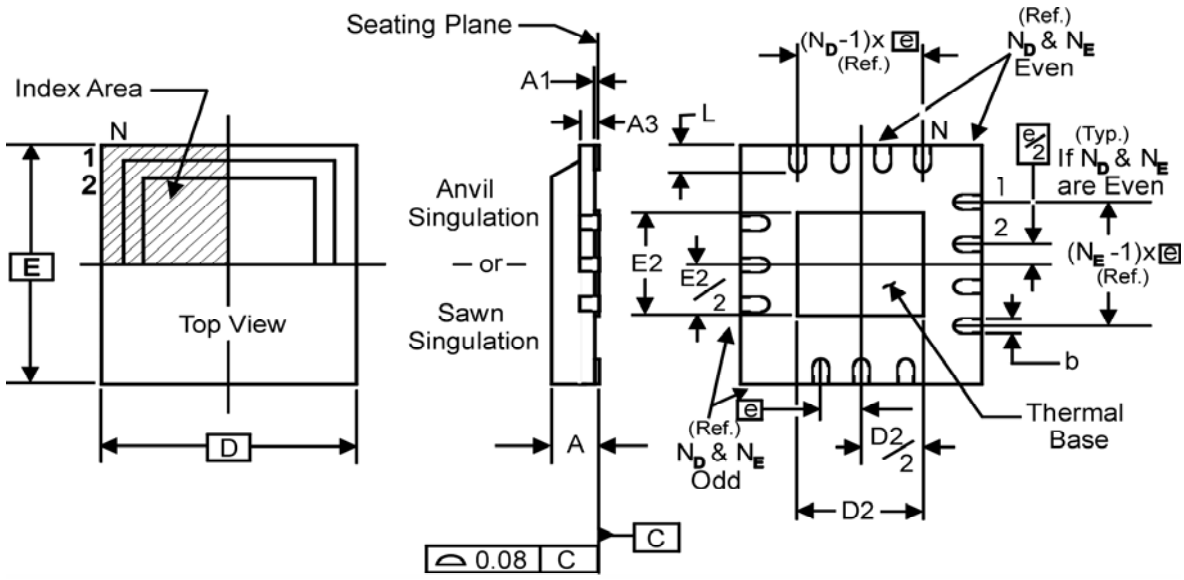


TABLE 5. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 6. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS858011AK	811A	16 Lead VFQFN	490 per tube	-40°C to 85°C
ICS858011AKT	811A	16 Lead VFQFN on Tape and Reel	2500	-40°C to 85°C