


FEATURES

- **Sample Rate: 170MSPS/135MSPS**
- **67.5dB SNR up to 140MHz Input**
- **80dB SFDR up to 170MHz Input**
- **775MHz Full Power Bandwidth S/H**
- **Single 3.3V Supply**
- **Low Power Dissipation: 890mW/660mW**
- LVDS, CMOS, or Demultiplexed CMOS Outputs
- Selectable Input Ranges: $\pm 0.5V$ or $\pm 1V$
- No Missing Codes
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Data Ready Output Clock
- Pin Compatible Family
 - 170MSPS: LTC2220 (12-Bit), LTC2230 (10-Bit)
 - 135MSPS: LTC2221 (12-Bit), LTC2231 (10-Bit)
- 64-Pin 9mm \times 9mm QFN Package

APPLICATIONS

- Wireless and Wired Broadband Communication
- Cable Head-End Systems
- Power Amplifier Linearization
- Communications Test Equipment

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DESCRIPTION

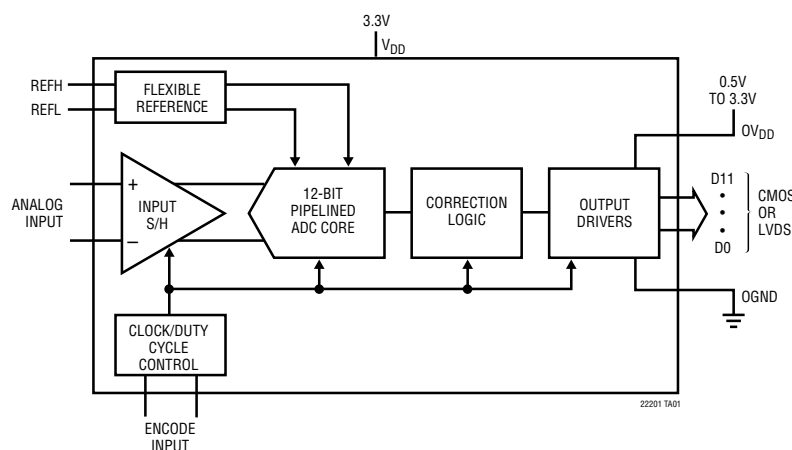
The LTC[®]2220 and LTC2221 are 170MSPS/135MSPS, sampling 12-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. The LTC2220/LTC2221 are perfect for demanding communications applications with AC performance that includes 67.5dB SNR and 80dB spurious free dynamic range for signals up to 170MHz. Ultralow jitter of 0.15ps_{RMS} allows undersampling of IF frequencies with excellent noise performance.

DC specs include ± 0.4 LSB INL (typ), ± 0.3 LSB DNL (typ) and no missing codes over temperature. The transition noise is a low 0.5LSB_{RMS}.

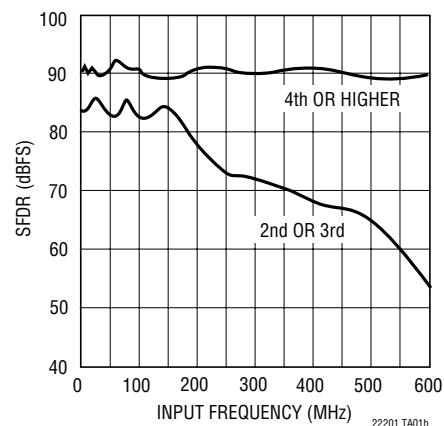
The digital outputs can be either differential LVDS, or single-ended CMOS. There are three format options for the CMOS outputs: a single bus running at the full data rate or two demultiplexed buses running at half data rate with either interleaved or simultaneous update. A separate output power supply allows the CMOS output swing to range from 0.5V to 3.3V.

The ENC⁺ and ENC⁻ inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



SFDR vs Input Frequency



22201p

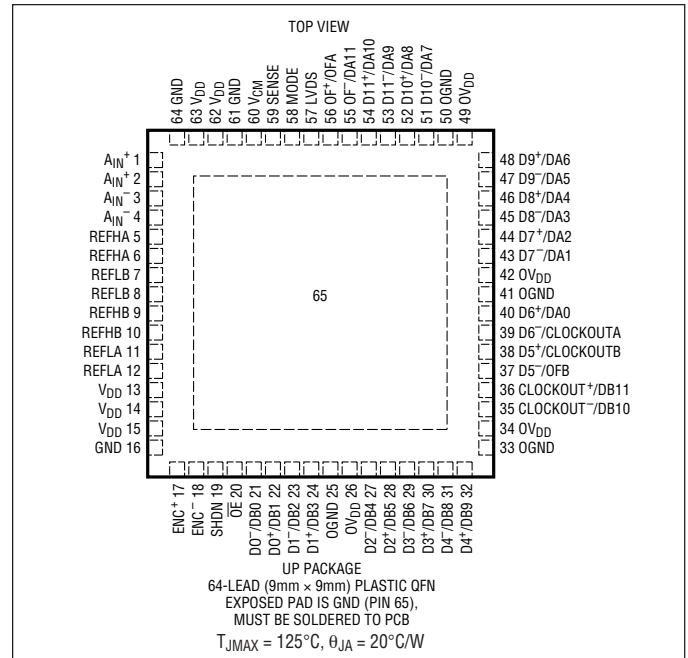
LTC2220/LTC2221

ABSOLUTE MAXIMUM RATINGS

$0V_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD})	4V
Digital Output Ground Voltage (OGND)	-0.3V to 1V
Analog Input Voltage (Note 3)	-0.3V to ($V_{DD} + 0.3V$)
Digital Input Voltage	-0.3V to ($V_{DD} + 0.3V$)
Digital Output Voltage	-0.3V to ($0V_{DD} + 0.3V$)
Power Dissipation	1500mW
Operating Temperature Range	
LTC2220C, LTC2221C	0°C to 70°C
LTC2220I, LTC2221I	-40°C to 85°C
Storage Temperature Range	-65°C to 125°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER	UP PART MARKING
LTC2220CUP	LTC2220UP
LTC2220IUP	LTC2220UP
LTC2221CUP	LTC2221UP
LTC2221IUP	LTC2221UP

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Note 4)

PARAMETER	CONDITIONS		LTC2220			LTC2221			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	Differential Analog Input (Note 5)	●	-1	±0.4	1	-1	±0.4	1	LSB
Differential Linearity Error	Differential Analog Input	●	-1	±0.3	1	-1	±0.2	1	LSB
Integral Linearity Error	Single-Ended Analog Input (Note 5)			±1			±1		LSB
Differential Linearity Error	Single-Ended Analog Input			±0.3			±0.2		LSB
Offset Error	(Note 6)	●	-20	±3	20	-20	±3	20	mV
Gain Error	External Reference	●	-3	±0.5	3	-3	±0.5	3	%FS
Offset Drift				±10			±10		μV/C
Full-Scale Drift	Internal Reference			±30			±30		ppm/C
	External Reference			±15			±15		ppm/C
Transition Noise	SENSE = 1V			0.5			0.5		LSB _{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	$3.1V < V_{DD} < 3.5V$	●	± 0.5 to ± 1		V	
$V_{IN, CM}$	Analog Input Common Mode	Differential Input	●	1	1.6	1.9	V
I_{IN}	Analog Input Leakage Current	$0 < A_{IN}^+, A_{IN}^- < V_{DD}$	●	-1	1	μA	
I_{SENSE}	SENSE Input Leakage	$0V < SENSE < 1V$	●	-1	1	μA	
I_{MODE}	MODE Pin Pull-Down Current to GND			10		μA	
I_{LVDS}	LVDS Pin Pull-Down Current to GND			10		μA	
t_{AP}	Sample and Hold Acquisition Delay Time			0		ns	
t_{JITTER}	Sample and Hold Acquisition Delay Time Jitter			0.15		pSRMS	
CMRR	Analog Input Common Mode Rejection Ratio			80		dB	
	Full Power Bandwidth	Figure 8 Test Circuit		775		MHz	

DYNAMIC ACCURACY

$T_A = 25^\circ\text{C}$, $A_{IN} = -1\text{dBFS}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LTC2220			LTC2221			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-Noise Ratio (Note 10)	5MHz Input (1V Range)		62.7			62.8		dB
		5MHz Input (2V Range)		67.7			67.8		dB
		70MHz Input (1V Range)		62.7			62.8		dB
		70MHz Input (2V Range)	66.5	67.6		66.5	67.8		dB
		140MHz Input (1V Range)		62.4			62.5		dB
		140MHz Input (2V Range)		67.5			67.5		dB
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic (Note 11)	5MHz Input (1V Range)		84			84		dB
		5MHz Input (2V Range)		84			84		dB
		70MHz Input (1V Range)		84			84		dB
		70MHz Input (2V Range)	75	84		75	84		dB
		140MHz Input (1V Range)		84			84		dB
		140MHz Input (2V Range)		84			84		dB
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher (Note 11)	5MHz Input (1V Range)		90			90		dB
		5MHz Input (2V Range)		90			90		dB
		70MHz Input (1V Range)		90			90		dB
		70MHz Input (2V Range)	80	90		80	90		dB
		140MHz Input (1V Range)		87			90		dB
		140MHz Input (2V Range)		87			90		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio (Note 12)	5MHz Input (1V Range)		62.7			62.8		dB
		5MHz Input (2V Range)		67.5			67.6		dB
		70MHz Input (1V Range)		62.7			62.8		dB
		70MHz Input (2V Range)	66	67.3		66	67.4		dB
IMD	Intermodulation Distortion	$f_{IN1} = 138\text{MHz}$, $f_{IN2} = 140\text{MHz}$		81			81		dBc

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	$I_{OUT} = 0$	1.575	1.600	1.625	V
V_{CM} Output Tempco			±25		ppm/C
V_{CM} Line Regulation	$3.1V < V_{DD} < 3.5V$		3		mV/V
V_{CM} Output Resistance	$-1mA < I_{OUT} < 1mA$		4		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
ENCODE INPUTS (ENC+, ENC-)							
V_{ID}	Differential Input Voltage		●	0.2		V	
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	●	1.1	1.6 2.5	V V	
R_{IN}	Input Resistance			6		k Ω	
C_{IN}	Input Capacitance	(Note 7)		3		pF	
LOGIC INPUTS (\overline{OE}, SHDN)							
V_{IH}	High Level Input Voltage	$V_{DD} = 3.3V$	●	2		V	
V_{IL}	Low Level Input Voltage	$V_{DD} = 3.3V$	●		0.8	V	
I_{IN}	Input Current	$V_{IN} = 0V$ to V_{DD}	●	-10	10	μA	
C_{IN}	Input Capacitance	(Note 7)		3		pF	
LOGIC OUTPUTS (CMOS MODE)							
$OV_{DD} = 3.3V$							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE} = \text{High}$ (Note 7)		3		pF	
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		50		mA	
I_{SINK}	Output Sink Current	$V_{OUT} = 3.3V$		50		mA	
V_{OH}	High Level Output Voltage	$I_O = -10\mu\text{A}$ $I_O = -200\mu\text{A}$	●	3.1	3.295 3.29	V V	
V_{OL}	Low Level Output Voltage	$I_O = 10\mu\text{A}$ $I_O = 1.6\text{mA}$	●		0.005 0.09	V V	
$OV_{DD} = 2.5V$							
V_{OH}	High Level Output Voltage	$I_O = -200\mu\text{A}$		2.49		V	
V_{OL}	Low Level Output Voltage	$I_O = 1.6\text{mA}$		0.09		V	
$OV_{DD} = 1.8V$							
V_{OH}	High Level Output Voltage	$I_O = -200\mu\text{A}$		1.79		V	
V_{OL}	Low Level Output Voltage	$I_O = 1.6\text{mA}$		0.09		V	
LOGIC OUTPUTS (LVDS MODE)							
V_{OD}	Differential Output Voltage	100 Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100 Ω Differential Load	●	1.125	1.250	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	LTC2220			LTC2221			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{DD}	Analog Supply Voltage		●	3.1	3.3	3.5	3.1	3.3	3.5	V
P_{SHDN}	Shutdown Power	SHDN = High, \overline{OE} = High, No CLK			2			2		mW
P_{NAP}	Nap Mode Power	SHDN = High, \overline{OE} = Low, No CLK			35			35		mW

LVDS OUTPUT MODE

OV_{DD}	Output Supply Voltage		●	3	3.3	3.6	3	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		264	290		196	216	mA
I_{OVDD}	Output Supply Current		●		55	61		55	61	mA
P_{DISS}	Power Dissipation		●		1050	1160		828	915	mW

CMOS OUTPUT MODE

OV_{DD}	Output Supply Voltage		●	0.5	3.3	3.6	0.5	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		264	290		196	216	mA
P_{DISS}	Power Dissipation				890			660		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LTC2220			LTC2221			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
f_S	Sampling Frequency		●	1		170	1		135	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off	●	2.8	2.94	500	3.5	3.7	500	ns
		Duty Cycle Stabilizer On	●	2	2.94	500	2	3.7	500	ns
t_H	ENC High Time	Duty Cycle Stabilizer Off	●	2.8	2.94	500	3.5	3.7	500	ns
		Duty Cycle Stabilizer On	●	2	2.94	500	2	3.7	500	ns
t_{AP}	Sample-and-Hold Aperture Delay				0			0		ns
$t_{\overline{OE}}$	Output Enable Delay	(Note 7)	●		5	10		5	10	ns

LVDS OUTPUT MODE

t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.2	3.5	1.3	2.2	3.5	ns
t_C	ENC to CLOCKOUT Delay	(Note 7)	●	1.3	2.2	3.5	1.3	2.2	3.5	ns
	DATA to CLOCKOUT Skew	$(t_C - t_D)$ (Note 7)	●	-0.6	0	0.6	-0.6	0	0.6	ns
	Rise Time				0.5			0.5		ns
	Fall Time				0.5			0.5		ns
	Pipeline Latency				5			5		Cycles

CMOS OUTPUT MODE

t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.1	3.5	1.3	2.1	3.5	ns
t_C	ENC to CLOCKOUT Delay	(Note 7)	●	1.3	2.1	3.5	1.3	2.1	3.5	ns
	DATA to CLOCKOUT Skew	$(t_C - t_D)$ (Note 7)	●	-0.6	0	0.6	-0.6	0	0.6	ns
Pipeline Latency	Full Rate CMOS				5			5		Cycles
	Demuxed Interleaved				5			5		Cycles
	Demuxed Simultaneous				5 and 6			5 and 6		Cycles

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD} , they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: $V_{DD} = 3.3V$, $f_{SAMPLE} = 170MHz$ (LTC2220) or $135MHz$ (LTC2221), LVDS outputs, differential $ENC^+/ENC^- = 2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a “best straight line” fit to the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from -0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

Note 8: Recommended operating conditions.

Note 9: $V_{DD} = 3.3V$, $f_{SAMPLE} = 170MHz$ (LTC2220) or $135MHz$ (LTC2221), differential $ENC^+/ENC^- = 2V_{P-P}$ sine wave, input range = $1V_{P-P}$ with differential drive, output $C_{LOAD} = 5pF$.

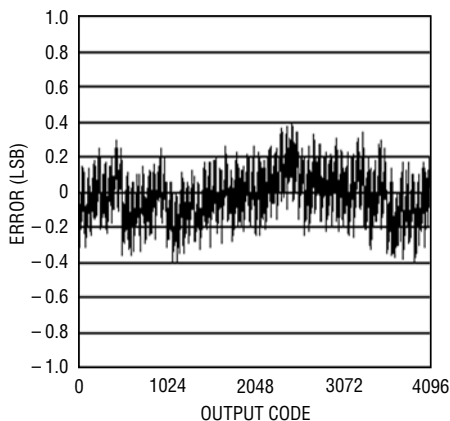
Note 10: SNR minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.7dB to 0.9dB lower.

Note 11: SFDR minimum values are for LVDS mode. Typical values are for both LVDS and CMOS modes.

Note 12: SINAD minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.5dB to 0.9dB lower.

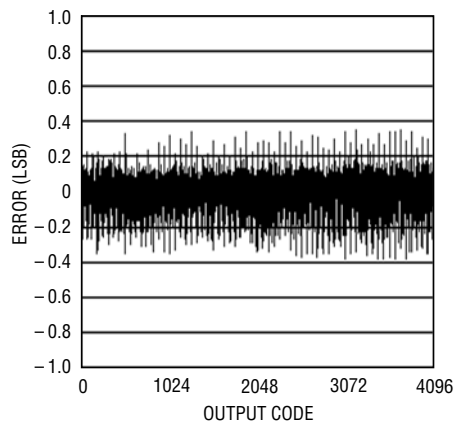
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise noted, Note 4)

LTC2220: INL, 2V Range



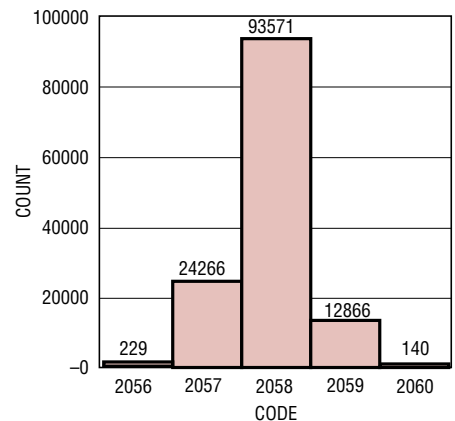
2220 G01

LTC2220: DNL, 2V Range



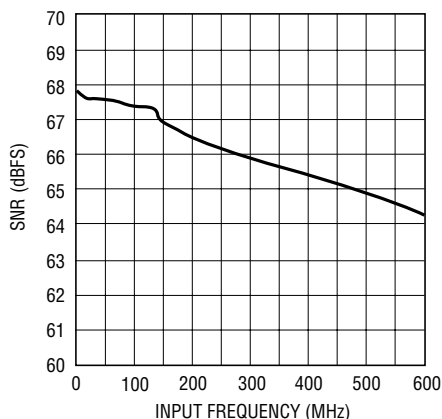
2220 G02

LTC2220: Noise Histogram



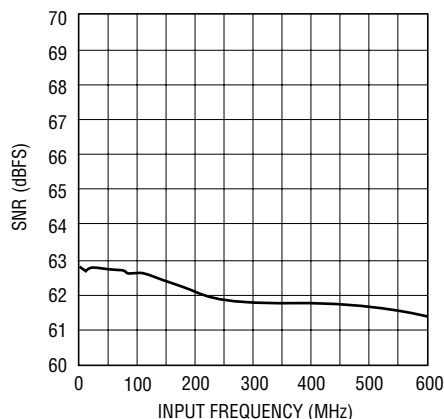
2220 G03

LTC2220: SNR vs Input Frequency, -1dB, 2V Range, LVDS Mode



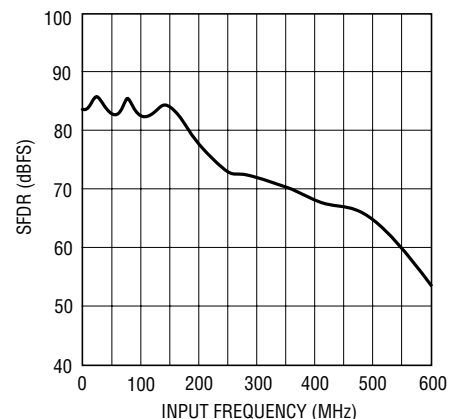
2220 G04

LTC2220: SNR vs Input Frequency, -1dB, 1V Range, LVDS Mode



2220 G05

LTC2220: SFDR (HD2 and HD3) vs Input Frequency, -1dB, 2V Range, LVDS Mode

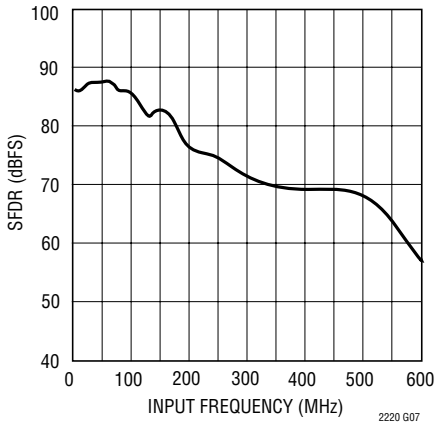


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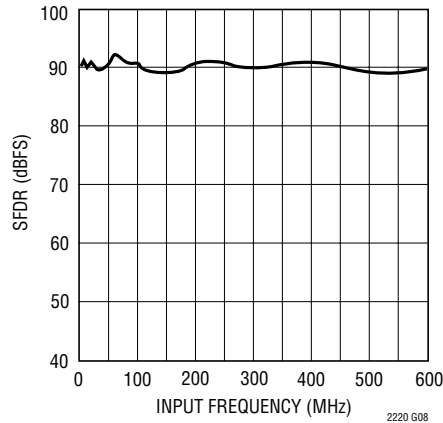
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TYPICAL PERFORMANCE CHARACTERISTICS

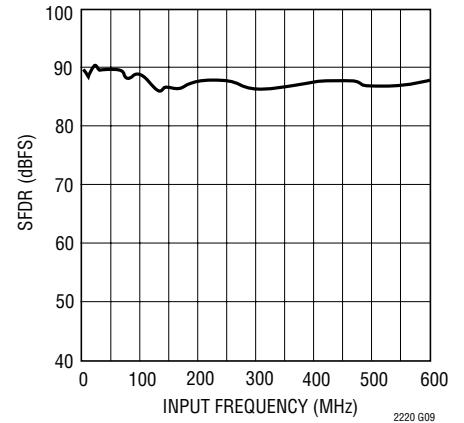
LTC2220: SFDR (HD2 and HD3) vs Input Frequency, -1dB, 1V Range, LVDS Mode



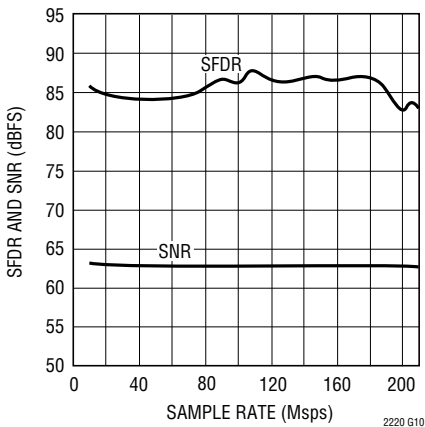
LTC2220: SFDR (HD4+) vs Input Frequency, -1dB, 2V Range, LVDS Mode



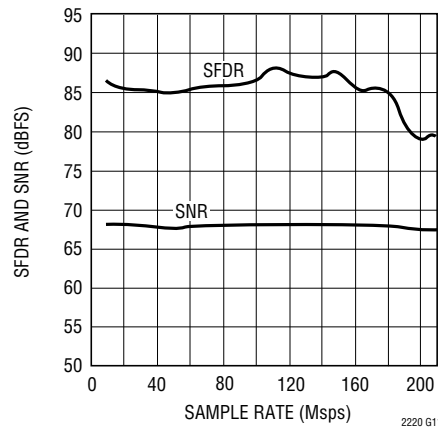
LTC2220: SFDR (HD4+) vs Input Frequency, -1dB, 1V Range, LVDS Mode



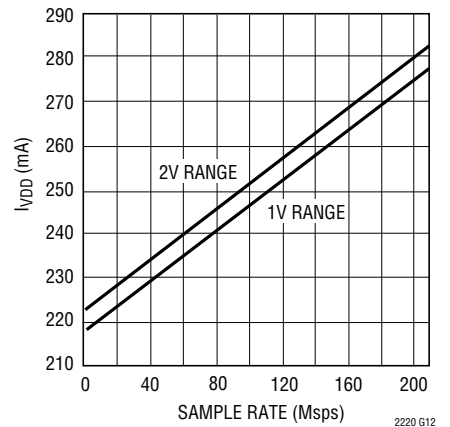
LTC2220: SFDR and SNR vs Sample Rate, 2V Range, $f_{IN} = 30\text{MHz}$, -1dB, LVDS Mode



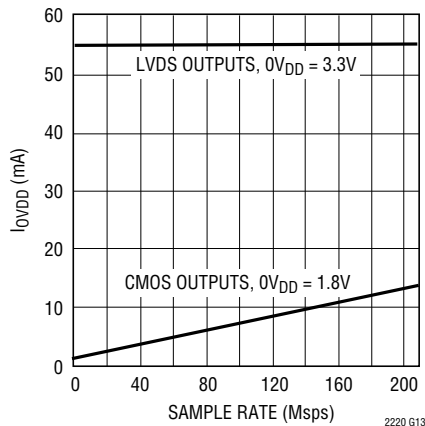
LTC2220: SFDR and SNR vs Sample Rate, 1V Range, $f_{IN} = 30\text{MHz}$, -1dB, LVDS Mode



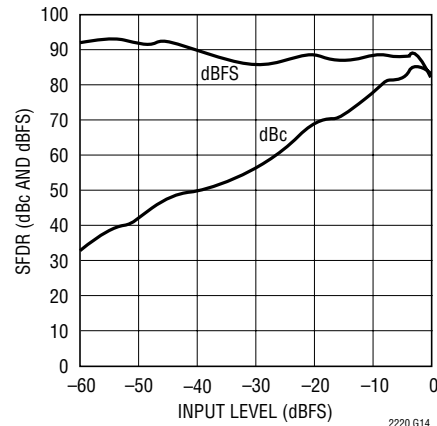
LTC2220: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, -1dB



LTC2220: I_{OVPD} vs Sample Rate, 5MHz Sine Wave Input, -1dB

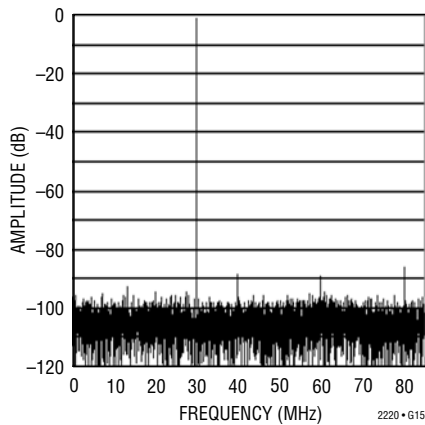


LTC2220: SFDR vs Input Level, $f_{IN} = 70\text{MHz}$, 2V Range

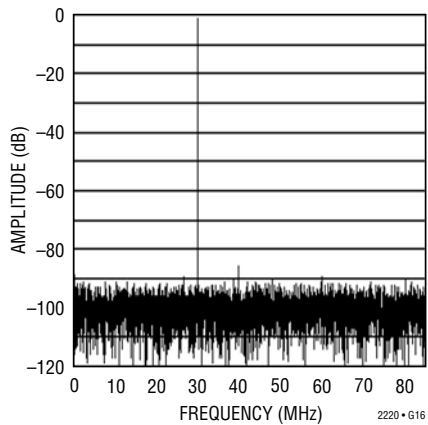


TYPICAL PERFORMANCE CHARACTERISTICS

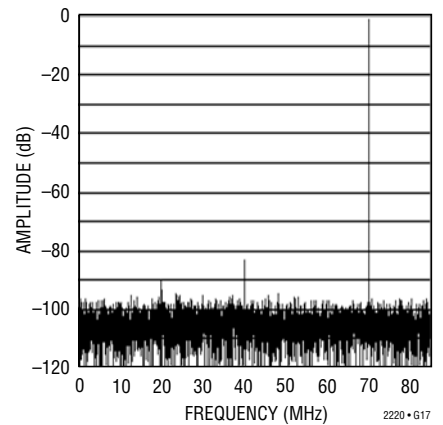
**LTC2220: 8192 Point FFT,
f_{IN} = 30MHz, -1dB, 2V Range,
LVDS Mode**



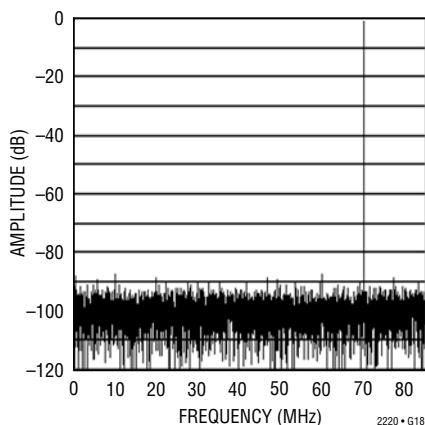
**LTC2220: 8192 Point FFT,
f_{IN} = 30MHz, -1dB, 1V Range,
LVDS Mode**



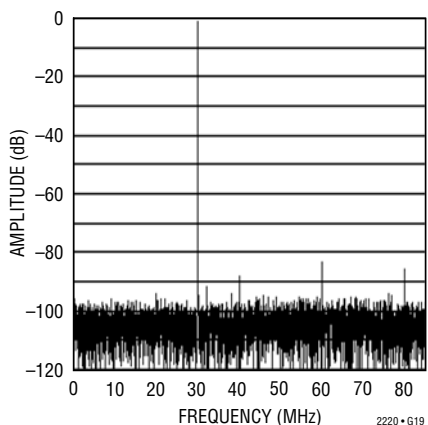
**LTC2220: 8192 Point FFT,
f_{IN} = 70MHz, -1dB, 2V Range,
LVDS Mode**



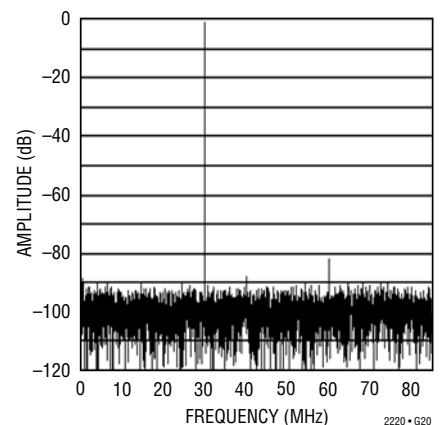
**LTC2220: 8192 Point FFT,
f_{IN} = 70MHz, -1dB, 1V Range,
LVDS Mode**



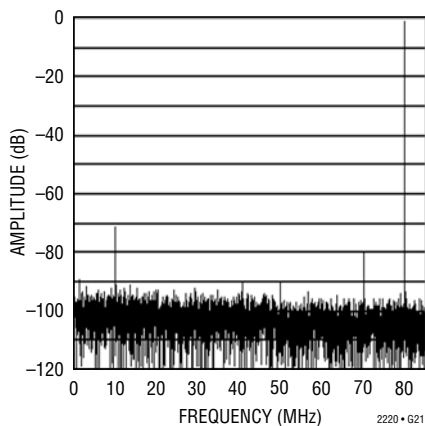
**LTC2220: 8192 Point FFT,
f_{IN} = 140MHz, -1dB, 2V
Range, LVDS Mode**



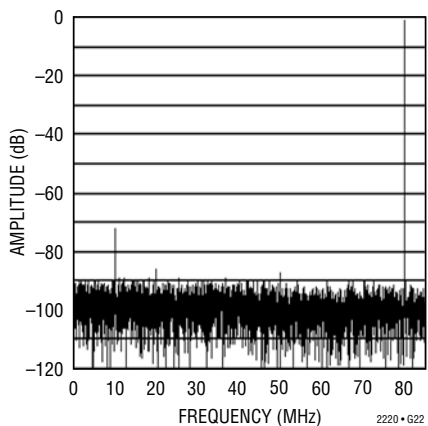
**LTC2220: 8192 Point FFT,
f_{IN} = 140MHz, -1dB, 1V
Range, LVDS Mode**



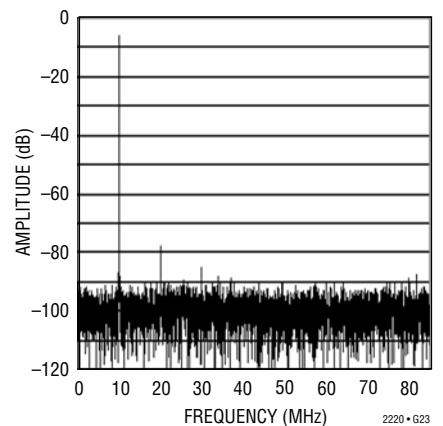
**LTC2220: 8192 Point FFT,
f_{IN} = 250MHz, -1dB, 2V
Range, LVDS Mode**



**LTC2220: 8192 Point FFT,
f_{IN} = 250MHz, -1dB, 1V
Range, LVDS Mode**

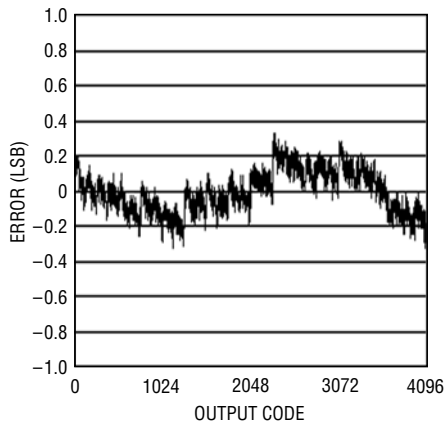


**LTC2220: 8192 Point FFT,
f_{IN} = 500MHz, -6dB, 1V
Range, LVDS Mode**



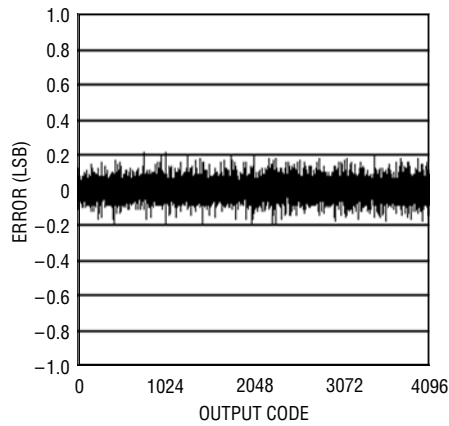
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2221: INL, 2V Range



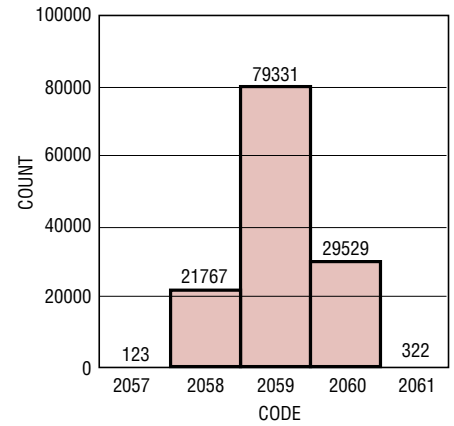
2221 G01

LTC2221: DNL, 2V Range



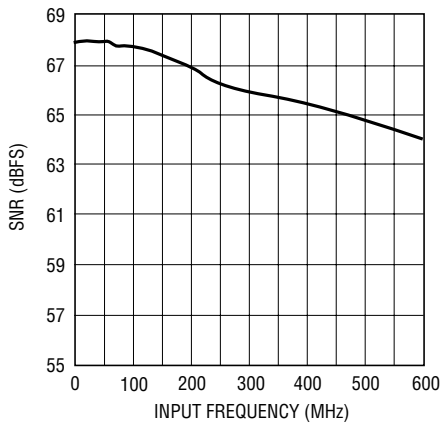
2221 G02

LTC2221: Noise Histogram



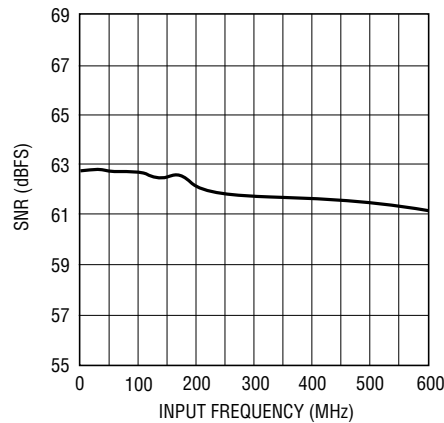
2221 G03

LTC2221: SNR vs Input Frequency, -1dB, 2V Range, LVDS Mode



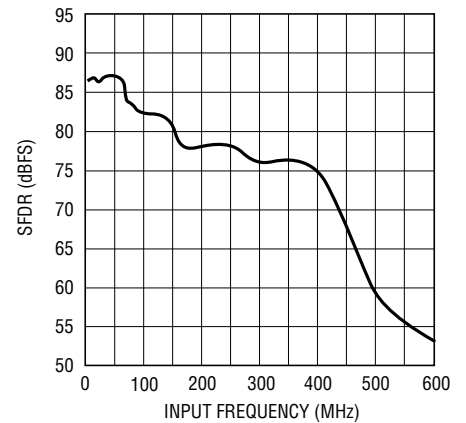
2221 G04

LTC2221: SNR vs Input Frequency, -1dB, 1V Range, LVDS Mode



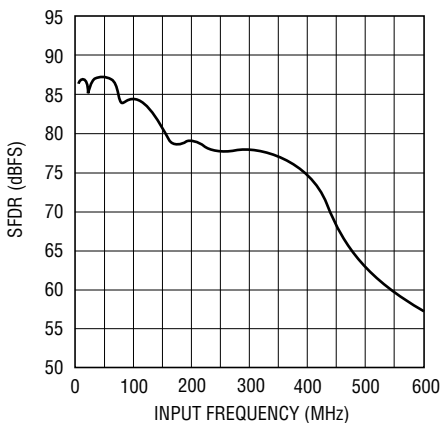
2221 G05

LTC2221: SFDR (HD2 and HD3) vs Input Frequency, -1dB, 2V Range, LVDS Mode



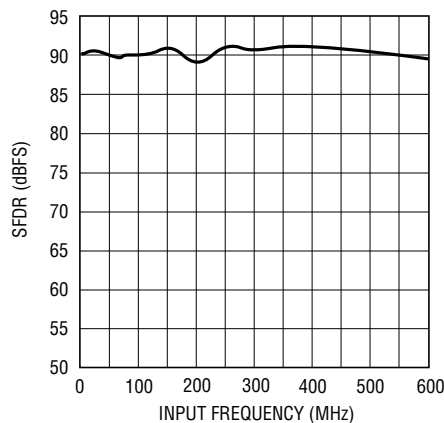
2221 G06

LTC2221: SFDR (HD2 and HD3) vs Input Frequency, -1dB, 1V Range, LVDS Mode



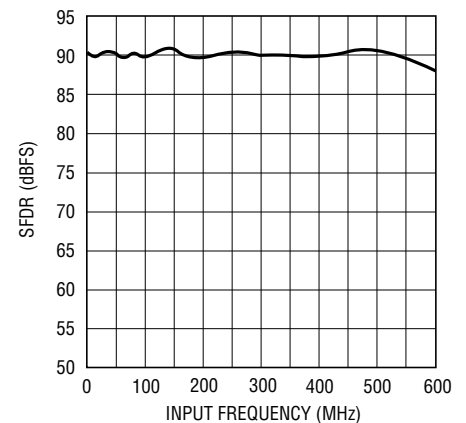
2221 G07

LTC2221: SFDR (HD4+) vs Input Frequency, -1dB, 2V Range, LVDS Mode



2221 G08

LTC2221: SFDR (HD4+) vs Input Frequency, -1dB, 1V Range, LVDS Mode

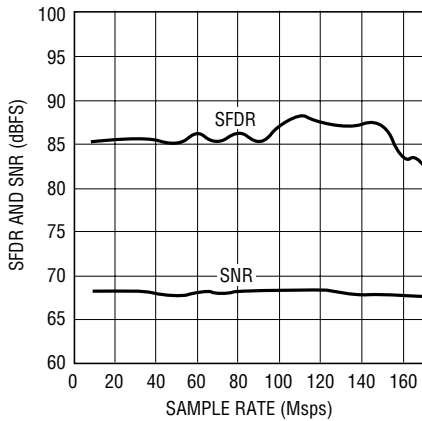


2221 G09

22201p

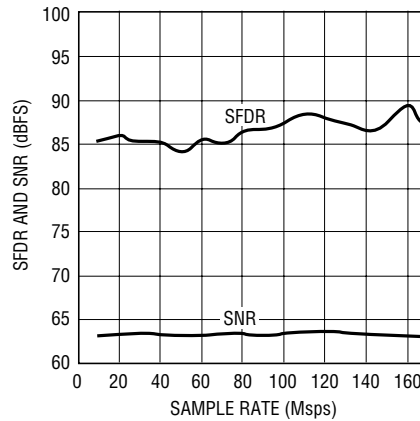
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2221: SFDR and SNR vs Sample Rate, 2V Range, $f_{IN} = 30\text{MHz}$, -1dB , LVDS Mode



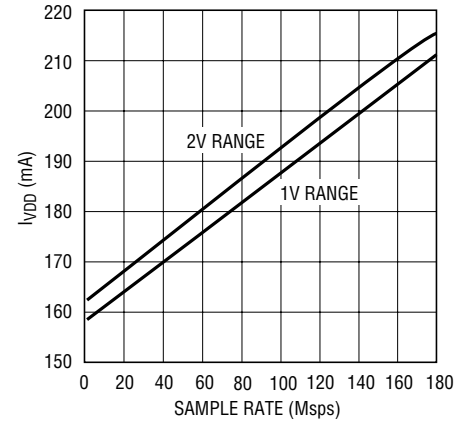
2221 G10

LTC2221: SFDR and SNR vs Sample Rate, 1V Range, $f_{IN} = 30\text{MHz}$, -1dB , LVDS Mode



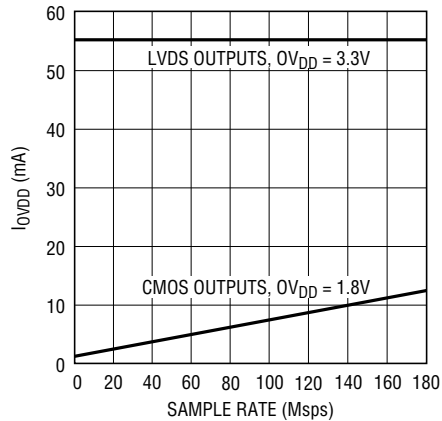
2221 G11

LTC2221: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, -1dB



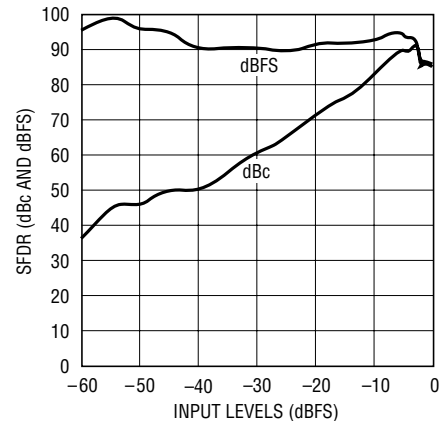
2221 G12

LTC2221: I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, -1dB



2221 G13

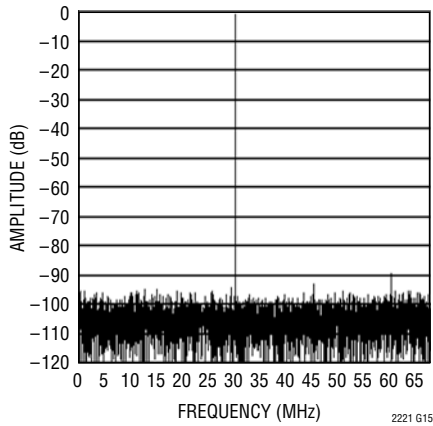
LTC2221: SFDR vs Input Level, $f_{IN} = 70\text{MHz}$, 2V Range



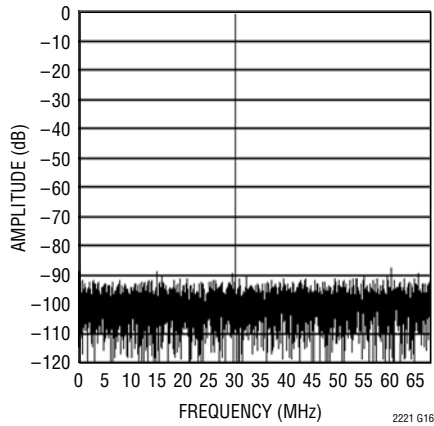
2221 G14

TYPICAL PERFORMANCE CHARACTERISTICS

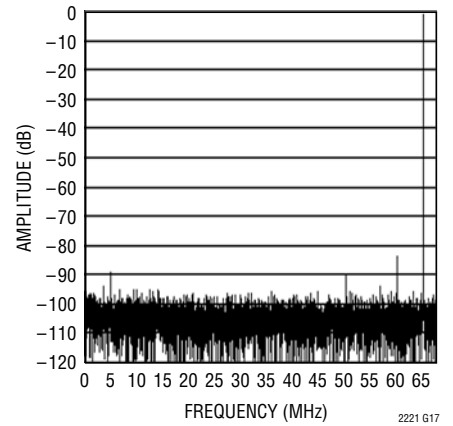
**LTC2221: 8192 Point FFT,
f_{IN} = 30MHz, -1dB, 2V Range,
LVDS Mode**



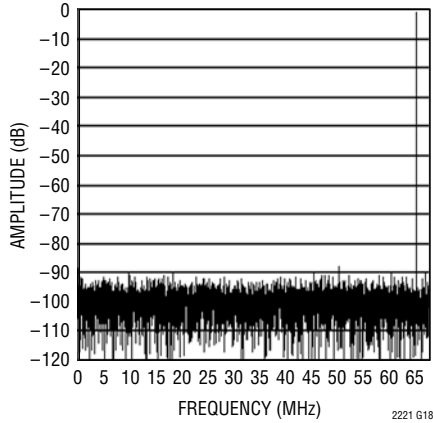
**LTC2221: 8192 Point FFT,
f_{IN} = 30MHz, -1dB, 1V Range,
LVDS Mode**



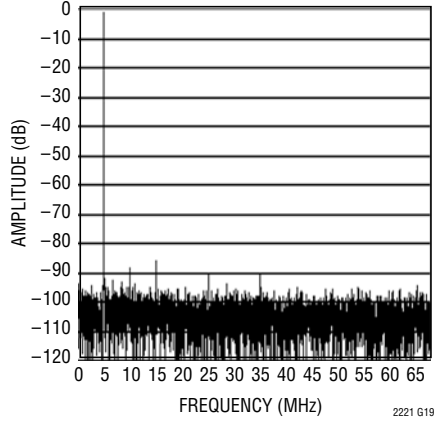
**LTC2221: 8192 Point FFT,
f_{IN} = 70MHz, -1dB, 2V Range,
LVDS Mode**



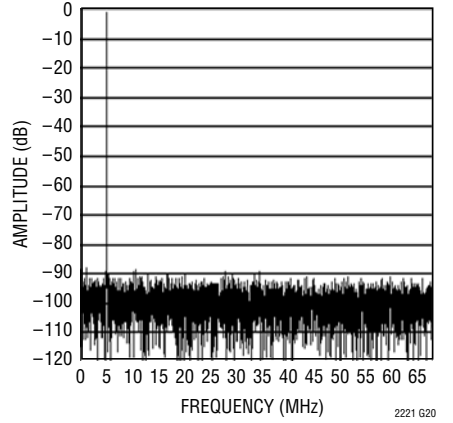
**LTC2221: 8192 Point FFT,
f_{IN} = 70MHz, -1dB, 1V Range,
LVDS Mode**



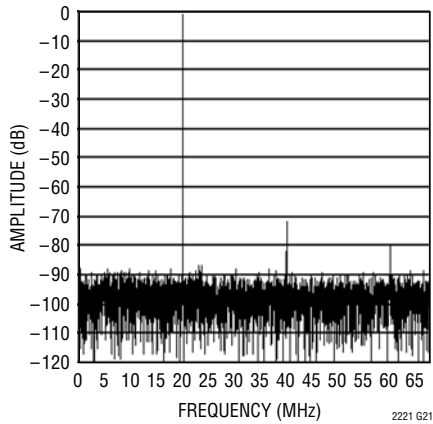
**LTC2221: 8192 Point FFT,
f_{IN} = 140MHz, -1dB, 2V
Range, LVDS Mode**



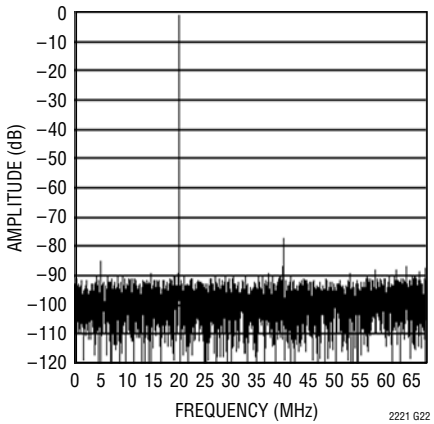
**LTC2221: 8192 Point FFT,
f_{IN} = 140MHz, -1dB, 1V
Range, LVDS Mode**



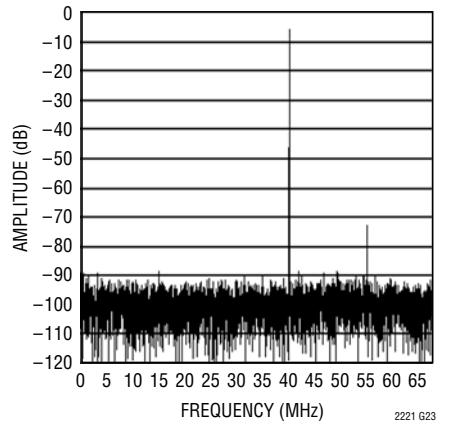
**LTC2221: 8192 Point FFT,
f_{IN} = 250MHz, -1dB, 2V
Range, LVDS Mode**



**LTC2221: 8192 Point FFT,
f_{IN} = 250MHz, -1dB, 1V
Range, LVDS Mode**



**LTC2221: 8192 Point FFT,
f_{IN} = 500MHz, -6dB, 1V
Range, LVDS Mode**



PIN FUNCTIONS

(CMOS Mode)

A_{IN}⁺ (Pins 1, 2): Positive Differential Analog Input.

A_{IN}⁻ (Pins 3, 4): Negative Differential Analog Input.

REFHA (Pins 5, 6): ADC High Reference. Bypass to Pins 7, 8 with 0.1 μ F ceramic chip capacitor, to Pins 11, 12 with a 2.2 μ F ceramic capacitor and to ground with 1 μ F ceramic capacitor.

REFLB (Pins 7, 8): ADC Low Reference. Bypass to Pins 5, 6 with 0.1 μ F ceramic chip capacitor. Do not connect to Pins 11, 12.

REFHB (Pins 9, 10): ADC High Reference. Bypass to Pins 11, 12 with 0.1 μ F ceramic chip capacitor. Do not connect to Pins 5, 6.

REFLA (Pins 11, 12): ADC Low Reference. Bypass to Pins 9, 10 with 0.1 μ F ceramic chip capacitor, to Pins 5, 6 with a 2.2 μ F ceramic capacitor and to ground with 1 μ F ceramic capacitor.

V_{DD} (Pins 13, 14, 15, 62, 63): 3.3V Supply. Bypass to GND with 0.1 μ F ceramic chip capacitors.

GND (Pins 16, 61, 64): ADC Power Ground.

ENC⁺ (Pin 17): Encode Input. Conversion starts on the positive edge.

ENC⁻ (Pin 18): Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1 μ F ceramic for single-ended ENCODE signal.

SHDN (Pin 19): Shutdown Mode Selection Pin. Connecting SHDN to GND and \overline{OE} to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and \overline{OE} to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and \overline{OE} to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and \overline{OE} to V_{DD} results in sleep mode with the outputs at high impedance.

\overline{OE} (Pin 20): Output Enable Pin. Refer to SHDN pin function.

DB0 - DB11 (Pins 21, 22, 23, 24, 27, 28, 29, 30, 31, 32, 35, 36): Digital Outputs, B bus. DB11 is the MSB. At high impedance in full rate CMOS mode.

OGND (Pins 25, 33, 41, 50): Output Driver Ground.

OV_{DD} (Pins 26, 34, 42, 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1 μ F ceramic chip capacitor.

OFB (Pin 37): Over/Under Flow Output for B bus. High when an over or under flow has occurred. At high impedance in full rate CMOS mode.

CLKOUTB (Pin 38): Data Valid Output for B bus. In demux mode with interleaved update, latch B bus data on the falling edge of CLKOUTB. In demux mode with simultaneous update, latch B bus data on the rising edge of CLKOUTB. This pin does not become high impedance in full rate CMOS mode.

CLKOUTA (Pin 39): Data Valid Output for A bus. Latch A bus data on the falling edge of CLKOUTA.

DA0 - DA11 (Pins 40, 43, 44, 45, 46, 47, 48, 51, 52, 53, 54, 55): Digital Outputs, A bus. DA11 is the MSB.

OFA (Pin 56): Over/Under Flow Output for A bus. High when an over or under flow has occurred.

LVDS (Pin 57): Output Mode Selection Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3V_{DD} selects demux CMOS mode with simultaneous update. Connecting LVDS to 2/3V_{DD} selects demux CMOS mode with interleaved update. Connecting LVDS to V_{DD} selects LVDS mode.

MODE (Pin 58): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects straight binary output format and turns the clock duty cycle stabilizer off. Connecting MODE to 1/3V_{DD} selects straight binary output format and turns the clock duty cycle stabilizer on. Connecting MODE to 2/3V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. Connecting MODE to V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 59): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a $\pm 0.5V$ input range. Connecting SENSE to V_{DD} selects the internal reference and a $\pm 1V$ input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. $\pm 1V$ is the largest valid input range.

V_{CM} (Pin 60): 1.6V Output and Input Common Mode Bias. Bypass to ground with 2.2 μ F ceramic chip capacitor.

GND (Exposed Pad): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

PIN FUNCTIONS

(LVDS Mode)

AIN⁺ (Pins 1, 2): Positive Differential Analog Input.

AIN⁻ (Pins 3, 4): Negative Differential Analog Input.

REFHA (Pins 5, 6): ADC High Reference. Bypass to Pins 7, 8 with 0.1 μ F ceramic chip capacitor, to Pins 11, 12 with a 2.2 μ F ceramic capacitor and to ground with 1 μ F ceramic capacitor.

REFLB (Pins 7, 8): ADC Low Reference. Bypass to Pins 5, 6 with 0.1 μ F ceramic chip capacitor. Do not connect to Pins 11, 12.

REFHB (Pins 9, 10): ADC High Reference. Bypass to Pins 11, 12 with 0.1 μ F ceramic chip capacitor. Do not connect to Pins 5, 6.

REFLA (Pins 11, 12): ADC Low Reference. Bypass to Pins 9, 10 with 0.1 μ F ceramic chip capacitor, to Pins 5, 6 with a 2.2 μ F ceramic capacitor and to ground with 1 μ F ceramic capacitor.

V_{DD} (Pins 13, 14, 15, 62, 63): 3.3V Supply. Bypass to GND with 0.1 μ F ceramic chip capacitors.

GND (Pins 16, 61, 64): ADC Power Ground.

ENC⁺ (Pin 17): Encode Input. Conversion starts on the positive edge.

ENC⁻ (Pin 18): Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1 μ F ceramic for single-ended ENCODE signal.

SHDN (Pin 19): Shutdown Mode Selection Pin. Connecting SHDN to GND and \overline{OE} to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and \overline{OE} to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and \overline{OE} to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and \overline{OE} to V_{DD} results in sleep mode with the outputs at high impedance.

\overline{OE} (Pin 20): Output Enable Pin. Refer to SHDN pin function.

D0⁻/D0⁺ to D11⁻/D11⁺ (Pins 21, 22, 23, 24, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 43, 44, 45, 46, 47, 48, 51, 52, 53, 54): LVDS Digital Outputs. All LVDS outputs require differential 100 Ω termination resistors at the LVDS receiver. D11⁻/D11⁺ is the MSB.

OGND (Pins 25, 33, 41, 50): Output Driver Ground.

OV_{DD} (Pins 26, 34, 42, 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1 μ F ceramic chip capacitor.

CLKOUT⁻/CLKOUT⁺ (Pins 35 to 36): LVDS Data Valid Output. Latch data on rising edge of CLKOUT⁻, falling edge of CLKOUT⁺.

OF⁻/OF⁺ (Pins 55 to 56): LVDS Over/Under Flow Output. High when an over or under flow has occurred.

LVDS (Pin 57): Output Mode Selection Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3V_{DD} selects demux CMOS mode with simultaneous update. Connecting LVDS to 2/3V_{DD} selects demux CMOS mode with interleaved update. Connecting LVDS to V_{DD} selects LVDS mode.

MODE (Pin 58): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects straight binary output format and turns the clock duty cycle stabilizer off. Connecting MODE to 1/3V_{DD} selects straight binary output format and turns the clock duty cycle stabilizer on. Connecting MODE to 2/3V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. Connecting MODE to V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 59): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ± 0.5 V input range. Connecting SENSE to V_{DD} selects the internal reference and a ± 1 V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ± 1 V is the largest valid input range.

V_{CM} (Pin 60): 1.6V Output and Input Common Mode Bias. Bypass to ground with 2.2 μ F ceramic chip capacitor.

GND (Exposed Pad): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

FUNCTIONAL BLOCK DIAGRAM

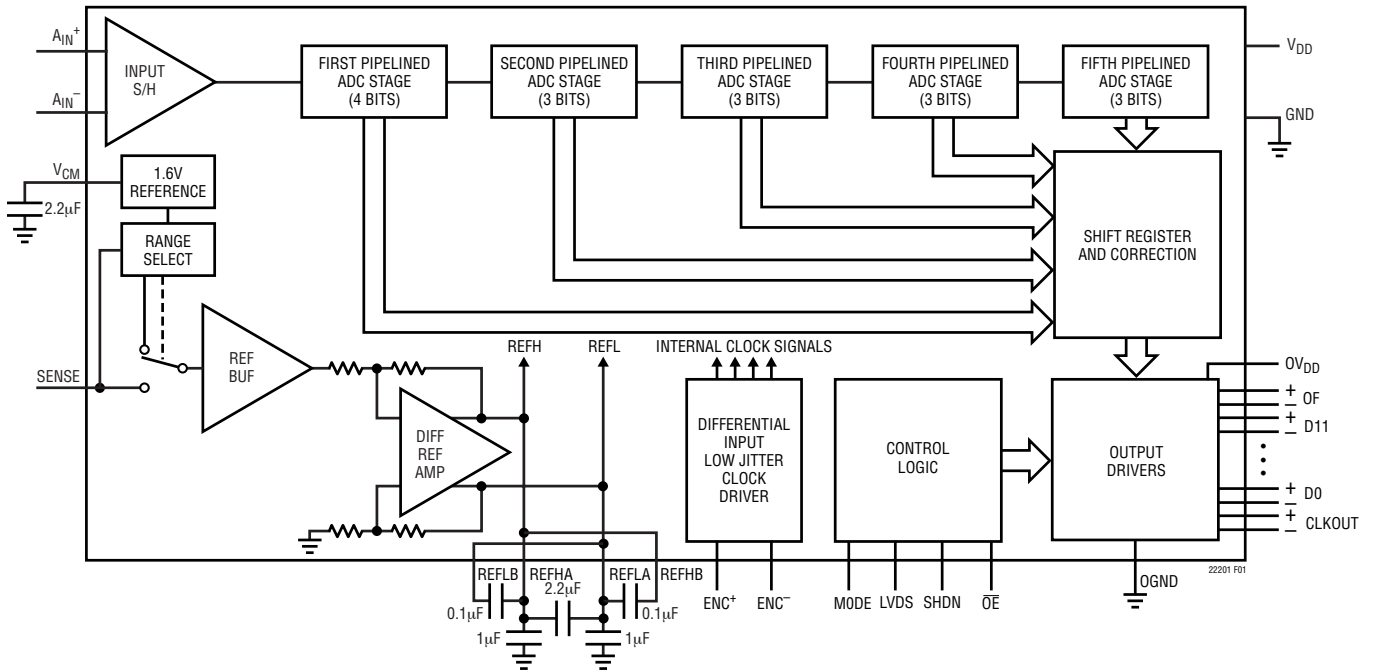
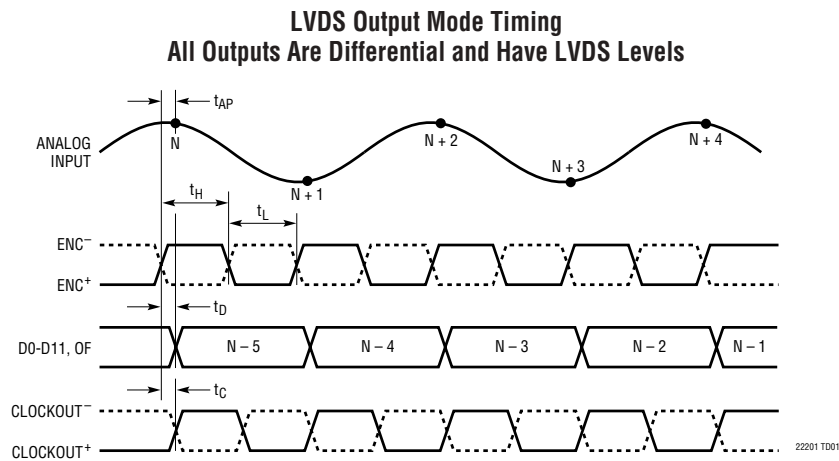


Figure 1. Functional Block Diagram

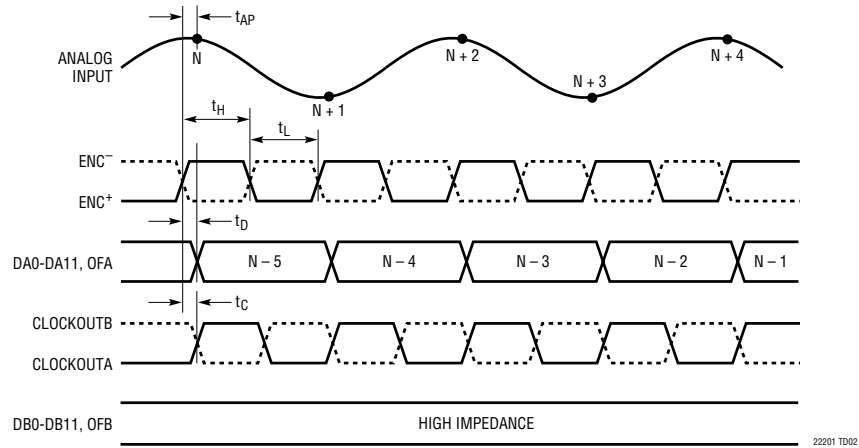
TIMING DIAGRAMS



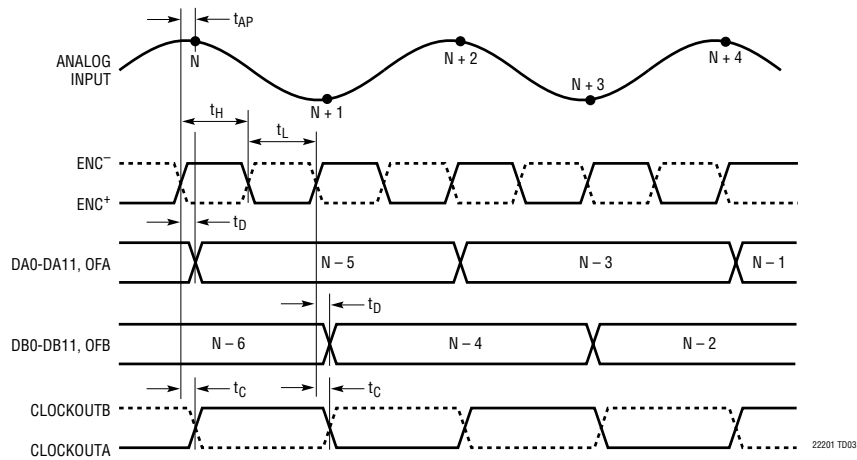
22201 TD01

TIMING DIAGRAMS

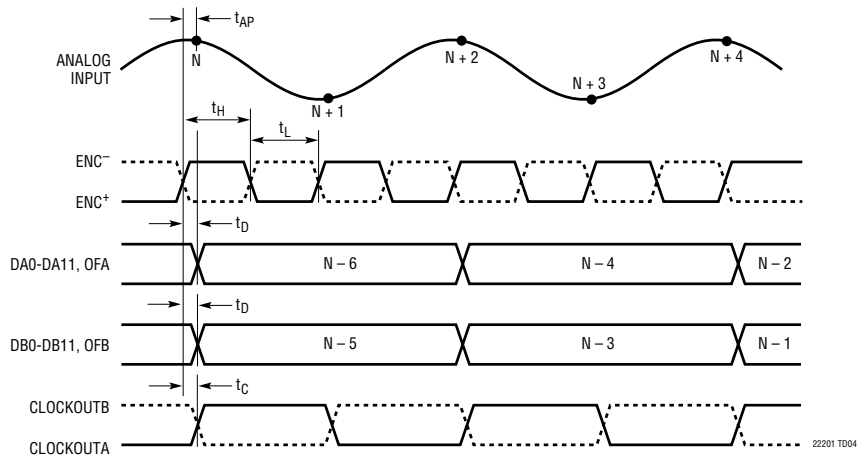
Full-Rate CMOS Output Mode Timing
All Outputs Are Single-Ended and Have CMOS Levels



Demultiplexed CMOS Outputs with Interleaved Update
All Outputs Are Single-Ended and Have CMOS Levels



Demultiplexed CMOS Outputs with Simultaneous Update
All Outputs Are Single-Ended and Have CMOS Levels



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio $[S/(N + D)]$ is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$\text{THD} = 20\text{Log} \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_n are the amplitudes of the second through n th harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $m f_a \pm n f_b$, where m and $n = 0, 1, 2, 3$, etc. The 3rd order intermodulation products are $2f_a + f_b$, $2f_b + f_a$, $2f_a - f_b$ and $2f_b - f_a$. The intermodulation distortion is defined as the ratio of the RMS value of either

input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$\text{SNR}_{\text{JITTER}} = -20\text{log} (2\pi) \cdot f_{\text{IN}} \cdot t_{\text{JITTER}}$$

CONVERTER OPERATION

As shown in Figure 1, the LTC2220/LTC2221 is a CMOS pipelined multistep converter. The converter has five pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost sensitive applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The encode input is differential for improved common mode noise immunity. The LTC2220/LTC2221 has two phases of operation, determined by the state of the differential $\text{ENC}^+/\text{ENC}^-$ input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC^+ high and ENC^+ less than ENC^- as ENC^+ low.

APPLICATIONS INFORMATION

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the “Input S/H” shown in the block diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2220/LTC2221 CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage.

When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions from high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

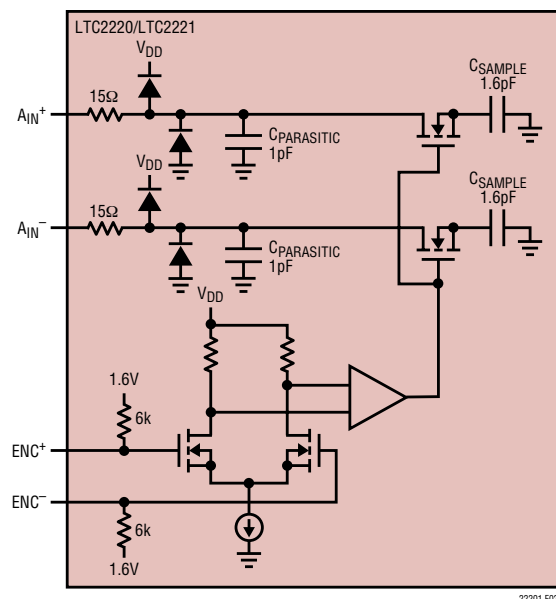


Figure 2. Equivalent Input Circuit

Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged. For a single-ended input, A_{IN+} should be driven with the input signal and A_{IN-} should be connected to 1.6V or V_{CM} .

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing $\pm 0.5V$ for

APPLICATIONS INFORMATION

the 2V range or $\pm 0.25V$ for the 1V range, around a common mode voltage of 1.6V. The V_{CM} output pin (Pin 60) may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with a 2.2 μF or greater capacitor.

Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTC2220/LTC2221 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC, the sample-and-hold circuit will connect the 1.6pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100 Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC2220/LTC2221 being driven by an RF transformer with a center tapped secondary. The

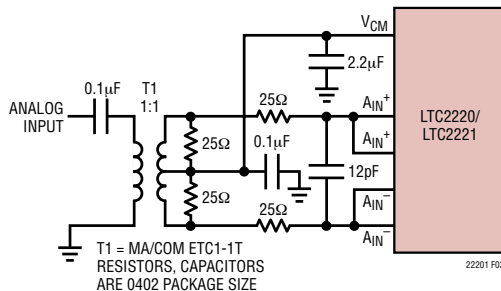


Figure 3. Single-Ended to Differential Conversion Using a Transformer

secondary center tap is DC biased with V_{CM} , setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100 Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

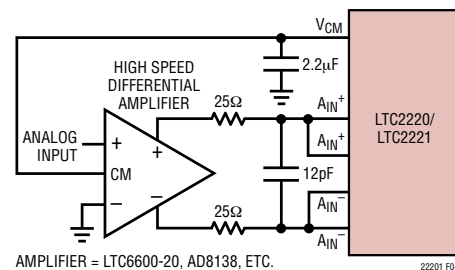


Figure 4. Differential Drive with an Amplifier

Figure 5 shows a single-ended input circuit. The impedance seen by the analog inputs should be matched. This circuit is not recommended if low distortion is required.

The 25 Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input. For input frequencies higher than 100MHz, the capacitor may need to be decreased to prevent excessive signal loss.

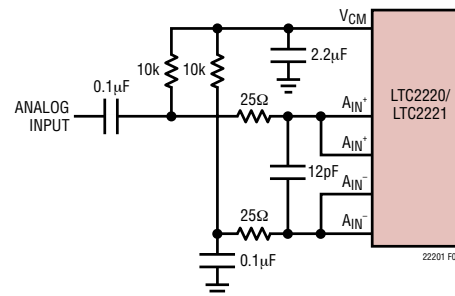


Figure 5. Single-Ended Drive

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Other voltage ranges in between the pin selectable ranges can be programmed with two external resistors as shown in Figure 10. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a $1\mu\text{F}$ ceramic capacitor.

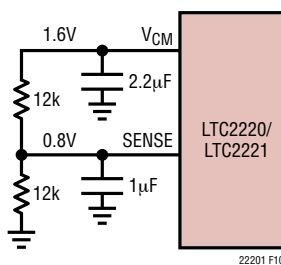


Figure 10. 1.6V Range ADC

Input Range

The input range can be set based on the application. The 2V input range will provide the best signal-to-noise performance while maintaining excellent SFDR. The 1V input range will have better SFDR performance, but the SNR will degrade by 5dB. See the Typical Performance Characteristics section.

Driving the Encode Inputs

The noise performance of the LTC2220/LTC2221 can depend on the encode signal quality as much as on the analog input. The ENC⁺/ENC⁻ inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.

2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise. The encode inputs have a common mode range of 1.1V to 2.5V. Each input may be driven from ground to V_{DD} for single-ended drive.

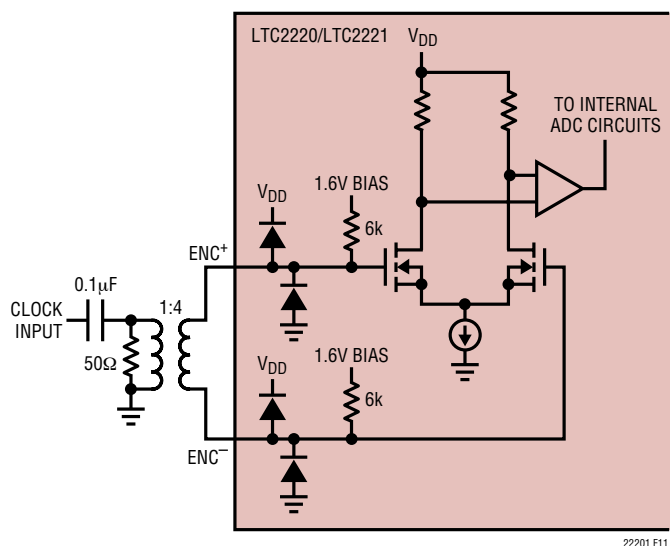


Figure 11. Transformer Driven ENC⁺/ENC⁻

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2220/LTC2221 is 170Msps (LTC2220) and 135Msps (LTC2221). For the ADC to operate properly, the encode signal should have a 50% ($\pm 5\%$) duty cycle. Each half cycle must have at least 2.8ns (LTC2220) or 3.5ns (LTC2221) for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the ENC⁺ pin to sample the analog input. The falling edge of ENC⁺ is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock

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duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2220/LTC2221 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2220/LTC2221 is 1Msps.

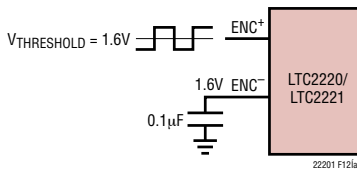


Figure 12a. Single-Ended ENC Drive, Not Recommended for Low Jitter

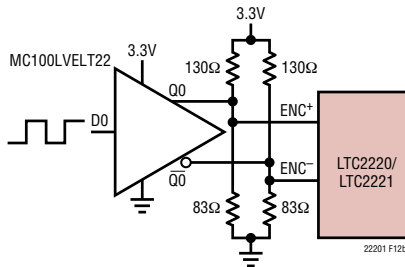


Figure 12b. ENC Drive Using a CMOS to PECL Translator

DIGITAL OUTPUTS

Digital Output Modes

The LTC2220/LTC2221 can operate in several digital output modes: LVDS, CMOS running at full speed, and CMOS demultiplexed onto two buses, each of which runs at half speed. In the demultiplexed CMOS modes the two buses (referred to as bus A and bus B) can either be updated on alternate clock cycles (interleaved mode) or simultaneously (simultaneous mode). For details on the clock timing, refer to the timing diagrams.

The LVDS pin selects which digital output mode the part uses. This pin has a four-level logic input which should be

connected to GND, $1/3V_{DD}$, $2/3V_{DD}$ or V_{DD} . An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 1 shows the logic states for the LVDS pin.

Table 1. LVDS Pin Function

LVDS	Digital Output Mode
GND	Full-Rate CMOS
$1/3V_{DD}$	Demultiplexed CMOS, Simultaneous Update
$2/3V_{DD}$	Demultiplexed CMOS, Interleaved Update
V_{DD}	LVDS

Digital Output Buffers (CMOS Modes)

Figure 13a shows an equivalent circuit for a single output buffer in the CMOS output mode. Each buffer is powered by OV_{DD} and $OGND$, which are isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to voltages as low as 0.5V. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

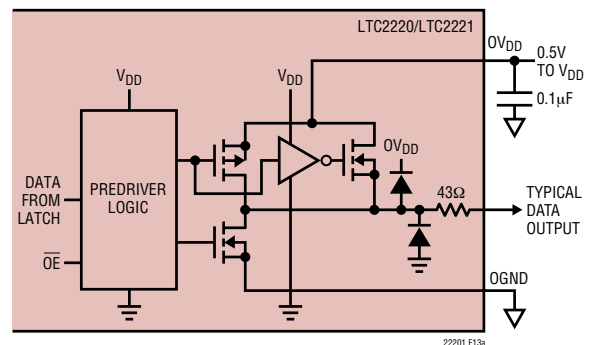


Figure 13a. Digital Output Buffer in CMOS Mode

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2220/LTC2221 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

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Digital Output Buffers (LVDS Mode)

Figure 13b shows an equivalent circuit for a differential output pair in the LVDS output mode. A 3.5mA current is steered from OUT^+ to OUT^- or vice versa which creates a $\pm 350mV$ differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to 1.25V. For proper operation each LVDS output pair needs an external 100Ω termination resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

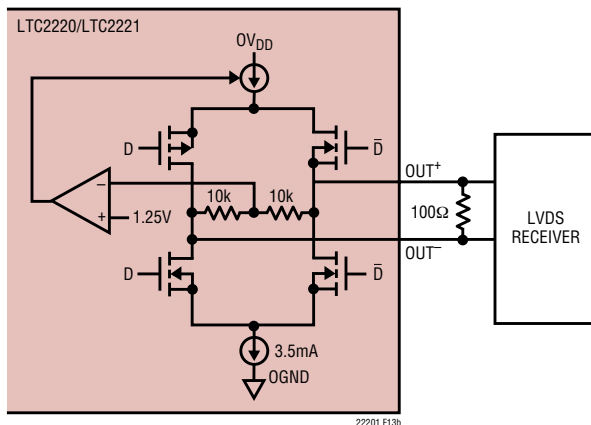


Figure 13b. Digital Output in LVDS Mode

Data Format

The LTC2220/LTC2221 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. Connecting MODE to GND or $1/3V_{DD}$ selects straight binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 2 shows the logic states for the MODE pin.

Table 2. MODE Pin Function

MODE Pin	Output Format	Clock Duty Cycle Stabilizer
0	Straight Binary	Off
$1/3V_{DD}$	Straight Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit indicates when the converter is overranged or underranged. In CMOS mode, a logic high on the OFA pin indicates an overflow or underflow on the A data bus, while a logic high on the OFB pin indicates an overflow or underflow on the B data bus. In LVDS mode, a differential logic high on the OF^+/OF^- pins indicates an overflow or underflow.

Output Clock

The ADC has a delayed version of the ENC^+ input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. In all CMOS modes, A bus data will be updated just after CLKOUTA rises and can be latched on the falling edge of CLKOUTA. In demux CMOS mode with interleaved update, B bus data will be updated just after CLKOUTB rises and can be latched on the falling edge of CLKOUTB. In demux CMOS mode with simultaneous update, B bus data will be updated just after CLKOUTB falls and can be latched on the rising edge of CLKOUTB. In LVDS mode, data will be updated just after $CLKOUT^+/CLKOUT^-$ rises and can be latched on the falling edge of $CLKOUT^+/CLKOUT^-$.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD} , should be tied to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 1.8V supply then OV_{DD} should be tied to that same 1.8V supply.

In the CMOS output mode, OV_{DD} can be powered with any voltage up to the V_{DD} of the part. $OGND$ can be powered with any voltage from GND up to 1V and must be less than OV_{DD} . The logic outputs will swing between $OGND$ and OV_{DD} .

In the LVDS output mode, OV_{DD} should be connected to a 3.3V supply and $OGND$ should be connected to GND.

Output Enable

The outputs may be disabled with the output enable pin, \overline{OE} . In CMOS or LVDS output modes \overline{OE} high disables all data outputs including OF and CLKOUT. The data access and bus

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relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity.

The Hi-Z state is not a truly open circuit; the output pins that make an LVDS output pair have a 20k resistance between them. Therefore in the CMOS output mode, adjacent data bits will have 20k resistance in between them, even in the Hi-Z state.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and \overline{OE} to V_{DD} results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and \overline{OE} to GND results in nap mode, which typically dissipates 35mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap mode all digital outputs are disabled and enter the Hi-Z state.

GROUNDING AND BYPASSING

The LTC2220/LTC2221 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the

printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital signal alongside an analog signal or underneath the ADC.

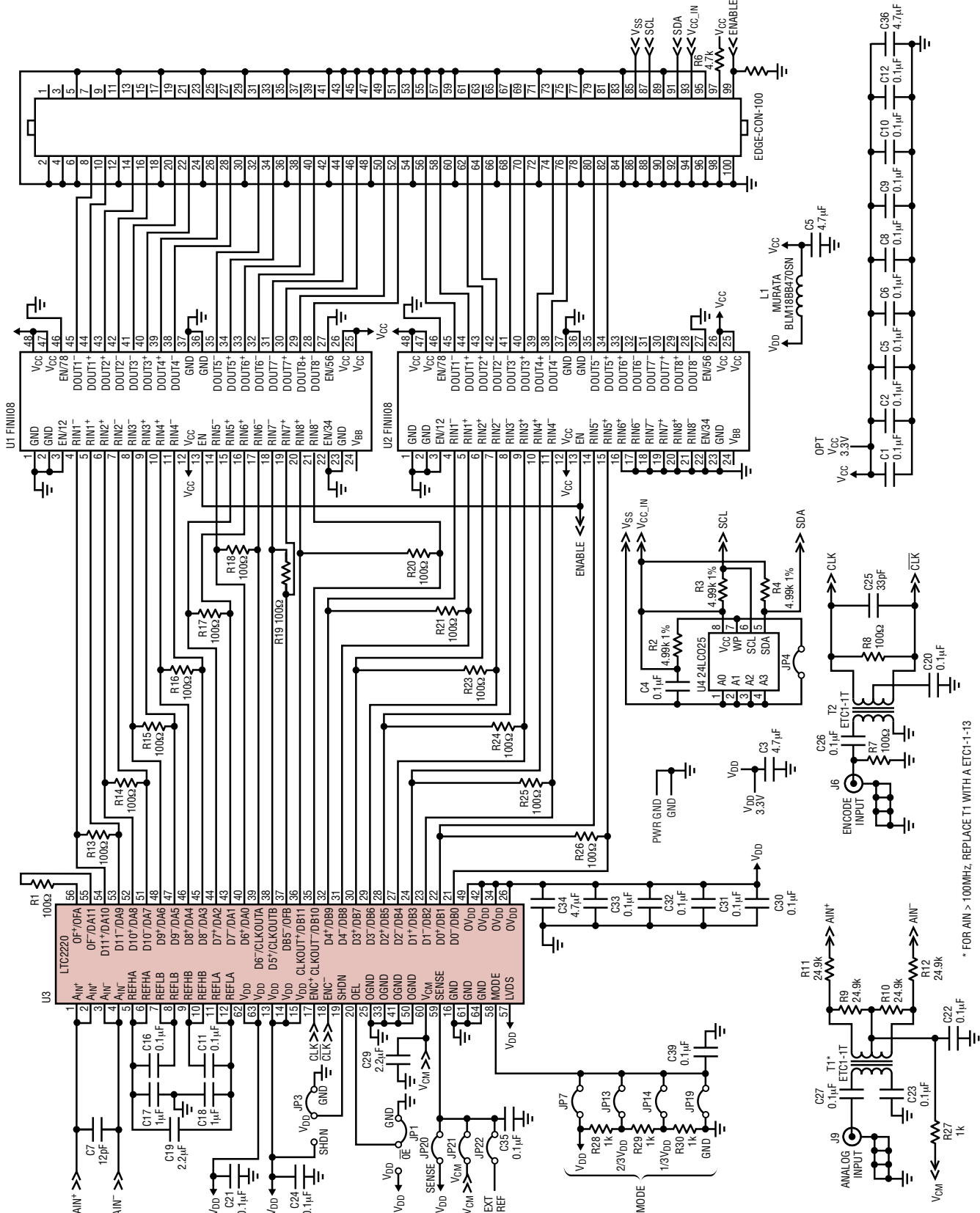
High quality ceramic bypass capacitors should be used at the V_{DD} , OV_{DD} , V_{CM} , REFHA, REFHB, REFLA and REFLB pins as shown in the block diagram on the front page of this data sheet. Bypass capacitors must be located as close to the pins as possible. Of particular importance are the capacitors between REFHA and REFLB and between REFHB and REFLA. These capacitors should be as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recommended. The 2.2 μ F capacitor between REFHA and REFLA can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2220/LTC2221 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

HEAT TRANSFER

Most of the heat generated by the LTC2220/LTC2221 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

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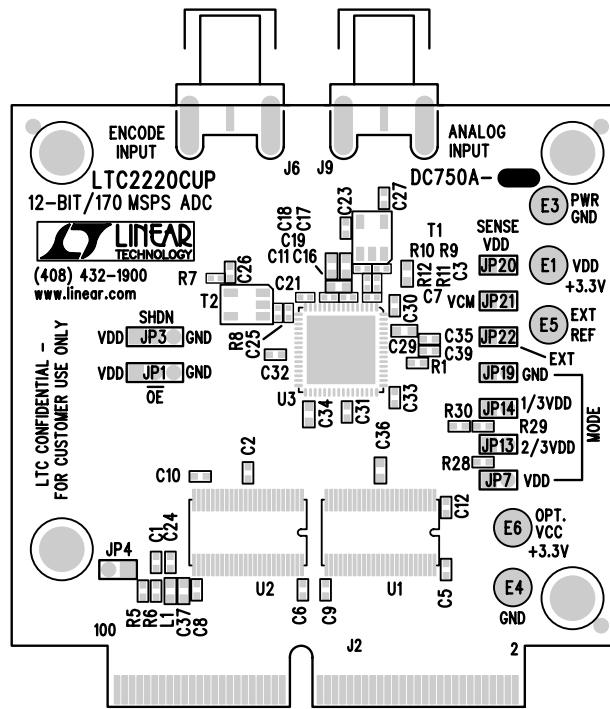


Evaluation Circuit Schematic of the LTC2220

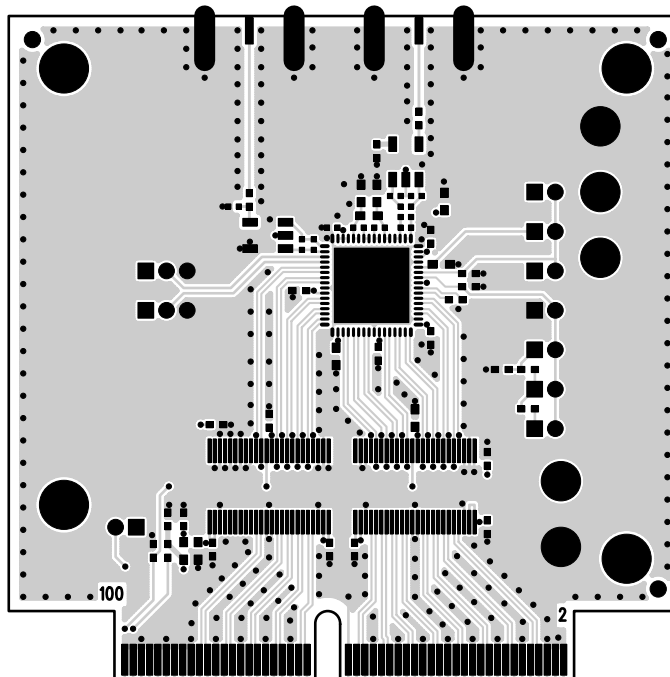
* FOR AIN > 100MHz, REPLACE T1 WITH A ETC1-1-13

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Silkscreen Top

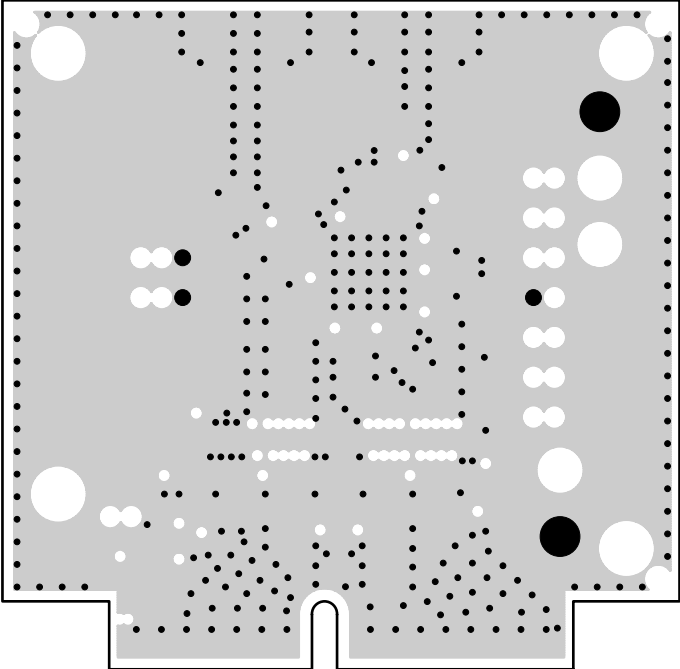


Layer 1 Component Side

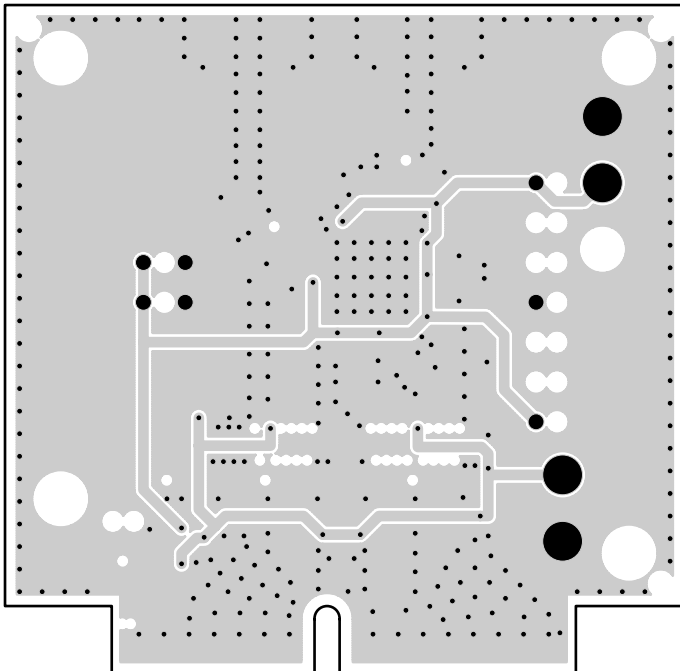


APPLICATIONS INFORMATION

Layer 2 GND Plane

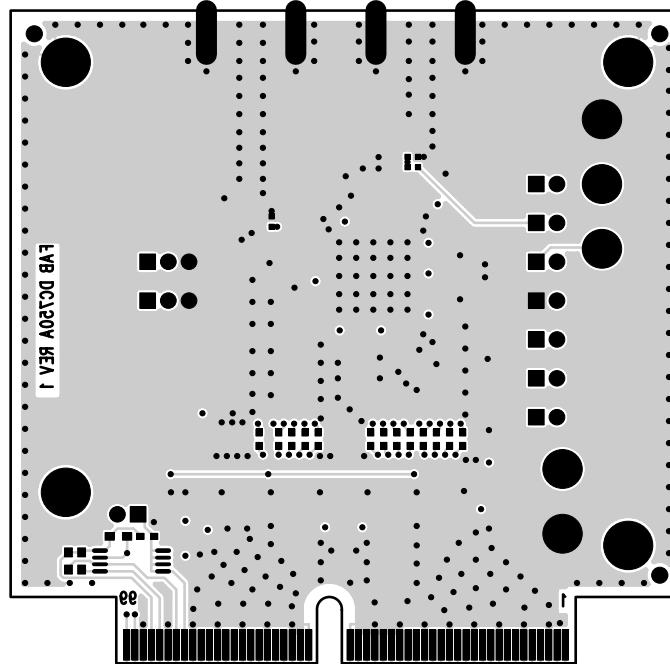


Layer 3 Power Plane



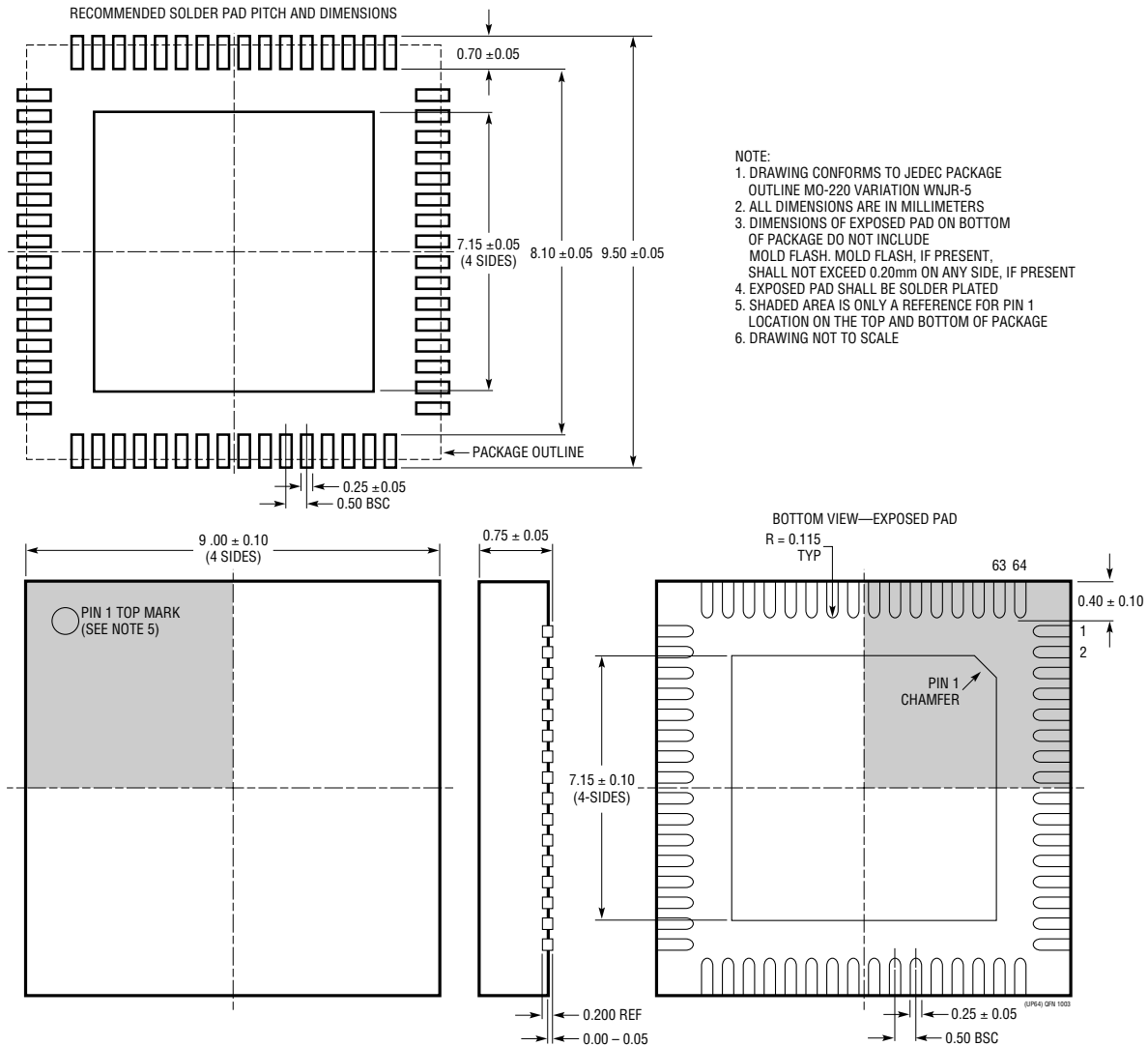
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Layer 4 Bottom Side



PACKAGE DESCRIPTION

UP Package 64-Lead Plastic QFN (9mm × 9mm) (Reference LTC DWG # 05-08-1705)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1747	12-Bit, 80Msps ADC	72dB SNR, 87dB SFDR, 48-Pin TSSOP Package
LTC1748	14-Bit, 80Msps ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1749	12-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 87dB SFDR
LTC1750	14-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm x 9mm QFN Package
LTC2221	12-Bit, 135Msps ADC	660mW, 67.5dB SNR, 9mm x 9mm QFN Package
LTC2222	12-Bit, 105Msps ADC	475mW, 67.9dB SNR, 7mm x 7mm QFN Package
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step

22201p