PRELIMINARY

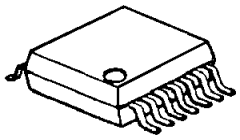
Analog Signal Input Monaural Class D Power Amplifier

■ GENERAL DESCRIPTION

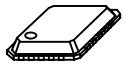
The **NJU8754** is an analog signal input monaural class D power amplifier. The **NJU8754** includes Inversion operatinal amplifier input circuit, PWM modulator, an output-short protector and a low voltage detector. The **NJU8754** incorporates BTL amplifier, which eliminate AC coupling capacitors, capable of driving up to 0.6W at 3.6V supply voltage with simple external LC low-pass filters.

The **NJU8754** features high power-efficiency by class-D operation and very small package, and is suited for cellular phone, PDA, etc.

■ PACKAGE OUTLINE



NJU8754V

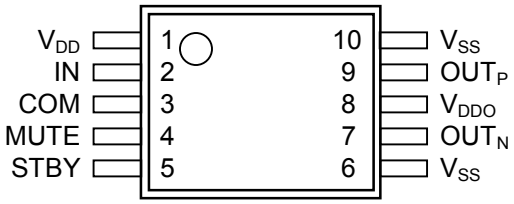


NJU8754KM1

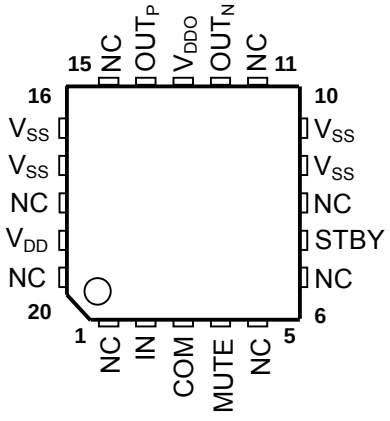
■ FEATURES

- Monaural Analog Signal Input
- Monaural BTL Output :1.2W at 5V into 8Ohms
  :0.6W at 3.6V into 8Ohms
- Standby(Hi-Z), Mute Control
- Built-in Short Protector
- Built-in Low Voltage Detector
- Operating Voltage :2.7 ~ 5.25V
- CMOS Technology
- Package Outline :SSOP10, QFN20

■ PIN CONFIGURATION

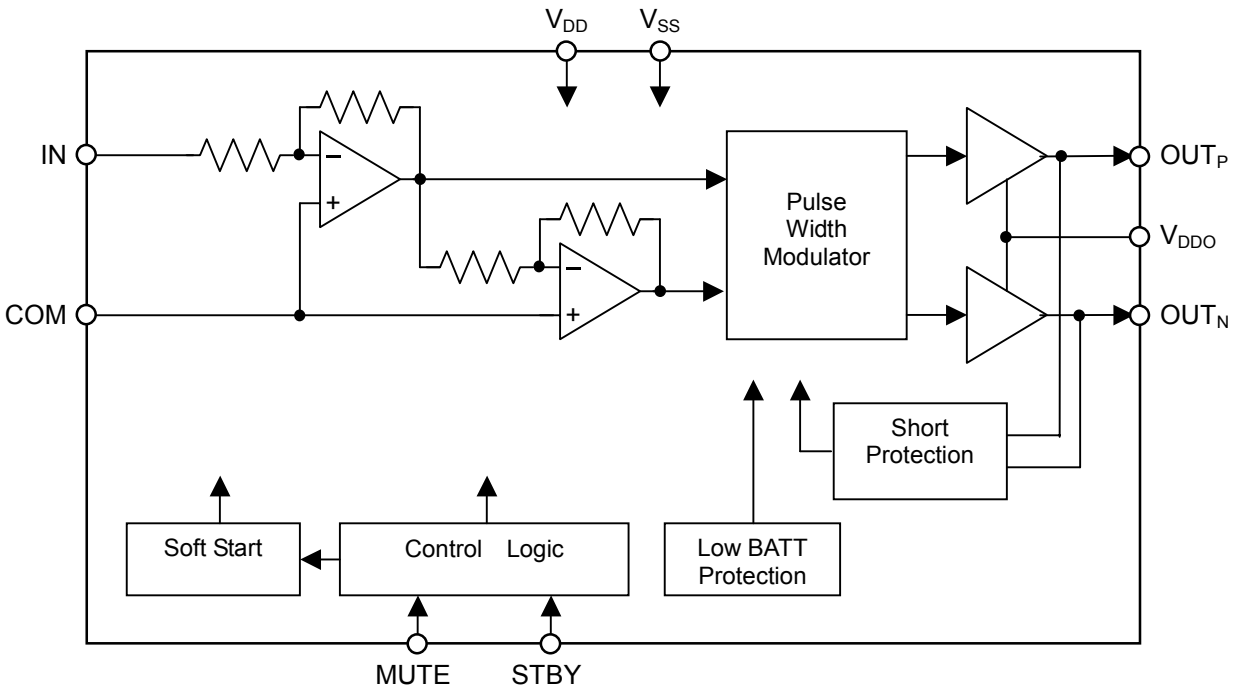


SSOP10



QFN20

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

No.		SYMBOL	I/O	FUNCTION
SSOP10	**QFN20**			
1	19	V_{DD}	–	Power supply : V_{DD}=3.6V
2	2	IN	I	Signal input
3	3	COM	–	Analog common
4	4	MUTE	I	Mute control Low : Mute ON High : Mute OFF
5	7	STBY	I	Standby control Low : Standby ON High : Standby OFF
6	9,10	V_{SS}	–	Power GND : V_{SS}=0V
7	12	OUT_N	O	Negative output
8	13	V_{DDO}	–	Output power supply
9	14	OUT_P	O	Positive output
10	16,17	V_{SS}	–	Power GND : V_{SS}=0V
–	1,5,6,8,11,15,18,20	NC	–	Non connection

*The relations of "V_{SS}= 0V" and "V_{DD}= V_{DDO}" must be maintained.
*V_{SS}(SSOP10:Pin No.6,10, QFN20:Pin No.9,10,16,17) should be connected at a nearest point to the IC.
*V_{DDO}(SSOP10:Pin No.8, QFN20:Pin No.13) should be connected at a nearest point to the IC.
*MUTE(SSOP10, QFN20:Pin No.4) and STBY(SSOP10:Pin No.5, QFN20:Pin No.7) must be connected to V_{DD}, when these pins are not used.

FUNCTIONAL DESCRIPTION

(1) Signal Output

The OUT_P and OUT_N generate PMW output signal, which will be converted to analog signal via external 2nd-order or higher LC filter. A switching regulator with a high response against a voltage fluctuation is the best selection for the $V_{DDO,}$ which is the power supply for output driver. To obtain better T.H.D. performance, the stabilization of the power is required.

(2) Standby

By setting the STBY pin to "L", the standby mode is enabled. In the standby mode, the entire functions of the **NJU8754** enter a low-power state, and the output pins(OUT_P and OUT_N) are in high impedance.

(3) Mute

By setting the MUTE pin to "L", the Mute function is enabled, and the output pins(OUT_P and OUT_N) output square wave(Duty: 50%).

(4) Low Voltage Detector

When the power supply voltage drops down to below V_{DD}(MIN), the internal oscillation is halted not to generate unwanted frequency, and the output pins(OUT_P and OUT_N) become in high impedance.

(5) Short Protection Circuit

The short protector, which protects the **NJU8754** from high short-circuit current, turns off the output driver. After about 5 seconds from the protection, the **NJU8754** returns to normal operation. The short protector is enabled in response to following accidents.

Short between OUT_P and OUT_N
Short between OUT_P and V_{SS}
Short between OUT_N and V_{SS}

Note 1) The detectable current and the period for the protection depend on the power supply voltage and ambient temperature.

Note 2) The short protector is not effective for a long term short-circuit but for an instantaneous accident. Continuous high-current may cause permanent damage to **NJU8754**.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD} V_{DDO}	-0.3 ~ +5.5 -0.3 ~ +5.5	V V
Input Voltage	Vin	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C
Power Dissipation	P_D	250 (SSOP10) TBD(QFN20)	mW

Note 1) All voltage are relative to "V_{SS}= 0V" reference.

Note 2) The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.

Note 3) De-coupling capacitors for V_{DD}-V_{SS} and V_{DDO}-V_{SS} should be connected for stable operation.

Note 4) Power Dissipation

The class-D amplifiers are more power efficient, and dissipate power less than general analog-amplifiers. In theory, the **NJU8754** actualize quite high output-power such as 1.2W at =5V operation with 8ohms load, it looks as if the **NJU8754** exceeds the absolute maximum rating of the power dissipation. However, in practice, the effective output-power of usual music sound is only about 1/10 of its maximum output power, thus it may never exceed the absolute maximum rating.

The maximum power dissipation in the system is calculated, as shown below.

$Pdmax(W) = (Tjmax(°C) - Ta(°C)) / \theta ja$

Pdmax: Maximum Power Dissipation, Tjmax: Junction Temperature = 125°C
Ta: Ambient Temperature, θja: Thermal Resistance of package(SSOP10) = 400°C/W

Power dissipation of the **NJU8754** itself is calculated, as shown below.

$Pd(W) = P_O(W) \times R_O(\Omega) / R_L(\Omega) + Pd_{IC}(W)$

Pd: Power Dissipation, P_O: Output Power, R_O: Internal Resistance(output driver)
R_L: Load Resistance, Pd_{IC}: Power of internal circuit

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=V_{DDO}= 3.6V, V_{SS}= 0V, Input Signal=1kHz, Input Signal Level=200mVrms, Frequency Band=20Hz~20kHz, Load Impedance=8Ω, 2nd-order 34kHz LC Filter(Q=0.85))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
V_{DD},V_{DDO} Supply Voltage	V_{DD}		2.7	3.6	5.25	V	
Input Impedance	Z_{IN}	IN pin	-	20	-	kΩ	
Voltage Gain	A_V		-	23	-	dB	
Output Power Efficiency	Eeff	Output THD=10%	80	83	-	%	4
Output THD	THD	V_{DD}=V_{DDO}=5.0V, Po=600mW		0.05	0.08	%	
		V_{DD}=V_{DDO}=3.6V, Po=300mW		0.07	0.1		
Output Power	Po	V_{DD}=V_{DDO}=5.0V Output THD=10%		1.2		W	
		V_{DD}=V_{DDO}=3.6V Output THD=10%		0.6			
S/N	SN	A weight	75	80	-	dB	
Operating Current (Standby)	I_{ST}		-	-	1	μA	
Operating Current (No signal input)	I_{DD}	V_{DD}=V_{DDO}=5.0V No Filter, No Load		4	6	mA	
		V_{DD}=V_{DDO}=3.6V No Filter, No Load		2.5	5		
Input Voltage	V_{IH}	MUTE, STBY pins	0.7V_{DD}	-	V_{DD}	V	
	V_{IL}	MUTE, STBY pins	0	-	0.3V_{DD}	V	
Input Leakage Current	I_{LK}	MUTE, STBY pins	-	-	±0.1	μA	

Note 5) Test system of the output THD and S/N
The output THD and S/N are tested in the system shown in Figure1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

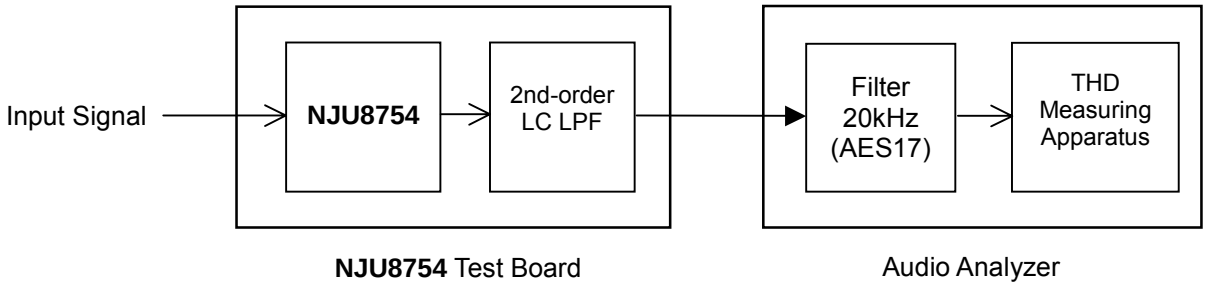
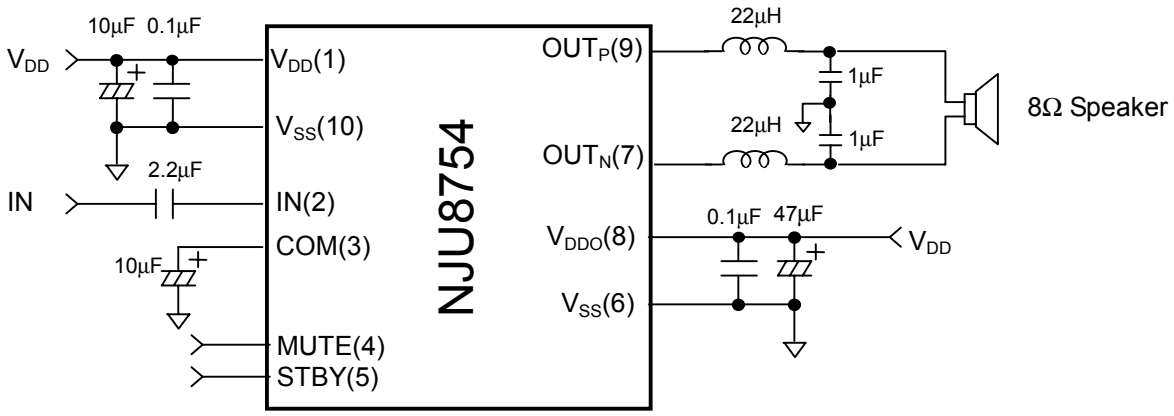


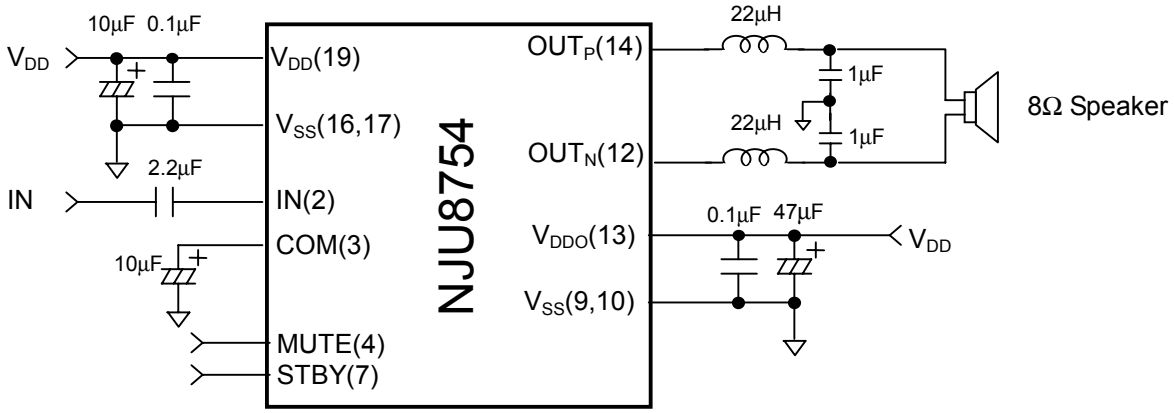
Figure 1. Output THD and S/N Test System

2nd-order LPF : fc=34kHz / Refer to “Typical Application Circuit”.
Filters : 22Hz HPF + 20kHz LPF(AES17)
(with the A-Weight filter for S/N and Dynamic-range tests)

■ TYPICAL APPLICATION CIRCUIT



SSOP10



QFN20

Note 6) De-coupling capacitors must be connected between each power supply pin and GND.
The capacity value should be adjusted on the application circuit and the operation temperature. It may malfunction if capacity value is small.

Note 7) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for better THD.
THD performance becomes worse by ripple if the capacity of De-coupling capacitor is small.

Note 8) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carefully to fit your application.
The cutoff frequency of the LC filter influences the quality of sound.
The Q factor of the LC filter must be less than "1". Otherwise, the operating current increases when the frequency of input signal is closed to the cutoff frequency.

Note 9) The transition time for MUTE and STBY signals must be less than 100μs. Otherwise, a malfunction may be occurred.

Note10) (1) – (19) indicates pin number.