# PM7380

# FREEDM-32P672

# REVISION B DEVICE ERRATA

**Issue 2**

**March 2000**

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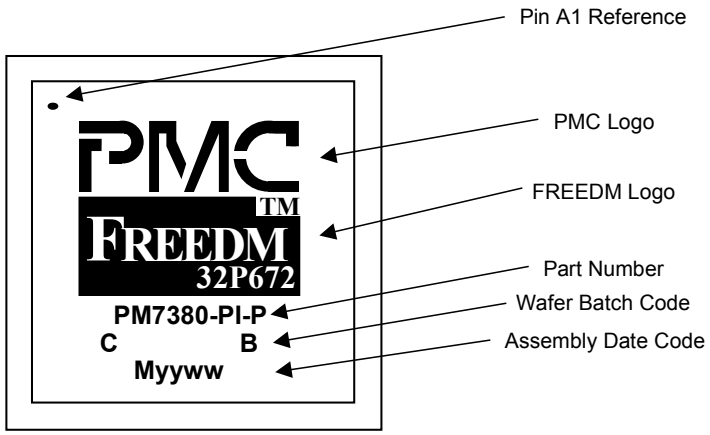
# 1. Introduction

In this document, Section 2 lists the known functional errata for revision B of PM7380 FREEDM-32P672 and Section 3 lists errors found in Issue 3 of the FREEDM-32P672 datasheet (PMC-1990262).

## 1.1. Device Identification

The information contained in Section 2 relates to Revision B of PM7380 FREEDM-32P672 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7380 FREEDM-32P672 Revision B is packaged in a 329-pin Plastic Ball Grid Array (PBGA).

Figure 1.1: PM7380 FREEDM-32P672 Branding Format.




**Not to Scale**

## 1.2. Reference

- PMC-1990262, FREEDM-32P672 Long Form Data Sheet, Issue 3.

## 2. FREEDM-32P672 Revision B Functional Deficiency List

This section lists the known functional deficiencies for Revision B of FREEDM-32P672 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

## 2.1. PCICLK and SYSCLK can not be asynchronous

### Description:

The FREEDM-32P672 will not operate successfully if the rising edges of PCICLK are close to either rising or falling edges of SYSCLK.

Through testing and simulation the specific failure conditions are predicted to be:

- The falling edge of SYSCLK precedes the rising edge of PCICLK by between 0.7 ns and 1.8 ns.
- The rising edge of SYSCLK occurs within ±0.5 ns of the rising edge of PCICLK.

If the two clocks are asynchronous these failure conditions will occur.

This errata item will be corrected in Revision C.

### Workarounds:

To ensure the failure regions are avoided, the SYSCLK and PCICLK should be kept synchronous, with some skew between the clock edges. This is most easily accomplished by tying the SYSCLK and PCICLKO pins together. The failure regions are both avoided due to the internal delay from PCICLK to PCICLKO.

Note: When using a 66 MHz PCI bus, this workaround violates the maximum frequency specification for SYSCLK of 40 MHz. As a result, this workaround is only suitable for prototype testing, and can not be relied upon for production purposes. For the production part, the upper limit of SYSCLK (over process, temperature and voltage) is predicted to be approximately 45 MHz, the exact value is subject to device characterisation.

### Performance with workaround:

FREEDM-32P672 works correctly.

### Performance without workaround:

The FREEDM-32P672 will fail to process packets, due to internal timing conflicts.

## 2.2. FREEDM registers cannot be accessed using fast back-to-back PCI transactions.

**Description:**

The FREEDM-32P672 Registers cannot be read from or written to using a fast back-to-back PCI transaction if the preceding PCI transaction also accessed the same FREEDM-32P672.

This errata item will be corrected in Revision C.

**Workarounds:**

Configure the PCI system not to use fast back-to-back PCI transactions when writing to or reading from FREEDM-32P672.

**Performance with workaround:**

FREEDM-32P672 works correctly.

**Performance without workaround:**

FREEDM-32P672 registers may become corrupted and reads of registers may return incorrect values.

## 2.3. FREEDM may not generate PCI disconnect if host attempts a read multiple command which reads beyond register address 0xFFF.

**Description:**

If a host incorrectly attempts a read multiple command whose address range spans beyond a point 4K bytes from the start of the FREEDM-32P672 register space, the FREEDM-32P672 may not issue a PCI disconnect and the PCI bus may hang.

**Workarounds:**

Ensure that the PCI host only accesses valid FREEDM-32P672 register addresses.

**Performance with workaround:**

FREEDM-32P672 works correctly.

**Performance without workaround:**

PCI bus may hang necessitating a system reset.

## 2.4. FREEDM may under-report number of Transmit FIFO underrun events if two such events occur close together.

### Description:

The FREEDM-32P672 reports underrun events on a per-channel basis to the host by setting bit STATUS[2] when a TDR is returned to the TDR Free Queue. If a packet underflows near the end of the packet and the next packet on the same channel underflows near the start of the packet, it is possible that only one TDR is returned to the TDR Free Queue with STATUS[2] set even though 2 underrun events occurred.

### Workarounds:

None.

### Performance without workaround:

Per channel underrun events can occasionally go unreported.

## 2.5. FREEDM may fail to Offset data as indicated in Receive Packet Descriptor.

### Description:

If a packet is received which spans more than one receive buffer and the size of any of the receive buffers is a multiple of the number of bytes being transferred across the PCI bus, the 'Offset' and 'Bytes in Buffer' fields may not be correctly written to the Receive Packet Descriptor (RPD) at the head of the buffer chain. The 'offset' field may be erroneous set to zero and the 'Bytes in Buffer' field may erroneously include the offset bytes in its count.

This errata item will be corrected in Revision C.

### Workarounds:

This failure can be avoided by setting the number of bytes of the PCI data transfer such that the size of the Partial Packet Buffer is not a multiple of the number of bytes of the PCI data transfer.

For example:

If Receive Packet Buffers of size 512 bytes are being used, set the XFER[3:0] of register 0x208 to a value such that the transfer size (16 * [XFER+1]) is not exactly divisible by 512 bytes. An XFER[3:0] value to 0xE, which equates to a transfer of 240 bytes, would avoid the errata.

### Performance with workaround:

The situation causing the errata is avoided. The 'offset' and 'Bytes in Buffer' fields in the RPD are set correctly.

### Performance without workaround:

The 'offset' and 'Bytes in Buffer' fields in the RPD may be set incorrectly and the host may interpret the result as if a number of bytes of invalid data were pre-pended to the packet.

## 3. Documentation Errors

This section lists the known documentation errors in Issue 3 of PMC-1990262 FREEDM-32P672 Datasheet.

Please report any documentation errors not covered in this document to PMC-Sierra.

## 3.1. SYSCLK Specification change

**Description:**

It has been shown in feature testing that the minimum SYSCLK frequency specification of 25 MHz is inadequate to guarantee error-free operation.

**Text Correction:**

SYSCLK is being specified such that SYSCLK frequency is greater than half of the PCICLK frequency.

It should also be noted that when configured to operate with 3 high speed links the SYSCLK frequency must be 45 MHz, as specified in the current datasheet.

The following text in Table 35 FREEDM-32P672 Link Input Timing characteristics, on page 320 of the FREEDM-32A672 Data Sheet,

"…

| | | | | |
|---|---|---|---|---|
| | SYSCLK Frequency | 25 | 45 | MHz |

…"

should be replaced with the following:

"…

| | | | | |
|---|---|---|---|---|
| | SYSCLK Frequency | 33 | 45 | MHz |

…".

## 4. Contacting PMC-Sierra

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## NOTES



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