CDB43L43

Evaluation Board for CS43L43 Rev D

Features

- Demonstrates recommended layout and grounding arrangements
- CS8415A receives AES/EBU, S/PDIF, and EIAJ-340 Compatible Digital Audio
- Patch Area
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

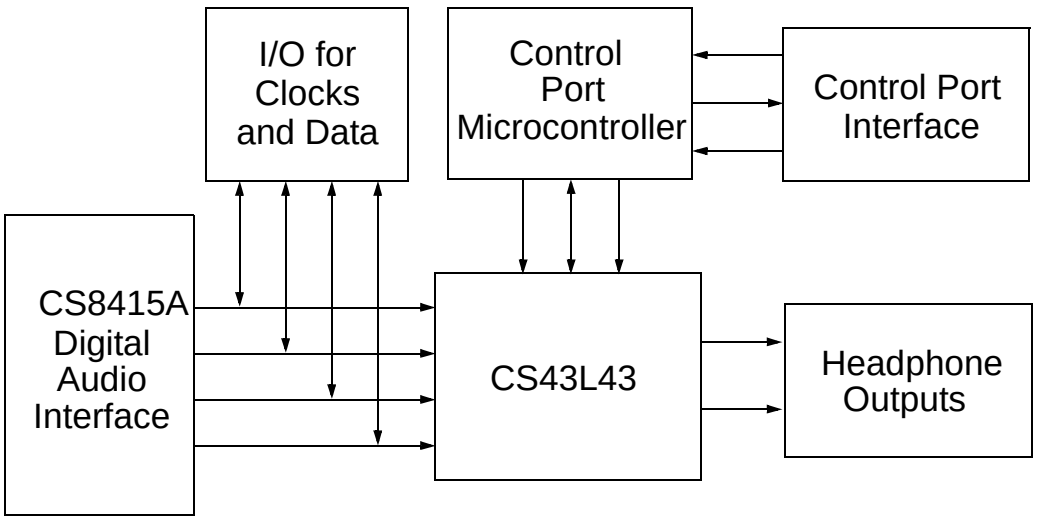
Description

The CDB43L43 evaluation board is an excellent means for quickly evaluating the CS43L43 24-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS43L43 (for control port mode only) and a power supply. Analog headphone outputs are provided via a 1/8" headphone jack and RCA phono jacks.

The CS8415A digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB43L43 Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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1. CDB43L43 SYSTEM OVERVIEW

The CDB43L43 evaluation board is an excellent means of quickly evaluating the CS43L43. The CS8415A digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB43L43 schematic has been partitioned into 10 schematics shown in Figures 2 through 11. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the the system diagram also includes the interconnections between the partitioned schematics.

2. CS43L43 DIGITAL TO ANALOG CONVERTER

A description of the CS43L43 is included in the CS43L43 datasheet.

3. CS8415A DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8415A Digital Audio Receiver, Figure 4. The outputs of the CS8415A include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 Fs master clock. The operation of the CS8415A and a discussion of the digital audio interface are included in the CS8415A datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 5. However, both inputs cannot be driven simultaneously.

4. CS8415A DATA FORMAT

The CS8415A data format is selected through the DIP switch. See Table 2 for details.

5. HEADPHONE OUTPUT

A 1/8 inch, stereo headphone jack is included on the evaluation board for connecting 16 ohm or greater headphones to the CS43L43. If no headphones are connected to the 1/8 inch jack, then a 16 ohm resistor is connected to each of the CS43L43 headphone outputs, HP_A and HP_B. This is useful when evaluating the CS43L43 headphone amplifier with test equipment that has high-impedance inputs. RCA jacks are also provided on the headphone outputs for easy connection to test equipment.

6. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, HDR1. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 10.

7. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by five binding posts (GND, +5 V, VL, VA, VA_HP), see Figure 12. The +5 V input supplies power to the +5 Volt digital circuitry (VA_+5, VD_+5), while the VL input supplies power to the Voltage Level Converters and the CS43L43 VL pin. VA and VA_HP supply power to the CS43L43. For ease of use, it is possible to connect VA, VA_HP and VL to the same supply.

WARNING: VA and VL must be between +1.7 V and +3.6 V. VA_HP must be between +0.9 V and +3.6 V. Operation outside of this range can cause permanent damage to the device. See the CS43L43 datasheet for more details.

8. GROUNDING AND POWER SUPPLY DECOUPLING

The CS43L43 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 9 details the power distribution used on this board. The decoupling capacitors are located as close to the CS43L43 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yields large reductions in radiated noise.

9. CONTROL PORT SOFTWARE

The CDB43L43 is shipped with Windows based software for interfacing with the CS43L43 control port via the serial connector, J1. The software can be used to communicate with the CS43L43 in Two Wire mode.

Note: DIP 2-4 must be set appropriately for control port mode operation.

10. POPGUARD® WORKAROUND

The CDB43L43 Rev A includes a hardware fix for the PopGuard® Transient Control feature of the CS43L43 Rev D. Please see the CS43L43 errata for further details. This additional hardware includes the transistors Q1, Q2, Q4, and Q5 as well as R13, R14, R24, R33, R34, and C7. Please refer to Figure 3. To bypass this hardware fix, stuff R18 and R19 with 0 ohm resistors and change R25 and R26 to 1 kohm resistors. The next silicon revision will address this issue.

11. CDB43L43 PERFORMANCE PLOTS

The CDB43L43 Rev A performance plots shown in Figures 13 through 18 were generated using an Audio Precision System Two Cascade with the S2-AES17LP 20 kHz brickwall filter applied. All tests were performed at a sampling rate of 48 kHz and with VL, VA, and VA_HP set to the indicated voltage supply.

12. CDB43L43 REV A ERRATA

1) R20 and R30 have been stuffed with 0 ohm resistors and 47 kohm pull-downs have been added to pins 3 and 28 of U4.
2) The DIP switch has been turned such that the “open” position is denoted by the “1” on the board.
3) R31 has been changed from a pull-up to a pull-down.
4) A 1 Mohm pull-down has been added to U10 pin 8, located near R24.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	Input	+ 5 Volt power
VA, VL	Input	+ 1.8 Volt to + 3.3 Volt power for the CS43L43 and the Voltage Level Converters
VA_HP	Input	+0.9 Volt to +3.3 Volt power for the CS43L43 headphone amp
GND	Input	Ground connection from power supply
Coax Input	Input	Digital audio interface input via coax
Optical Input	Input	Digital audio interface input via optical
HDR1	Input/Output	I/O for master, serial, left/right clocks and serial data
Serial Port	Input/Output	Serial connection to PC for Two Wire mode control port signals
HDR2	Input/Output	I/O for Two Wire mode control port signals
HP_A (J3)	Output	Channel A headphone output
HP_B (J2)	Output	Channel B headphone output
HP_A&B (J10)	Output	Channel A and B headphone output

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
Program/Run	Programming switch for the control port microcontroller	Program*Run	Configures CDB43L43 to program the µC Configures CDB43L43 for normal operation
HRM/BRM	Seclects High Rate or Base Rate Mode	HRM (/2) *BRM (x1)	Selects High Rate Mode Selects Base Rate Mode
EXT/INT SCLK	Selects SCLK Mode	INT*EXT	Internal SCLK Mode External SCLK Mode
Reset (S1)	Resets the CDB43L43		
DIP 1	Enable/Disable the CS8415A	*0 1	CS8415A is enabled Disabled (External Clocks and Data via HDR1)
DIP 2-4	Configures the interface format and CS43L43 operational mode	*000 001 010 011 100	Control Port mode Stand Alone mode, I2S Stand Alone mode, LJ24 Stand Alone mode, RJ16 (8415A not avail.) Stand Alone mode, RJ24

Note: *Default factory settings

Table 2. CDB43L43 Jumper and Switch settings

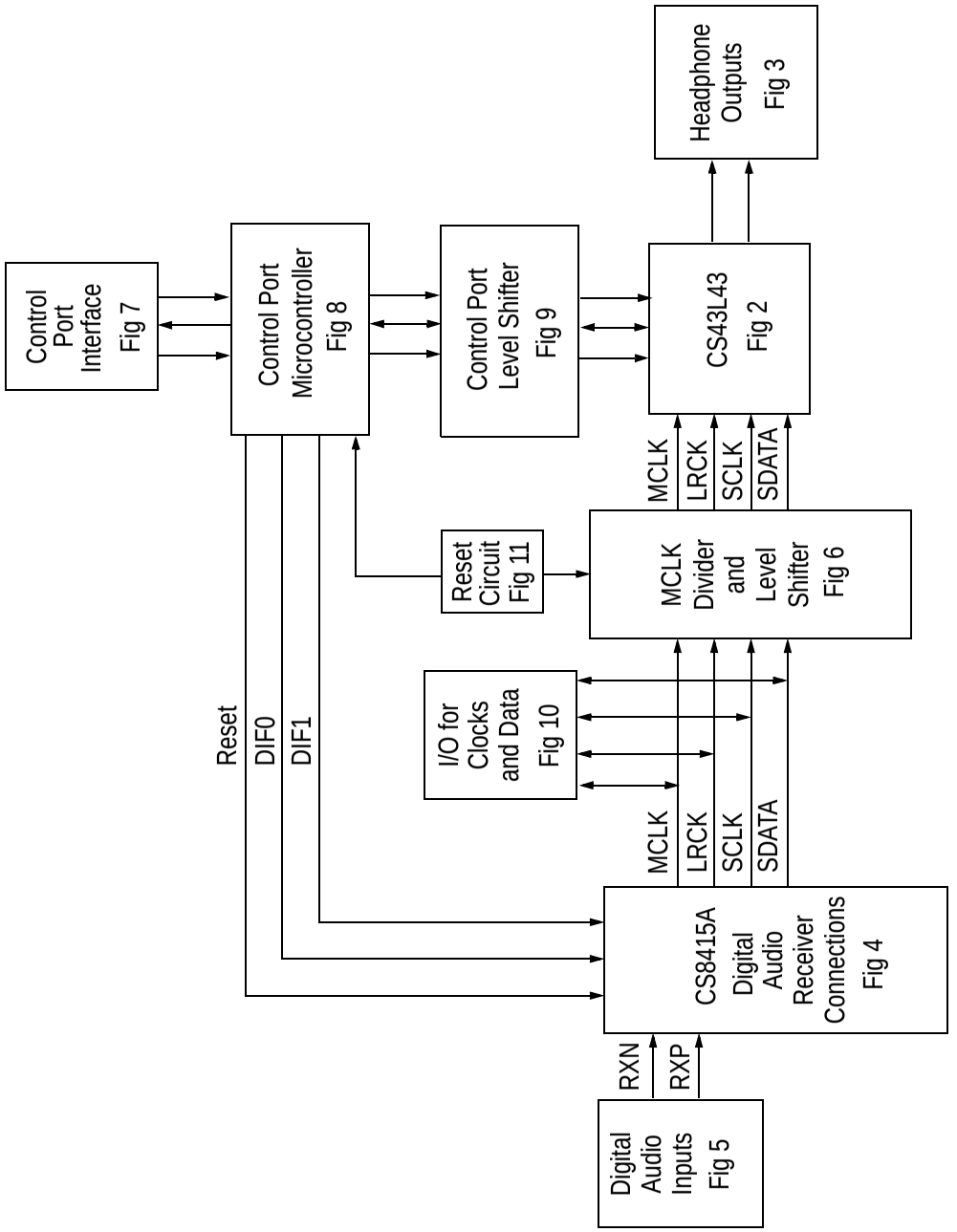


Figure 1. System Block Diagram and Signal Flow

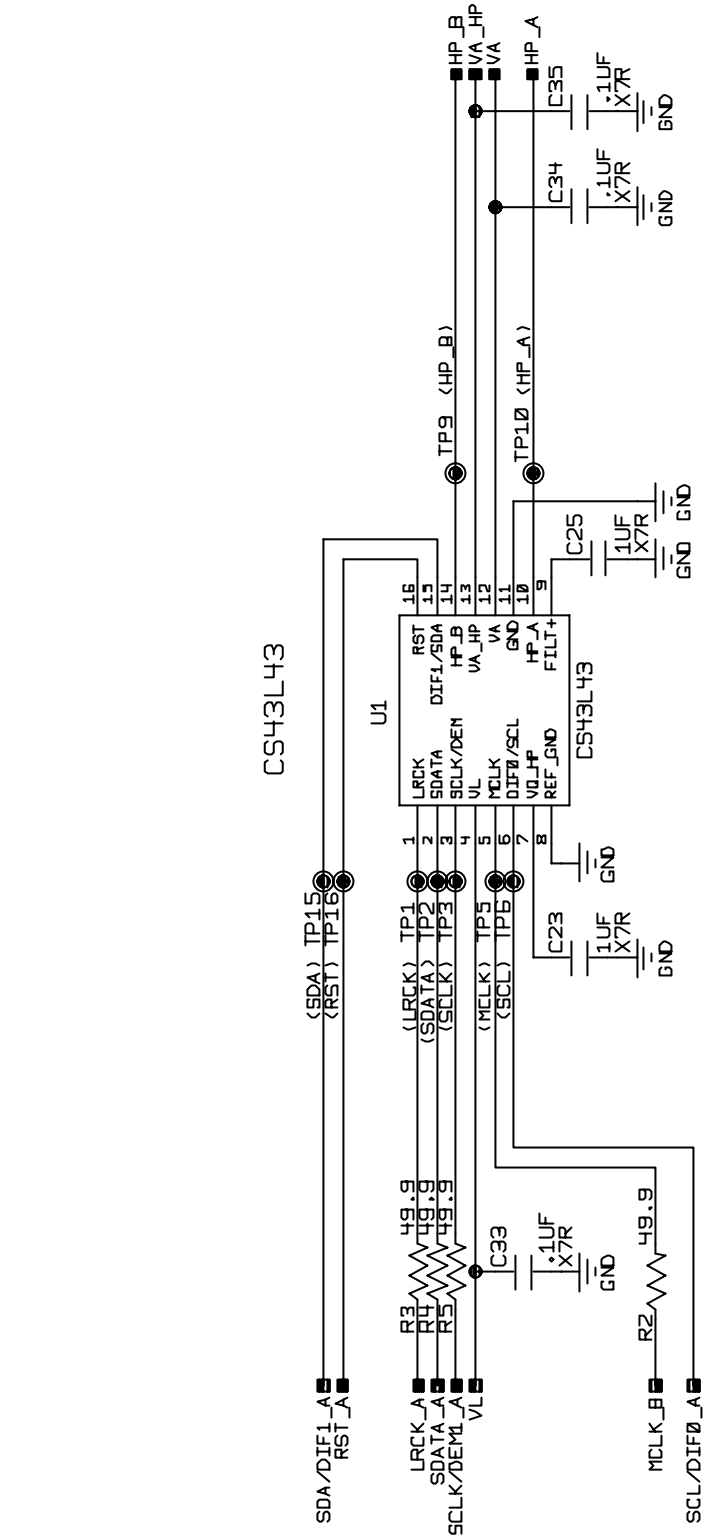


Figure 2. CS43L43

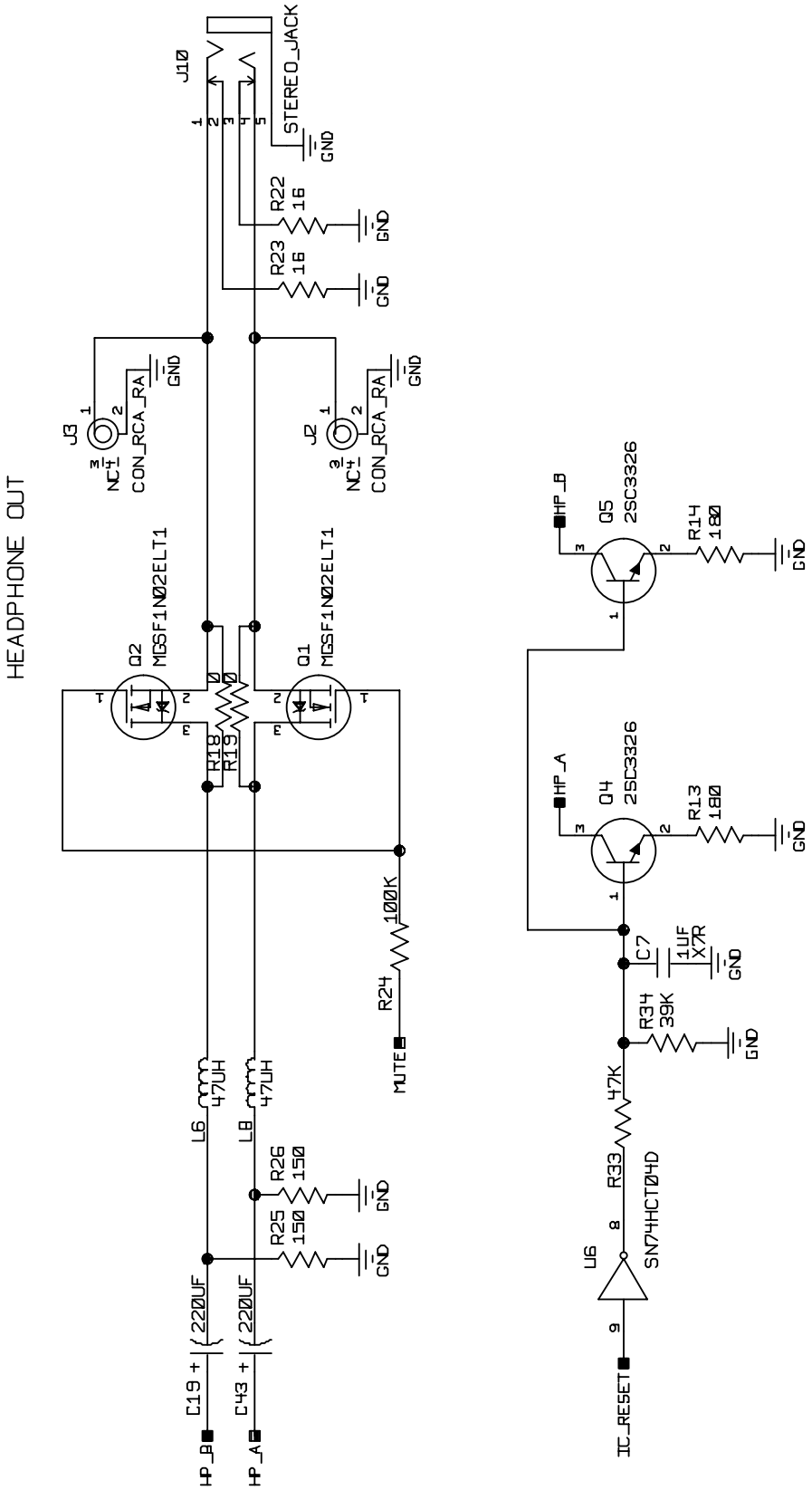


Figure 3. Headphone Outputs

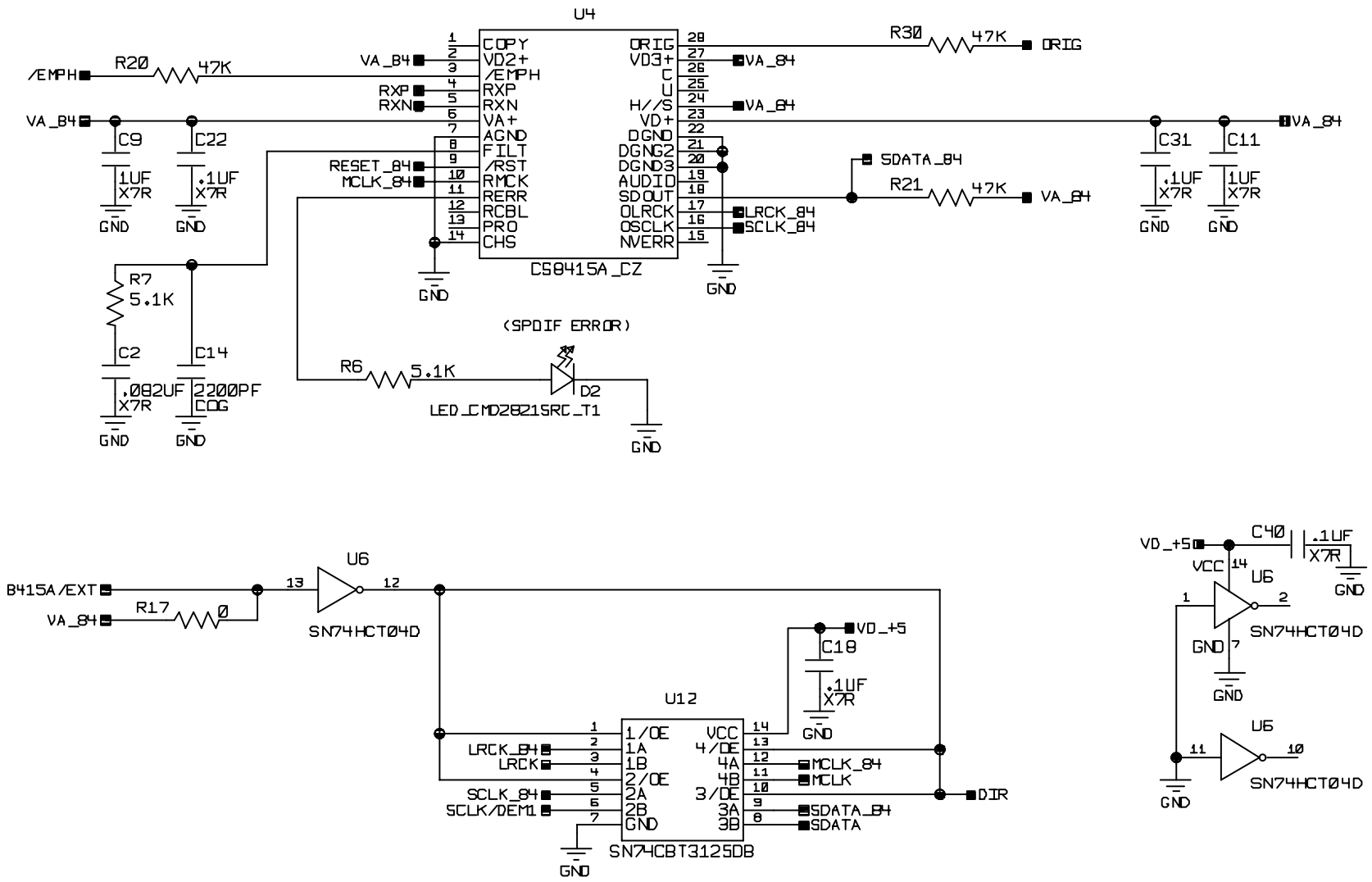
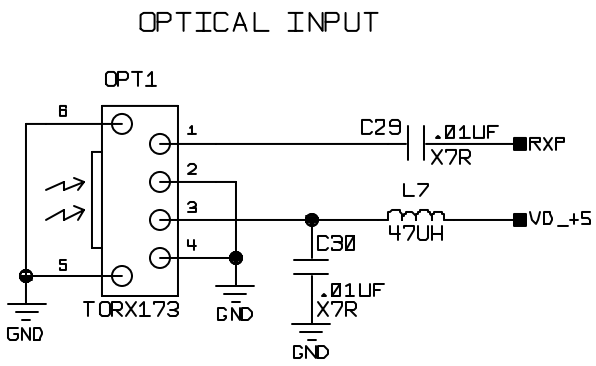


Figure 4. CS8415A Digital Audio Receiver



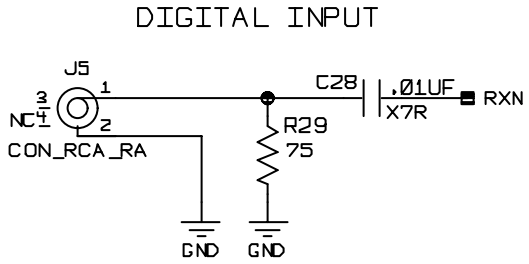


Figure 5. Digital Audio Inputs

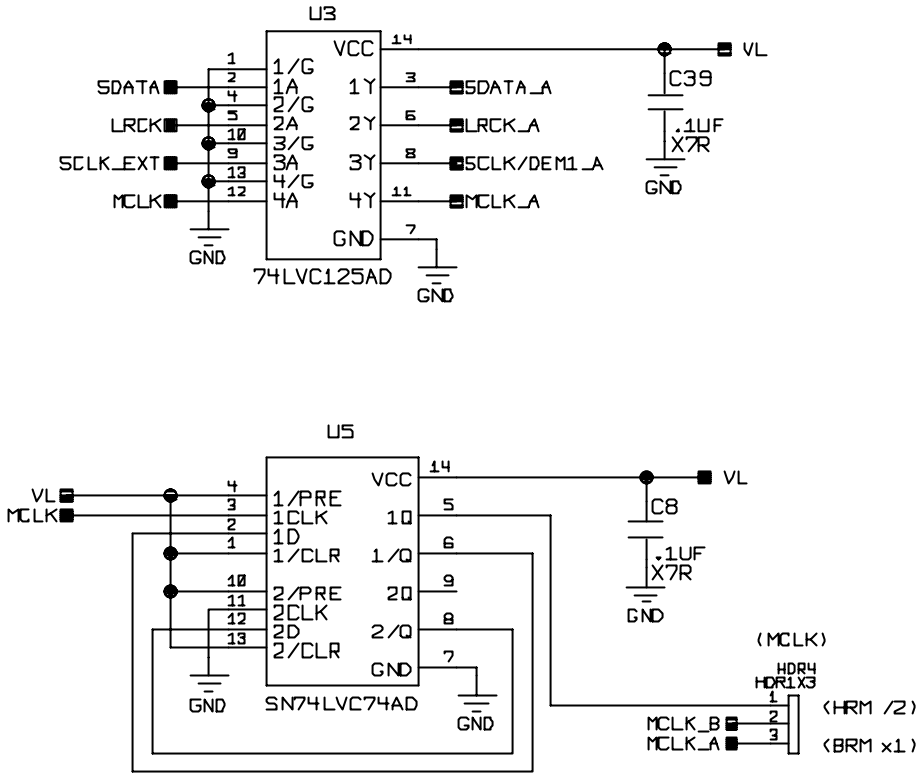


Figure 6. MCLK Divider and Level Shifter

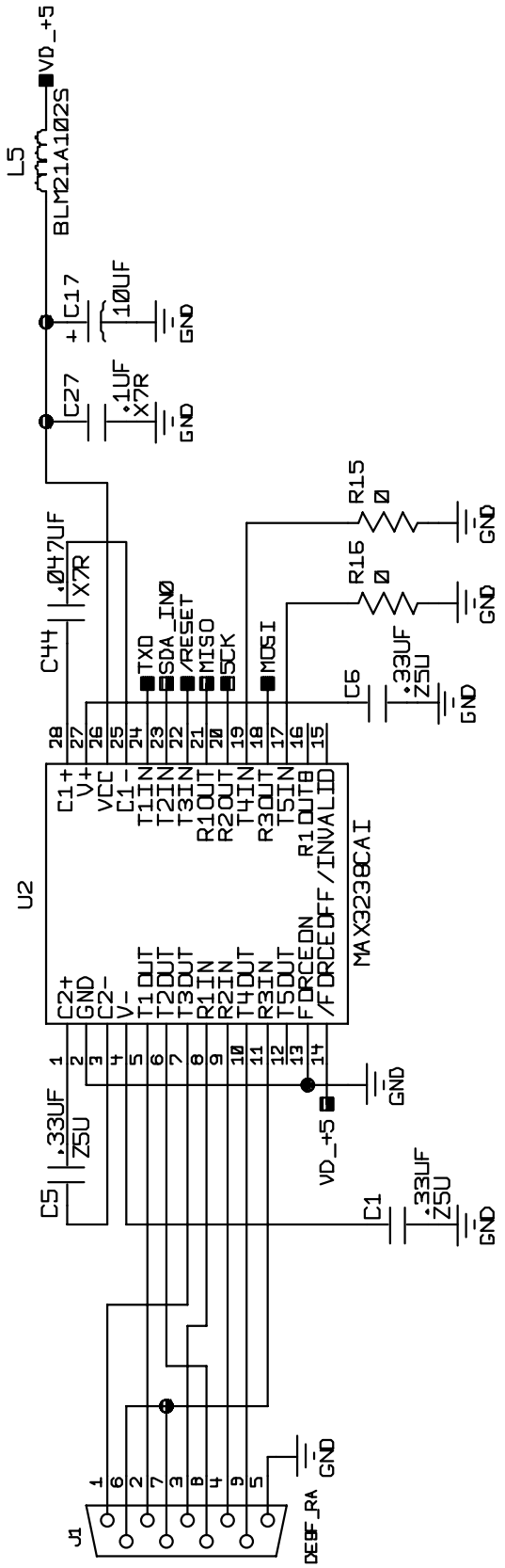


Figure 7. Control Port Interface

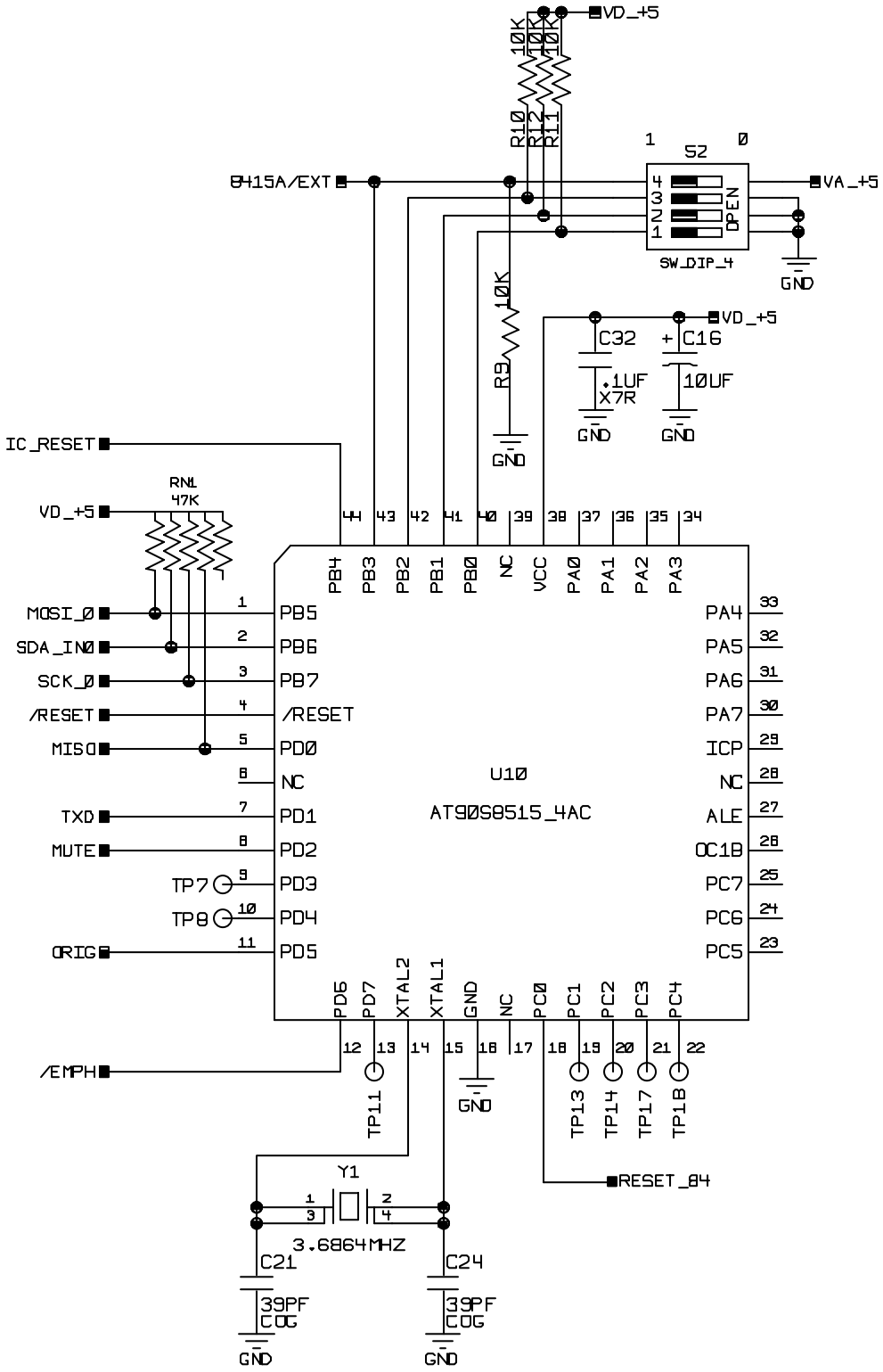


Figure 8. Control Port Microcontroller

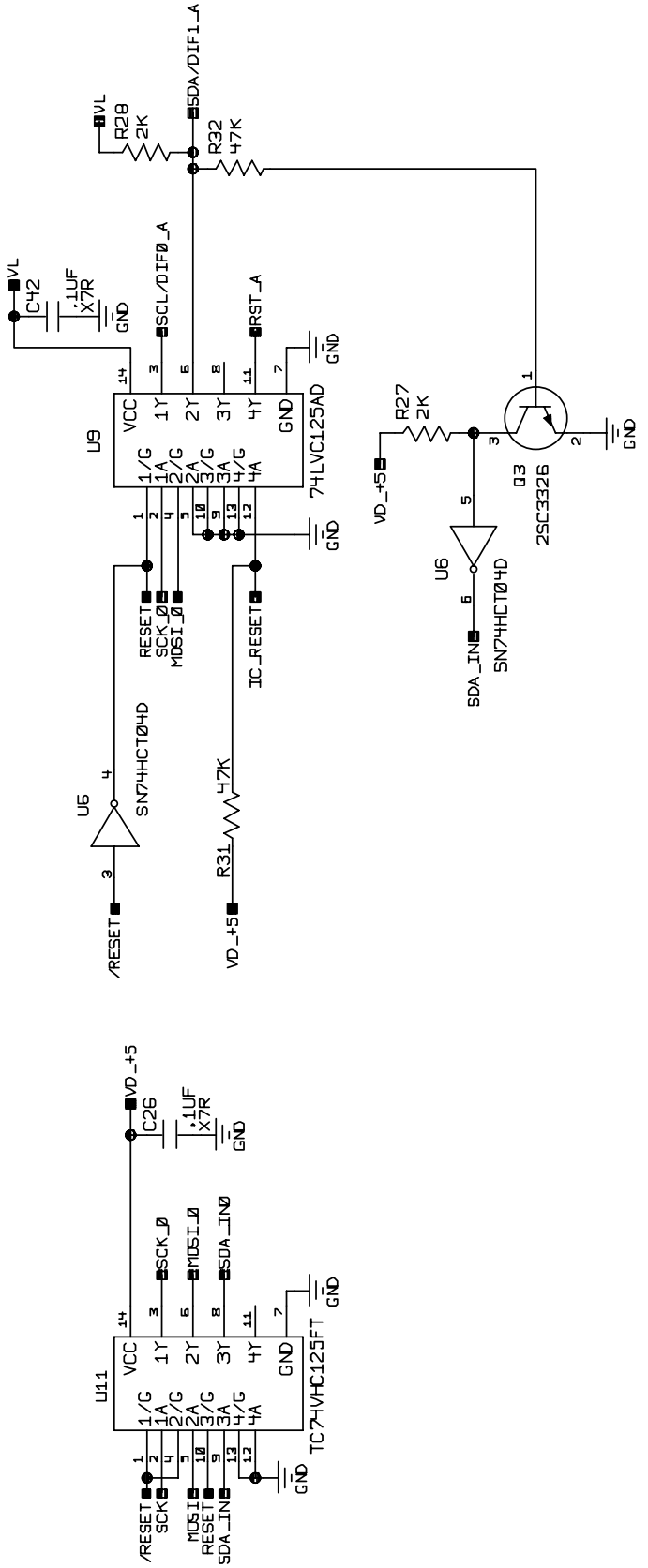


Figure 9. Control Port Level Shifter

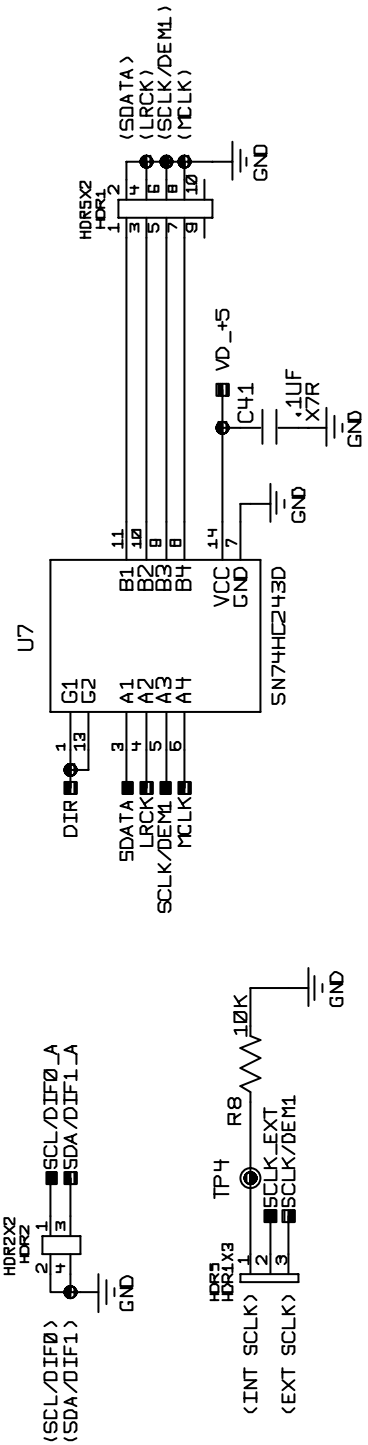


Figure 10. I/O for Clocks and Data

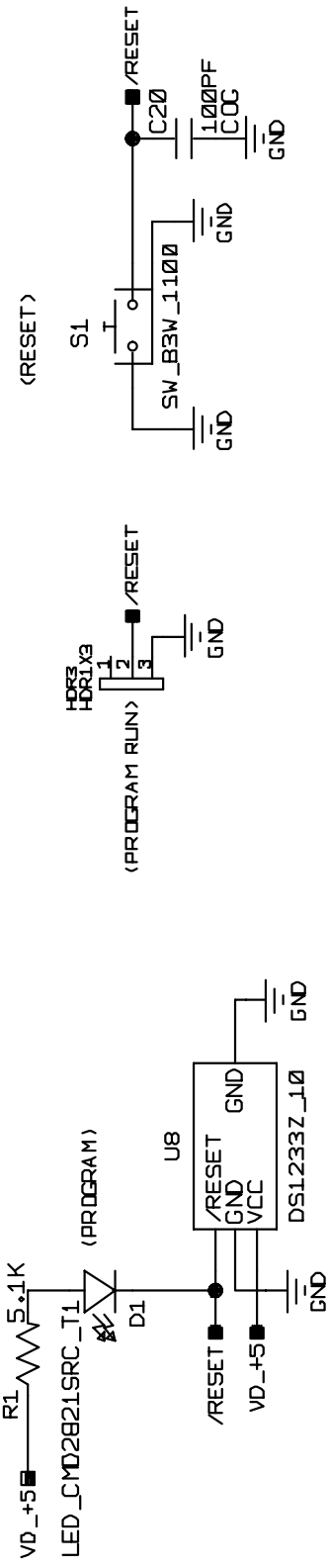


Figure 11. Reset Circuit

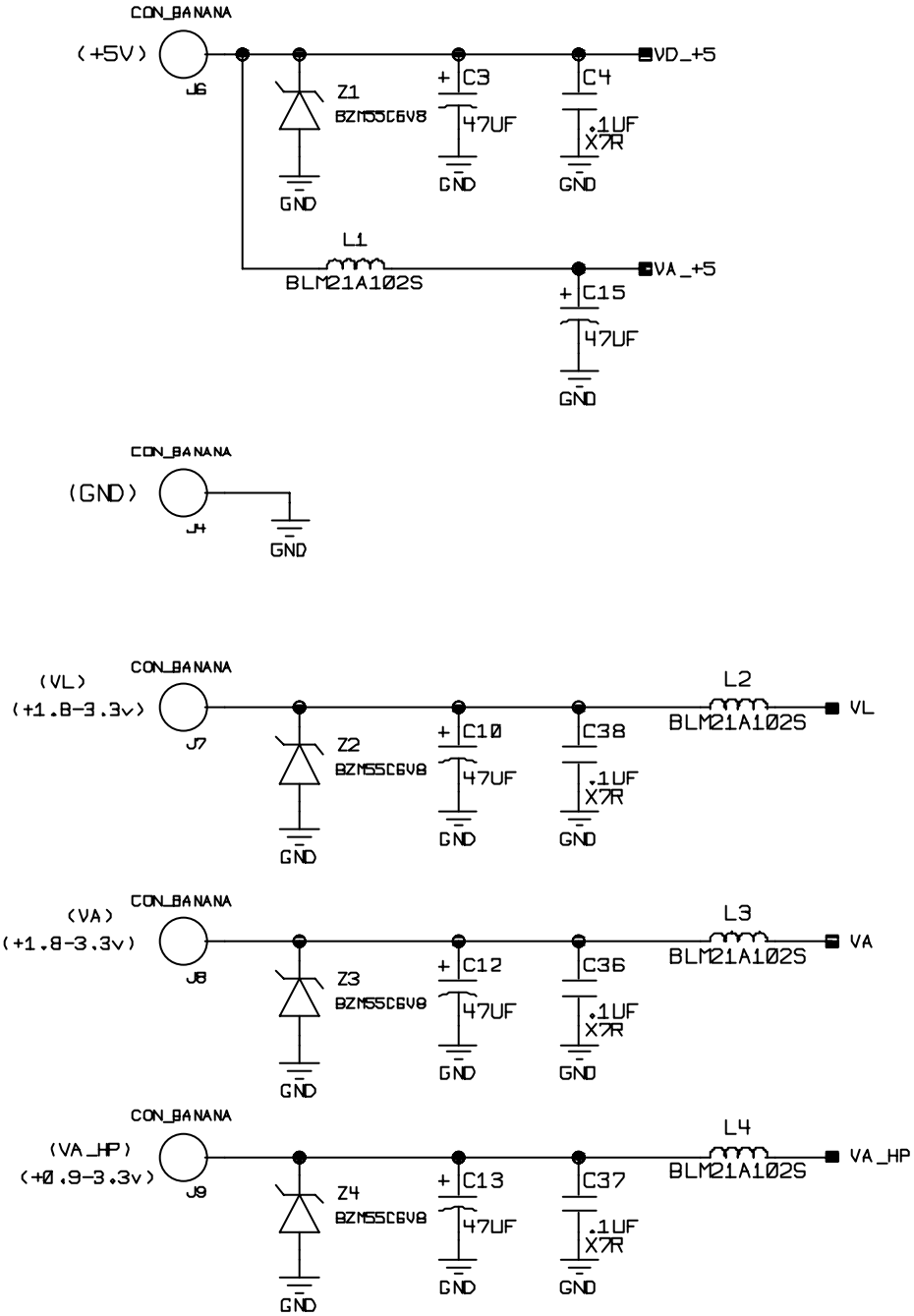


Figure 12. Power Supply

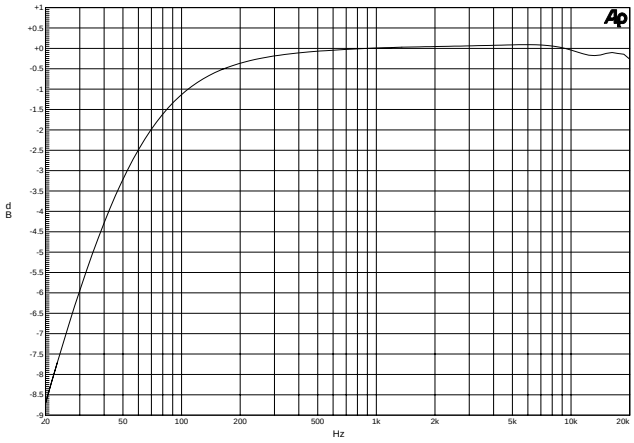


Figure 13. Frequency Response at 1.8 V

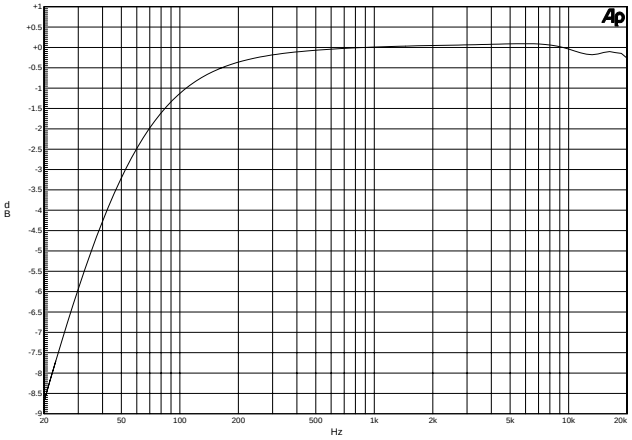


Figure 14. Frequency Response at 3.0 V

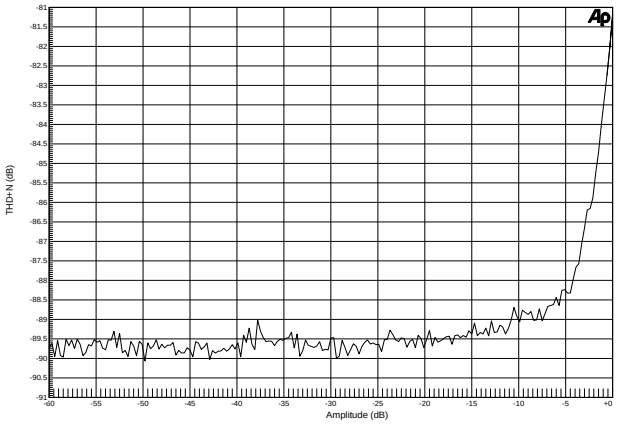


Figure 15. THD+N versus Amplitude at 1.8 V

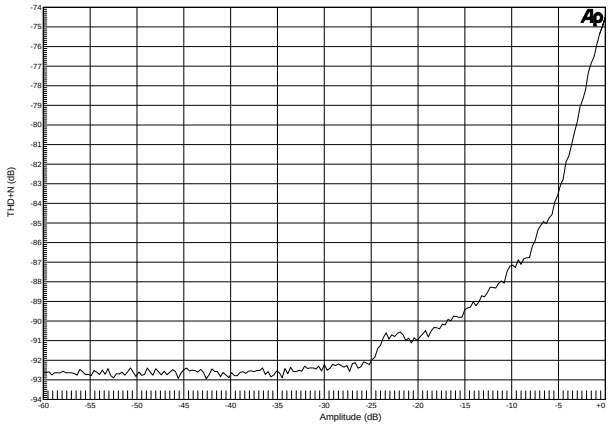


Figure 16. THD+N versus Amplitude at 3.0 V

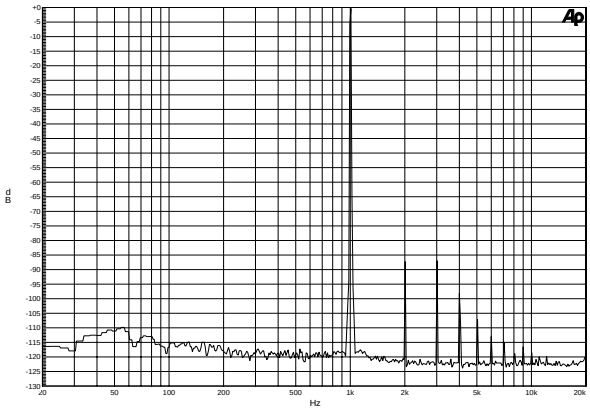


Figure 17. FFT of 1 kHz Sine Wave at 1.8 V

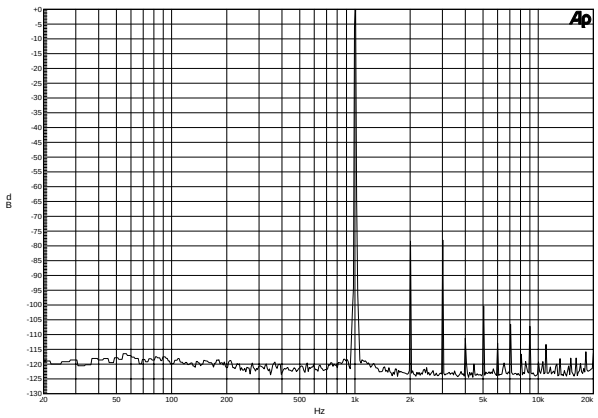


Figure 18. FFT of 1 kHz Sine Wave at 3.0 V

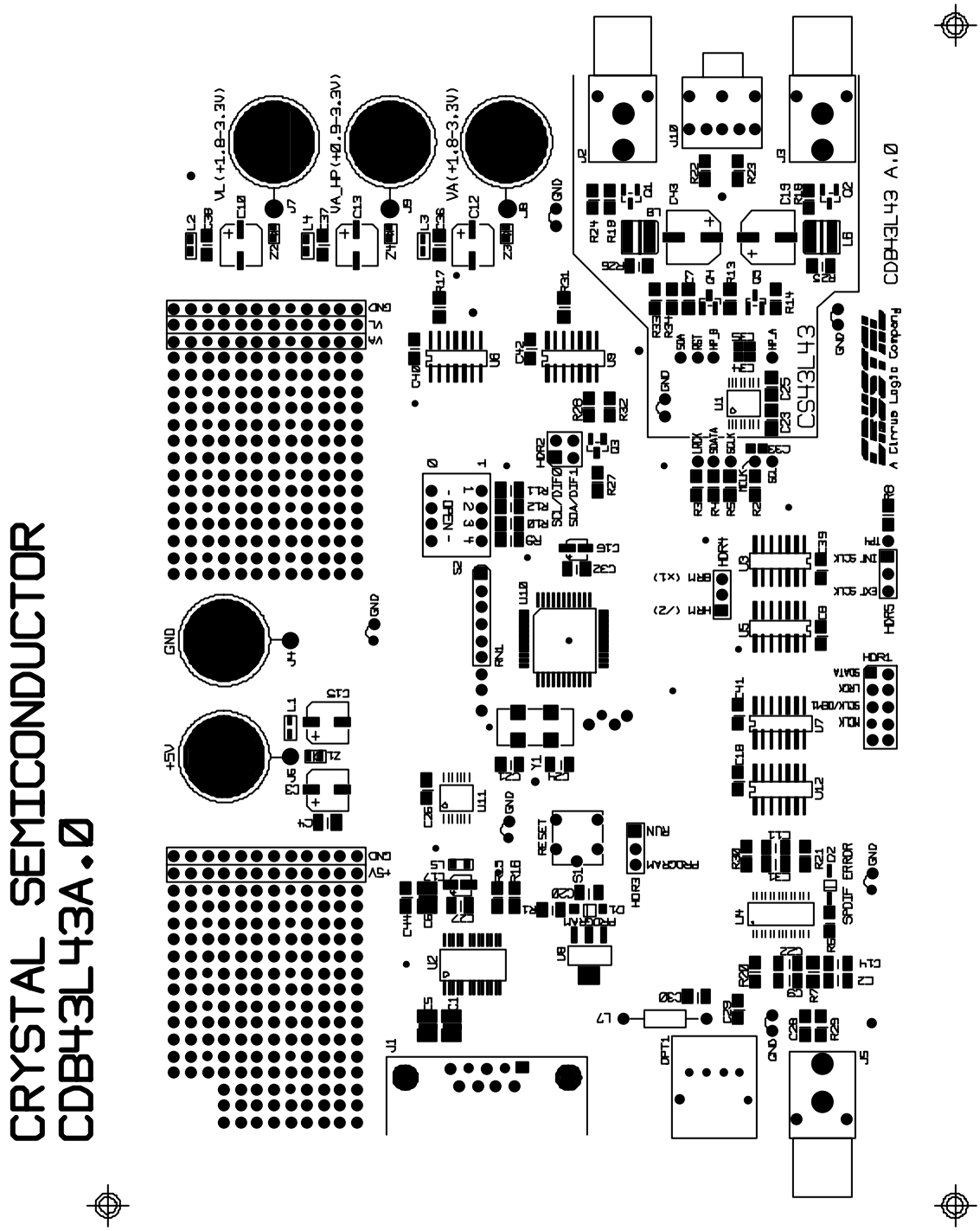


Figure 19. Silkscreen Top

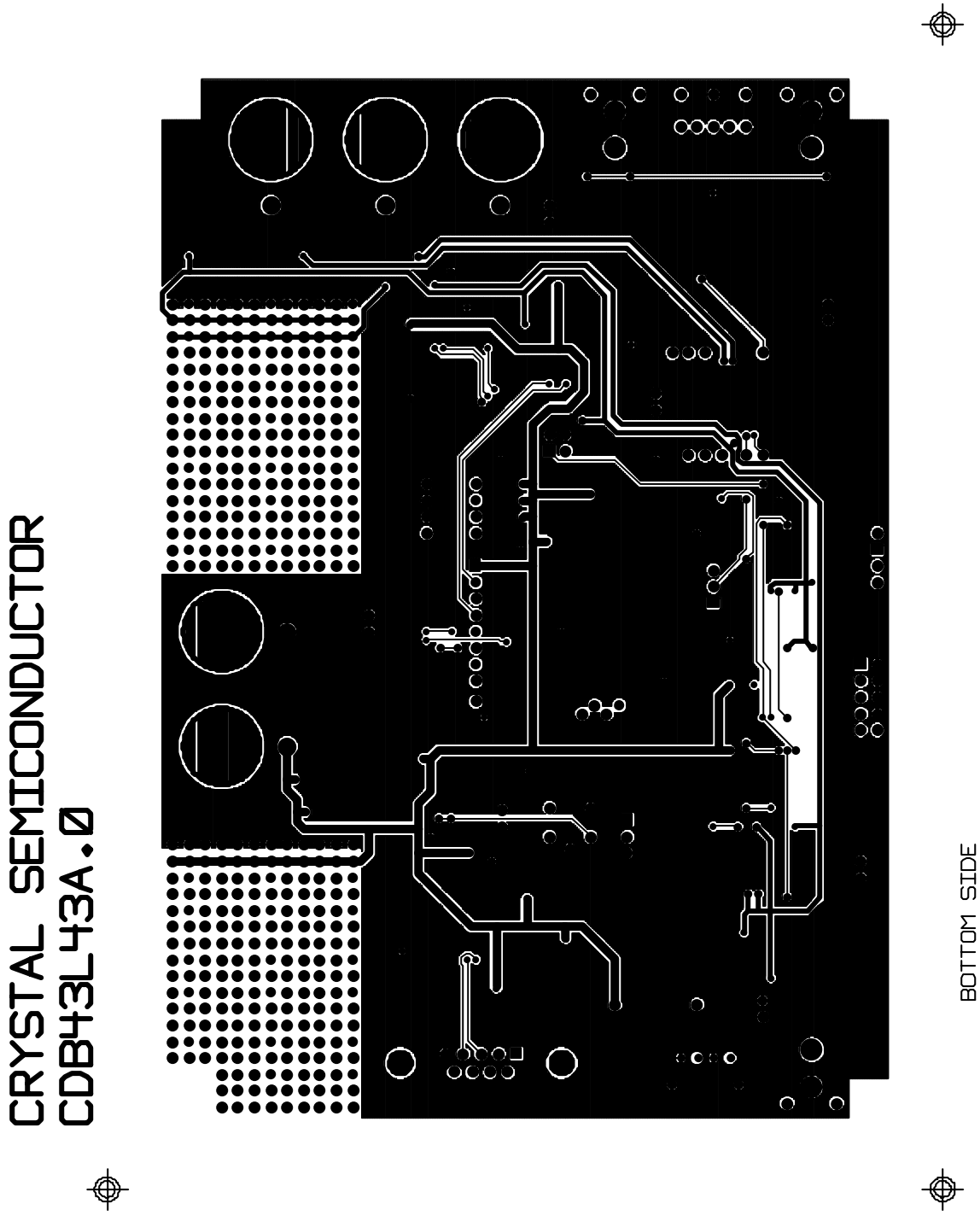


Figure 21. Bottom Side

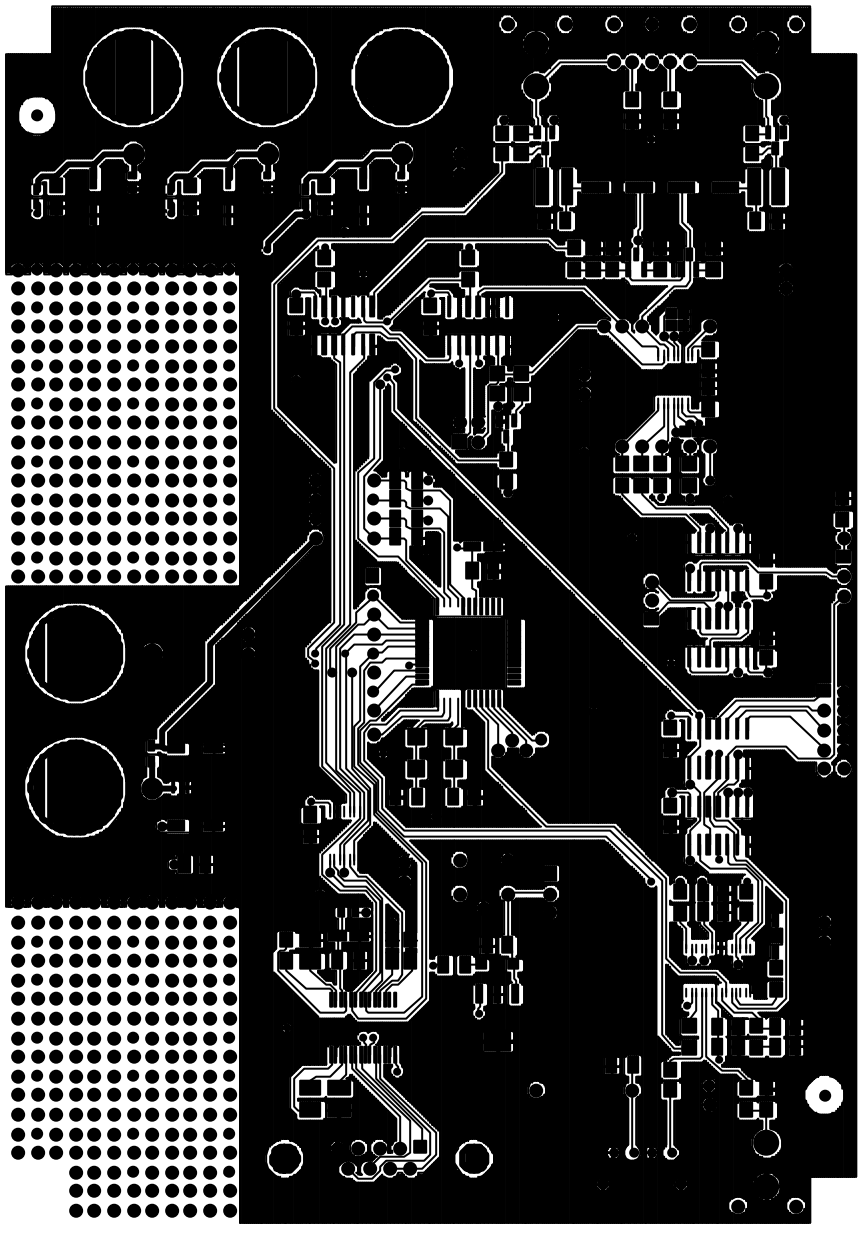


Figure 20. Top Side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