SONY

CXG1082EN

Receive Dual Low Noise Amplifier/Mixer

Description

The CXG1082EN is a receive dual low noise amplifier/mixer MMIC. This IC is designed using the Sony's GaAs J-FET process.

Features

- High conversion gain: Gp = 17dB (LNA Typ.)
  Gc = 11 to 12dB (MIX Typ.)
- Low noise figure: NF = 1.5dB (LNA Typ.)
  NF = 4.2dB (MIX Typ.)
- Single 3V power supply operation
- Low LO input power operation P_{LO} = –15dBm
- Single CTL pin achieved by the built-in inverter circuit
- 16-pin VSON package

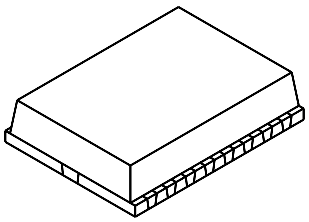
Applications

800MHz Japan digital cellular telephones (PDC)

Structure

GaAs J-FET MMIC

16 pin VSON (Plastic)



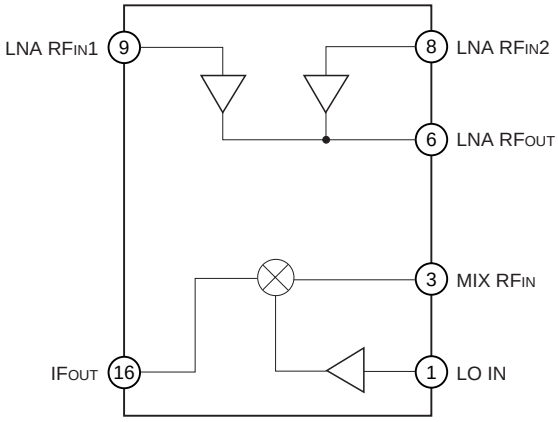
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+13	dBm
• Current consumption	I_{DD}	15	mA
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

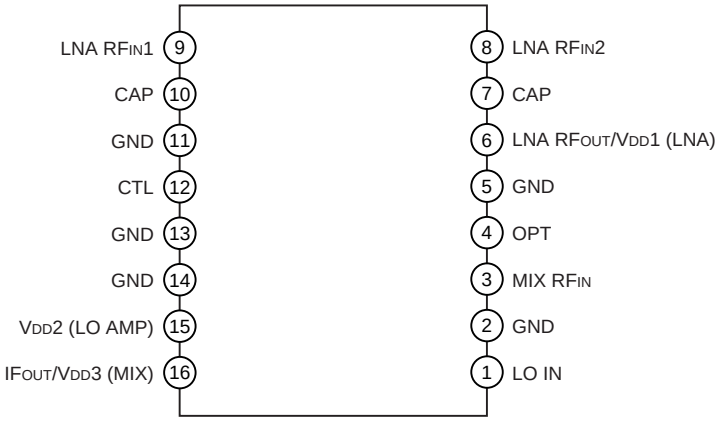
Recommended Operating Voltages

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.3	V

Block Diagram



Pin Configuration



GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E00408-PS

Electrical Characteristics

Conditions: V_{DD} = 3.0V, V_{CTL} (H) = 3.0V, V_{CTL} (L) = 0V, $f_{RF}1$ = 870MHz, $f_{RF}2$ = 820MHz, $f_{LO} = f_{RF} - 130$MHz, P_{LO} = –15dBm, Ta = 25°C, unless otherwise specified

Low Noise Amplifier Block

Item	Symbol	Path	RF frequency	V_{CTL}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	H	—	1.9	2.5	mA	When no signal
			—	L	—	1.9	2.5		
Control current	I_{CTL}	—	—	H	—	55	80	µA	
			—	L	–1	0	—		
Power gain	Gp	$RF_{IN}1 \rightarrow RF_{OUT}$	$f_{RF}1$	H	15	17	19	dB	When a small signal
				L	—	–20	–15		
		$RF_{IN}2 \rightarrow RF_{OUT}$	$f_{RF}2$	H	—	–25	–20		
				L	15	17	19		
Noise figure	NF	$RF_{IN}1 \rightarrow RF_{OUT}$	$f_{RF}1$	H	—	1.5	2.0	dB	
		$RF_{IN}2 \rightarrow RF_{OUT}$	$f_{RF}2$	L	—	1.5	2.0		
Input IP3	IIP3	$RF_{IN}1 \rightarrow RF_{OUT}$	$f_{RF}1$	H	–13	–9	—	dBm	*1
		$RF_{IN}2 \rightarrow RF_{OUT}$	$f_{RF}2$	L	–13	–9	—		
Isolation	Iso	$RF_{OUT} \rightarrow RF_{IN}1$	$f_{RF}1$	H	17	22	—	dBm	When a small signal
		$RF_{OUT} \rightarrow RF_{IN}2$	$f_{RF}2$	L	18	23	—		

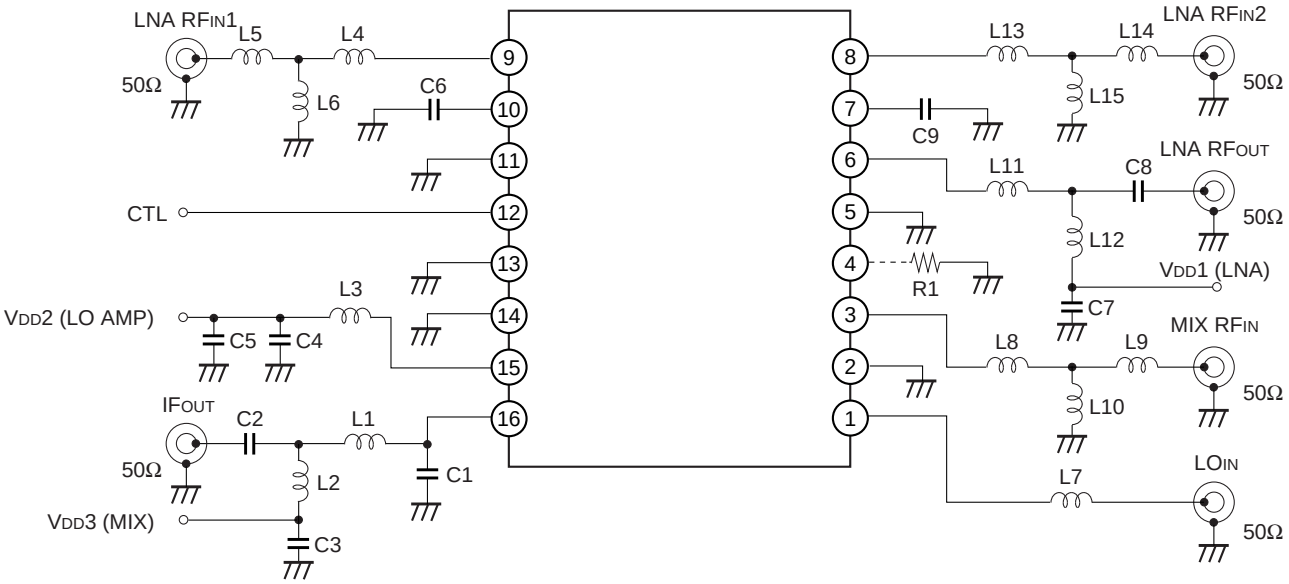
Mixer Block

Item	Symbol	RF frequency	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	4.5	6.0	mA	When no signal
Power gain	Gc	$f_{RF}1$	10	12	14	dB	When a small signal
		$f_{RF}2$	9	11	13		
Noise figure	NF	$f_{RF}1$	—	4.2	6.0	dB	
		$f_{RF}2$	—	4.2	6.0		
Input IP3	IIP3	$f_{RF}1$	–4.0	–1.0	—	dBm	*1
		$f_{RF}2$	–3.5	–0.5	—		
LO to RF leak level	Plk	$f_{RF}1$	—	–31	–26	dBm	f_{LO} = 740MHz
		$f_{RF}2$	—	–31	–26		f_{LO} = 690MHz

The values shown above are the specified values on the Sony's recommended evaluation board. (When no option pin resistor is added.)

*1 Conversion from the IM3 suppression ratio for two-wave input: PRF = –30dBm (low noise amplifier block)/ –25dBm (mixer block) at fRFoffset = 100kHz.

Recommended Evaluation Circuit

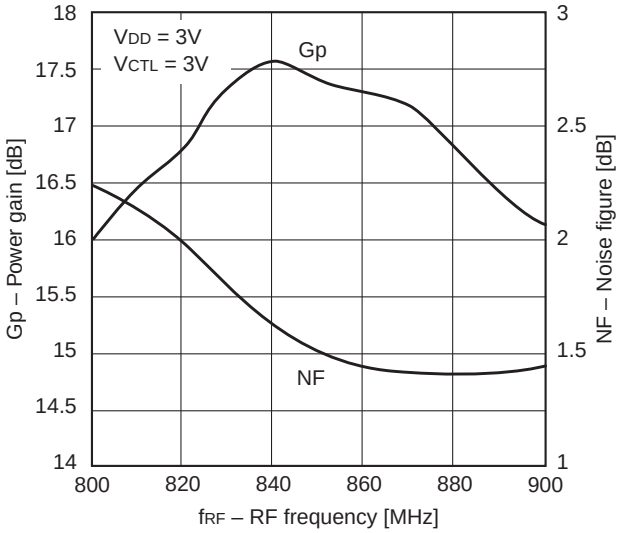


L1	150nH	L11	18nH	C6	18pF
L2	120nH	L12	10nH	C7	1000pF
L3	33nH	L13	22nH	C8	100pF
L4	18nH	L14	5.6nH	C9	56pF
L5	6.8nH	L15	22nH	R1	
L6	27nH	C1	6pF		
L7	33nH	C2	1000pF		
L8	27nH	C3	1000pF		
L9	5.6nH	C4	100pF		
L10	12nH	C5	1000pF		

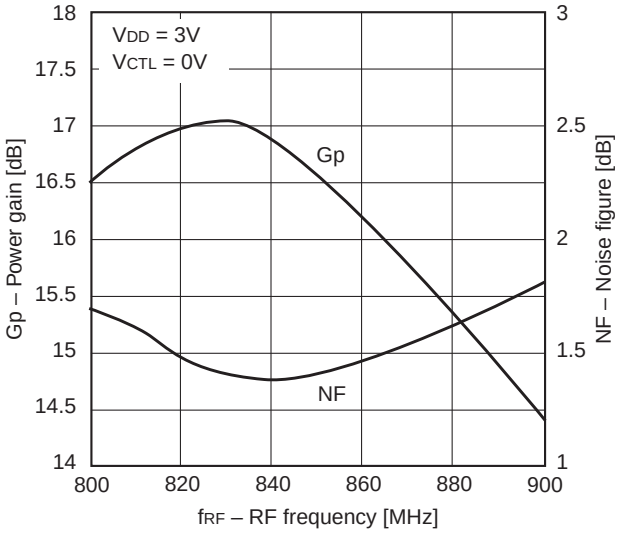
Example of Representative Characteristics (Ta = 25°C)

Low Noise Amplifier Block

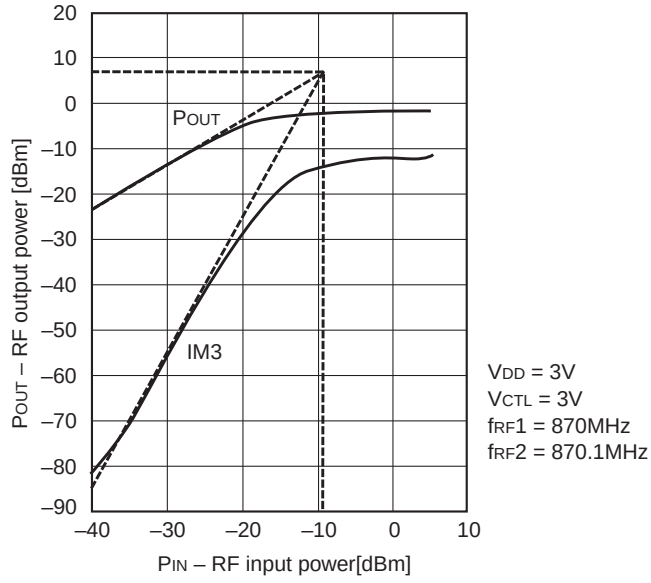
Path $RF_{IN}1 \rightarrow RF_{OUT}$
Gp, NF vs. f_{RF}



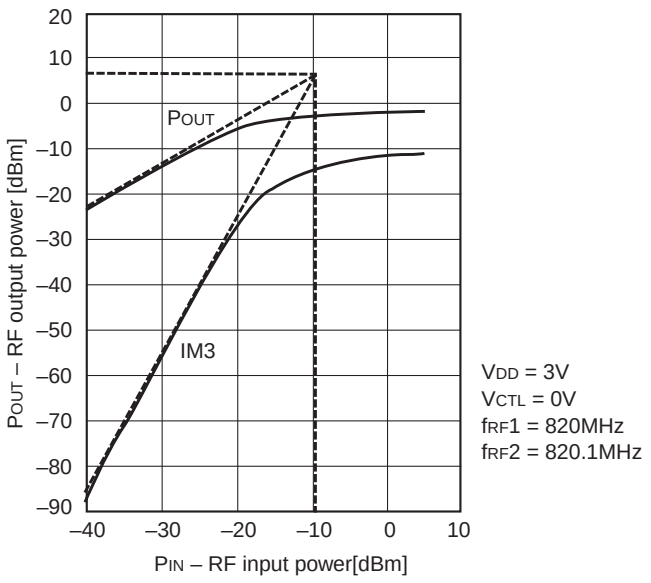
Path $RF_{IN}2 \rightarrow RF_{OUT}$
Gp, NF vs. f_{RF}



Path $RF_{IN}1 \rightarrow RF_{OUT}$
P_{OUT}, IM3 vs. P_{IN}

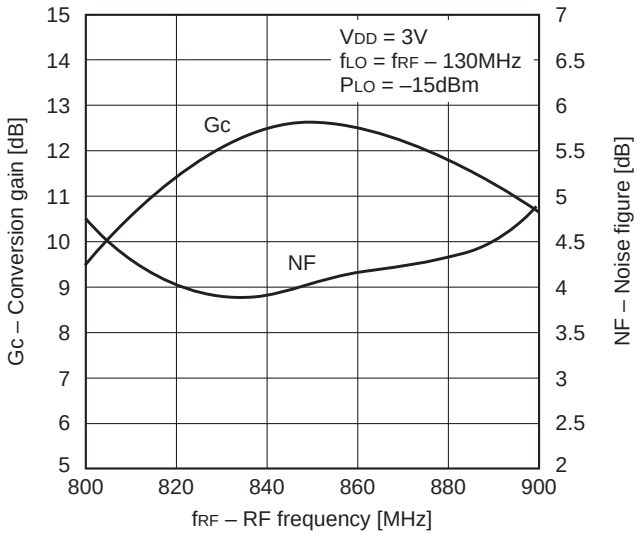


Path $RF_{IN}2 \rightarrow RF_{OUT}$
P_{OUT}, IM3 vs. P_{IN}

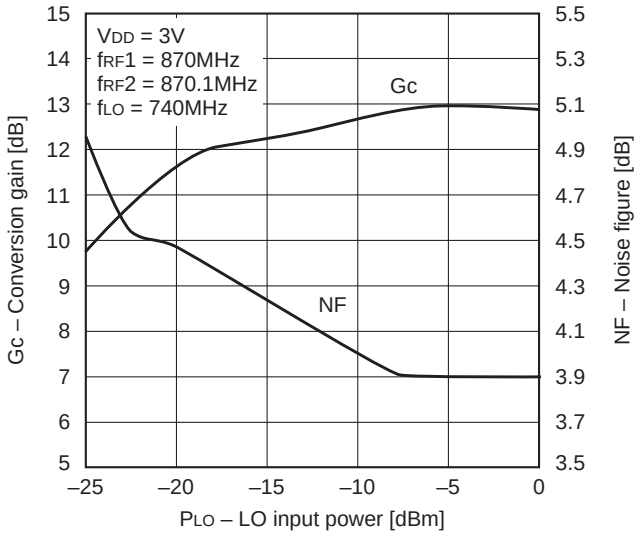


Mixer Block

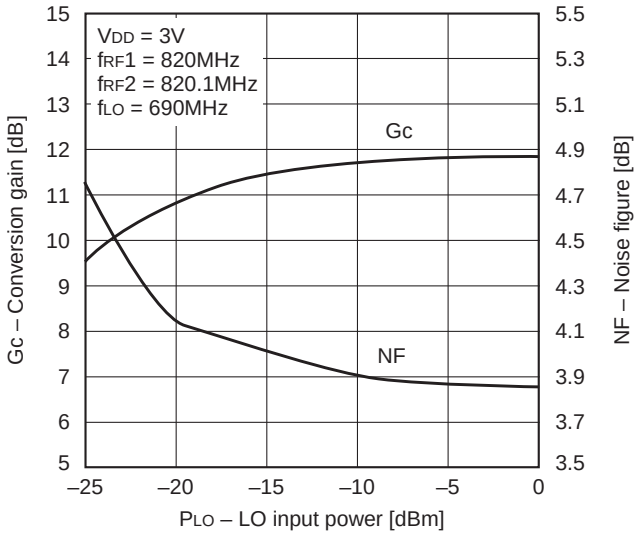
Gc, NF vs. f_{RF}



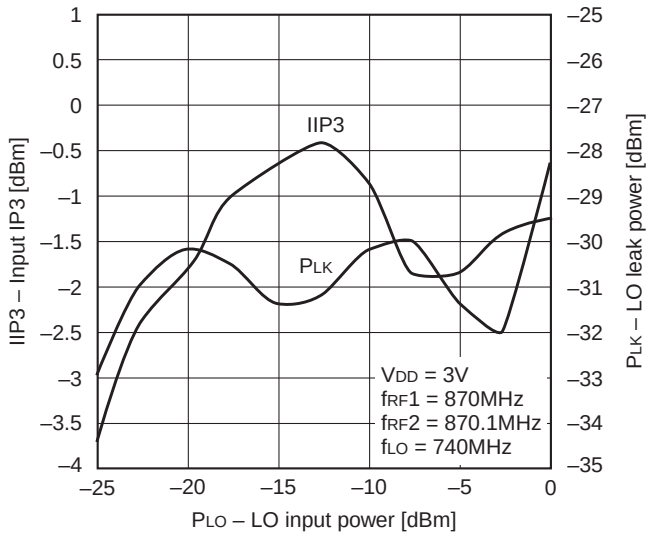
Gc, NF vs. P_{LO}



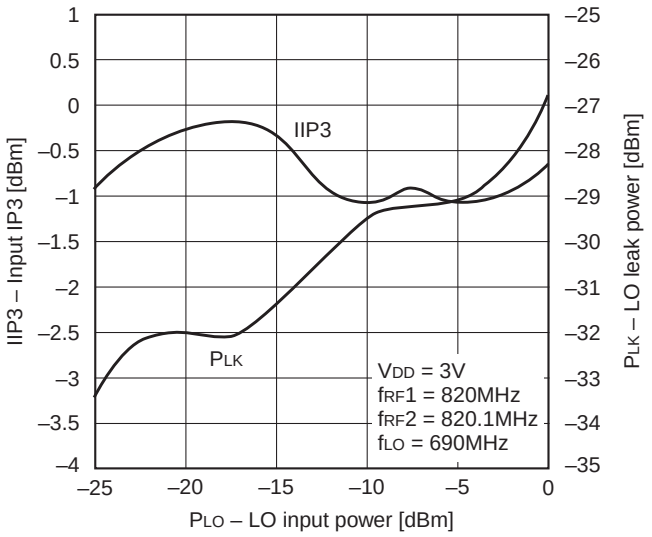
Gc, NF vs. P_{LO}



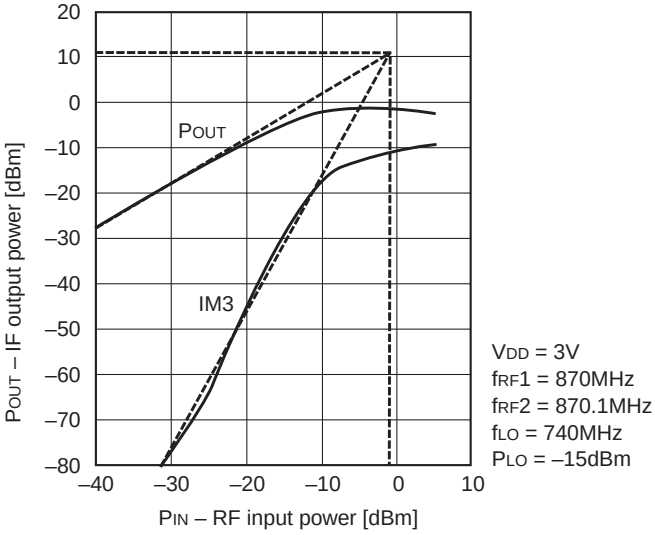
IIP3, PLK vs. PLO



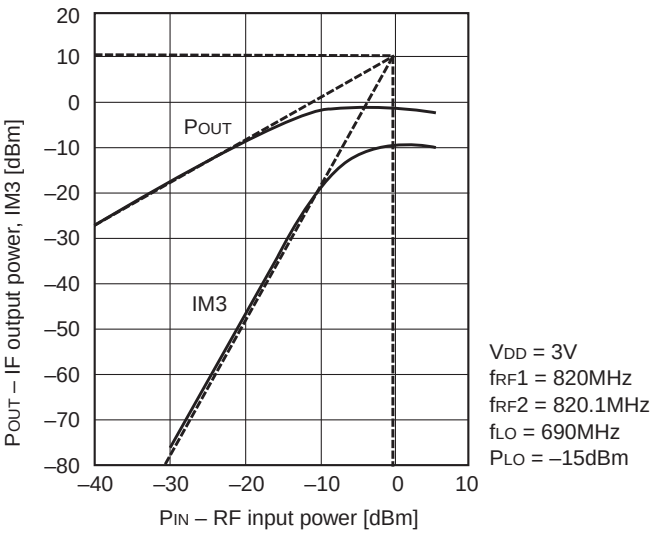
IIP3, PLK vs. PLO



POUT, IM3 vs. PIN



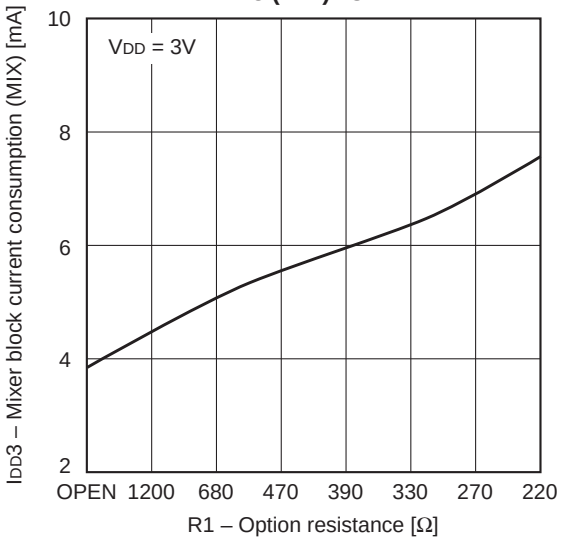
POUT, IM3 vs. PIN



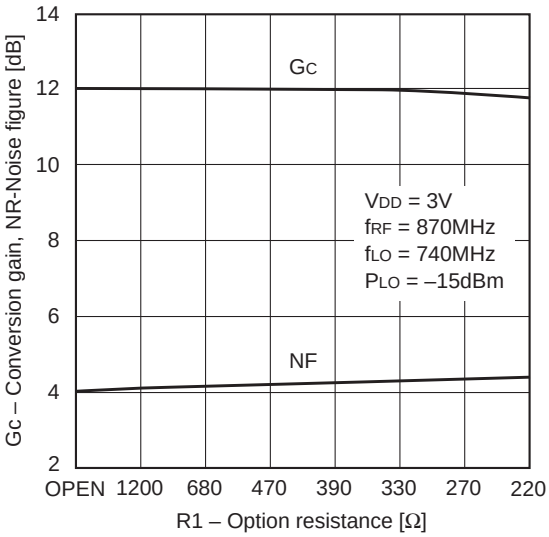
Example of Characteristics for Option Resistance R1 Changed (Ta = 25°C)

Mixer Block

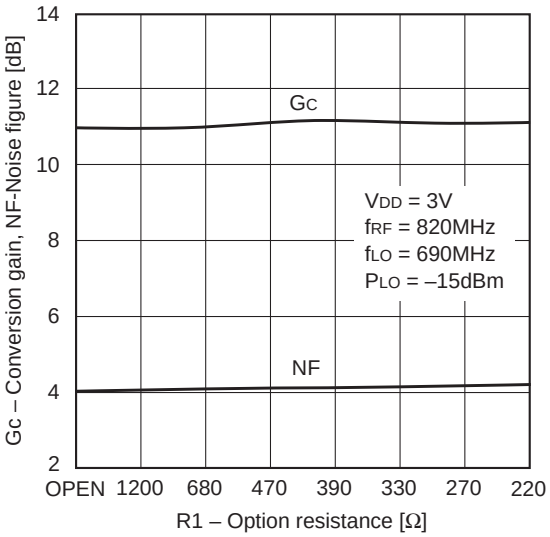
IDD3 (MIX) vs. R1



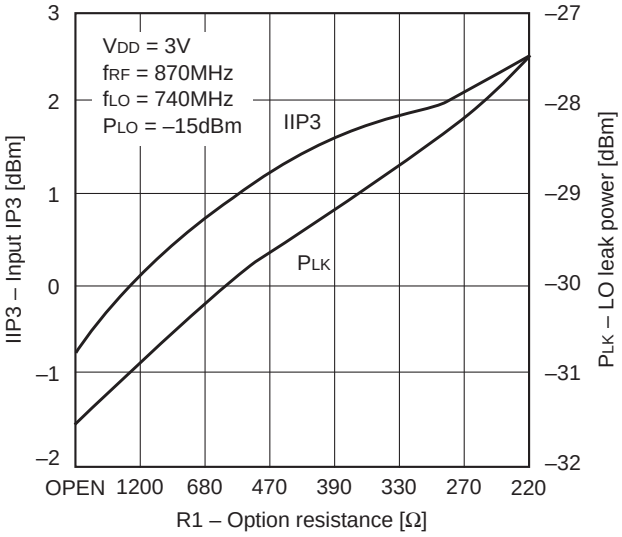
Gc, NF vs. R1



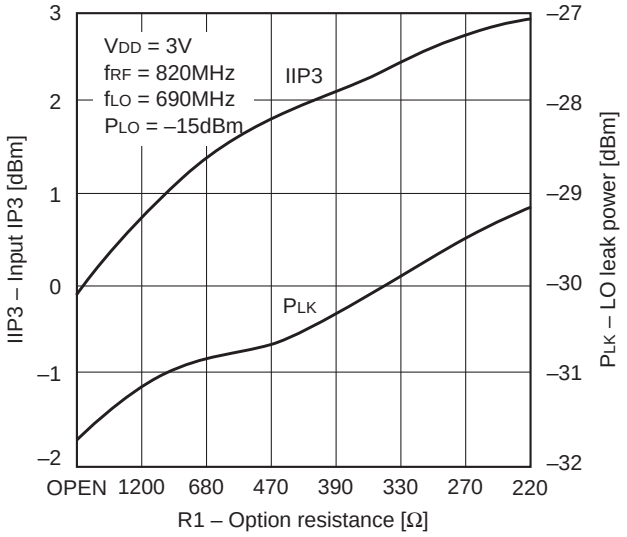
Gc, NF vs. R1



IIP3, PLK vs. R1

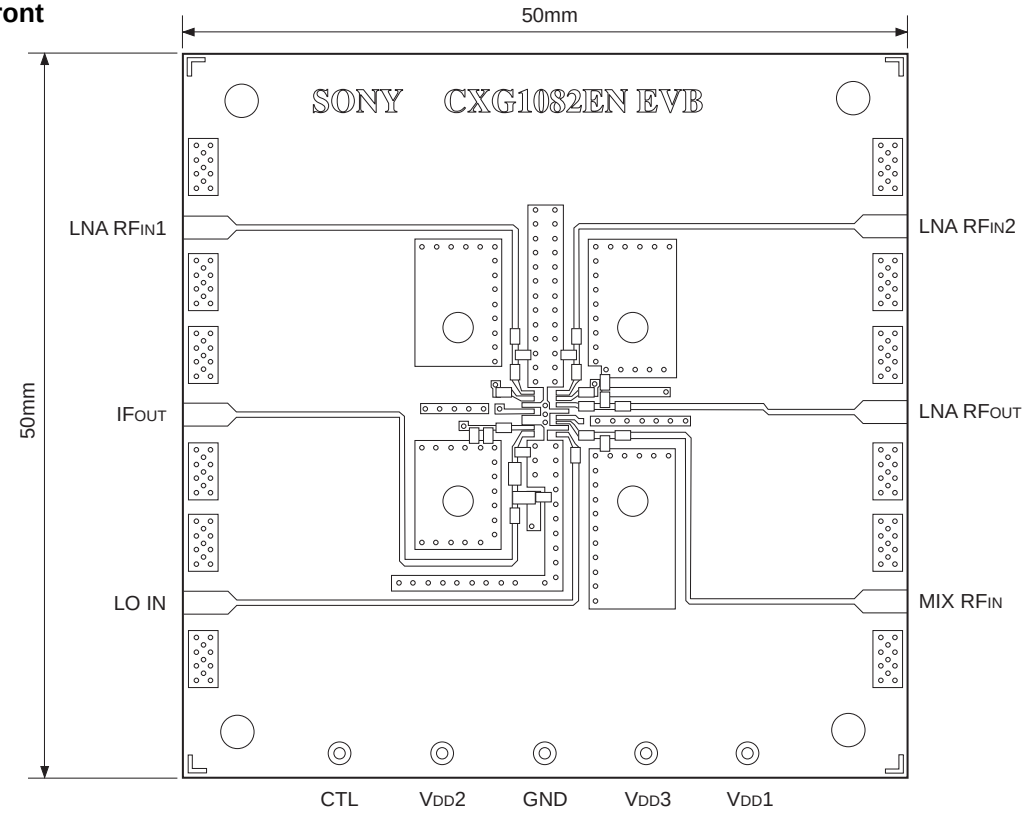


IIP3, PLK vs. R1



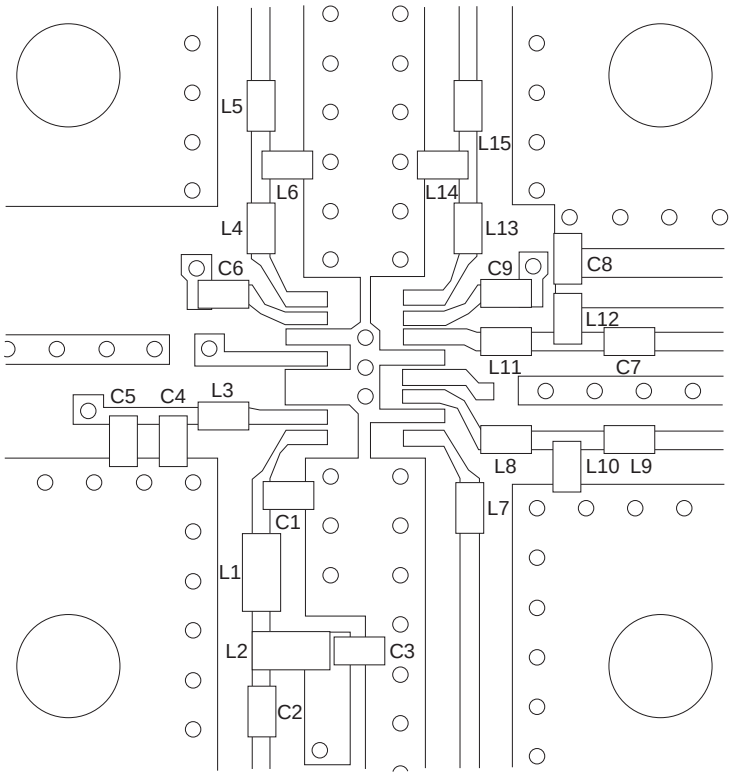
Recommended Evaluation Board

Front



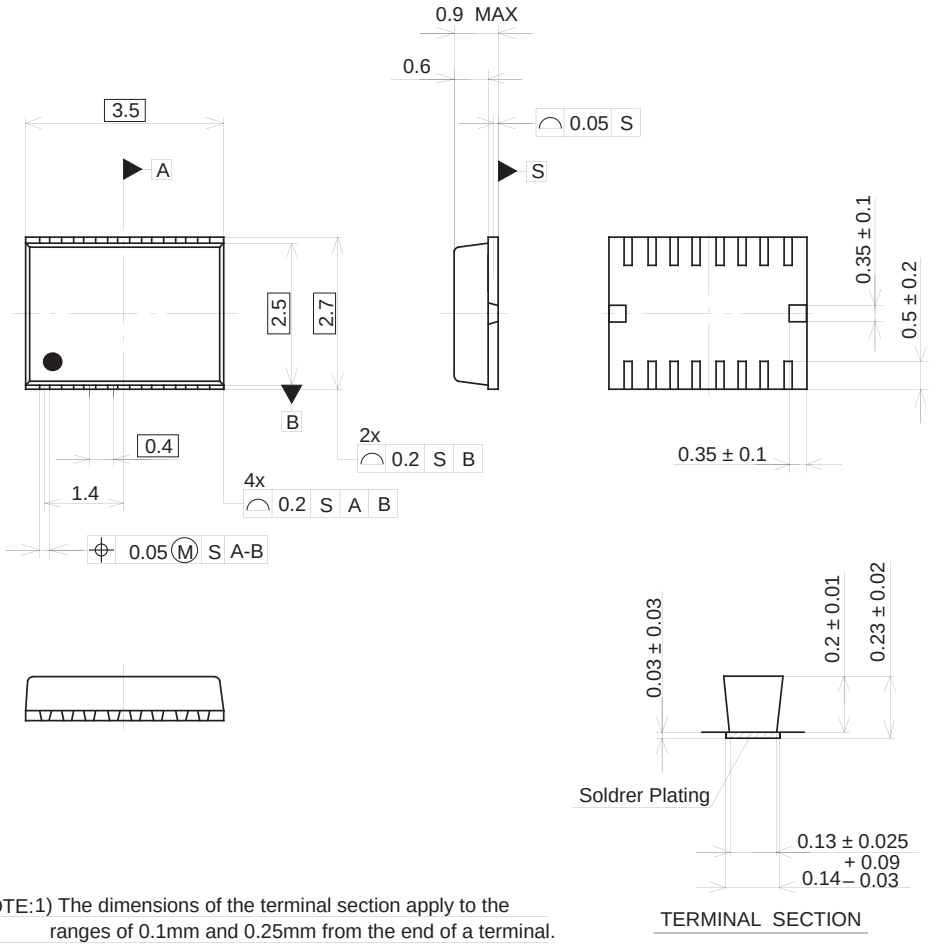
Glass fabric-base 4-layer epoxy board (thickness: 0.2mm × 2)
GND for the whole 2nd and 3rd layers

Enlarged Diagram of Center Part



Package Outline Unit: mm

16PIN VSON(PLASTIC)



NOTE:1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

TERMINAL SECTION

SONY CODE	VSON-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g