PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS87366

## 1-TO-6, DIFFERENTIAL TO 3.3V LVPECL CLOCK GENERATOR W/FORWARD ERROR CORRECTION

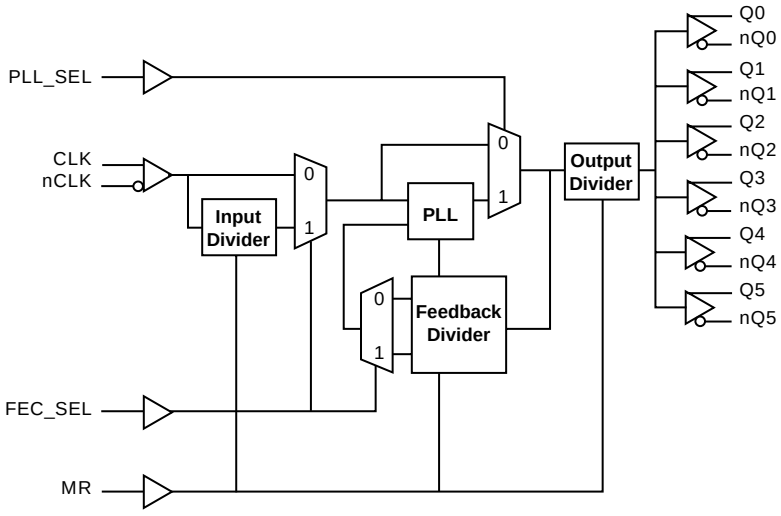
## GENERAL DESCRIPTION

The ICS87366 is a 1-to-6, Differential to 3.3V LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87366 can multiply the reference clock times 3 or multiply times 3 * 66/64 thereby applying an FEC rate to the reference clock. The ICS87366 is an ideal device in any application requiring x3 multiplication with an 66/64 FEC option while maintaining low jitter. Common applications may include networking and storage area networks.

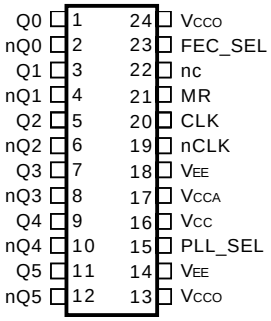
## FEATURES

- 6 differential LVPECL outputs
- 1 differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency: FEC_SEL = 0, 159.375MHz
  FEC_SEL = 1, 164.355MHz
- Cycle-to-cycle jitter: FEC_SEL = 0, 15ps (typical)
  FEC_SEL = 1, 20ps (typical)
- Full 3.3V or 3.3V core/2.5V output supply voltage
- 0°C to 70°C ambient operating temperature

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS87366**
**24-Lead, 300-MIL SOIC**
7.5mm x 15.33mm x 2.3mm body package
**M Package**
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 4 | Q1, nQ1 | Output | | Differential output pair. LVPECL interface levels. |
| 5, 6 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |
| 7, 8 | Q3, nQ3 | Output | | Differential output pair. LVPECL interface levels. |
| 9, 10 | Q4, nQ4 | Output | | Differential output pair. LVPECL interface levels. |
| 11, 12 | Q5, nQ5 | Output | | Differential output pair. LVPECL interface levels. |
| 13, 24 | $V_{CCO}$ | Power | | Output supply pins. |
| 14, 18 | $V_{EE}$ | Power | | Negative supply pins. |
| 15 | PLL_SEL | Input | Pullup | Selects between the PLL and CLK, nCLK as the input to the dividers. When HIGH, selects PLL. When LOW, selects CLK, nCLK. LVCMOS / LVTTL interface levels. |
| 16 | $V_{CC}$ | Power | | Core supply pin. |
| 17 | $V_{CCA}$ | Power | | Analog supply pin. |
| 19 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}$/2 defaults when left floating. |
| 20 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 21 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels. |
| 22 | nc | Unused | | No connect. |
| 23 | FEC_SEL | Input | Pullup | Select pin controls the Feedback Divide value. LVCMOS / LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |

**TABLE 3. FUNCTION TABLE**

| Inputs | | |
|---|---|---|
| **MR** | **FEC_SEL** | **Multiplier** |
| 1 | X | Reset: Qx = LOW, nQx = HIGH |
| 0 | 0 | 3 |
| 0 | 1 | 3 x 33/32 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 50°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | TBD | | mA |
| $I_{CCA}$ | Analog Supply Current | | | TBD | | mA |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | PLL_SEL, MR, FEC_SEL | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | PLL_SEL, MR, FEC_SEL | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | MR | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | PLL_SEL, FEC_SEL | $V_{CC} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | MR | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | PLL_SEL, FEC_SEL | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nCLK | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | nCLK | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage | | | 0.15 | | 1.0 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 0.5 | | $V_{CC}$ - 0.85 | V |

NOTE 1: Common mode input voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC}$ + 0.3V.

**TABLE 4D. LVPECL DC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = 3.3V±5%, $V_{CCO}$ = 3.3V±5% OR 2.5V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO}$ - 1.4 | | $V_{CCO}$ - 1.0 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO}$ - 2.0 | | $V_{CCO}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | µA |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$ - 2V.

**TABLE 5A. AC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = $V_{CCO}$ = 3.3V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 159.375 | | 164.355 | MHz |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 3 | FEC_SEL = 0 | | 15 | | ps |
| | | FEC_SEL = 1 | | 20 | | ps |
| *t*sk(o) | Output Skew; NOTE 1, 3 | | | TBD | | ps |
| *t*sk(pp) | Part-to-Part Skew, NOTE 2 | | | TBD | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | | 50 | | % |
| $t_{LOCK}$ | PLL Lock Time | | | | 1 | ms |

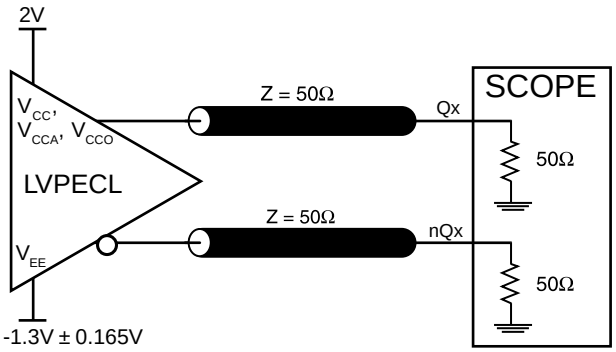
NOTE 1: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO}$/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5B. AC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = 3.3V±5%, $V_{CCO}$ = 2.5V±5%, $T_A$ = 0°C TO 70°C

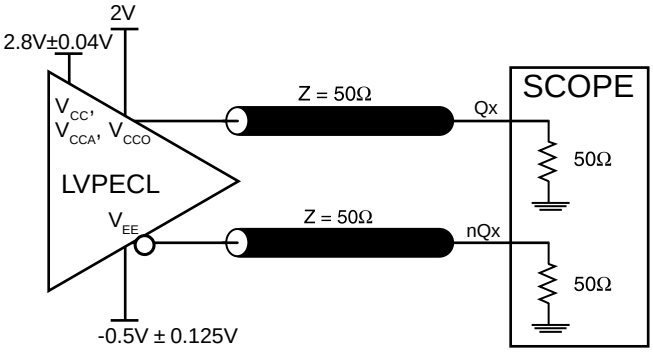
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 159.375 | | 164.355 | MHz |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 3 | FEC_SEL = 0 | | TBD | | ps |
| | | FEC_SEL = 1 | | TBD | | ps |
| *t*sk(o) | Output Skew; NOTE 1, 3 | | | TBD | | ps |
| *t*sk(pp) | Part-to-Part Skew, NOTE 2 | | | TBD | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | | 50 | | % |
| $t_{LOCK}$ | PLL Lock Time | | | | 1 | ms |

NOTE 1: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO}$/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

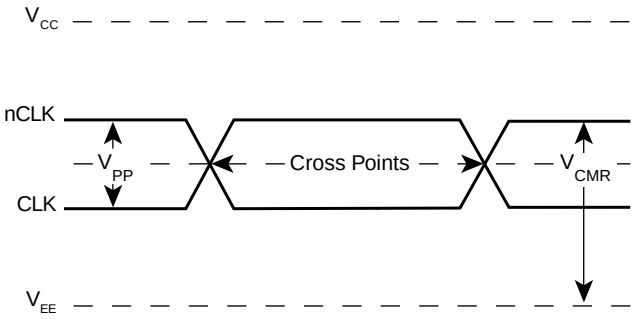
# PARAMETER MEASUREMENT INFORMATION



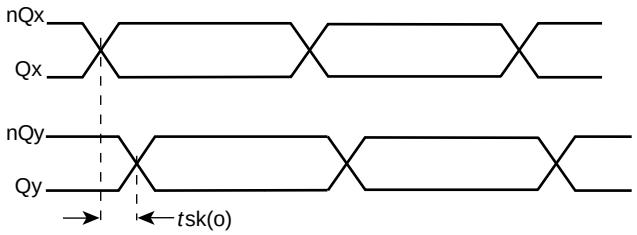

**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



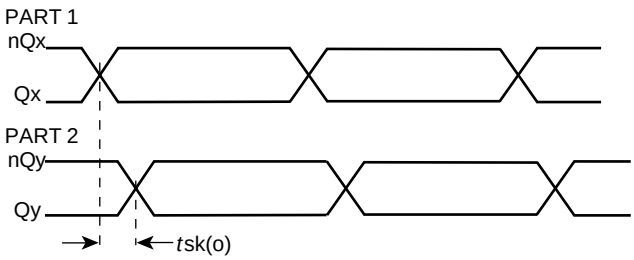

**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



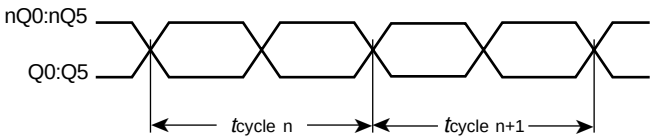

**DIFFERENTIAL INPUT LEVEL**




**OUTPUT SKEW**



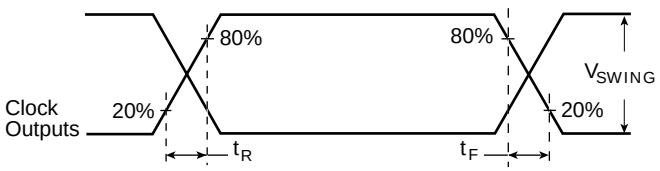

**PART-TO-PART SKEW**



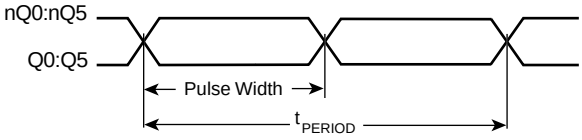

$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

**CYCLE-TO-CYCLE JITTER**




**OUTPUT RISE/FALL TIME**




$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87366 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$ and $V_{CCO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$ pin.

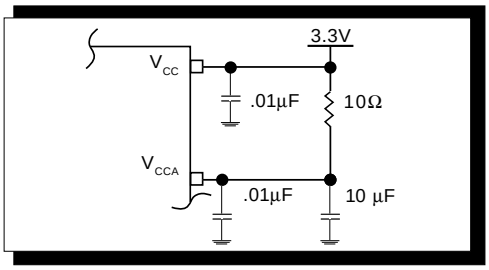



FIGURE 1. POWER SUPPLY FILTERING

## TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

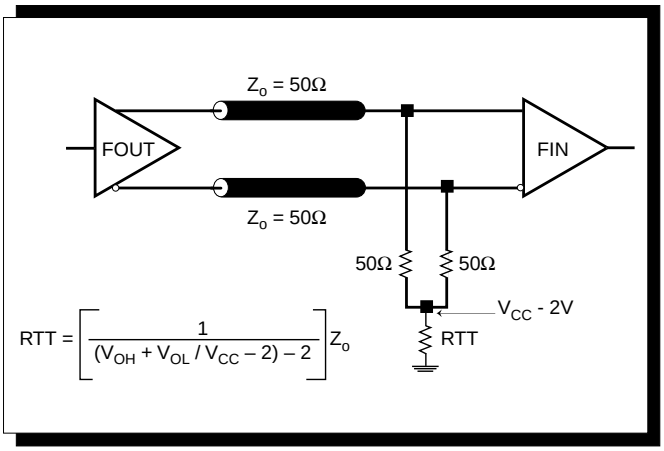



FIGURE 2A. LVPECL OUTPUT TERMINATION

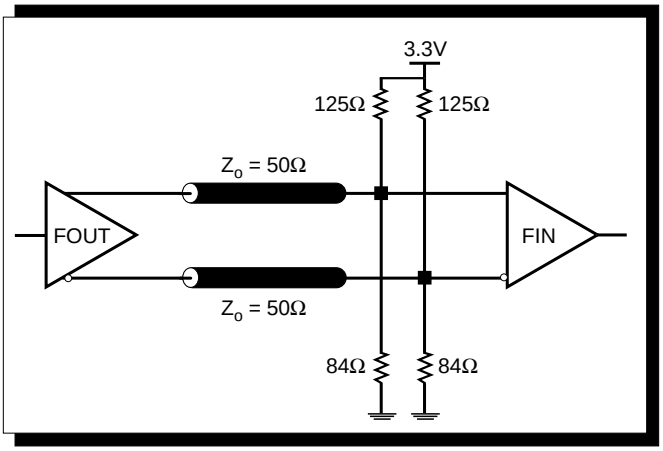



FIGURE 2B. LVPECL OUTPUT TERMINATION

## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

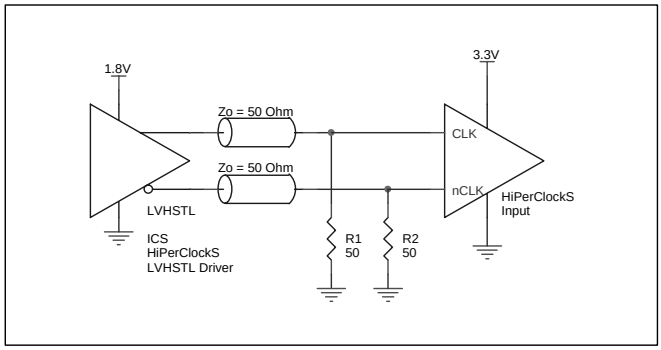



**FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER**

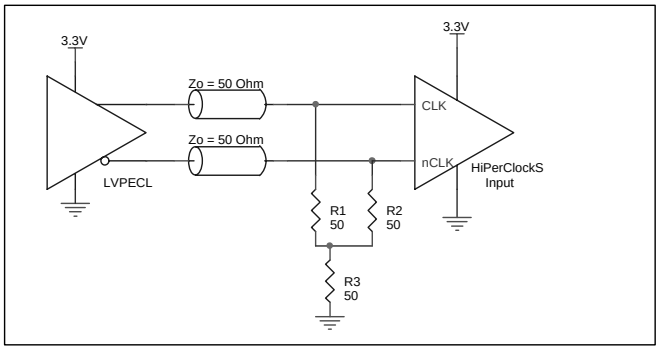



**FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

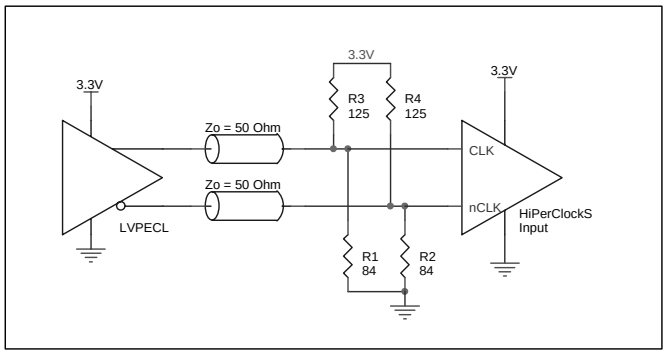



**FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**

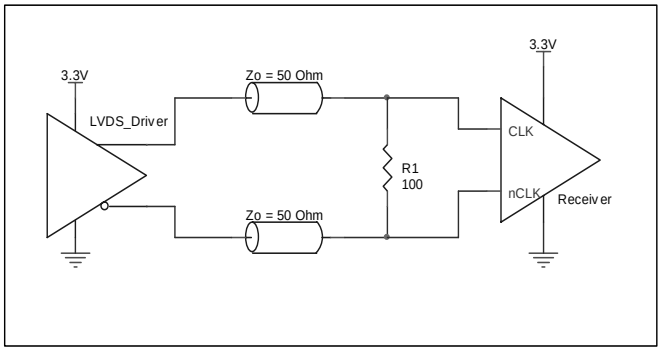



**FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

# RELIABILITY INFORMATION

**TABLE 6. $\theta_{JA}$ VS. AIR FLOW TABLE**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 50°C/W | 43°C/W | 38°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## TRANSISTOR COUNT

The transistor count for ICS87366 is: 3069

## PACKAGE OUTLINE - M SUFFIX

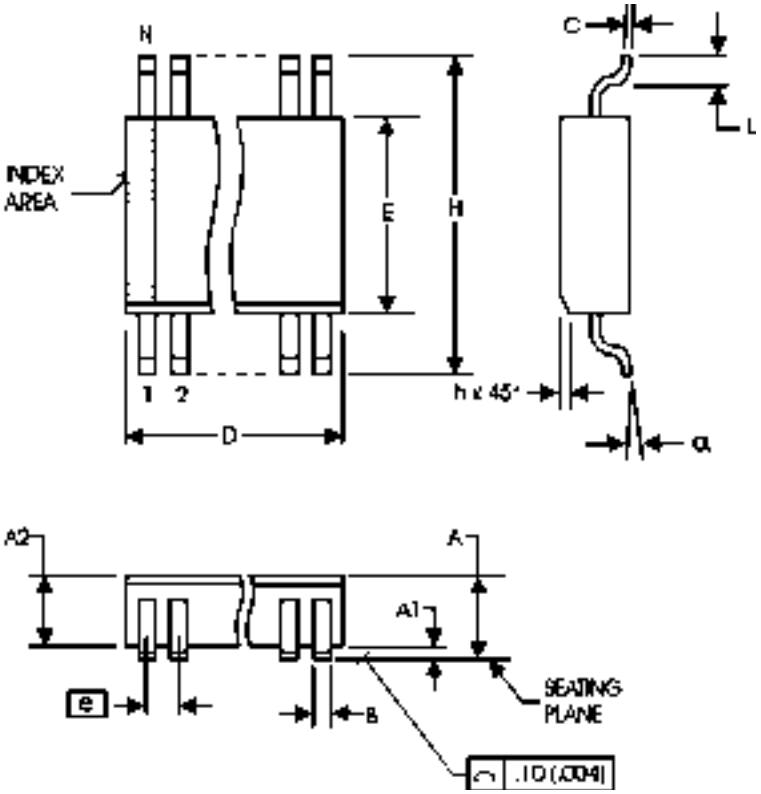



**TABLE 7. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 24 | |
| A | -- | 2.65 |
| A1 | 0.10 | -- |
| A2 | 2.05 | 2.55 |
| B | 0.33 | 0.51 |
| C | 0.18 | 0.32 |
| D | 15.20 | 15.85 |
| E | 7.40 | 7.60 |
| e | 1.27 BASIC | |
| H | 10.00 | 10.65 |
| h | 0.25 | 0.75 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-013, MO-119

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS87366AM | ICS87366AM | 24 Lead SOIC | 30 per tube | 0°C to 70°C |
| ICS87366AMT | ICS87366AM | 24 Lead SOIC on Tape and Reel | 1000 | 0°C to 70°C |