

# IS61C1024 IS61C1024L



## 128K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 1997

### FEATURES

- High-speed access time: 12, 15, 20, 25 ns
- Low active power: 600 mW (typical)
- Low standby power: 500  $\mu$ W (typical) CMOS standby
- Output Enable ( $\overline{OE}$ ) and two Chip Enable ( $\overline{CE1}$  and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ( $\pm 10\%$ ) power supply
- Low power version available: IS61C1024L
- Commercial and industrial temperature ranges available

### DESCRIPTION

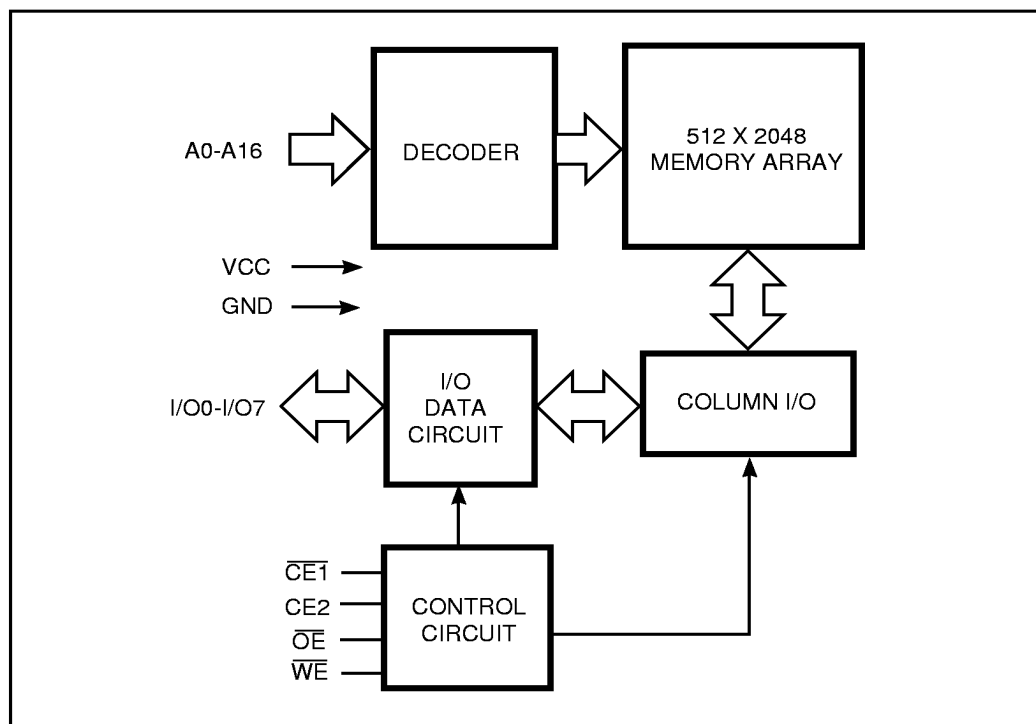
The *ISSI* IS61C1024 and IS61C1024L are very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ISSI's* high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE1}$  is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs,  $\overline{CE1}$  and CE2. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS61C1024 and IS61C1024L are available in 32-pin 300-mil and 400-mil plastic DIP and SOJ, and TSOP (type 1) packages.

### FUNCTIONAL BLOCK DIAGRAM

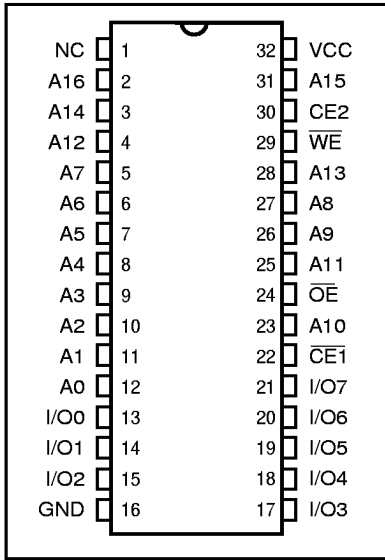


ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 1997, Integrated Silicon Solution, Inc.

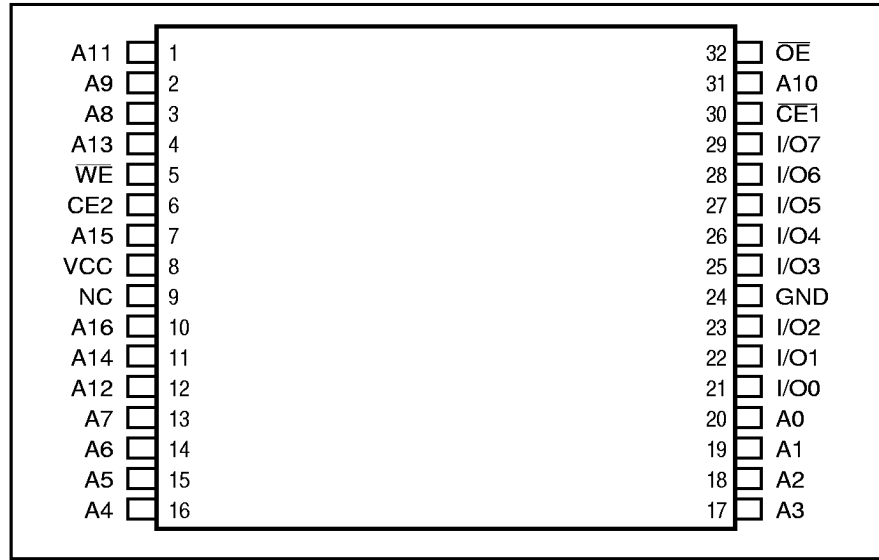
**Integrated Silicon Solution, Inc.**

SR028-1H  
07/18/97

**PIN CONFIGURATION**  
32-Pin SOJ



**PIN CONFIGURATION**  
32-Pin TSOP (Type 1)



**PIN DESCRIPTIONS**

|                  |                     |
|------------------|---------------------|
| A0-A16           | Address Inputs      |
| $\overline{CE1}$ | Chip Enable 1 Input |
| CE2              | Chip Enable 2 Input |
| $\overline{OE}$  | Output Enable Input |
| $\overline{WE}$  | Write Enable Input  |
| I/O0-I/O7        | Input/Output        |
| Vcc              | Power               |
| GND              | Ground              |

**OPERATING RANGE**

| Range      | Ambient Temperature | Vcc <sup>(1)</sup> |
|------------|---------------------|--------------------|
| Commercial | 0°C to +70°C        | 5V ± 10%           |
| Industrial | -40°C to +85°C      | 5V ± 10%           |

**Note:**

1. Vcc = 5V ± 5% for 12 ns devices.

**TRUTH TABLE**

| Mode            | $\overline{WE}$ | $\overline{CE1}$ | CE2 | $\overline{OE}$ | I/O Operation | Vcc Current |
|-----------------|-----------------|------------------|-----|-----------------|---------------|-------------|
| Not Selected    | X               | H                | X   | X               | High-Z        | Isb1, Isb2  |
| (Power-down)    | X               | X                | L   | X               | High-Z        | Isb1, Isb2  |
| Output Disabled | H               | L                | H   | H               | High-Z        | Icc1, Icc2  |
| Read            | H               | L                | H   | L               | Dout          | Icc1, Icc2  |
| Write           | L               | L                | H   | X               | Din           | Icc1, Icc2  |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol            | Parameter                            | Value        | Unit |
|-------------------|--------------------------------------|--------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V    |
| T <sub>BIAS</sub> | Temperature Under Bias               | -55 to +125  | °C   |
| T <sub>STG</sub>  | Storage Temperature                  | -65 to +150  | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.5          | W    |
| I <sub>OUT</sub>  | DC Output Current (LOW)              | 20           | mA   |

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

| Symbol           | Parameter          | Conditions            | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 0V  | 5    | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 0V | 7    | pF   |

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5.0V.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

| Symbol          | Parameter                        | Test Conditions  |              | Min.     | Max.                  | Unit |
|-----------------|----------------------------------|--|--------------|----------|-----------------------|------|
| V <sub>OH</sub> | Output HIGH Voltage              | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA            |              | 2.4      | —                     | V    |
| V <sub>OL</sub> | Output LOW Voltage               | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA             |              | —        | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH Voltage               |  |              | 2.2      | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub> | Input LOW Voltage <sup>(1)</sup> |  |              | -0.3     | 0.8                   | V    |
| I <sub>LI</sub> | Input Leakage                    | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                      | Com.<br>Ind. | -2<br>-5 | 2<br>5                | μA   |
| I <sub>LO</sub> | Output Leakage                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub><br>Outputs Disabled | Com.<br>Ind. | -2<br>-5 | 2<br>5                | μA   |

**Notes:**

1. V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.

**IS61C1024 POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol           | Parameter  | Test Conditions   |      | -12 ns |      | -15 ns |      | -20 ns |      | -25 ns |      | Unit |
|------------------|--|---|------|--------|------|--------|------|--------|------|--------|------|------|
|                  |  |   |      | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| I <sub>CC1</sub> | V <sub>CC</sub> Operating Supply Current         | V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$<br>I <sub>OUT</sub> = 0 mA, f = 0  | Com. | —      | 140  | —      | 140  | —      | 140  | —      | 140  | mA   |
|                  |  |   | Ind. | —      | 140  | —      | 140  | —      | 140  | —      | 140  |      |
| I <sub>CC2</sub> | V <sub>CC</sub> Dynamic Operating Supply Current | V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>   | Com. | —      | 220  | —      | 200  | —      | 170  | —      | 150  | mA   |
|                  |  |   | Ind. | —      | 220  | —      | 200  | —      | 170  | —      | 150  |      |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>$\overline{CE1} \geq V_{IH}$ , f = 0 or<br>CE2 ≤ V <sub>IL</sub> , f = 0     | Com. | —      | 40   | —      | 40   | —      | 40   | —      | 40   | mA   |
|                  |  |   | Ind. | —      | 60   | —      | 60   | —      | 60   | —      | 60   |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>CC</sub> = Max.,<br>$\overline{CE1} \leq V_{CC} - 0.2V$ ,<br>CE2 ≤ 0.2V<br>V <sub>IN</sub> > V <sub>CC</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 | Com. | —      | 30   | —      | 30   | —      | 30   | —      | 30   | mA   |
|                  |  |   | Ind. | —      | 40   | —      | 40   | —      | 40   | —      | 40   |      |

**Notes:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**IS61C1024L POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol           | Parameter  | Test Conditions   |      | -12 ns |      | -15 ns |      | -20 ns |      | -25 ns |      | Unit |
|------------------|--|---|------|--------|------|--------|------|--------|------|--------|------|------|
|                  |  |   |      | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| I <sub>CC1</sub> | V <sub>CC</sub> Operating Supply Current         | V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$<br>I <sub>OUT</sub> = 0 mA, f = 0  | Com. | —      | 85   | —      | 85   | —      | 85   | —      | 85   | mA   |
|                  |  |   | Ind. | —      | 110  | —      | 110  | —      | 110  | —      | 110  |      |
| I <sub>CC2</sub> | V <sub>CC</sub> Dynamic Operating Supply Current | V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>   | Com. | —      | 175  | —      | 160  | —      | 150  | —      | 150  | mA   |
|                  |  |   | Ind. | —      | 175  | —      | 160  | —      | 150  | —      | 150  |      |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>$\overline{CE1} \geq V_{IH}$ , f = 0 or<br>CE2 ≤ V <sub>IL</sub> , f = 0     | Com. | —      | 40   | —      | 40   | —      | 40   | —      | 40   | mA   |
|                  |  |   | Ind. | —      | 60   | —      | 60   | —      | 60   | —      | 60   |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>CC</sub> = Max.,<br>$\overline{CE1} \leq V_{CC} - 0.2V$ ,<br>CE2 ≤ 0.2V<br>V <sub>IN</sub> > V <sub>CC</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 | Com. | —      | 500  | —      | 500  | —      | 500  | —      | 500  | μA   |
|                  |  |   | Ind. | —      | 750  | —      | 750  | —      | 750  | —      | 750  |      |

**Notes:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol                           | Parameter                                | -12  |      | -15 ns |      | -20 ns |      | -25 ns |      | Unit |
|----------------------------------|--|------|------|--------|------|--------|------|--------|------|------|
|                                  |  | Min. | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>RC</sub>                  | Read Cycle Time                          | 12   | —    | 15     | —    | 20     | —    | 25     | —    | ns   |
| t <sub>AA</sub>                  | Address Access Time                      | —    | 12   | —      | 15   | —      | 20   | —      | 25   | ns   |
| t <sub>OH</sub>                  | Output Hold Time                         | 3    | —    | 3      | —    | 3      | —    | 3      | —    | ns   |
| t <sub>ACE1</sub>                | $\overline{CE1}$ Access Time             | —    | 12   | —      | 15   | —      | 20   | —      | 25   | ns   |
| t <sub>ACE2</sub>                | CE2 Access Time                          | —    | 12   | —      | 15   | —      | 20   | —      | 25   | ns   |
| t <sub>DOE</sub>                 | $\overline{OE}$ Access Time              | —    | 6    | —      | 7    | —      | 9    | —      | 9    | ns   |
| t <sub>LZOE<sup>(2)</sup></sub>  | $\overline{OE}$ to Low-Z Output          | 0    | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>HZOE<sup>(2)</sup></sub>  | $\overline{OE}$ to High-Z Output         | 0    | 6    | 0      | 6    | 0      | 7    | 0      | 10   | ns   |
| t <sub>LZCE1<sup>(2)</sup></sub> | $\overline{CE1}$ to Low-Z Output         | 2    | —    | 2      | —    | 3      | —    | 3      | —    | ns   |
| t <sub>LZCE2<sup>(2)</sup></sub> | CE2 to Low-Z Output                      | 2    | —    | 2      | —    | 3      | —    | 3      | —    | ns   |
| t <sub>HZCE<sup>(2)</sup></sub>  | $\overline{CE1}$ or CE2 to High-Z Output | 0    | 7    | 0      | 8    | 0      | 9    | 0      | 10   | ns   |
| t <sub>PU<sup>(3)</sup></sub>    | $\overline{CE1}$ or CE2 to Power-Up      | 0    | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>PD<sup>(3)</sup></sub>    | $\overline{CE1}$ or CE2 to Power-Down    | —    | 12   | —      | 12   | —      | 18   | —      | 20   | ns   |

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC TEST CONDITIONS**

| Parameter                                   | Unit                  |
|---|-----------------------|
| Input Pulse Level                           | 0V to 3.0V            |
| Input Rise and Fall Times                   | 3 ns                  |
| Input and Output Timing and Reference Level | 1.5V                  |
| Output Load                                 | See Figures 1a and 1b |

**AC TEST LOADS**

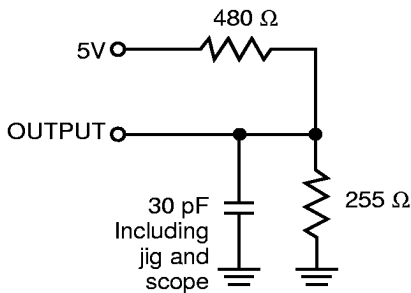


Figure 1a.

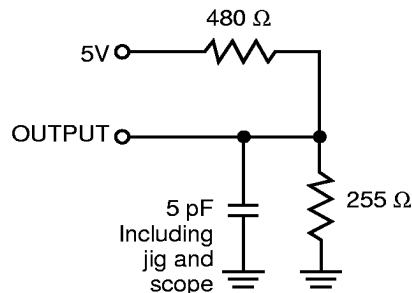
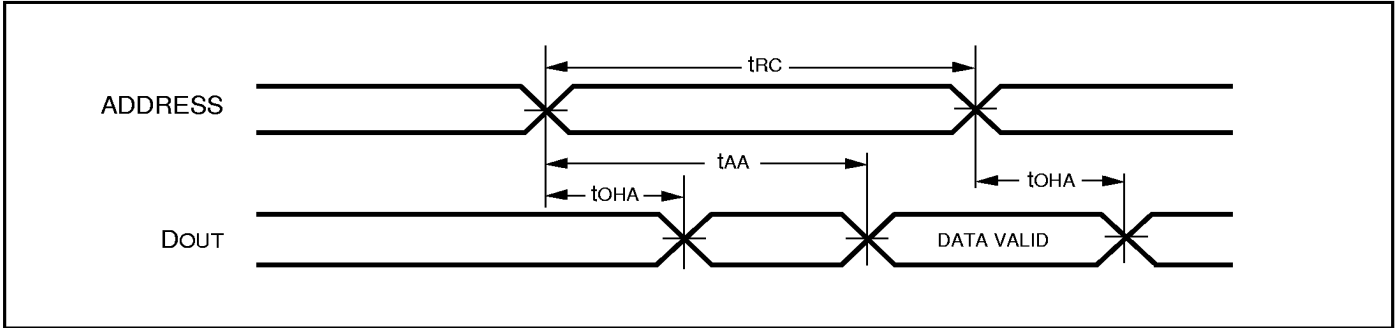


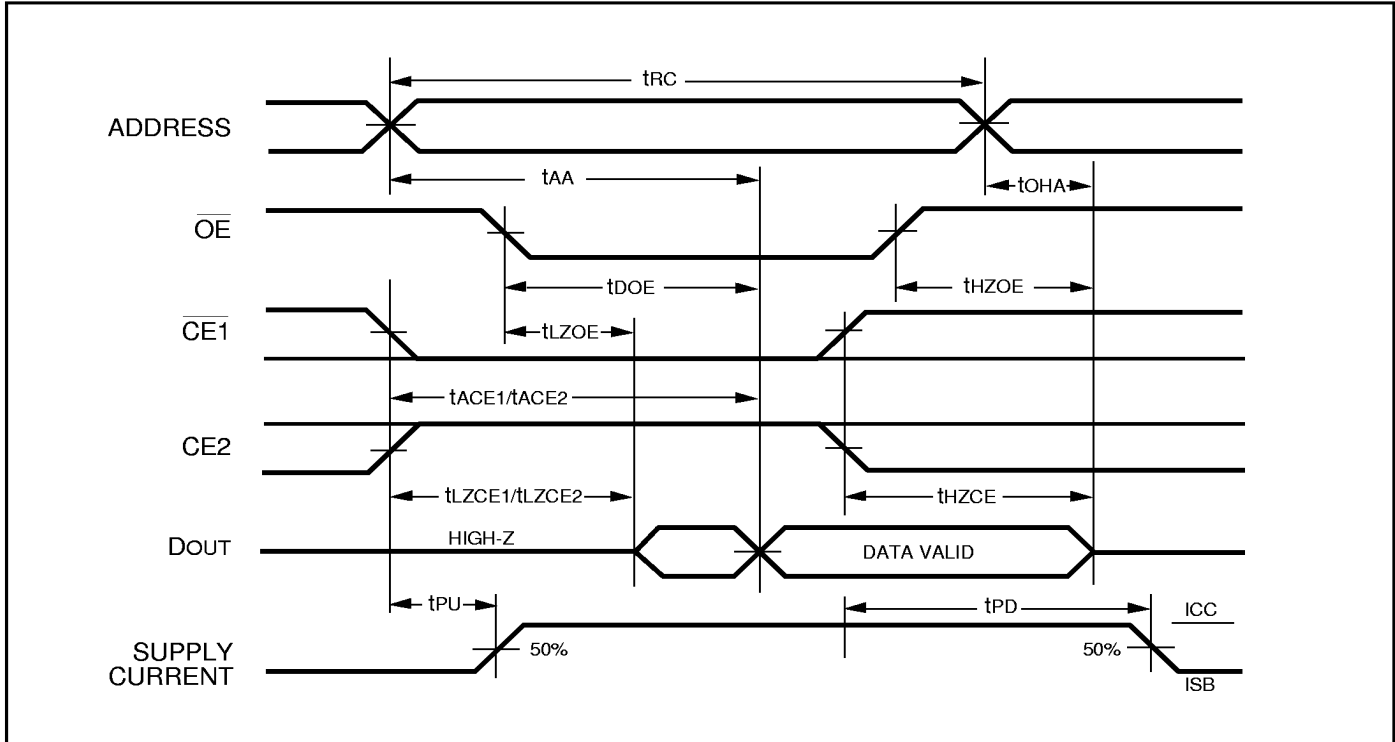
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}$  LOW and CE2 HIGH transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range, Standard and Low Power)

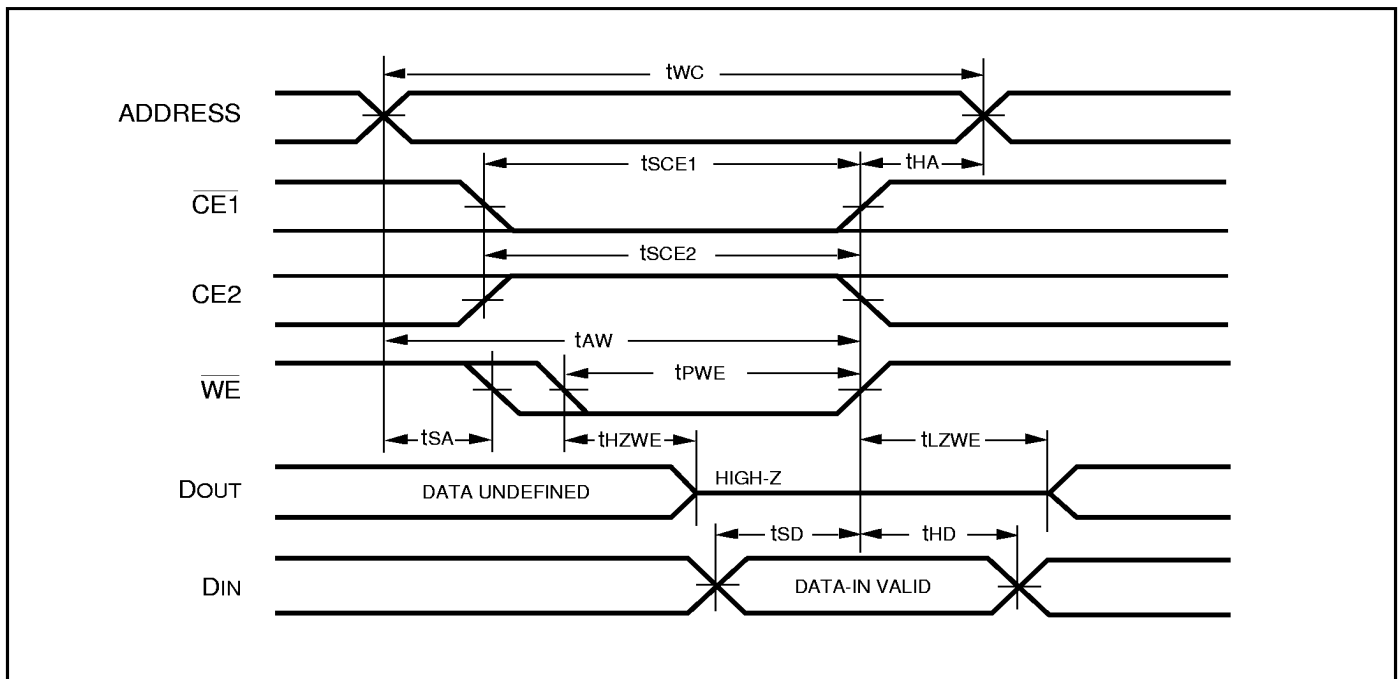
| Symbol                          | Parameter                            | -12 ns |      | -15 ns |      | -20 ns |      | -25 ns |      | Unit |
|---------------------------------|--------------------------------------|--------|------|--------|------|--------|------|--------|------|------|
|                                 |                                      | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>WC</sub>                 | Write Cycle Time                     | 12     | —    | 15     | —    | 20     | —    | 25     | —    | ns   |
| t <sub>SCE1</sub>               | $\overline{CE1}$ to Write End        | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| t <sub>SCE2</sub>               | CE2 to Write End                     | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| t <sub>AW</sub>                 | Address Setup Time to Write End      | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| t <sub>HA</sub>                 | Address Hold from Write End          | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>SA</sub>                 | Address Setup Time                   | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>PWE<sup>(4)</sup></sub>  | $\overline{WE}$ Pulse Width          | 10     | —    | 10     | —    | 12     | —    | 15     | —    | ns   |
| t <sub>SD</sub>                 | Data Setup to Write End              | 7      | —    | 8      | —    | 10     | —    | 12     | —    | ns   |
| t <sub>HD</sub>                 | Data Hold from Write End             | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>HZWE<sup>(2)</sup></sub> | $\overline{WE}$ LOW to High-Z Output | —      | 7    | —      | 7    | —      | 10   | —      | 12   | ns   |
| t <sub>LZWE<sup>(2)</sup></sub> | $\overline{WE}$ HIGH to Low-Z Output | 2      | —    | 2      | —    | 2      | —    | 2      | —    | ns   |

**Notes:**

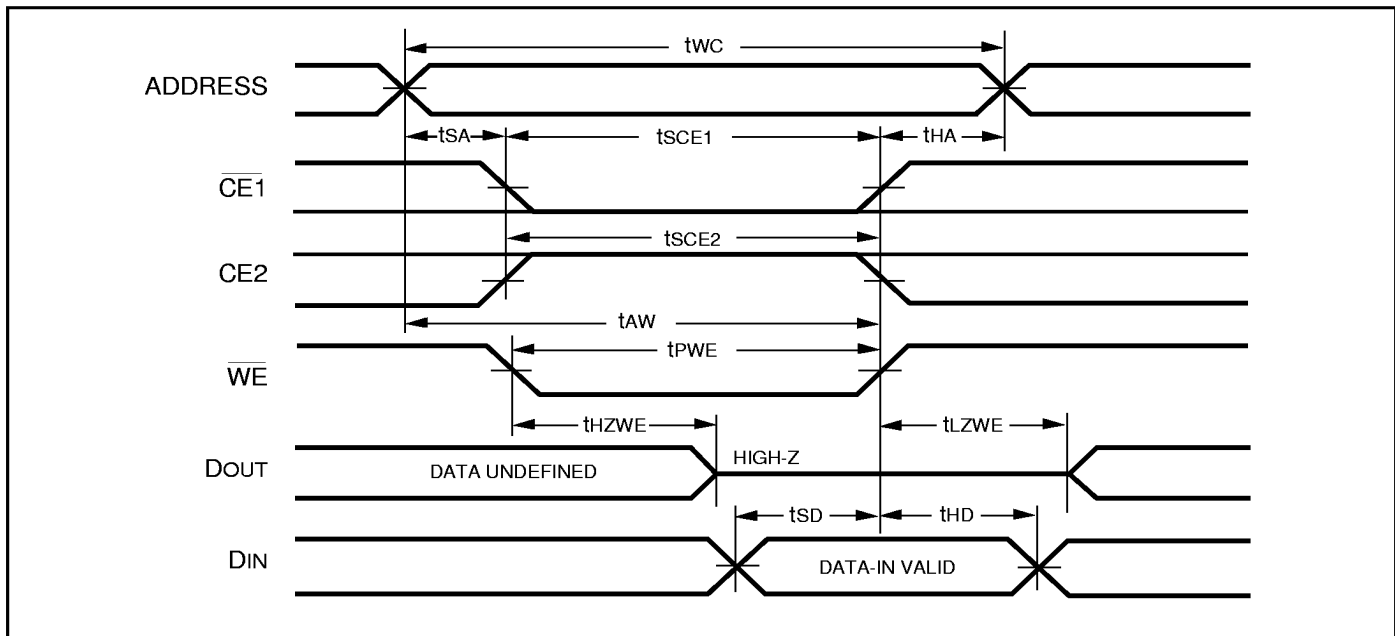
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with  $\overline{OE}$  HIGH.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**



**WRITE CYCLE NO. 2 ( $\overline{CE1}$ , CE2 Controlled)<sup>(1,2)</sup>**



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} = V_{IH}$ .

**IS61C1024 STANDARD VERSION  
ORDERING INFORMATION  
Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part No. | Package             |
|------------|----------------|---------------------|
| 12         | IS61C1024-12JR | 300-mil Plastic SOJ |
| 12         | IS61C1024-12NR | 300-mil Plastic DIP |
| 12         | IS61C1024-12KR | 400-mil Plastic SOJ |
| 12         | IS61C1024-12MR | 400-mil Plastic DIP |
| 12         | IS61C1024-12TR | TSOP, Type 1        |
| <hr/>      |                |                     |
| 15         | IS61C1024-15J  | 300-mil Plastic SOJ |
| 15         | IS61C1024-15N  | 300-mil Plastic DIP |
| 15         | IS61C1024-15K  | 400-mil Plastic SOJ |
| 15         | IS61C1024-15M  | 400-mil Plastic DIP |
| 15         | IS61C1024-15T  | TSOP, Type 1        |
| <hr/>      |                |                     |
| 20         | IS61C1024-20J  | 300-mil Plastic SOJ |
| 20         | IS61C1024-20N  | 300-mil Plastic DIP |
| 20         | IS61C1024-20K  | 400-mil Plastic SOJ |
| 20         | IS61C1024-20M  | 400-mil Plastic DIP |
| 20         | IS61C1024-20T  | TSOP, Type 1        |
| <hr/>      |                |                     |
| 25         | IS61C1024-25J  | 300-mil Plastic SOJ |
| 25         | IS61C1024-25N  | 300-mil Plastic DIP |
| 25         | IS61C1024-25K  | 400-mil Plastic SOJ |
| 25         | IS61C1024-25M  | 400-mil Plastic DIP |
| 25         | IS61C1024-25T  | TSOP, Type 1        |

**IS61C1024 STANDARD VERSION  
ORDERING INFORMATION  
Industrial Range: -40°C to +85°C**

| Speed (ns) | Order Part No.  | Package             |
|------------|-----------------|---------------------|
| 12         | IS61C1024-12JRI | 300-mil Plastic SOJ |
| 12         | IS61C1024-12NRI | 300-mil Plastic DIP |
| 12         | IS61C1024-12KRI | 400-mil Plastic SOJ |
| 12         | IS61C1024-12MRI | 400-mil Plastic DIP |
| 12         | IS61C1024-12TRI | TSOP, Type 1        |
| <hr/>      |                 |                     |
| 15         | IS61C1024-15JI  | 300-mil Plastic SOJ |
| 15         | IS61C1024-15NI  | 300-mil Plastic DIP |
| 15         | IS61C1024-15KI  | 400-mil Plastic SOJ |
| 15         | IS61C1024-15MI  | 400-mil Plastic DIP |
| 15         | IS61C1024-15TI  | TSOP, Type 1        |
| <hr/>      |                 |                     |
| 20         | IS61C1024-20JI  | 300-mil Plastic SOJ |
| 20         | IS61C1024-20NI  | 300-mil Plastic DIP |
| 20         | IS61C1024-20KI  | 400-mil Plastic SOJ |
| 20         | IS61C1024-20MI  | 400-mil Plastic DIP |
| 20         | IS61C1024-20TI  | TSOP, Type 1        |
| <hr/>      |                 |                     |
| 25         | IS61C1024-25JI  | 300-mil Plastic SOJ |
| 25         | IS61C1024-25NI  | 300-mil Plastic DIP |
| 25         | IS61C1024-25KI  | 400-mil Plastic SOJ |
| 25         | IS61C1024-25MI  | 400-mil Plastic DIP |
| 25         | IS61C1024-25TI  | TSOP, Type 1        |



**IS61C1024L LOW POWER VERSION**  
**ORDERING INFORMATION**  
**Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part No.  | Package             |
|------------|-----------------|---------------------|
| 12         | IS61C1024L-12JR | 300-mil Plastic SOJ |
|            | IS61C1024L-12NR | 300-mil Plastic DIP |
|            | IS61C1024L-12KR | 400-mil Plastic SOJ |
|            | IS61C1024L-12MR | 400-mil Plastic DIP |
|            | IS61C1024L-12TR | TSOP, Type 1        |
| 15         | IS61C1024L-15J  | 300-mil Plastic SOJ |
|            | IS61C1024L-15N  | 300-mil Plastic DIP |
|            | IS61C1024L-15K  | 400-mil Plastic SOJ |
|            | IS61C1024L-15M  | 400-mil Plastic DIP |
|            | IS61C1024L-15T  | TSOP, Type 1        |
| 20         | IS61C1024L-20J  | 300-mil Plastic SOJ |
|            | IS61C1024L-20N  | 300-mil Plastic DIP |
|            | IS61C1024L-20K  | 400-mil Plastic SOJ |
|            | IS61C1024L-20M  | 400-mil Plastic DIP |
|            | IS61C1024L-20T  | TSOP, Type 1        |
| 25         | IS61C1024L-25J  | 300-mil Plastic SOJ |
|            | IS61C1024L-25N  | 300-mil Plastic DIP |
|            | IS61C1024L-25K  | 400-mil Plastic SOJ |
|            | IS61C1024L-25M  | 400-mil Plastic DIP |
|            | IS61C1024L-25T  | TSOP, Type 1        |

**IS61C1024L LOW POWER VERSION**  
**ORDERING INFORMATION**  
**Industrial Range: -40°C to +85°C**

| Speed (ns) | Order Part No.   | Package             |
|------------|------------------|---------------------|
| 12         | IS61C1024L-12JRI | 300-mil Plastic SOJ |
|            | IS61C1024L-12NRI | 300-mil Plastic DIP |
|            | IS61C1024L-12KRI | 400-mil Plastic SOJ |
|            | IS61C1024L-12TRI | TSOP, Type 1        |
| 15         | IS61C1024L-15JI  | 300-mil Plastic SOJ |
|            | IS61C1024L-15NI  | 300-mil Plastic DIP |
|            | IS61C1024L-15KI  | 400-mil Plastic SOJ |
|            | IS61C1024L-15TI  | TSOP, Type 1        |
| 20         | IS61C1024L-20JI  | 300-mil Plastic SOJ |
|            | IS61C1024L-20NI  | 300-mil Plastic DIP |
|            | IS61C1024L-20KI  | 400-mil Plastic SOJ |
|            | IS61C1024L-20TI  | TSOP, Type 1        |
| 25         | IS61C1024L-25JI  | 300-mil Plastic SOJ |
|            | IS61C1024L-25NI  | 300-mil Plastic DIP |
|            | IS61C1024L-25KI  | 400-mil Plastic SOJ |
|            | IS61C1024L-25TI  | TSOP, Type 1        |